# De-multiplexer

# Introduction

- A De-multiplexer is a combinational circuit that has only 1 input line and $2^N$ output lines.
- Simply, the multiplexer is a single-input and multi-output combinational circuit.
- The information is received from the single input lines and directed to the output line.

- On the basis of the values of the selection lines, the input will be connected to one of these outputs.
- De-multiplexer is opposite to the multiplexer.
- Unlike encoder and decoder, there are n selection lines and $2^n$ outputs. So, there is a total of $2^n$ possible combinations of inputs.
- De-multiplexer is also treated as **De-mux**.

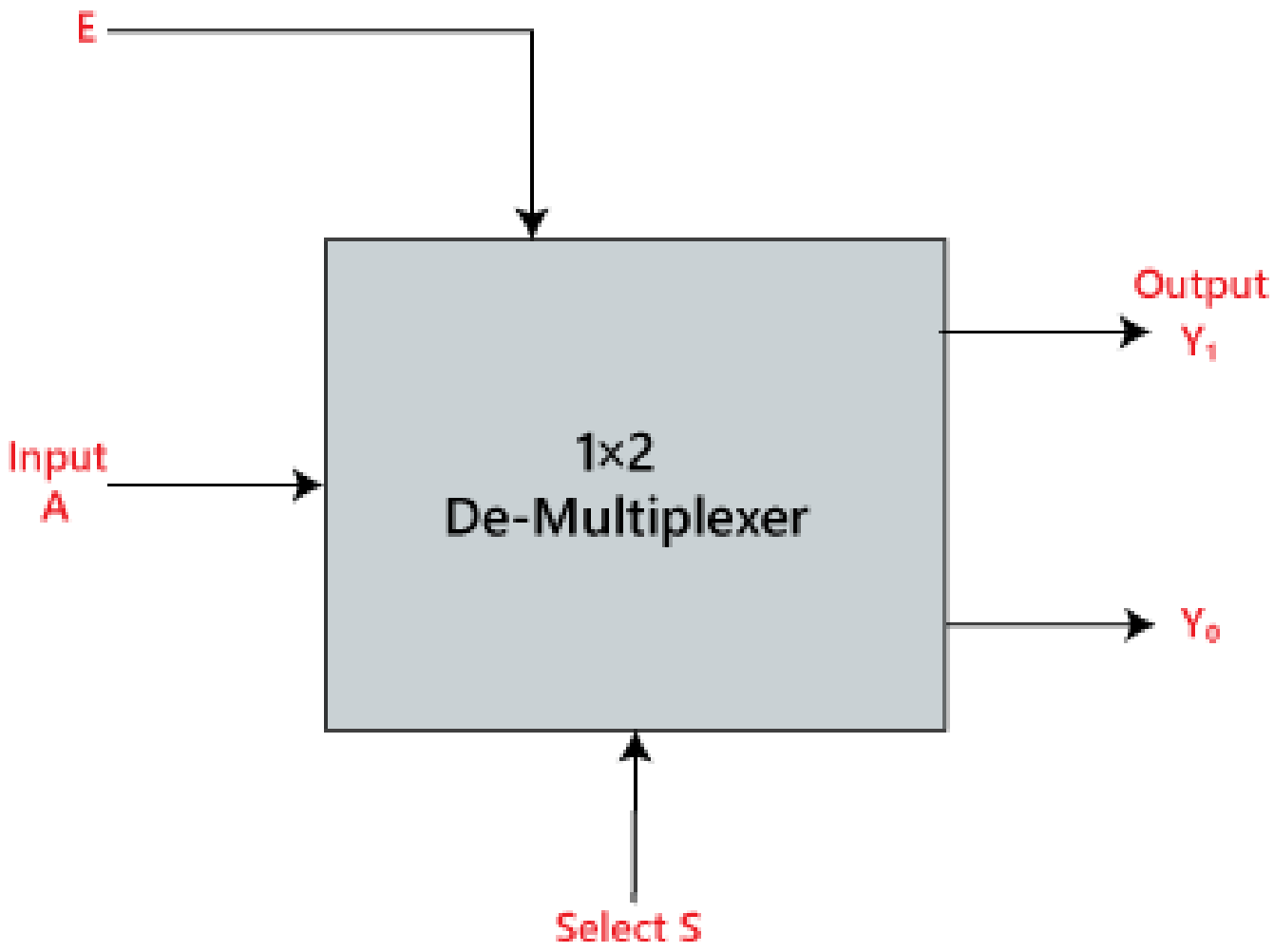
# Types

- There are various types of De-multiplexer which are as follows:

# 1×2 De-multiplexer:

- In the 1 to 2 De-multiplexer, there are only two outputs,
- i.e., $Y_0$, and $Y_1$,
- 1 selection lines, i.e., $S_0$,
- and single input, i.e., A.
- On the basis of the selection value, the input will be connected to one of the outputs.
- The block diagram and the truth table of the 1×2 multiplexer are given below.

# Block Diagram:



# Truth Table:

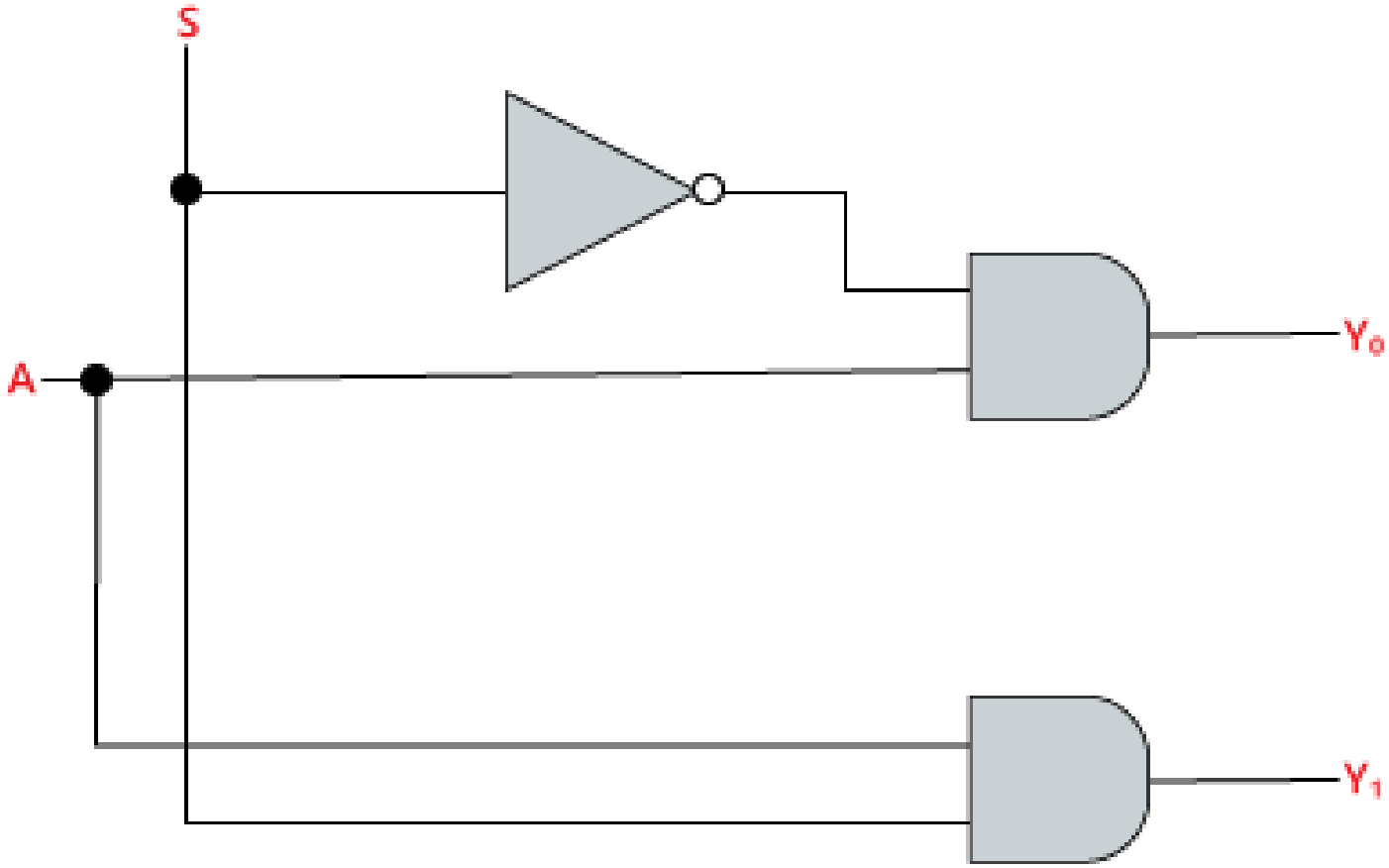
| INPUTS | Output | |
|---|---|---|
| $S_0$ | $Y_1$ | $Y_0$ |
| 0 | 0 | A |
| 1 | A | 0 |

The logical expression of the term Y is as follows:

$Y_0=S_0'.A$

$Y_1=S_0.A$

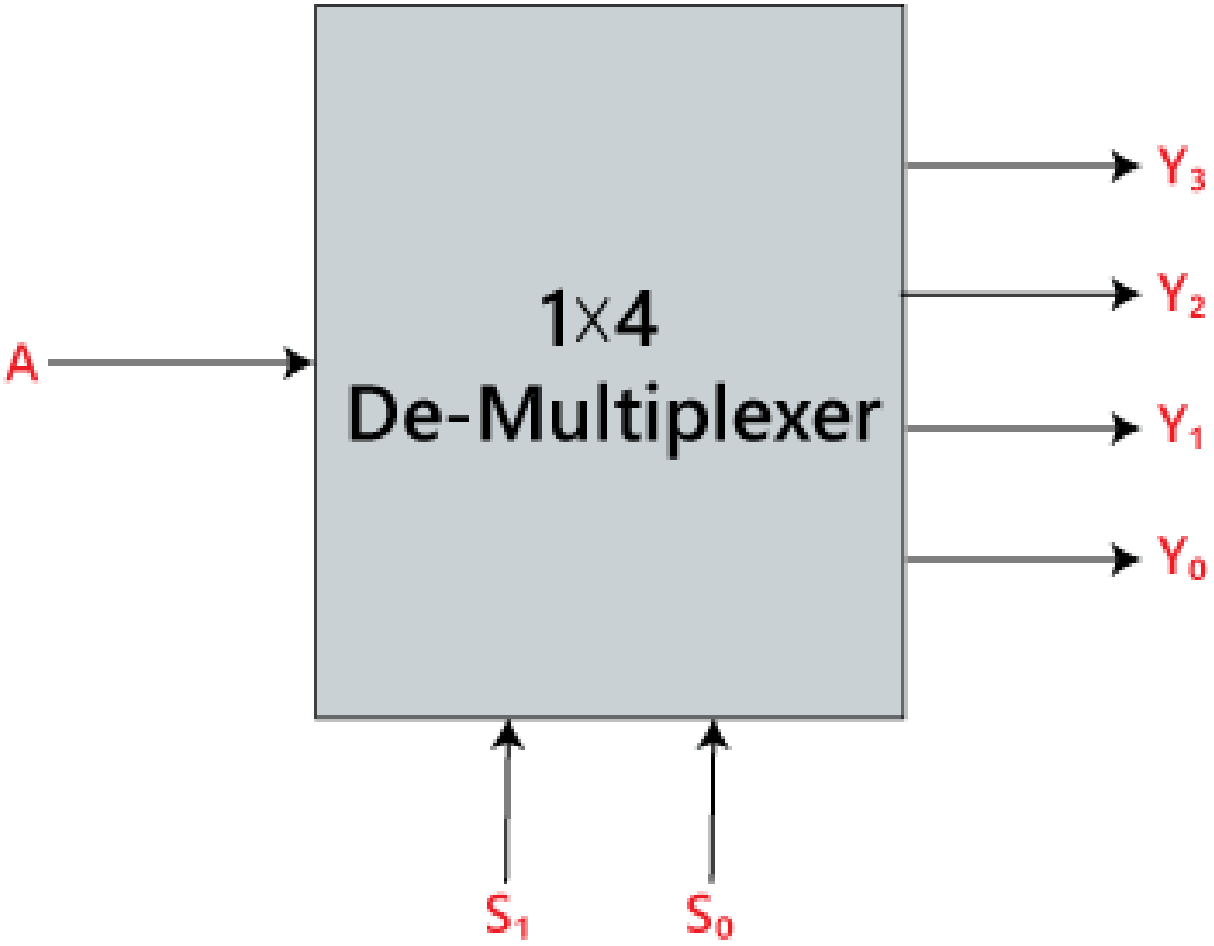
Logical circuit of the above expressions is given below:



# 1×4 De-multiplexer:

- In 1 to 4 De-multiplexer, there are total of four outputs, i.e., $Y_0$, $Y_1$, $Y_2$, and $Y_3$,
- 2 selection lines, i.e., $S_0$ and $S_1$
- and single input, i.e., A.
- On the basis of the combination of inputs which are present at the selection lines $S_0$ and $S_1$, the input be connected to one of the outputs.
- The block diagram and the truth table of the 1×4 multiplexer are given below.

# Block Diagram:

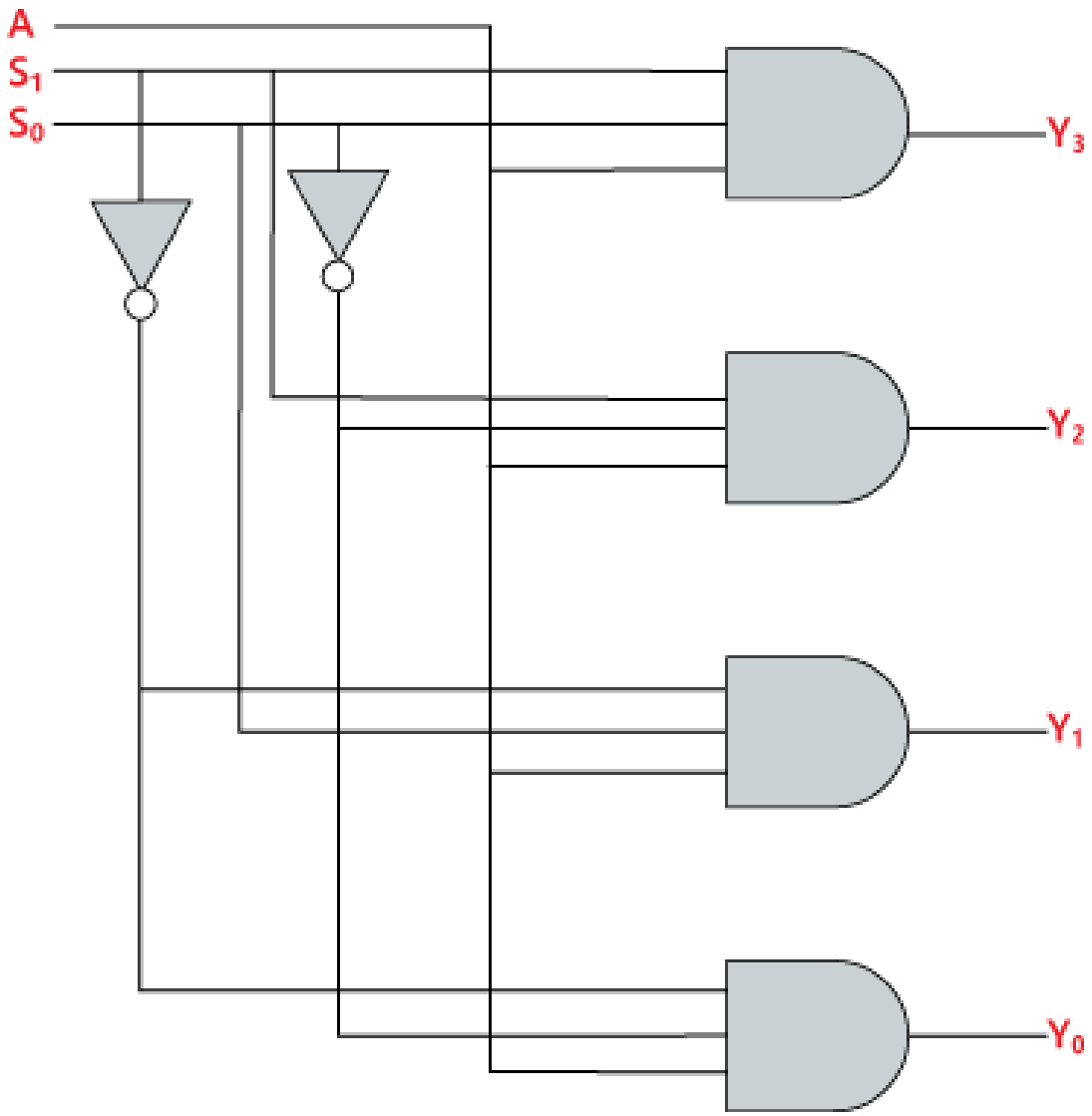


# Truth Table:

| INPUTS | | Output | | | |
|---|---|---|---|---|---|
| $S_1$ | $S_0$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
| 0 | 0 | 0 | 0 | 0 | A |
| 0 | 1 | 0 | 0 | A | 0 |
| 1 | 0 | 0 | A | 0 | 0 |
| 1 | 1 | A | 0 | 0 | 0 |

- The logical expression of the term Y is as follows:
- $Y_0 = S_1' S_0' A$
  $y_1 = S_1' S_0 A$
  $y_2 = S_1 S_0' A$
  $y_3 = S_1 S_0 A$

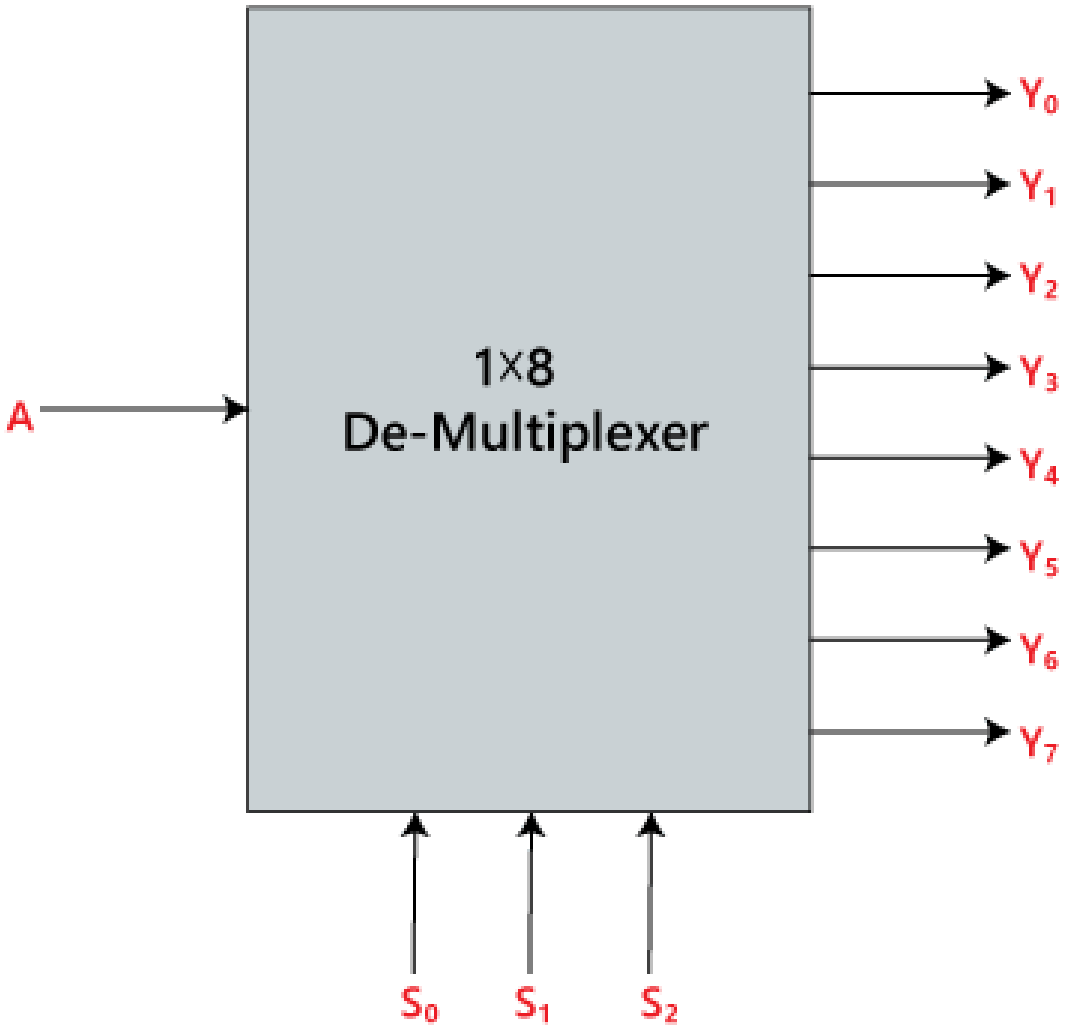
Logical circuit of the above expressions is given below:



# 1×8 De-multiplexer

- In 1 to 8 De-multiplexer, there are total of eight outputs, i.e., $Y_0$, $Y_1$, $Y_2$, $Y_3$, $Y_4$, $Y_5$, $Y_6$, and $Y_7$,
- 3 selection lines, i.e., $S_0$, $S_1$and $S_2$
- and single input, i.e., A.
- On the basis of the combination of inputs which are present at the selection lines $S^0$, $S^1$ and $S_2$, the input will be connected to one of these outputs.
- The block diagram and the truth table of the 1×8 de-multiplexer are given below.

# Block Diagram:



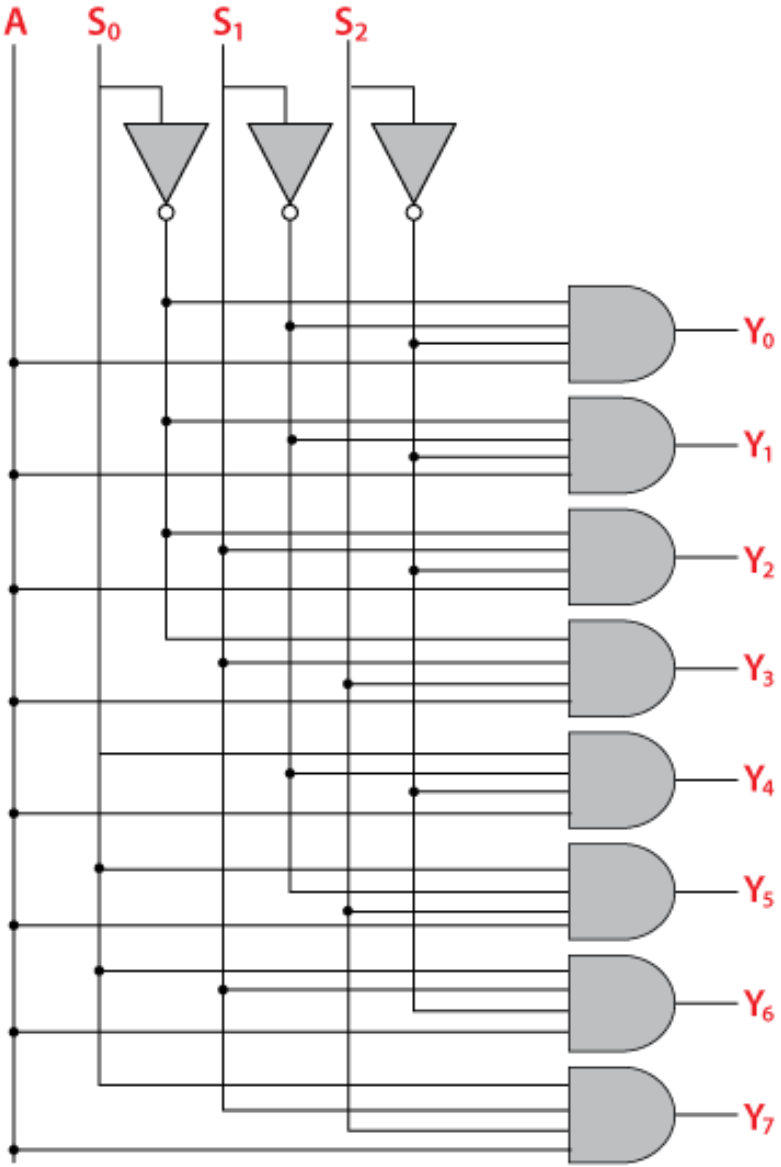
# Truth Table:

| INPUTS | | | Output | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $S_2$ | $S_1$ | $S_0$ | $Y_7$ | $Y_6$ | $Y_5$ | $Y_4$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

# The logical expression of the term Y is as follows:

- $Y_0=S_0'.S_1'.S_2'.A$
  $Y_1=S_0.S_1'.S_2'.A$
  $Y_2=S_0'.S_1.S_2'.A$
  $Y_3=S_0.S_1.S_2'.A$
  $Y_4=S_0'.S_1'.S_2\ A$
  $Y_5=S_0.S_1'.S_2\ A$
  $Y_6=S_0'.S_1.S_2\ A$
  $Y_7=S_0.S_1.S_3.A$

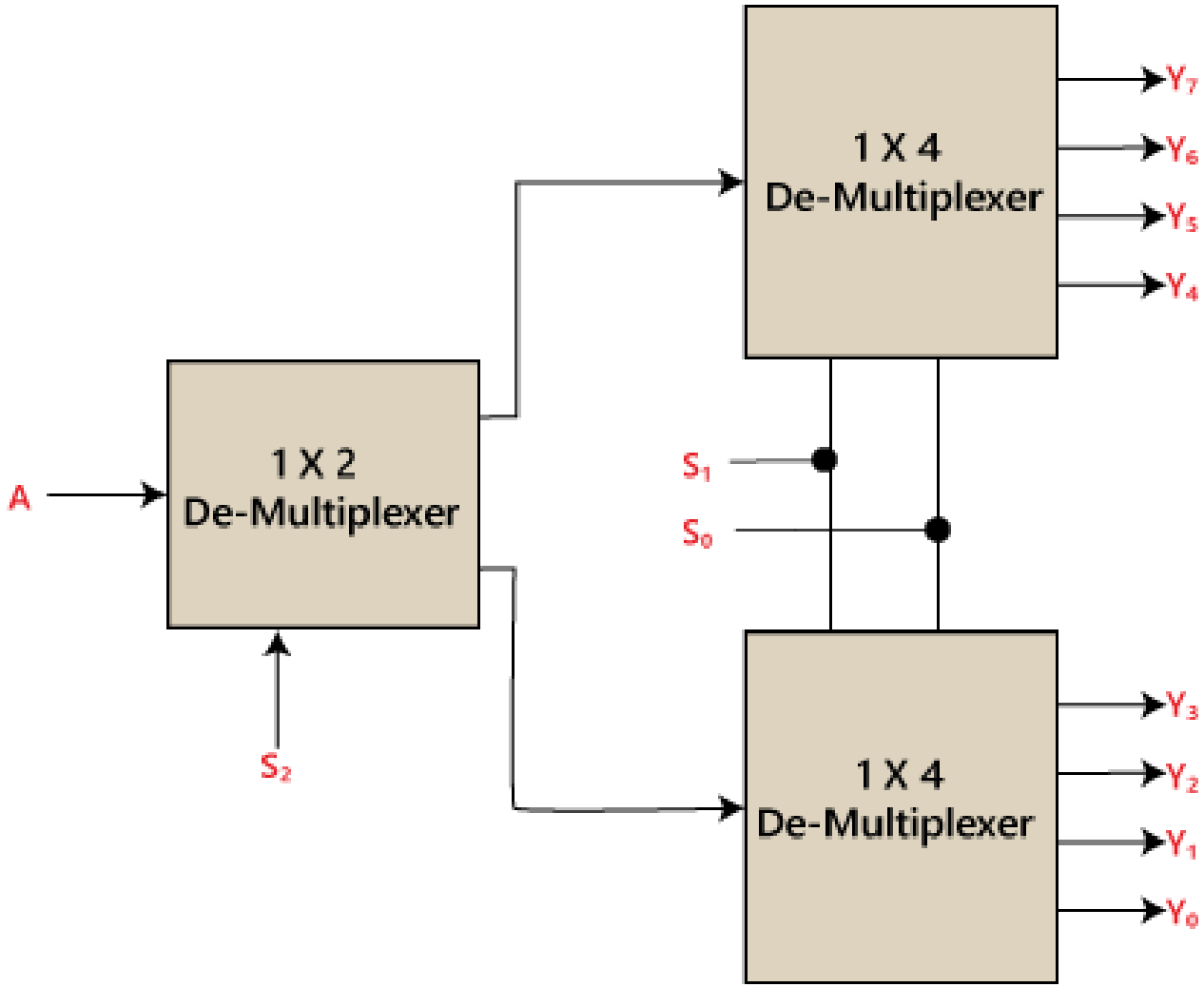
Logical circuit of the above expressions is given below:



# 1×8 De-multiplexer using 1×4 and 1×2 de-multiplexer

- We can implement the 1×8 de-multiplexer using a lower order de-multiplexer.
- To implement the 1×8 de-multiplexer, we need two 1×4 de-multiplexer and one 1×2 de-multiplexer.
- The 1×4 multiplexer has 2 selection lines, 4 outputs, and 1 input.
- The 1×2 de-multiplexer has only 1 selection line.

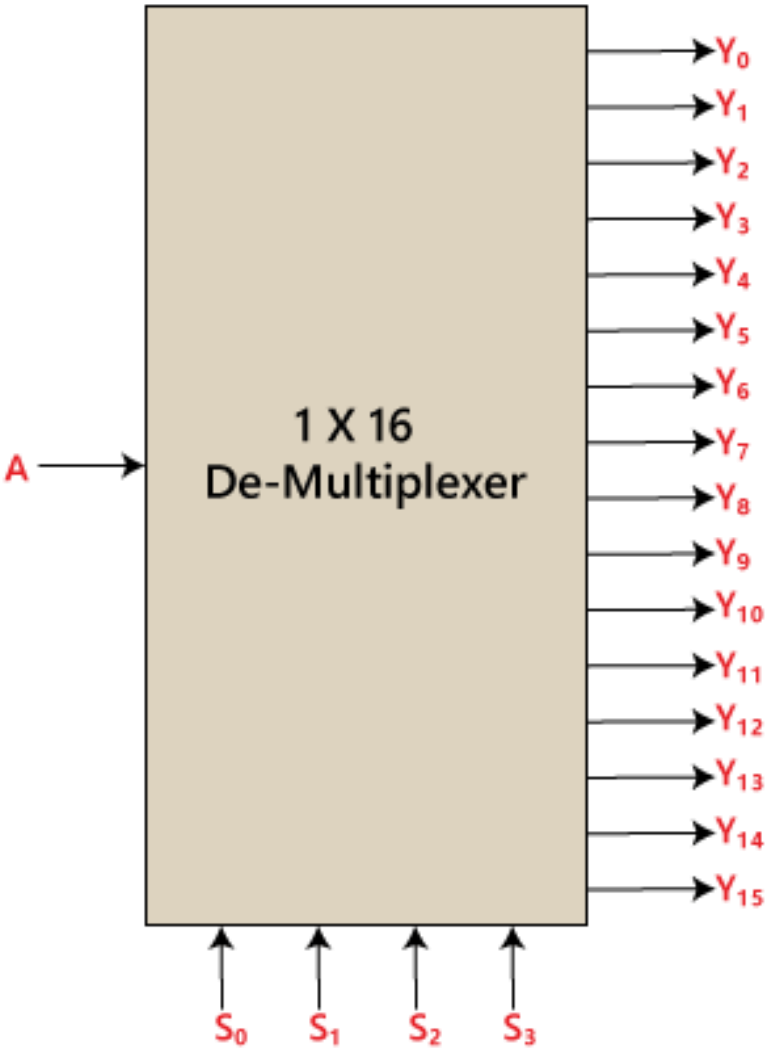
- For getting 8 data outputs, we need two 1×4 de-multiplexer.
- The 1×2 de-multiplexer produces two outputs.
- So, in order to get the final output, we have to pass the outputs of 1×2 de-multiplexer as an input of both the 1×4 de-multiplexer.
- The block diagram of 1×8 de-multiplexer using 1×4 and 1×2 de-multiplexer is given below.


1 X 4
De-Multiplexer
Y7
Y6
Y5
Y4
1 X 2
De-Multiplexer
A
S1
S0
S2
1 X 4
De-Multiplexer
Y3
Y2
Y1
Y0

# 1 x 16 De-multiplexer

- In 1×16 de-multiplexer, there are total of 16 outputs, i.e., $Y_0$, $Y_1$, …, $Y_{16}$, 4 selection lines, i.e., $S_0$, $S_1$, $S_2$, and $S_3$ and single input, i.e., A.
- On the basis of the combination of inputs which are present at the selection lines $S^0$, $S^1$, and $S_2$, the input will be connected to one of these outputs.
- The block diagram and the truth table of the 1×16 de-multiplexer are given below.

# Block diagram



# Truth Table:

| INPUTS | | | | OUTPUTS | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $S_3$ | $S_2$ | $S_1$ | $S_0$ | $Y_{15}$ | $Y_{14}$ | $Y_{13}$ | $Y_{12}$ | $Y_{11}$ | $Y_{10}$ | $Y_9$ | $Y_8$ | $Y_7$ | $Y_6$ | $Y_5$ | $Y_4$ | $Y_3$ | $Y_2$ | $Y_1$ | $Y_0$ |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

# The logical expression of the term Y is as follows:

$Y_0=A.S_0'.S_1'.S_2'.S_3'$

$Y_1=A.S_0'.S_1'.S_2'.S_3$

$Y_2=A.S_0'.S_1'.S_2.S_3'$

$Y_3=A.S_0'.S_1'.S_2.S_3$

$Y_4=A.S_0'.S_1.S_2'.S_3'$

$Y_5=A.S_0'.S_1.S_2'.S_3$

$Y_6=A.S_0'.S_1.S_2.S_3'$

$Y_7=A.S_0'.S_1.S_2.S_3$

$Y_8=A.S_0.S_1'.S_2'.S_3'$

$Y_9=A.S_0.S_1'.S_2'.S_3$

$Y_{10}=A.S_0.S_1'.S_2.S_3'$

$Y_{11}=A.S_0.S_1'.S_2.S_3$

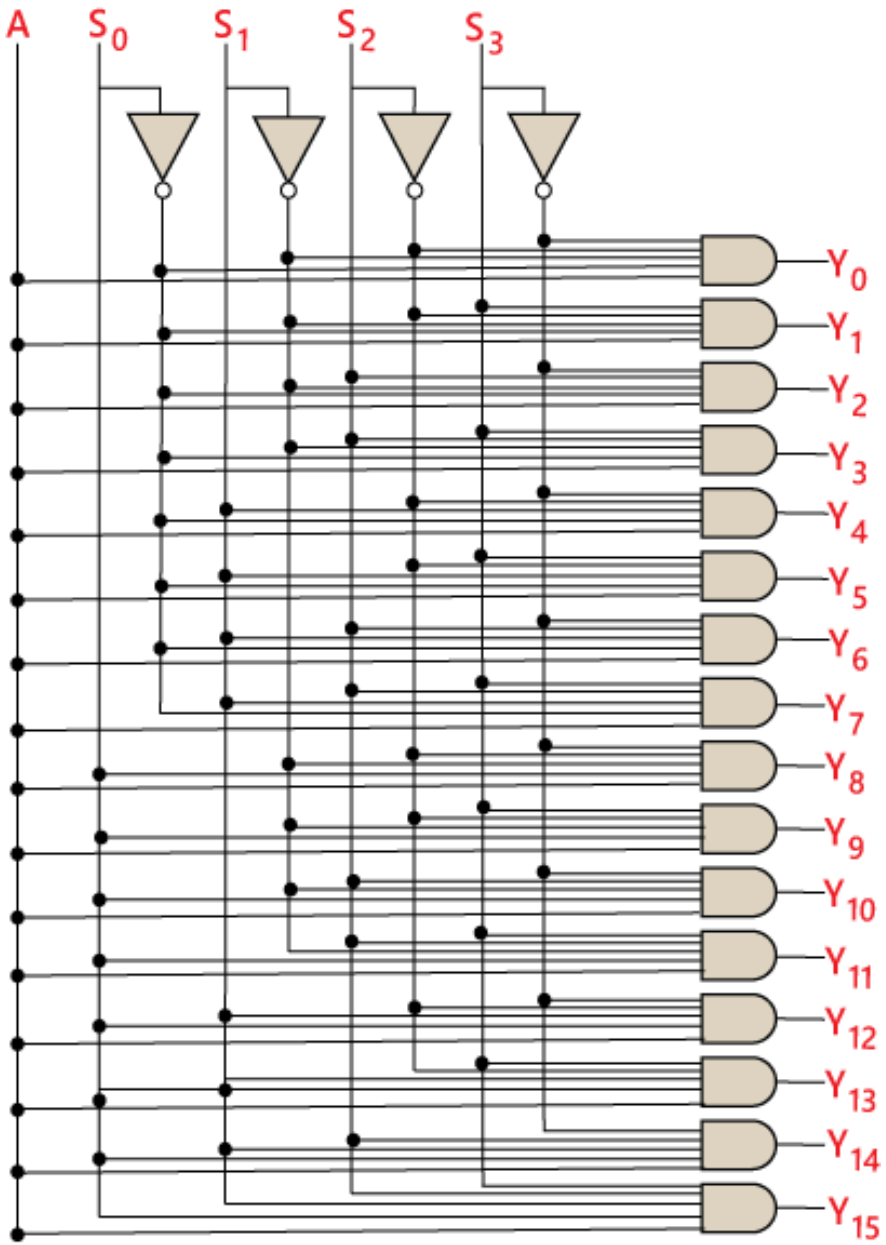
$Y_{12}=A.S_0.S_1.S_2'.S_3'$

$Y_{13}=A.S_0.S_1.S_2'.S_3$

$Y_{14}=A.S_0.S_1.S_2.S_3'$

$Y_{15}=A.S_0.S_1.S_2'.S_3$

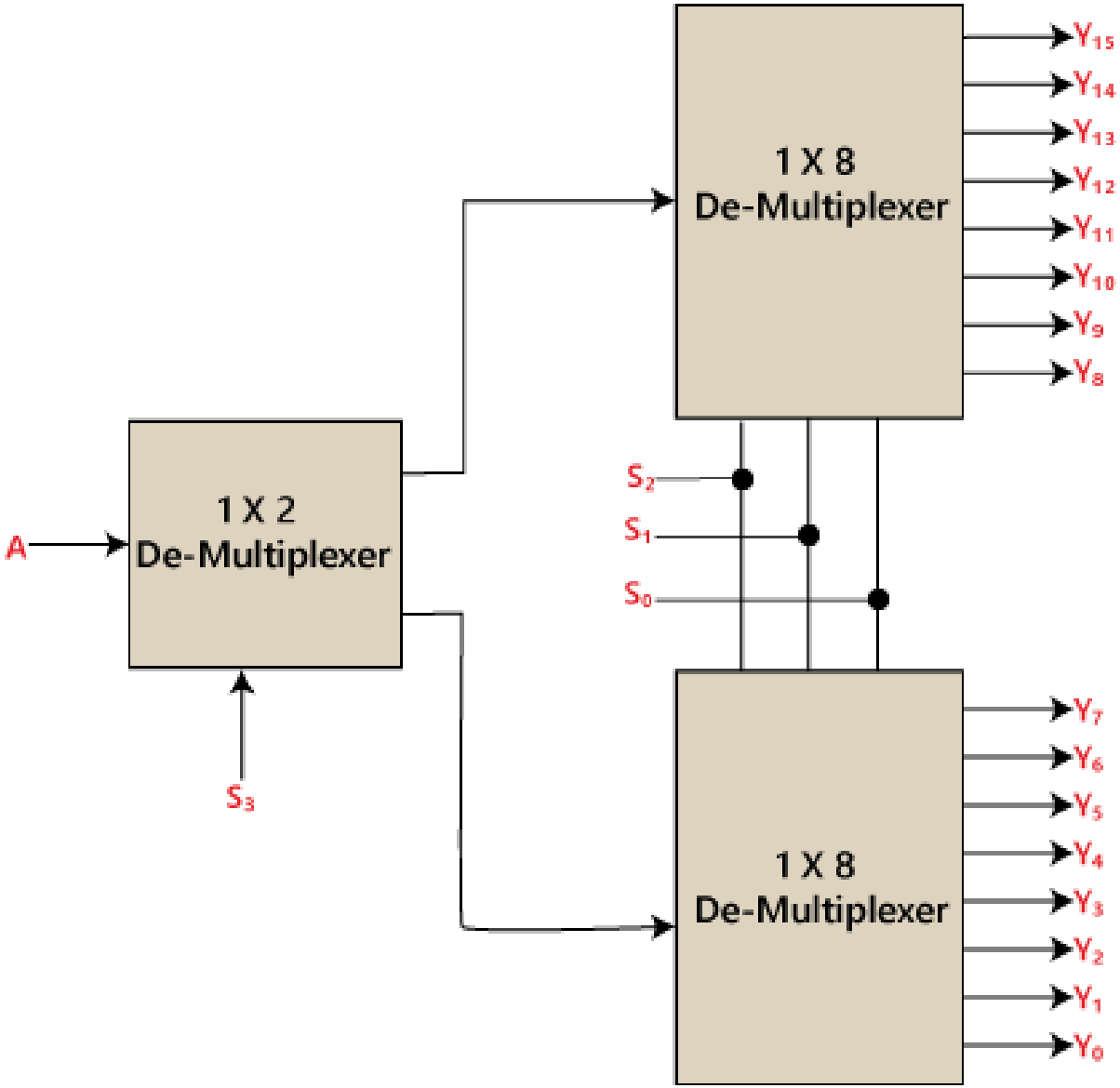
Logical circuit of the above expressions is given below:



# 1×16 de-multiplexer using 1×8 and 1×2 de-multiplexer

- We can implement the 1×16 de-multiplexer using a lower order de-multiplexer.
- To implement the 1×16 de-multiplexer, we need two 1×8 de-multiplexer and one 1×2 de-multiplexer.
- The 1×8 multiplexer has 3 selection lines, 1 input, and 8 outputs.
- The 1×2 de-multiplexer has only 1 selection line.

- For getting 16 data outputs, we need two 1×8 de-multiplexer.
- The 1×8 de-multiplexer produces eight outputs. So, in order to get the final output, we need a 1×2 de-multiplexer to produce two outputs from a single input.
- Then we pass these outputs into both the de-multiplexer as an input.
- The block diagram of 1×16 de-multiplexer using 1×8 and 1×2 de-multiplexer is given below.


1 X 8
De-Multiplexer
1 X 2
De-Multiplexer
1 X 8
De-Multiplexer
A
S3
S2
S1
S0
Y15
Y14
Y13
Y12
Y11
Y10
Y9
Y8
Y7
Y6
Y5
Y4
Y3
Y2
Y1
Y0