INTEL 80386 MICROPROCESSOR

FEATURES OF 80386:

Two versions of 80386 are commonly available:

1) 80386DX

2)80386SX

80386DX

1) 32 bit address bus
   32bit data bus
2) Packaged in 132 pin ceramic
   pin grid array(PGA)
3) Address 4GB of memory

80386SX

1) 24 bit address bus 16 bit data bus
2) 100 pin flat package
3) 16 MB of memory

Features of 80386

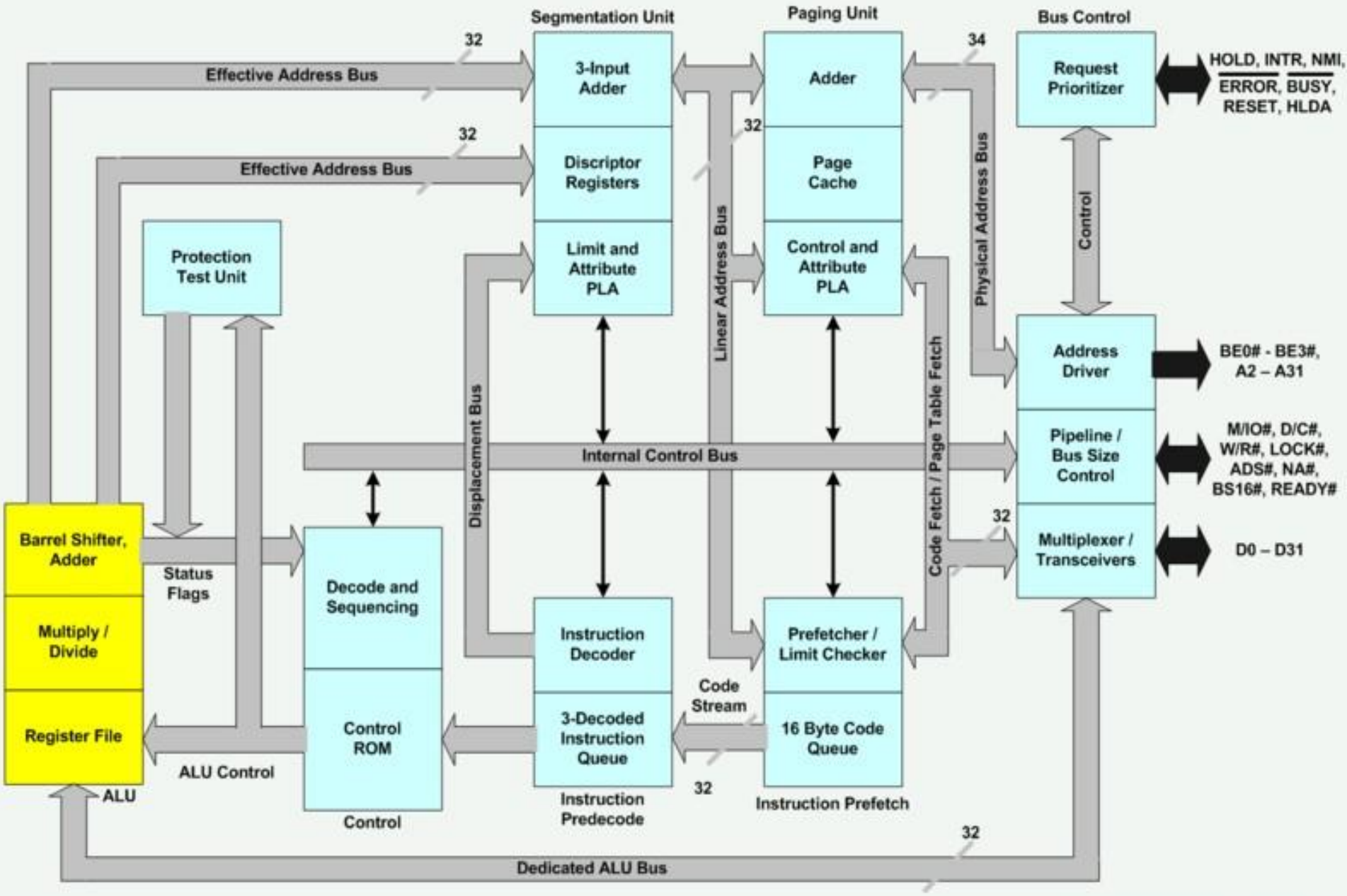
- 32 bit processor, it has 32 bit ALU which allows to process 32 bit data at a time.
- 32 bit address bus, therefore it can access 4GB physical memory and 64Terabytes of Virtual memory.
- It has pipeline architecture which allows simultaneous instruction fetching, decoding, and executing and memory management. Because of instruction pipelining higher bus bandwidth & on chip address translation mechanism, the average execution time has been significantly reduced.
- It allows user to switch between different OS such as DOS and UNIX
- Operates in Real, Protected and Virtual 8086 mode.

Features of 80386

- It compatible with 8086,8088, 80186, 80286 architecture.
- It has different data types like bits, byte, word, double word, Quadword, Tenbytes integer (signed and unsigned form).
- It has Separate pins for its address and data line, this result in higher performance and easier hardware design.
- Prefetch unit permits to prefetch upto 16bytes of instruction code. Therefore fetch time for most instruction is hidden, increase the performance.

Features of 80386

- It contains dedicated hardware for performing high speed address calculation, logical to linear address translation and protection check.
- It contain translation lookside buffer (TLB) that store recently used page directory and page table entries. This buffer consists of 32 sets of table entries which allow direct access of 128kbyts of paged memory



ARCHITECTURE OF INTEL 80386

PLA: Programmable Logic Array

Architecture of 80386

- The Internal Architecture of 80386 is divided into 3 sections.
    1 Central processing unit(CPU)
        a. Execution Unit
        b. Instruction Unit
    2 Memory management unit(MMU)
        a. Segmentation Unit
        b. Paging Unit
    3 Bus interface unit(BIU)
- Central processing unit is further divided into Execution unit(EU) and Instruction unit(IU)

Architecture of 80386

1 Central processing unit(CPU)

a) Execution Unit : Reads the instruction from the instruction queue and execute the instruction.

Consists of three subunits : control, data and protection test unit

I) Control Unit: It contains microcode and special hardware allows processor to reduce time required for execution of multiply and divide instruction. It also speeds the effective address calculation.

II) Data Unit: Responsible for data operations requested by the control unit. It contains ALU, eight 32 bit general purpose registers and 64 bit barrel shifter. The barrel shifter is used for multiple bit shifts in one clock. Thus it increases the speed of all shift and rotate operations.

Architecture of 80386

III) Protection Test Unit: checks for segmentation violations under the control of the microcode.

b) Instruction Decode Unit : Takes instruction byte from the code prefetch queue and translates them in to microcode. The decoded instructions are then stored in the instruction queue.

2) Memory Management Unit

a) Segmentation Unit: Translate logical address to linear addresses at the request of execution unit. Compares the effective address for the length limit specified in the segment descriptor. Adds the segment base and the effective address to generate linear address. Before calculation of linear address it also checks access rights. It provides a 4 level protection mechanism for protecting and isolating the system code and data from those of the application program

Architecture of 80386

b) Paging Unit: Translate linear addresses generated by the segmentation unit into physical addresses. If paging unit is not enabled, the physical address is the same as the linear address. It give physical address to the Bus Interface Unit to perform memory and I/O accesses. It organizes the physical memory in terms of pages of 4kbyts size each.

3) Bus Control Unit:

Is the 80836 communication with the outside world. It provides a full 32 bit bi-directional data and 32- bit address bus. Responsible for following operations

i) Accepts internal requests for code fetch and for data transfers from the code fetch unit and from the execution unit. It then prioritize the request and generates signals to perform bus cycles.

Architecture of 80386

ii)It send address, data and control signals to communicate with memory and I/O devices

iii)It controls the interface to external bus masters and coprocessors.

iv)It also provides the address relocation facility.

Instruction Prefetch Unit

Fetches sequentially the instruction byte stream from the memory. It uses bus control unit to fetch instruction bytes when it is not performing bus cycles. These prefetched instruction bytes are stored in 16 bytes code queue. When jump or call instructions are executed, the contents of the prefetched and decode queues are cleared out

Instruction Predecode Unit :

Takes instruction byte from the instruction perfetch queue and translate them into microcode. The decoded instruction then stored in instruction queue.