Assignment No. 04

M T W T F S S
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YOUVA

Q1. What is parallel processing ? Explain the types of parallel processing.

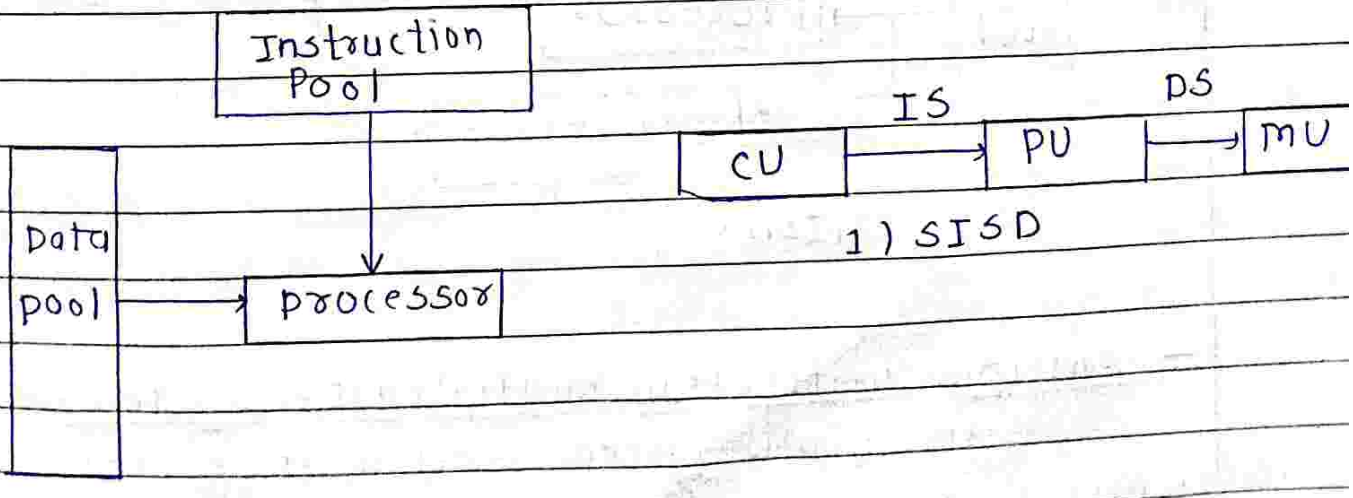
1. Parallel processing is a method in computing of running two or more processors to handle separate parts of an overall task
2. Breaking up different parts of a task among multiple processors will help reduce the amount of time to run a program.
3. Parallel processing is commonly used to perform complex tasks and computations.
4. The crux of parallel processing are CPUs. Based on the number of instruction and data streams that can be processed simultaneously, computing systems are classified into four major categories.

Flynn's classification -

1. Single-instruction, single-data systems

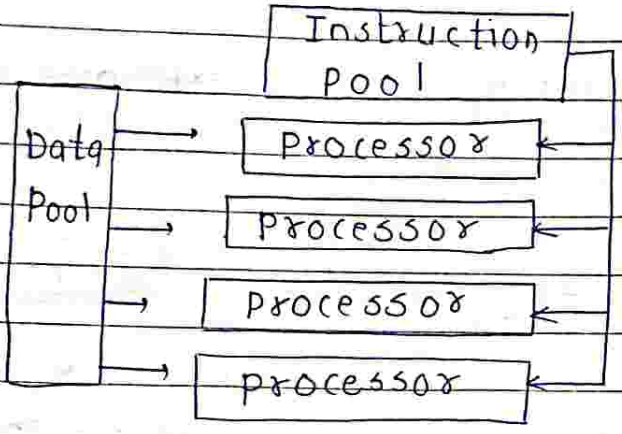
An SISD computing system is a uniprocessor machine which is capable of executing a single instruction, operating on a single data stream.

All the instructions and data to be processed have to be stored in primary memory



2. Single instruction multiple data systems -

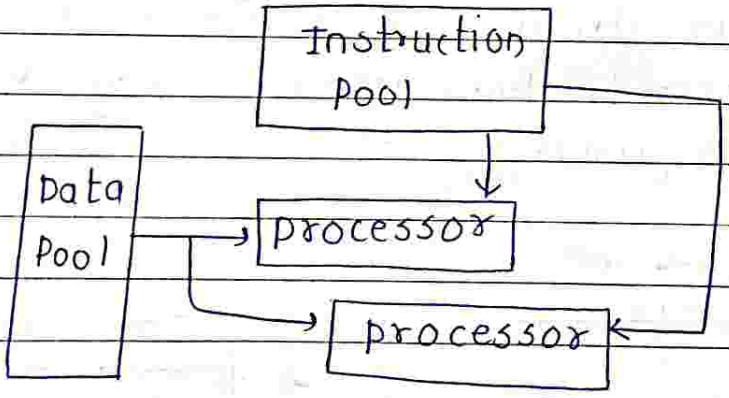
An SIMD system is a multiprocessor machine capable of executing the same instruction on all the CPUs but operating on different data streams



SIMD

3. Multiple - instruction single data systems -

An MISD computing system is a multiprocessor machine capable of executing different instructions on different PEs but all of them operating on the same dataset.



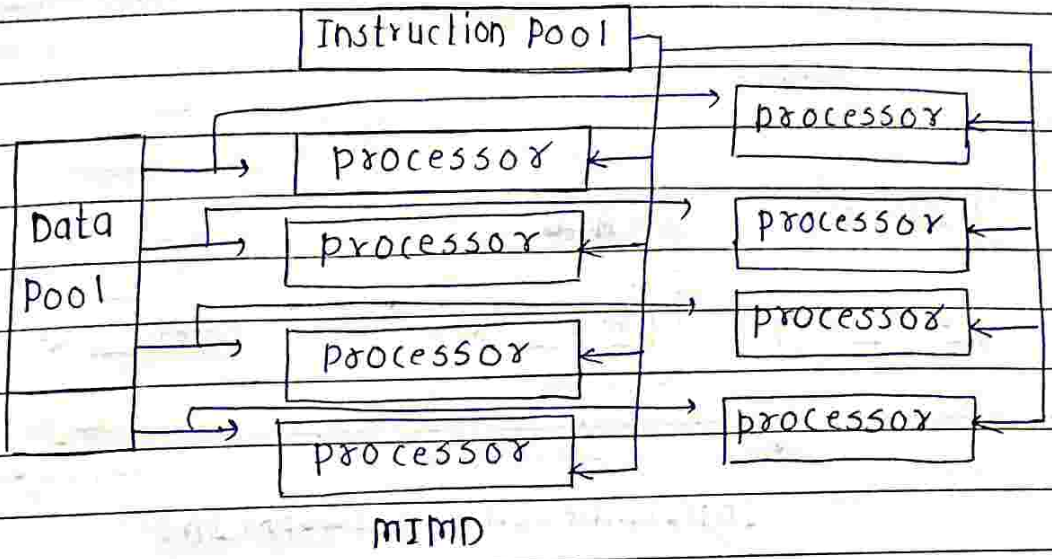
MISD

4. Multiple instruction multiple data systems -

An MIMD system is a multiprocessor machine which is capable of executing multiple instructions on multiple data sets.

Each PE in the MIMD model has separate instruction and data streams.

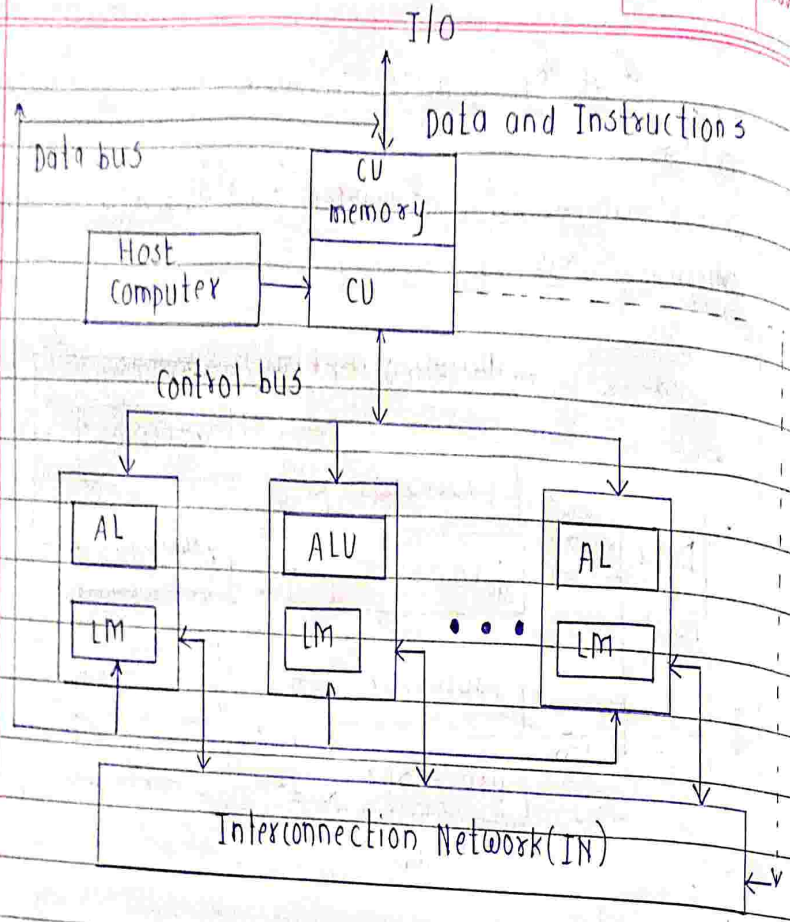
Unlike SIMD and MISD machines, PEs in MIMD machines work asynchronously.



MIMD

Q.2. Explain the working of array processor with neat diagram.

1. A processor which is used to perform different computations on a huge array of data is called an array processor.
2. The other terms used for this processor are vector processors or multiprocessors.
3. The processor performs only single instruction at a time on an array of data.
4. An array processor includes a number of ALUs which allows all the array elements to be processed together.
5. Each ALU in the processor is provided with local memory which is known as processing element or PE.
6. The array processing architecture is known as a 2-dimensional array or matrix.
7. The architecture is implemented by the two-dimensional processor.



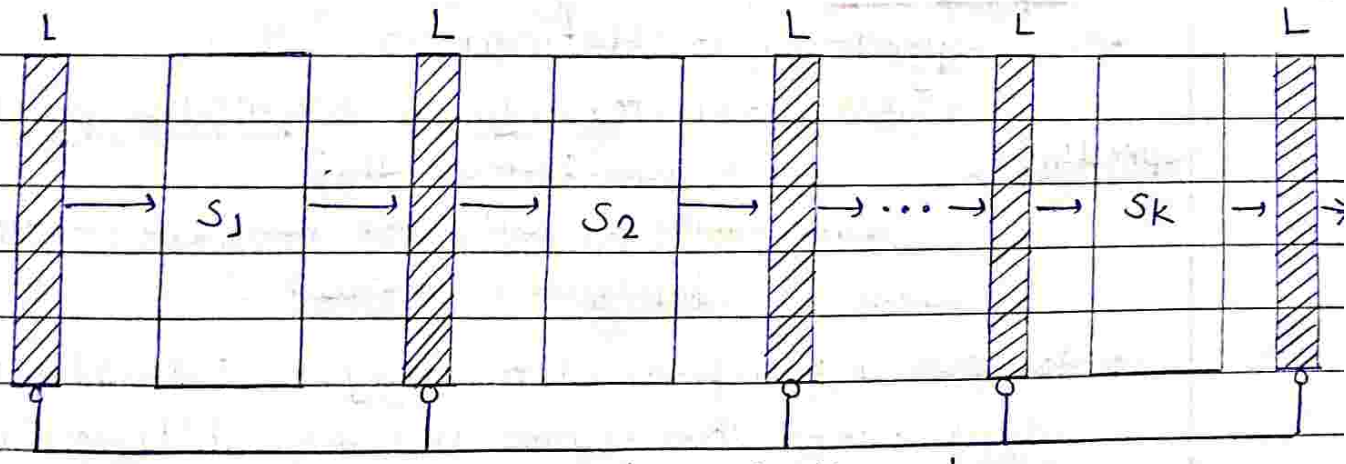
Array Processor

Working of array processor

1. An array processor has an architecture mainly designed for processing arrays of numbers.
2. This processor architecture contains a number of processors that works simultaneously, each handling one array element.
3. To get the same effect within a conventional processor, the operation should be applied to every array element sequentially and much more slowly.
4. This processor is a self-contained unit connected to the main computer through an interal bus or an I/O port.
5. This processor increases the overall speed of instruction processing.
6. These processors operate asynchronously from the host CPU to improve the overall system capacity.

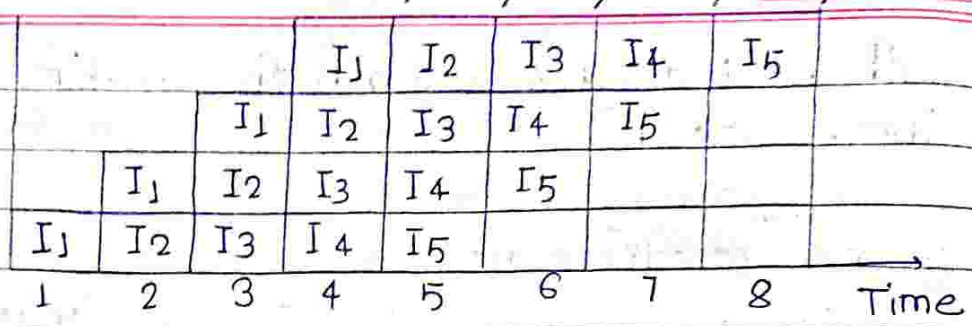
Q3. With neat diagram explain the working of basic linear pipeline.

1. In pipelining, we divide a task into set of subtasks.
2. The precedence relation of a set of subtasks $\{T_1, T_2, \ldots, T_k\}$ for a given task T implies that the same task T_j cannot start until some earlier task T_i finishes.
3. A pipeline can process successive subtasks if
   - subtasks have linear precedence order
   - Each subtasks take nearly same time to complete
4. Basic linear pipeline consists of cascade of processing stages.
   - Stages: Pure combinational circuits performing arithmetic or logic operations over the data flowing through the pipe.
   - stages are separated by high speed interface latches:
   - Latches: Fast registers holding intermediate results between stages.



L: Latches S_1, S_2 etc: Pipeline stages

Basic linear pipeline: The flow of data in a linear pipeline having four stages for the evaluation of a function on five inputs is as shown below:



- The vertical axis represents four stages
- The horizontal axis represents time in units of clock period of the pipeline

$$T = \max_{i=1}^{k} \{\tau_i\} + t_l = t_m + t_l$$

$$T_p = kT + (n-1)T = [k + (n-1)]T \simeq [4+4]T = 8T$$

k - stages , T - clock period , t_l - time delay of latch

Q.4. what are the performance parameters of pipeline $s = 4$, $n = 5$. calculate speedup, throughput, efficiency

There are three performance parameters of pipeline are present :

1. <u>speed-up</u>

- speed-up is defined as

$$\text{speedup} = \frac{\text{Time taken for a given computation by a non-pipelined functional unit}}{\text{Time taken for the same computation by a pipelined version}}$$

- Assume a function of k stages of equal complexity which takes the same amount of time T.
- Non-pipelined function will take kT time for one input

then $\text{speedup} = \frac{nkT}{(k+n-1)T} = \frac{nk}{(k+n-1)}$

For $s = 4$ i.e $k = 4$ and $n = 5$

$$\text{speedup} = \frac{5 \times 4}{(4+5-1)} = \frac{20}{8} = 2.5$$

2. Efficiency

- Efficiency can be defined as

Efficiency = Number of stage time units actually used during computation / Total number of stage time units available during that computation

- It is an indicator of how efficiently the resources of the pipeline are used.

$$\text{Efficiency} = \frac{nk}{k[k+(n-1)]}$$

For $k=4$ and $n=5$

$$\text{Efficiency} = \frac{5\times 4}{4[4+(5-1)]} = \frac{20}{4[4+4]} = \frac{20}{32} = 0.625$$

3. Throughput

- It is the average number of results computed per unit time.
- Throughput = Efficiency × Frequency

$$\text{Throughput} = \frac{n}{[k+n-1]T}$$

For $k=4$ and $n=5$

$$\text{Throughput} = \frac{5}{[4+5-1]T} = \frac{5}{8T} = 0.625\frac{1}{T}$$

Q.5 What is memory interleaving. Explain C-access memory organization

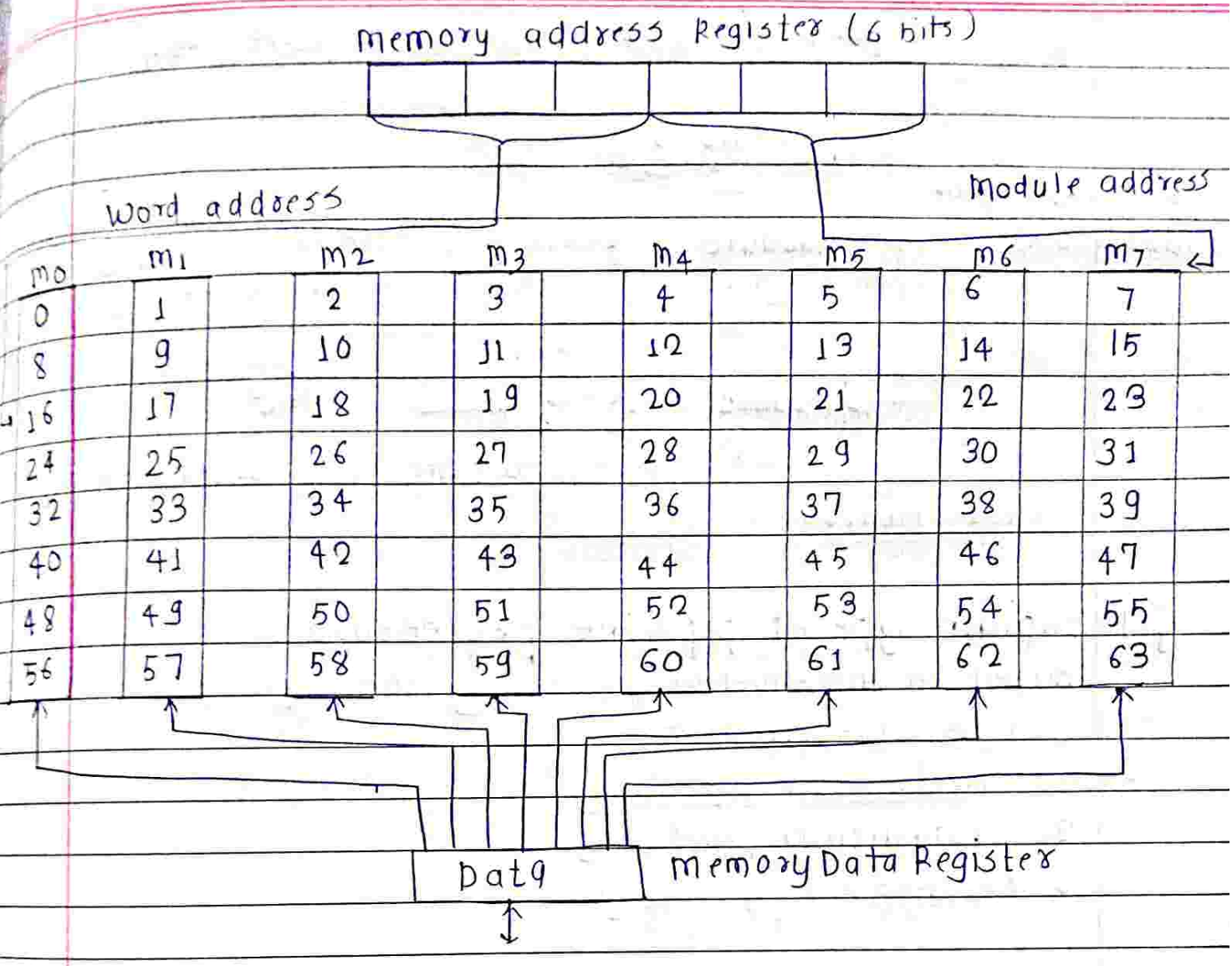
1. Memory interleaving is the technique used to increase the throughput.
2. The core idea is to split the memory system into independent banks, which can answer read or write requests in parallel.

3. It is done by interleaving the address space.
4. Consecutive cells in the address space are assigned to different memory banks
5. There are two types memory interleaving :
   i. Low order interleaving
      low order interleaving spreads contiguous memory location across the modules horizontally

   ii. High order interleaving
      High order interleaving uses the high order bits as the module address and the low order bits as the word address

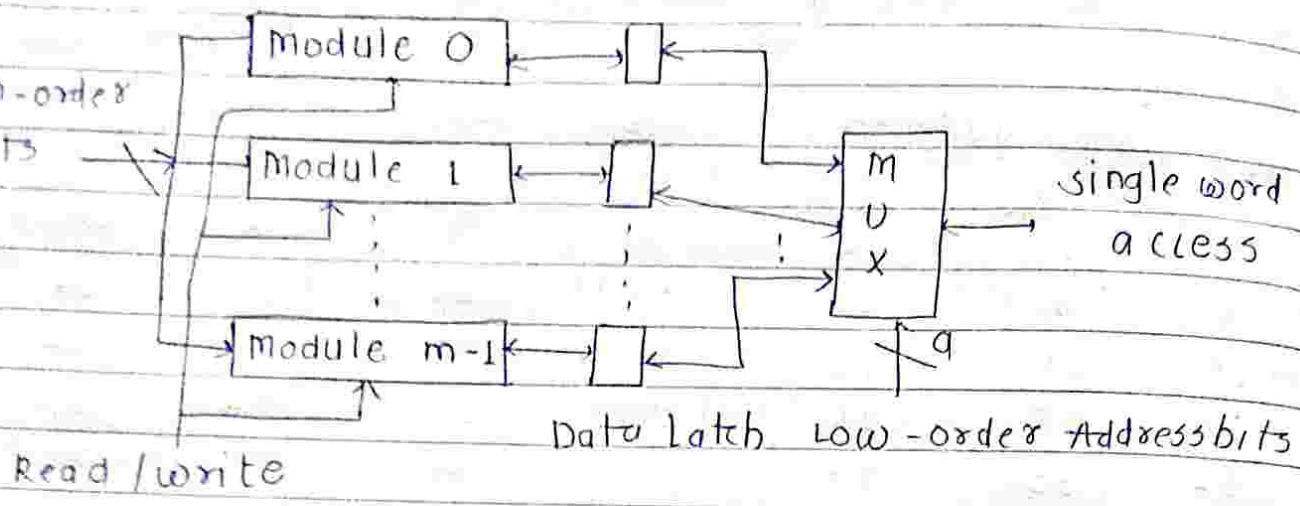
C- access memory organization
1. It is simple to high ordered interleaving
2. Lower order bits select modules
3. Higher order bits select words
4. It allows concurrent access
5. When a memory is N-way interleaved, we always find that $N = 2^k$.
   For $k=1$, we have 2-way interleaving
   For $k=2$, we have 4-way interleaving
   For $k=3$, we have 8-way interleaving
   For $k=4$, we have 16-way interleaving
6. In C-access memory organization, a main memory formed with $m = 2^a$ memory modules.
7. Each containing $w = 2^b$ words of memory cells.
8. a = low order bits, b = high order bits
   n = a+b (address length)

e.g. 8-way interleaved memory
$m = 8, w = 8, m = 2^3, w = 2^3 \therefore a = 3, b = 3$



Q.6 Explain s-access memory organization with diagram

1. It is simple to low ordered interleaving
2. High order bits select modules
3. Words from modules are latched at the same time
4. Low order bits select words from data latches.
5. This is done through the multiplexer with higher speed.
6. It allows simultaneous access.
7. At the end of each memory cycle $m = 2^q$ consecutive words are latched in the databuffer simultaneously.
8. Access phase of last access overlapped with fetch phase of the current access.
9. m words takes one memory cycle.



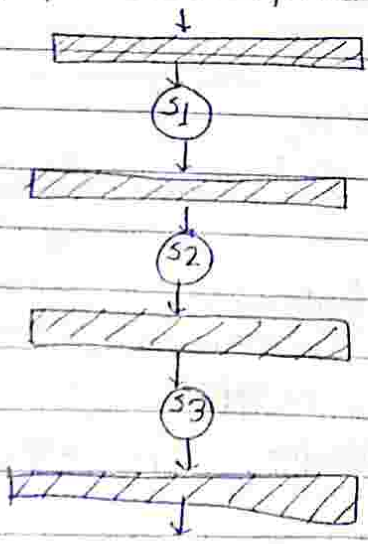
Q.7. Explain type of pipeline processors.

. Based on the level of processing, the pipelined processors can be classified as:

1. Arithmetic pipelining
2. Instruction pipelining
3. Processor pipelining

1. Arithmetic Pipelining

• The arithmetic logic units of a computer can be segmented for pipelined operations in various data formats



2. Instruction Pipelining

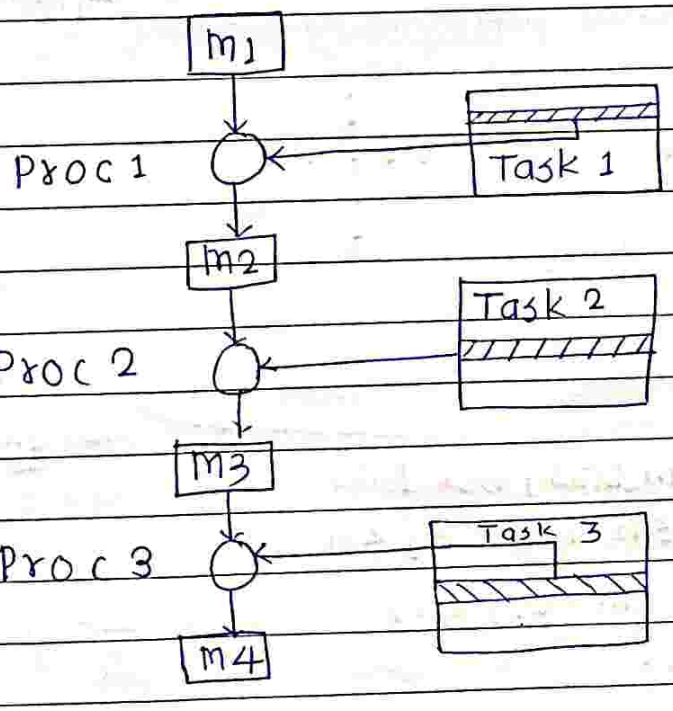
• The execution of a stream of instructions can be

pipelined by overlapping the execution of current instruction with the fetch, decode, and operand fetch of the subsequent instructions.

- It is also called instruction look-ahead

3. Processor Pipelining

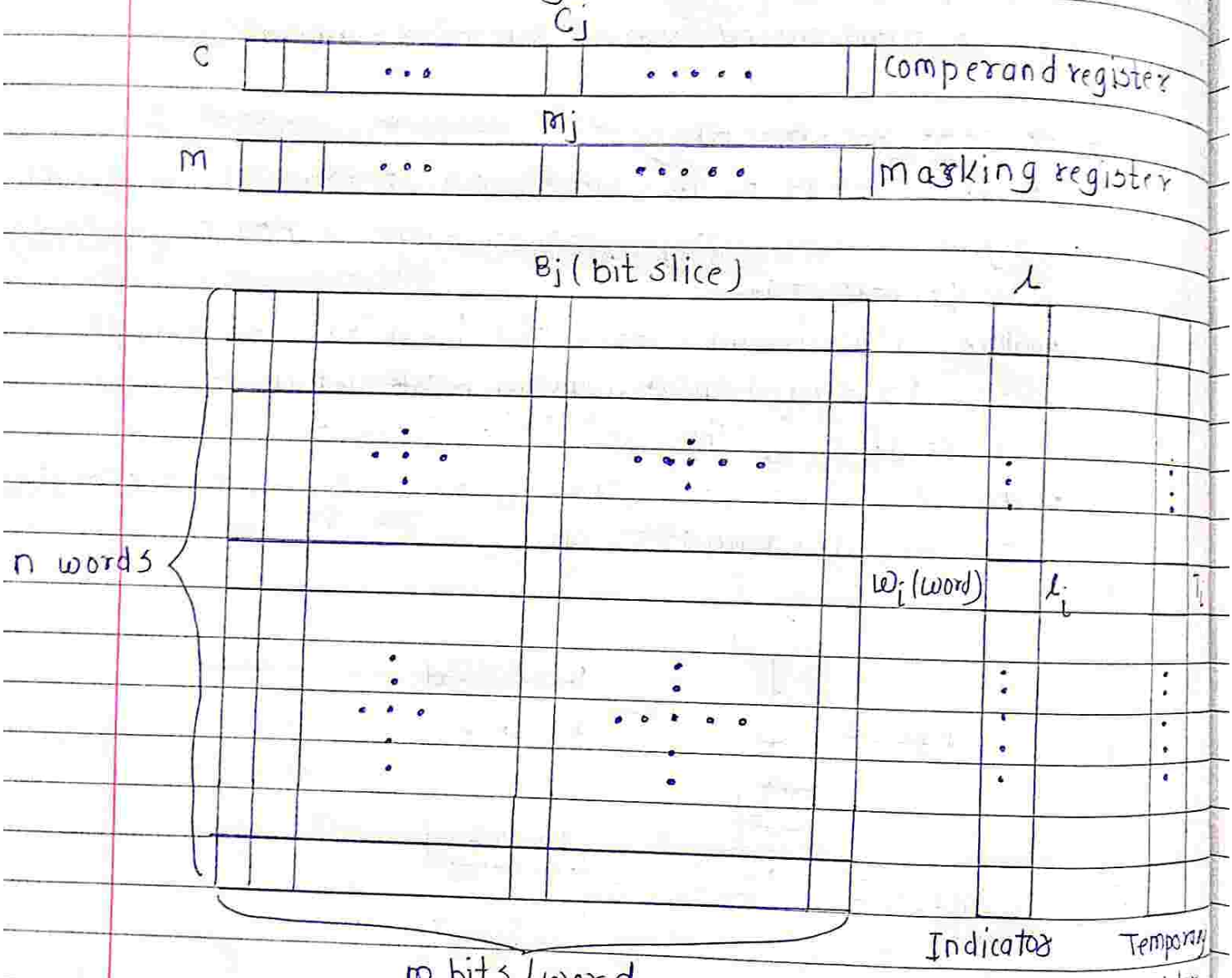
- This refers to the processing of same data stream by a cascade of processors each of which processes a specific task.
- The data stream passes the first processor with results stored in a memory block which is also accessible by the second processor.
- The second processor then passes the refined results to the third and so on



Q.8. Explain the structure of associative processor memory.

1. The associate memory is organized in w words with b bits per word.
2. In w × b array, each bit is called a cell
3. Each cell is made up of a flip-flop that contains some comparison logic gates for pattern match and read-

4 A group of bit cells of all the words at the same position in a vertical column is called bit slice as shown in figure.



5. Registers used in associative memory organizations
   - Comparand Register : Used to hold the operands which are being searched for, or being compared with.
   - Masking Register : Used to enable or disable the bit slices.
   - Indicator (I) and Temporary (T) Registers :

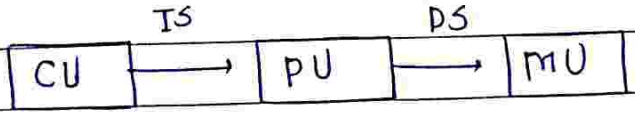
Indicator register is used to hold the current match patterns and temporary registers are used to hold the previous match patterns.

6. Bit parallel organization
All words are used in parallel. All bit slices which are not masked off by the masking pattern.

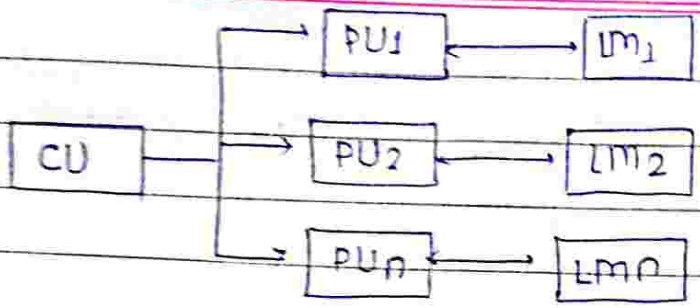
7. Bit serial organization
when the associative memory organization adopts bit serially then it is called bit serial organization.

Q.9. Explain Flynn's classification. Multiplicity of instruction stream and data stream
1. Flynn's classification refers to a classification of parallel computer architectures.
2. Parallel computers can be classified by the concurrency in processing sequences data or instructions from the perspective of an assembly language programmar.
3. Computers can be divided into the following major groups according to Flynn's classification.

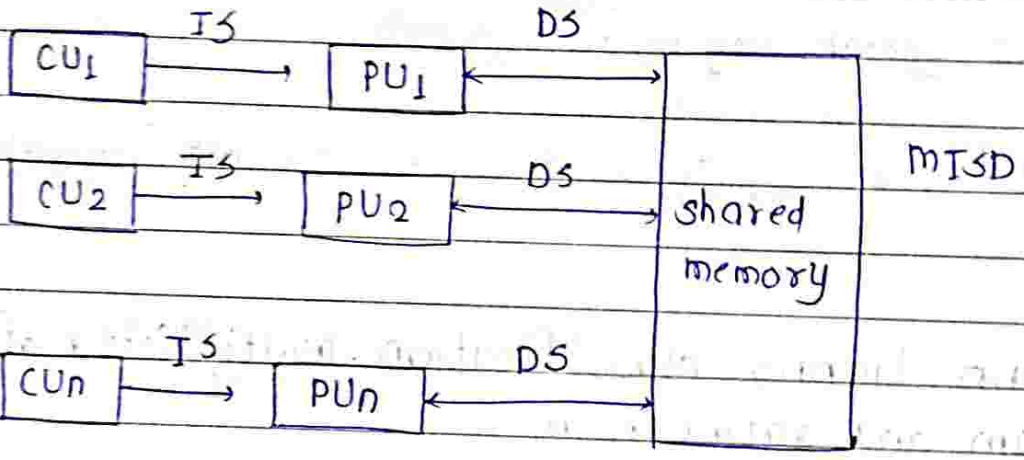
i. SISD : It depicts the structure of a single computer, which includes a control unit, a memory unit and a processor unit.



ii. SIMD : It symbolises an organization with a large number of processing units overseen by a central control unit.



iii. MISD : Because no real system has been built using the MISD structure, it is primarily of theoretical importance.



iv. MIMD : All processors of a parallel computer could execute distinct instructions and act on different data at the same time in this configuration