KOLHAPUR INSTITUTE OF TECHNOLOGY'S,
COLLEGE OF ENGINEERING (AUTONOMOUS), KOLHAPUR
(AFFILIATED TO SHIVAJI UNIVERSITY, KOLHAPUR)

MSE

S. Y. B. Tech. (Computer Science & Engineering) (Sem-III)
MID SEMESTER EXAMINATION, SEPTEMBER-2019
Digital Logic Design & Microprocessor (UCSE0304)

Day and Date: Saturday,21/09/2019
Time: 10:00 AM to 12:00 Noon

PRN No:

Max Marks- 50

Instructions:

i) **All questions are compulsory.**
ii) **Figure to right indicates full Marks.**
iii) **Assume suitable data wherever necessary.**

		Marks	CO's	B.L
Q.1	**Attempt any three**	**18**		
A	Expand the expression f = A(A'+B)(A'+B+C') to minterms and maxterms	6	CO1	L2
B	Illustrate Flag Register in Detail	6	CO2	L2
C	Explain Half & Full adders. Also draw full adder using Two half adder	6	CO1	L2
D	Minimize the logic function using K-map F(A,B,C,D)=∑M(4,6,10,12,13,15)	6	CO1	L3
Q.2	**Attempt any two**	**16**		
A	Design a 4-bit a) Ring Counter b) Mod-10 counter	8	CO1	L3
B	Explain Architecture of 8085 in detail	8	CO2	L2
C	How JK flip flop solves invalid input problem of SR flip flop. Also explain ways to overcome Race around condition	8	CO1	L1
Q.3	**Attempt any two**	**16**		
A	Draw and explain following Registers. 1)SISO 2) SIPO 3) PISO 4) PIPO	8	CO1	L3
B	Draw opcode fetch & memory write machine cycle diagram.	8	CO2	L3
C	Compare synchronous and Ripple counters. Also construct 2-bit synchronous counter.	8	CO1	L2

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