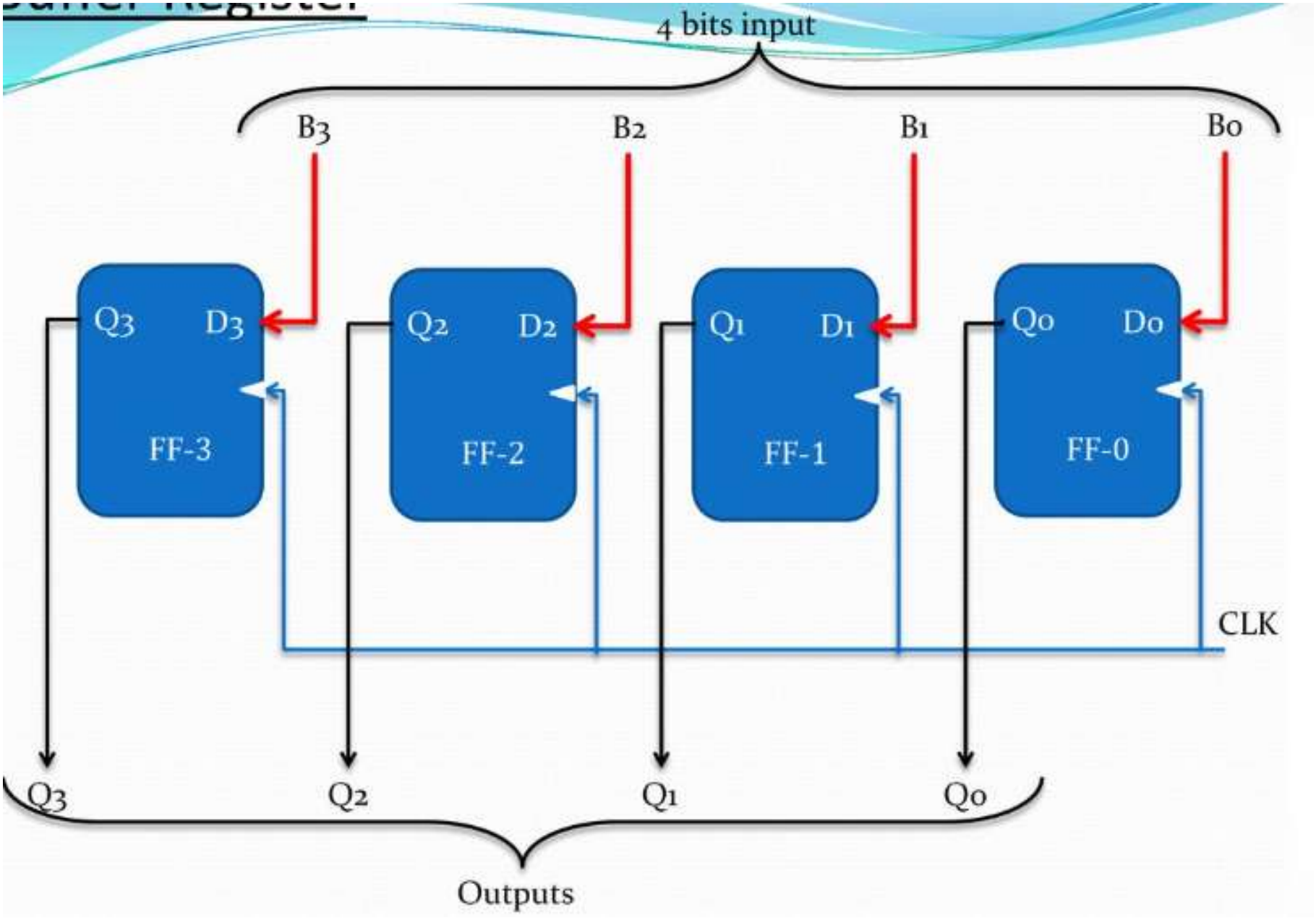
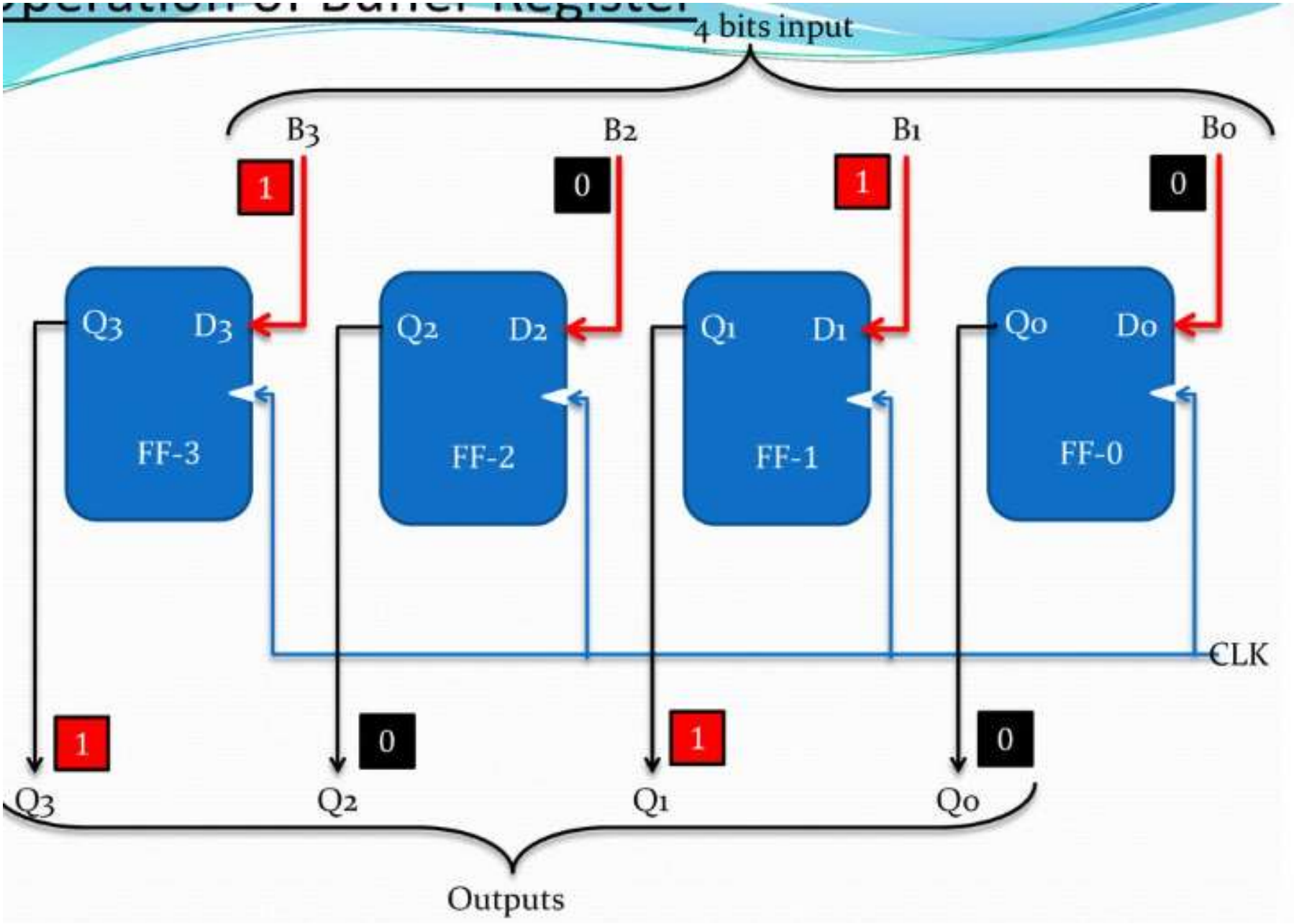
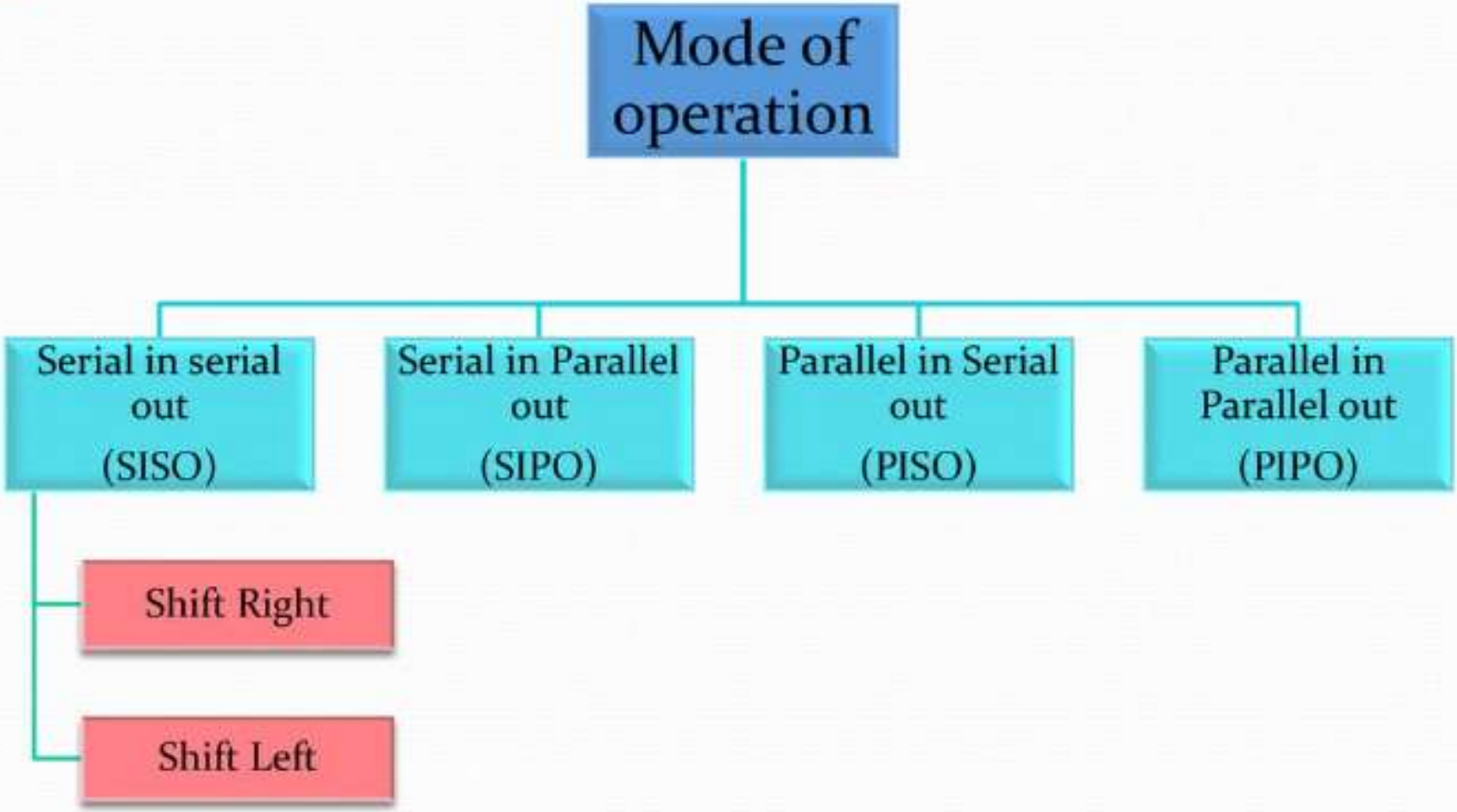
Shift registers


4 bits input
B3
B2
B1
B0
Q3
D3
FF-3
Q2
D2
FF-2
Q1
D1
FF-1
Q0
D0
FF-0
CLK
Q3
Q2
Q1
Q0
Outputs


4 bits input
B3
B2
B1
B0
1
0
1
0
Q3
D3
Q2
D2
Q1
D1
Q0
D0
FF-3
FF-2
FF-1
FF-0
CLK
1
0
1
0
Q3
Q2
Q1
Q0
Outputs

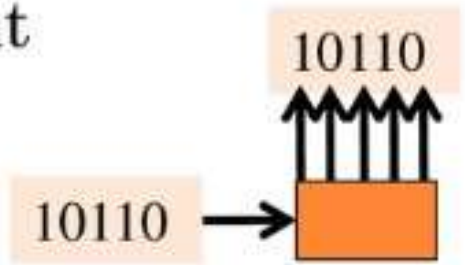
Classification of Registers :



Combinations of Data Transfer Methods

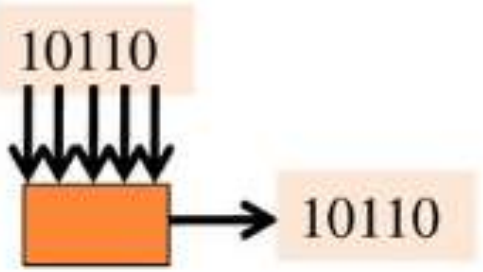
- SISO: Serial In, Serial Out

- SIPO: Serial In, Parallel Out

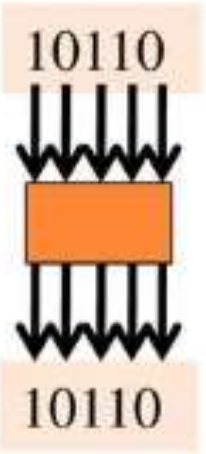


Combinations of Data Transfer Methods

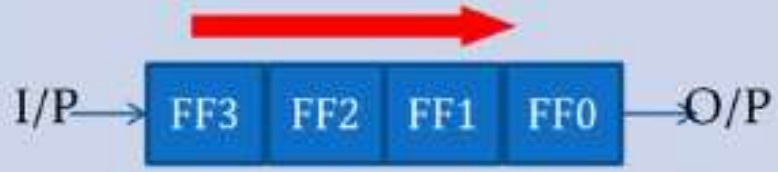
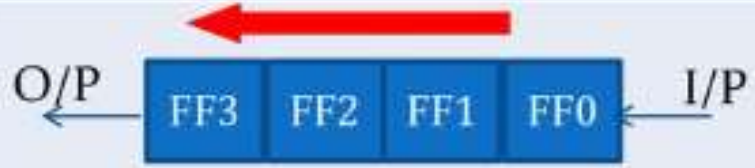
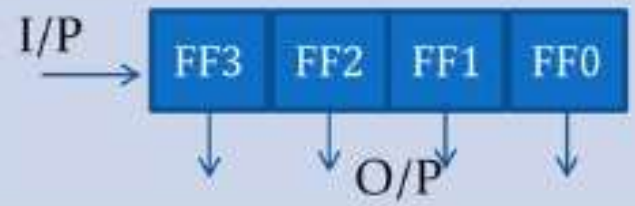
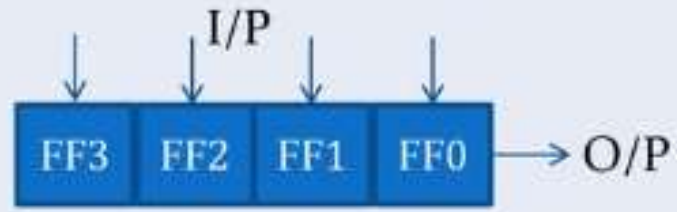
- PISO: Parallel In, Serial Out



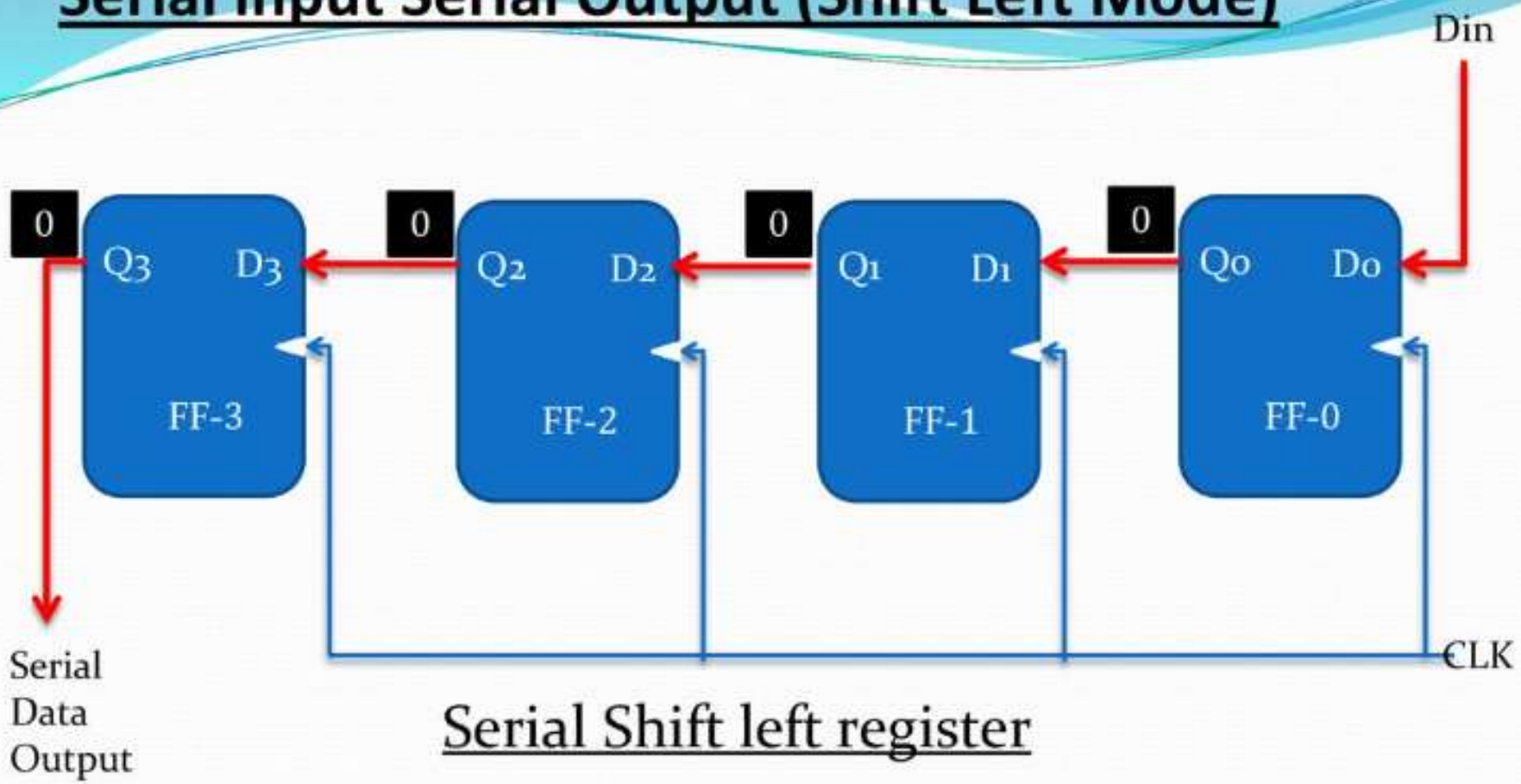
- PIPO: Parallel In, Parallel Out



Shift Register

Sr. No.	Mode	Illustrative Diagram	Comments
1.	SISO (Shift Right)		Data bits shift from Left to Right by 1 position per clock cycle.
2.	SISO (Shift Left)		Data bits shift from Right to Left by 1 position per clock cycle.
3.	SIPO		All o/p bits are made aval. simult. after **4-clcok pulse**
4.	PISO		All i/p bits are applied simult and. After **4-clk pulse** the required o/p is available serially.

Serial input Serial Output (Shift Left Mode)



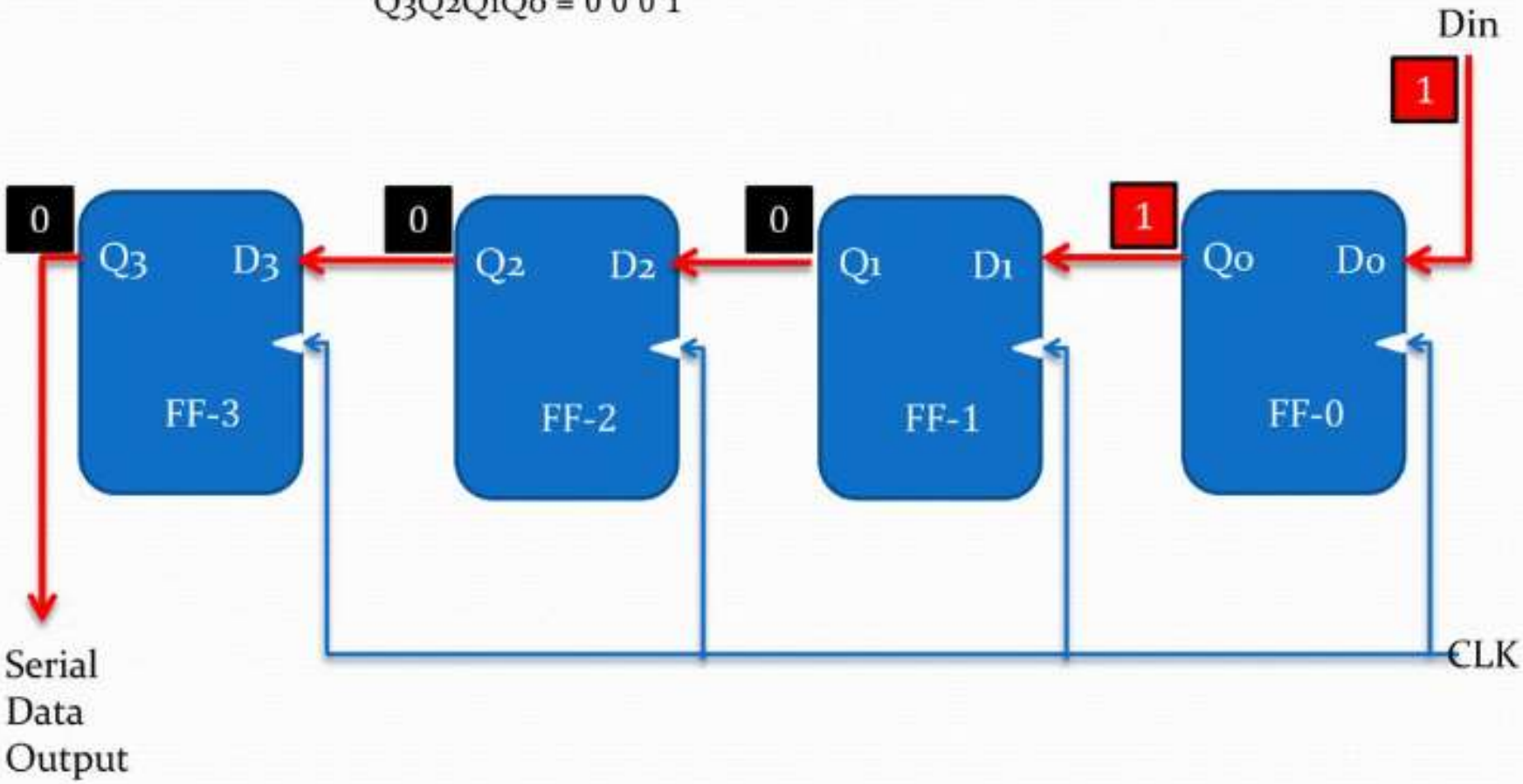
Serial Shift left register

- Before application of clock let assume all outputs are zero and apply MSB bit of the number to entered to Din. So Din = Do = 1.

Serial input Serial Output (Shift Left Mode)

- Apply the clock . On the first falling edge of clock, the FF-0 is SET and the stored data in the register is

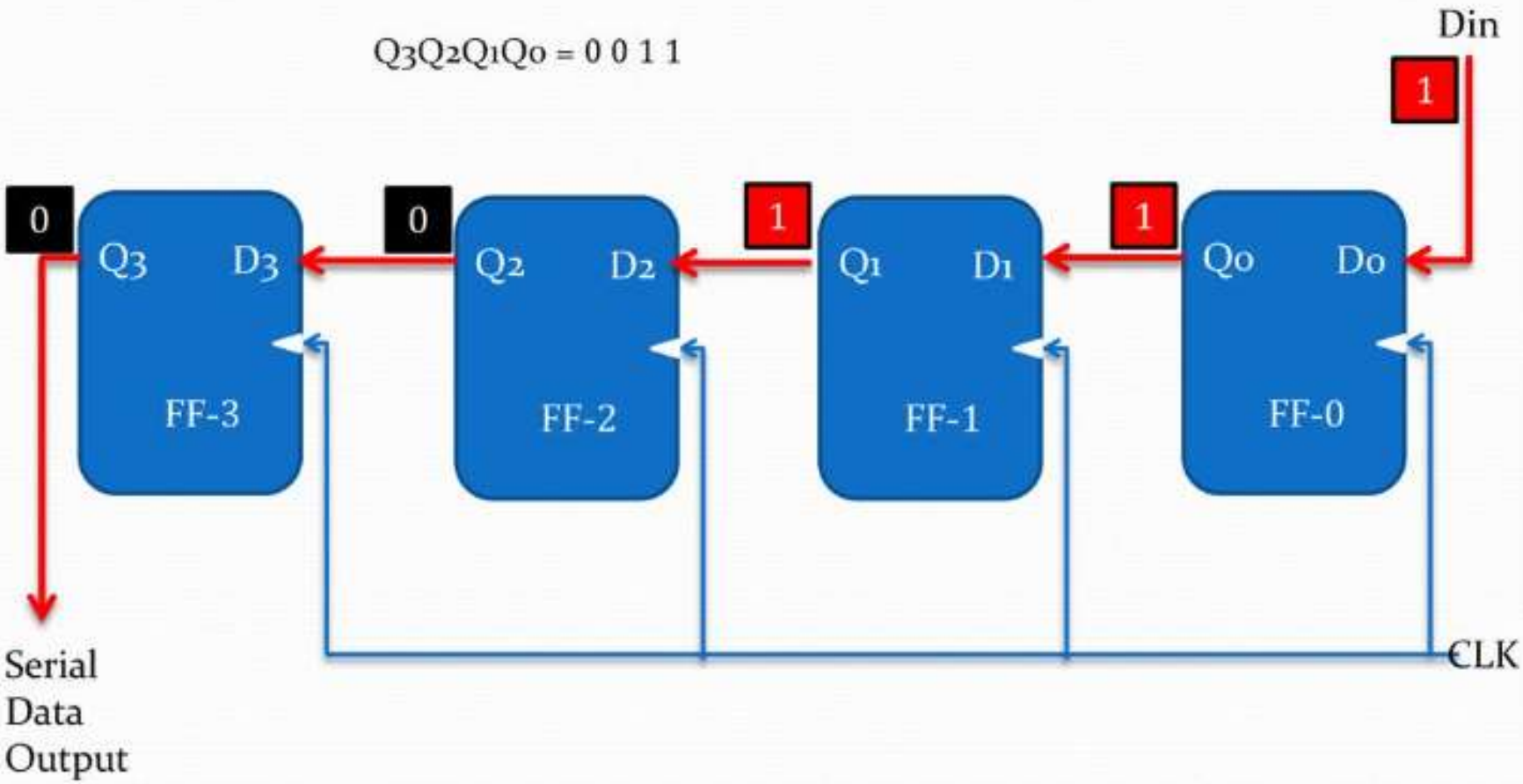
$Q_3Q_2Q_1Q_0 = 0\ 0\ 0\ 1$



Serial input Serial Output (Shift Left Mode)

- Apply the NEXT bit to Din . So if Din =1.
- As soon as the next positive edge of the clock hits. FF- 1 will SET and the stored data changes to,

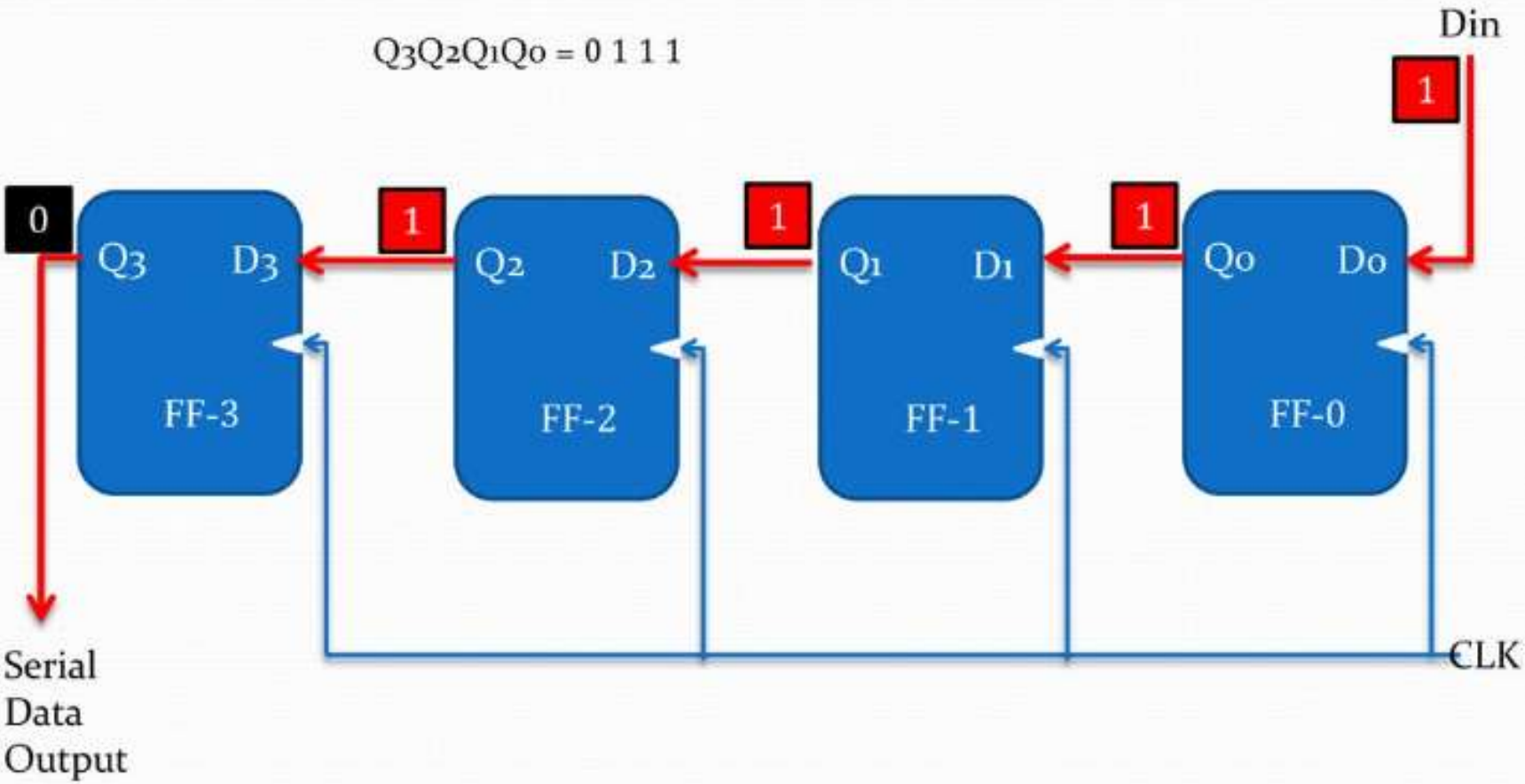
$Q_3Q_2Q_1Q_0 = 0\ 0\ 1\ 1$



Serial input Serial Output (Shift Left Mode)

- Apply the NEXT bit to Din . So if Din =1.
- As soon as the next positive edge of the clock hits. FF- 2will SET and the stored data changes to,

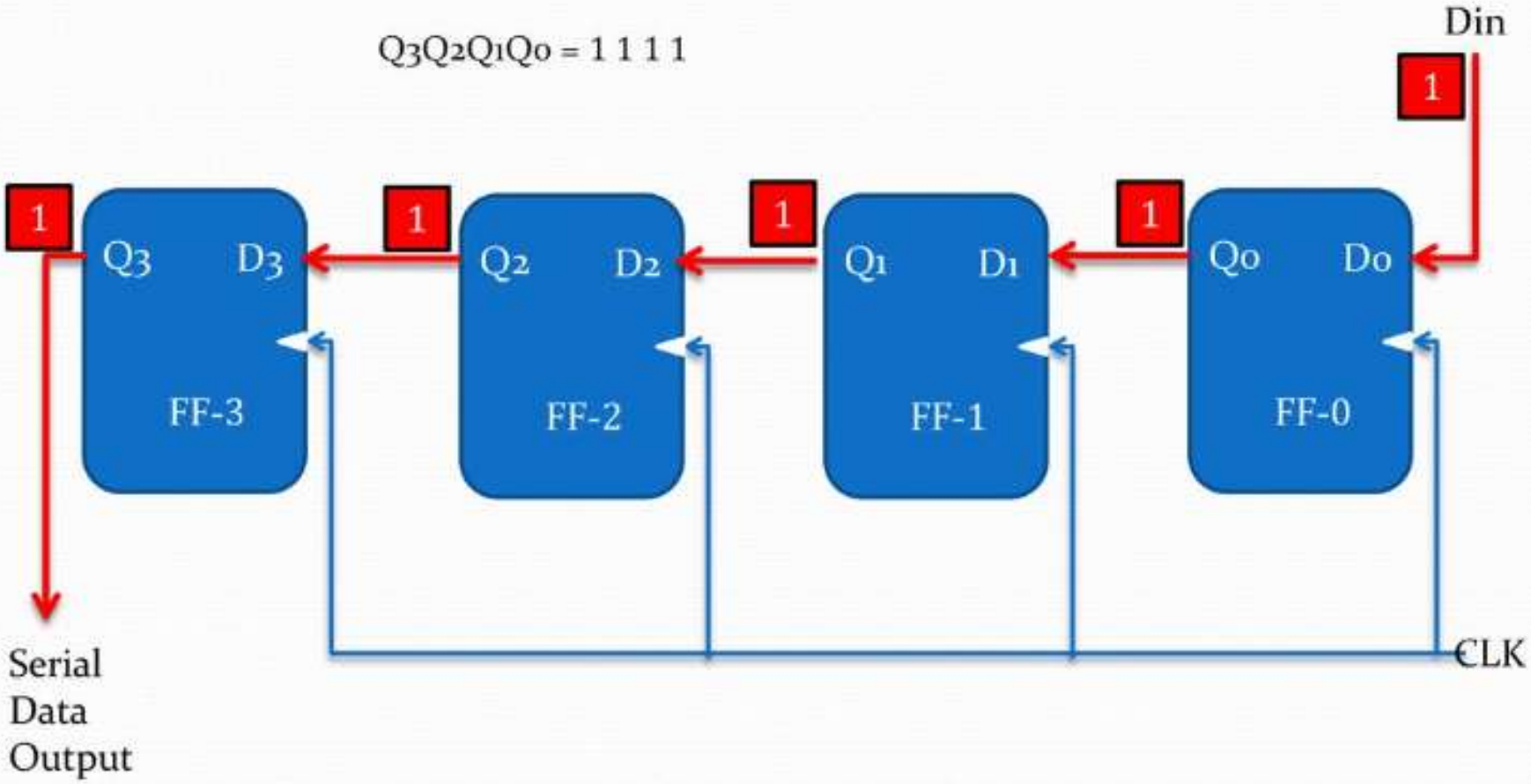
$Q_3Q_2Q_1Q_0 = 0\ 1\ 1\ 1$



Serial input Serial Output (Shift Left Mode)

- Apply the NEXT bit to Din . So if Din =1.
- As soon as the next positive edge of the clock hits. FF- 3will SET and the stored data changes to,

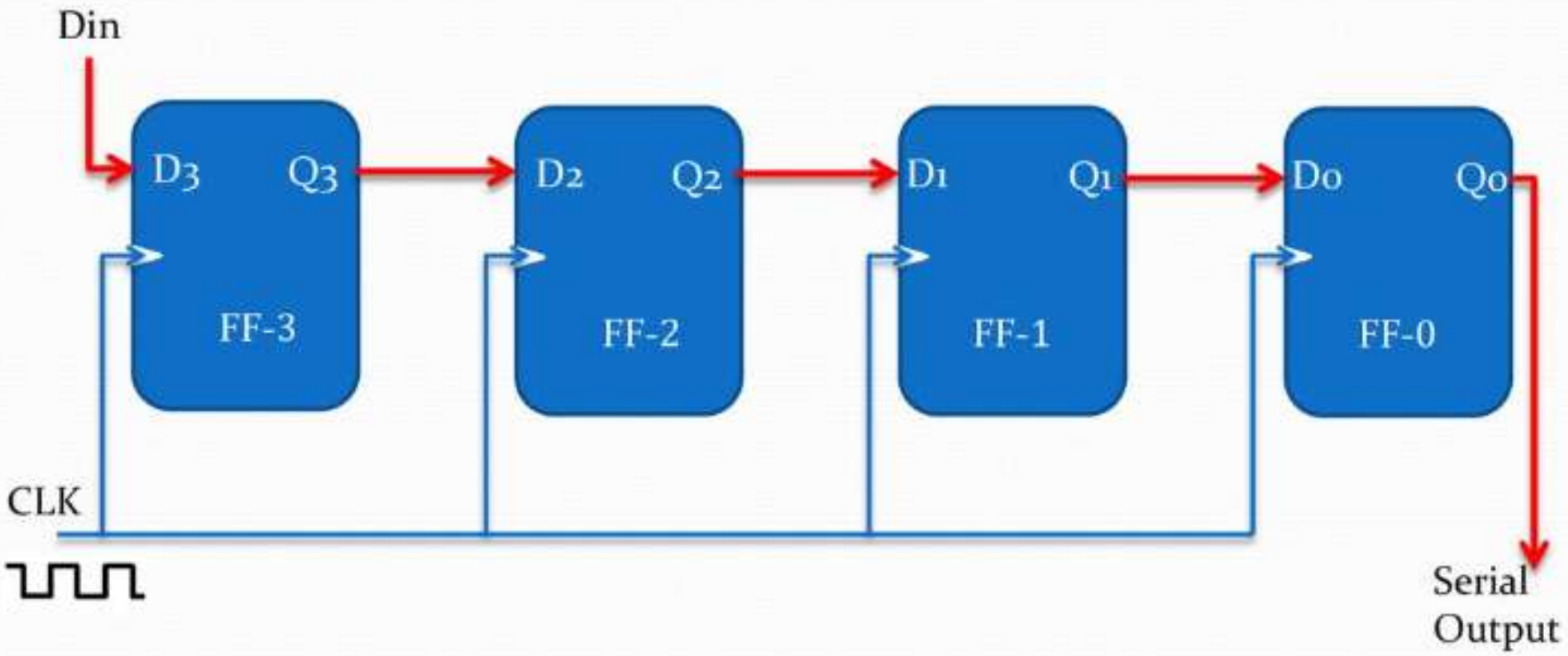
$Q_3Q_2Q_1Q_0 = 1\ 1\ 1\ 1$



Summary of shift left operation

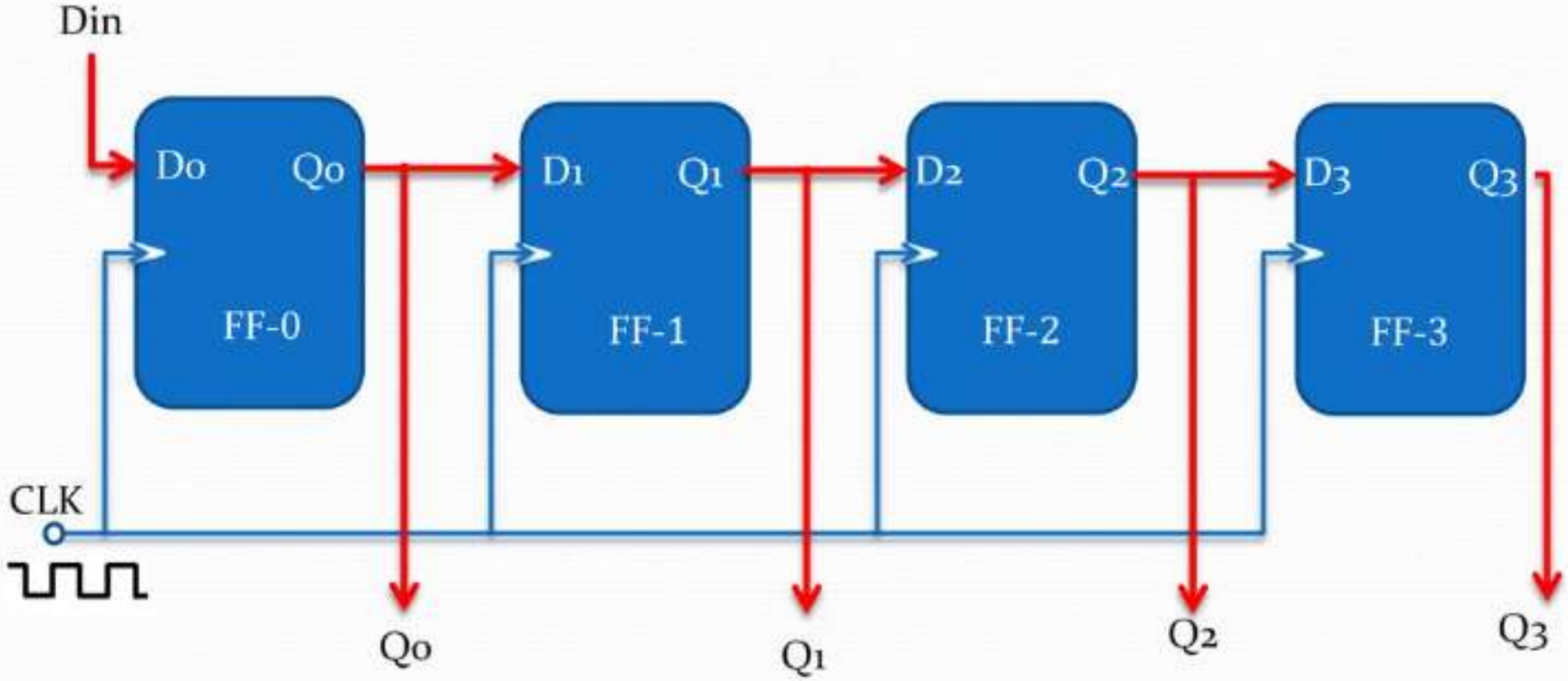
CLK	Q_3	$Q_2=D_3$	$Q_1=D_2$	$Q_0=D_1$	Serial input Din = Do
	0	0	0	0	
↑	0	0	0	1	1
↑	0	0	1	1	1
↑	0	1	1	1	1
↑	1	1	1	1	1

Serial input Serial Output (Shift Right Mode)



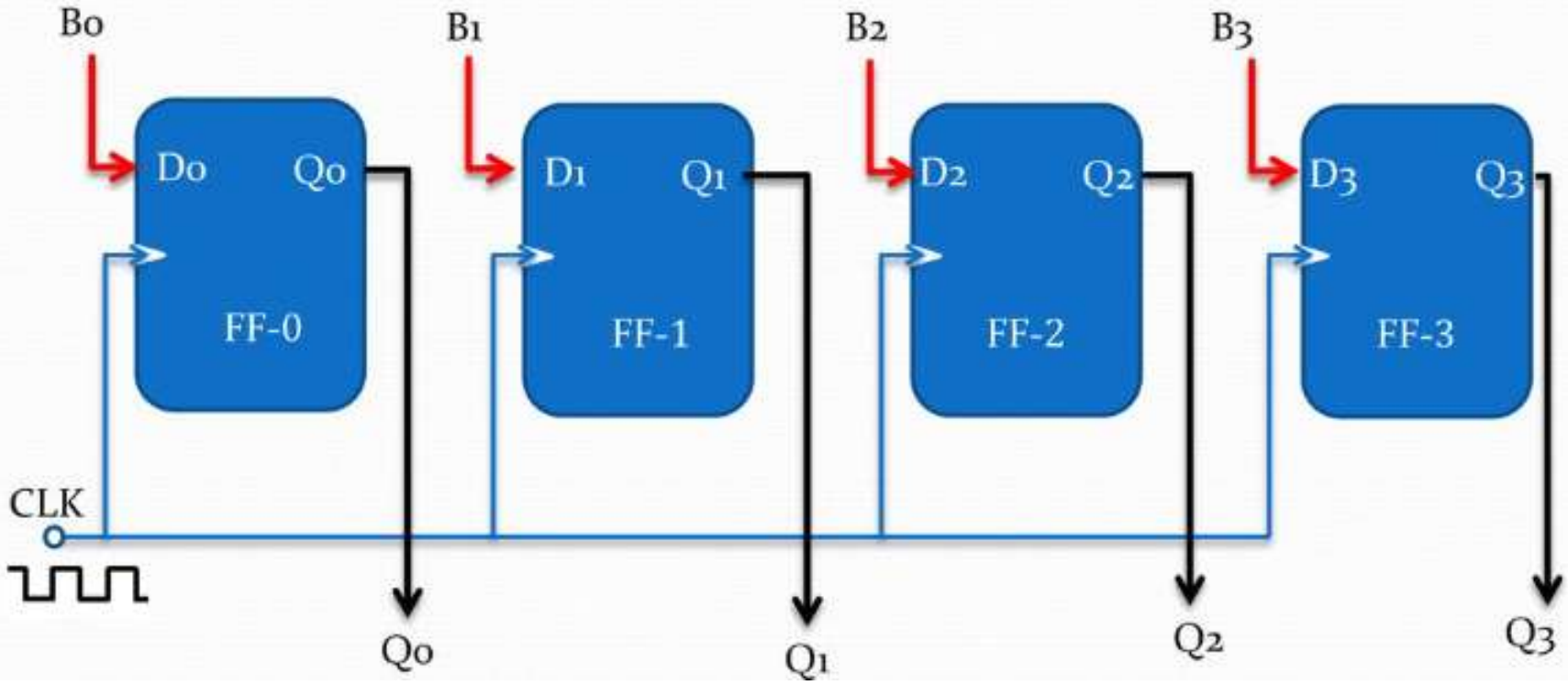
Serial input Parallel Output (SIPO)

- In this operation the data is entered serially and taken out in parallel.
- That means first the data is loaded bit by bit. The output are disabled as the loading is taking place.
- Number of clock cycles required to load a four bits data is 4. Hence the speed of operation of SIPO mode is same as that of SISO mode.



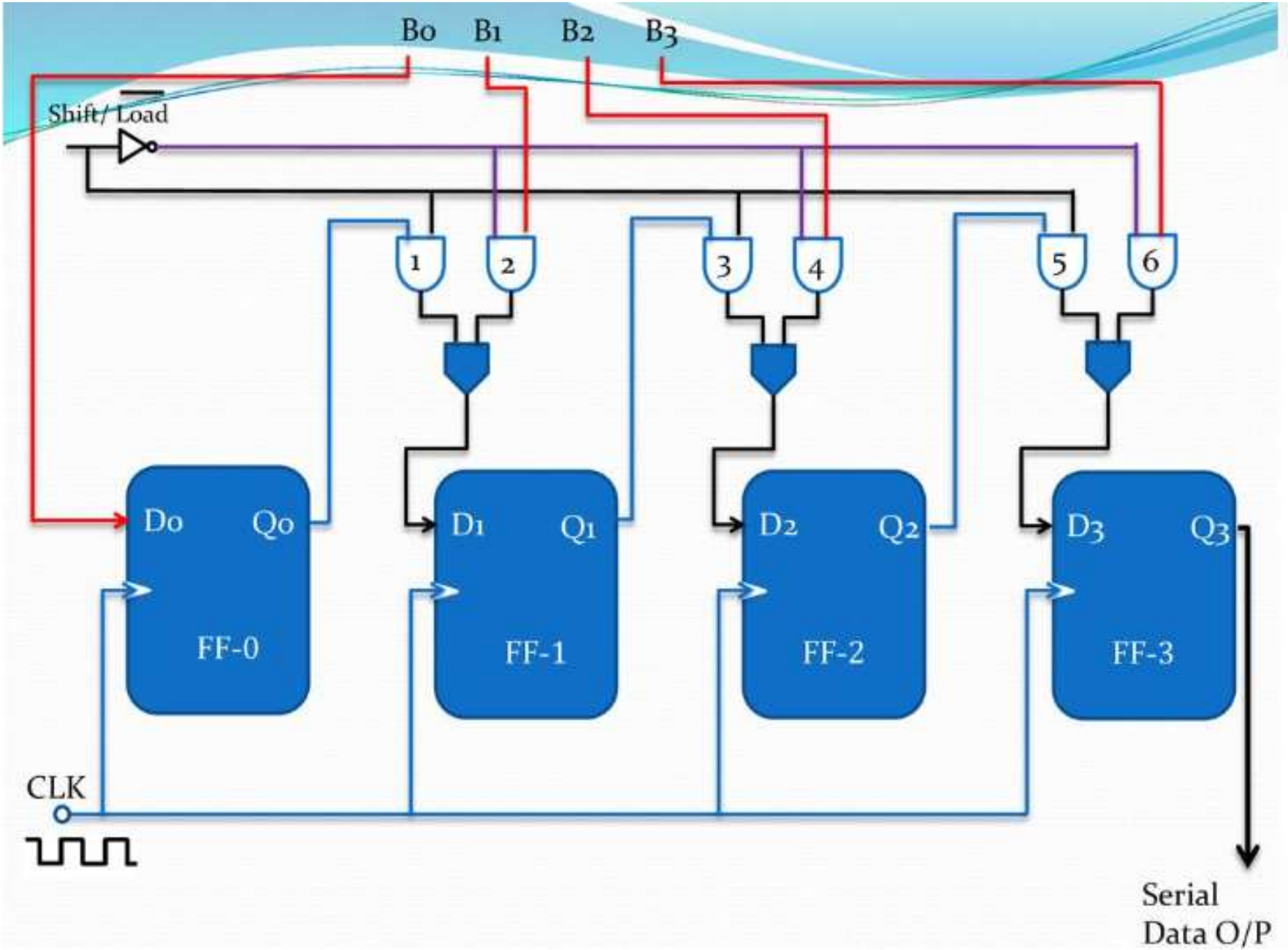
Parallel input Parallel Output (PIPO)

- In this operation the data are entered parallel.
- The 4-bit binary input B_0, B_1, B_2, B_3 is applied to data inputs D_0, D_1, D_2 and D_3 respectively of the four flip-flops.
- As soon as a positive clock edge is applied, the input binary bits will be loaded into the flip-flops simultaneously.
- The loaded bits will appear simultaneously to the output side. **ONLY ONE CLOCK IS ESSENTIAL TO LOAD ALL THE BITS.**

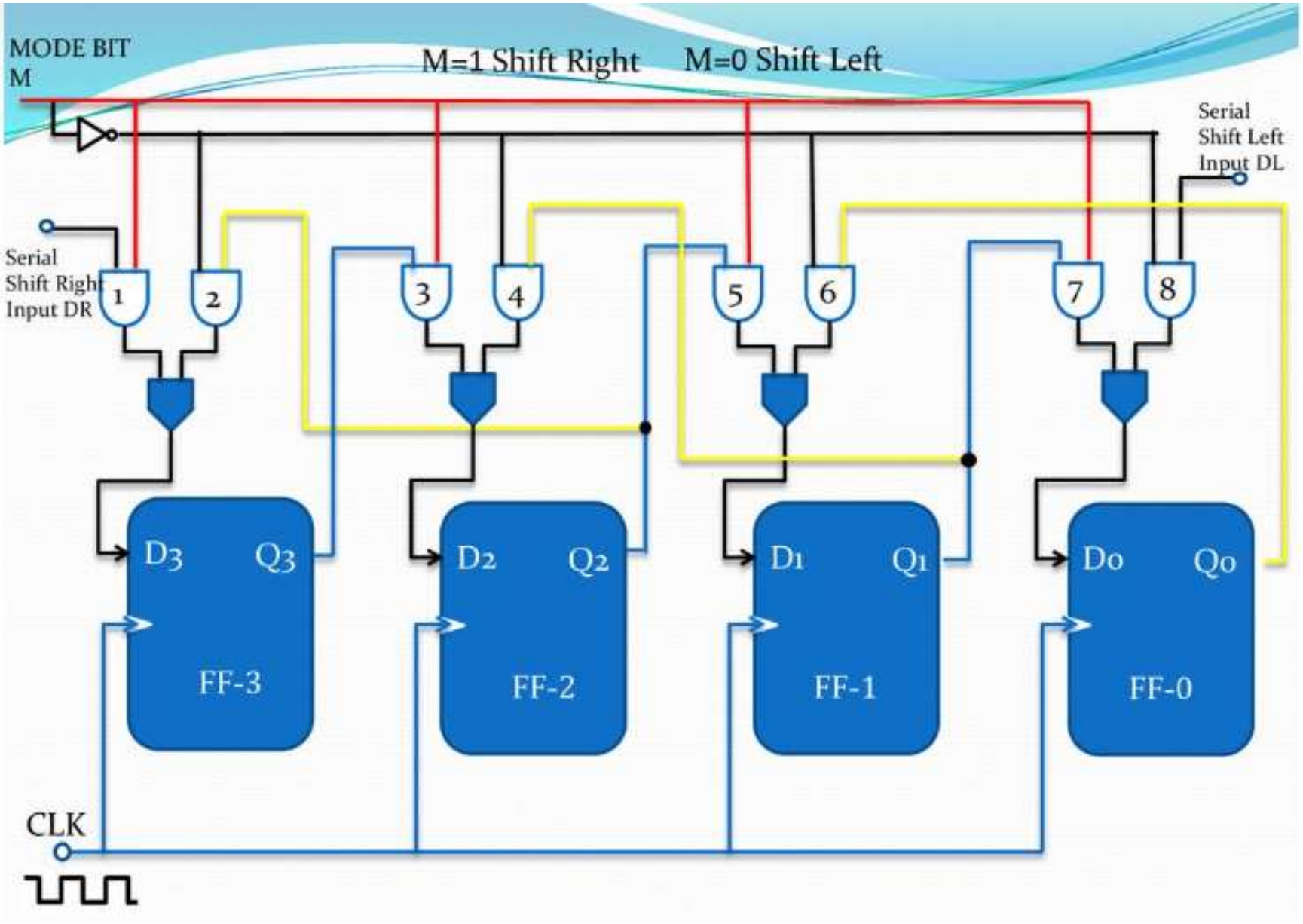


Parallel input Serial Output (PISO)

- In this operation the data are entered parallel.
- Output of pervious FF is connected to the input of the next via a combinational circuit.
- The binary input data B_0, B_1, B_2, B_3 is applied through the same the combinational circuit.
- There are two modes in which this circuit can work namely **shift mode or load mode**.


B0
B1
B2
B3
Shift/ Load
1
2
3
4
5
6
D0
Q0
FF-0
D1
Q1
FF-1
D2
Q2
FF-2
D3
Q3
FF-3
CLK
Serial
Data O/P

4 bit bidirectional shift registers



4-bits Universal Shift Register

Mode Control		Register Operation
S_1	S_0	
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel load

Applications of shift Register

1. For Temporary data storage.
2. For multiplication and division
3. As a delay line
4. Ring Counter
5. Parallel to serial converter