MSE (SEM-III)

KOLHAPUR INSTITUTE OF TECHNOLOGY'S,
COLLEGE OF ENGINEERING (AUTONOMOUS), KOLHAPUR
(AFFILIATED TO SHIVAJI UNIVERSITY, KOLHAPUR)

Second Year B. Tech. (Computer Science & Engineering)

MID SEMESTER EXAMINATION, SEPTEMBER 2018

DIGITAL LOGIC DESIGN & MICROPROCESSORS (UCSE0304)

Day and Date: Friday, 21/09/2018
Time: 09:30 AM to 11:30 AM

PRN No. :

Max Marks- **50**

Instructions:

i) All questions are compulsory.
ii) Figure to right indicate full Marks.
iii) Assume suitable data wherever necessary.

		Marks	CO's	Blooms Level	PO Level
Q.1	**Attempt any three**	**18**			
A	Explain Design of Full Adder	6	CO1	L1	PO1
B	Convert Following Numbers to mentioned number systems: i) $(6327)_8 = (?)_{10}$ ii) $(2F9A)_{16} = (?)_2$ iii) $(95.5)_{10} = (?)_{16}$	6	CO1	L2	PO1
C	Describe Flag Register of 8085	6	CO2	L1	PO3
D	Minimize the logic function using K-map $F(A,B,C,D)=\sum m(0,1,2,3,5,7,8,9,11,14)$	6	CO1	L2	PO1
Q.2	**Attempt any two**	**16**			
A	Implement $F(A,B,C,D) =\sum m(1,4,5,7,9,12,13)$ using 4x1 MUX	8	CO1	L4	PO1
B	What is Addressing Mode? Explain Different Addressing Modes in 8085 with example	8	CO2	L4	PO3
C	What are vectored interrupts? How interrupt is handled in 8085?	8	CO2	L2	PO3
Q.3	**Attempt any two**	**16**			
A	Design 4 bit UP –Ripple Counter	8	CO1	L3	PO1
B	Draw and Explain 8085 Architecture	8	CO3	L3	PO2
C	In 8085 how multiplexed address lines are de-multiplexed?	8	CO3	L3	PO2

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