

## 8085 Microprocessor

## \* The 8085-MPU

- i) 8-bit general purpose microprocessor
- ii) 40-pin IC package
- iii) 8085 This 5 indicates +5V power supply.
- iv) 8-bit data bus  $2^8 = 256$  bits
- v) 16-bit address bus  $2^{16} = 65536$  bits = 64KB
- vi) max frequency = 3MHz

## 1] Arithmetic &amp; logic unit (ALU)

- i) It performs the arithmetic & logic operations such as addition, subtraction, AND, OR etc.
- ii) It uses data from memory & from accumulator to perform operations.
- iii) The result of operations are stored in the accumulator

## 2] Accumulator

- i) 8-bit register
- ii) 'A'  $\rightarrow$  Accumulator
- iii) store the result of operations

## 3] Registers:

- i) 6 registers, one accumulator, one flag
- ii) B, C, D, E, H, L  $\rightarrow$  8-bit registers.

B	C
D	E
H	L

- iii) 3 register pairs  $\rightarrow$  B-C, D-E, H-L to handle 16-bit data.



iv) The programmer uses these registers to store or copy data into register by using data copy instructions.

4] Flag registers :- (8 bit register)

- i) 5 Flip/Flops
- ii) flags are set or reset after an operation according to data condition of the result in the accumulator and other registers.

D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
S	Z	AC		P			CY

① sign flag (s)

② zero flag (z)

③ Auxiliary Carry (AC)

④ Parity (P)

⑤ Cy (carry)

- ① S = 1 (set) → negative  
= 0 (reset) → positive
- ② P = 1 (set) → even no. of 1's  
= 0 (reset) → odd no. of 1's
- ③ Z = 1 (set) → result = 0  
= 0 (reset) → result ≠ 0
- ④ AC = 1 (set) → D<sub>3</sub> generates a carry  
it is used internally for BCD operations.
- ⑤ CY = 1 (set) → an arithmetic op. generates a carry.

Two 16-bit registers

- Stack pointer (SP)
- Program counter (PC)

5] Program counter :-

- i) deals with sequencing in the execution of instructions.
- ii) memory register.
- iii) MP uses this register to hold the address of the next instruction.
- iv) PC points to the memory location from which the next byte is to be fetched.
- v) When a byte is fetched, the program counter is automatically incremented by one to point to the next memory location.

6] Stack pointer :-

- i) 16 bit memory register
- ii) It points to a memory location in RAM memory called stack.
- iii) The beginning - [ → an array of memory locations of the stack is defined by loading 16-bit address in the stack pointer

7] Instruction Register/Decoder :-

- i) 8-bit register that temporarily stores the current instruction of a program.
- ii) Decoder decodes or interprets the instruction.
- iii) Decoded instruction is then passed to the next stage.

8] Control unit :-

- i) Generates signals on data bus, address bus, and control bus within microprocessor to carry out the instruction which has been decoded.



8.1) Data bus:- Carries data in binary form between microprocessor & other external units.

It is used to transmit data, result of arithmetic and logic operations.

8-bit data bus

Bidirectional

$D_0 - D_7$

8.2) Address bus:- It carries addresses of the memory locations or other devices.

16-bit  $A_0 - A_{15}$

unidirectional

$A_0 - A_7$

Lower order

address / bus

+

multiplexed with

data bus ( $D_0 - D_7$ )

↓

$AD_0 - AD_7$

$A_8 - A_{15}$

Higher order

Address bus

8.3) Control bus:- i) It provides lines which have specific functions for coordinating and controlling microprocessor operations.  
ii) Carries control signals partly unidirectional & partly <sup>bi</sup>directional.

9) Control and status signal

① ALE (output) Address Latch enabled

It is a pulse provided when an address appears on  $AD_0 - AD_7$  lines.

$ALE = 1 \rightarrow$  Address

$ALE = 0 \rightarrow$  data



②  $\overline{RD}$  (active low)

→ ~~RD~~ signal = 0 → active → performs read operation  
→ — 1 — 1 → inactive.

→ The read signal indicates that data are being read from the selected I/O or memory device & that they are available on the data bus.

③  $\overline{WR}$  (active low signal) :- The write signal indicates that data on the data bus are to be written into a selected memory or I/O location.

④  $IO/\overline{M}$  :- Input-Output | Memory signal.  
↓ (Active High)      ↓ (Active Low)  
↓                      ↓  
1                      0

when  $IO/\overline{M} = 0 \rightarrow$  memory operation

— 1 — 1 → Input-Output — 0 —

⑤ Status signal :-  $S_1$  &  $S_0$

$S_1$	$S_0$	States of MP
0	0	Halt
0	1	Write
1	0	Read
1	1	Fetch

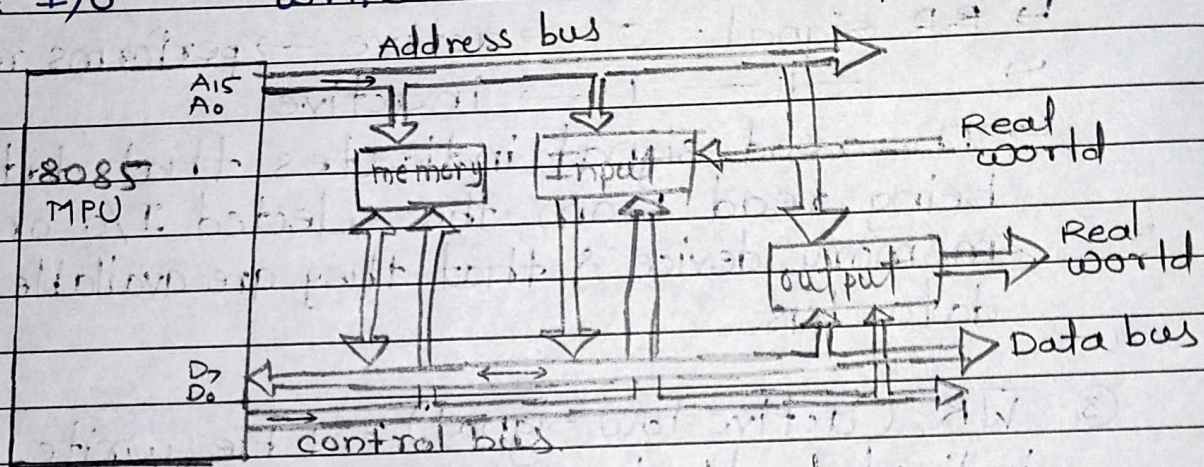


\* Memory read  $\rightarrow$  data/instruction from memory.

- \* Memory write  $\rightarrow$  write into memory.

- \* I/O read  $\rightarrow$  data/instr. from I/O device.

- \* I/O write  $\rightarrow$  write into output devices



8085-Bus structure, itai



# \* Pin diagram of 8085

$X_1$	1	8085 Microprocessor	40	Vcc
$X_2$	2		39	HOLD
RESET OUT	3		38	HLDA
SOD	4		37	CLK (OUT)
SID	5		36	RESET IN
TRAP	6		35	READY
RST 7.5	7		34	IO/M
RST 6.5	8		33	$S_1$
RST 5.5	9		32	$\overline{RD}$
INTR	10		31	$\overline{WR}$
$\overline{INTA}$	11		30	ALE
AD <sub>0</sub>	12		29	$S_0$
AD <sub>1</sub>	13		28	A <sub>15</sub>
AD <sub>2</sub>	14		27	A <sub>14</sub>
AD <sub>3</sub>	15		26	A <sub>13</sub>
AD <sub>4</sub>	16		25	A <sub>12</sub>
AD <sub>5</sub>	17		24	A <sub>11</sub>
AD <sub>6</sub>	18		23	A <sub>10</sub>
AD <sub>7</sub>	19		22	A <sub>9</sub>
V <sub>ss</sub>	20		21	A <sub>8</sub>