Intel 80286

Salient features of 80286

- High performance microprocessor with memory management and protection
  - 80286 is the first member of the family of advanced microprocessors with built-in/on-chip memory management and protection abilities primarily designed for multi-user/multitasking systems
- Available in 12.5MHz, 10MHz & 8MHz clock frequencies

Salient features of 80286

bus and memory sizes cont…

- The 80286 CPU, with its 24-bit address bus is able to address 16MB of physical memory.
- 1GB of virtual memory for each task

Microprocessor	Data bus width	Address bus width	Memory size
8086	16	20	1M
80186	16	20	1M
80286	**16**	**24**	**16M**

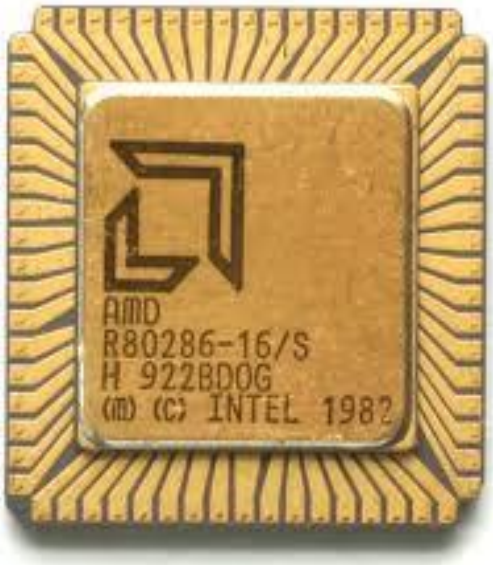
Salient features of 80286 Operating Modes

Intel 80286 has 2 operating modes:

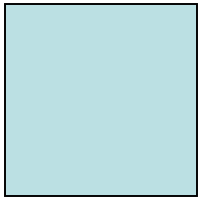
- Real Address Mode :
  - 80286 is just a fast 8086 --- up to 6 times faster
  - All memory management and protection mechanisms are disabled
  - 286 is object code compatible with 8086
- Protected Virtual Address Mode
  - 80286 works with all of its memory management and protection capabilities with the advanced instruction set.
  - it is source code compatible with 8086

Salient features of 80286 cont…

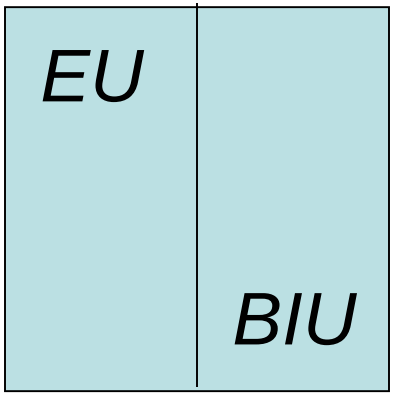
- 286 includes special instructions to support operating system.
  - for example, one instruction can
    - i) ends the current task
    - ii) save its states
    - iii) switch to a new task
    - iv) load its states and
    - v) begin executing the new task
- housed in 68-pin package



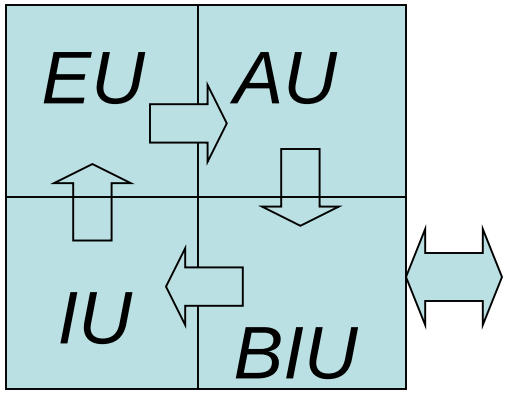
Internal Block Diagram of 80286



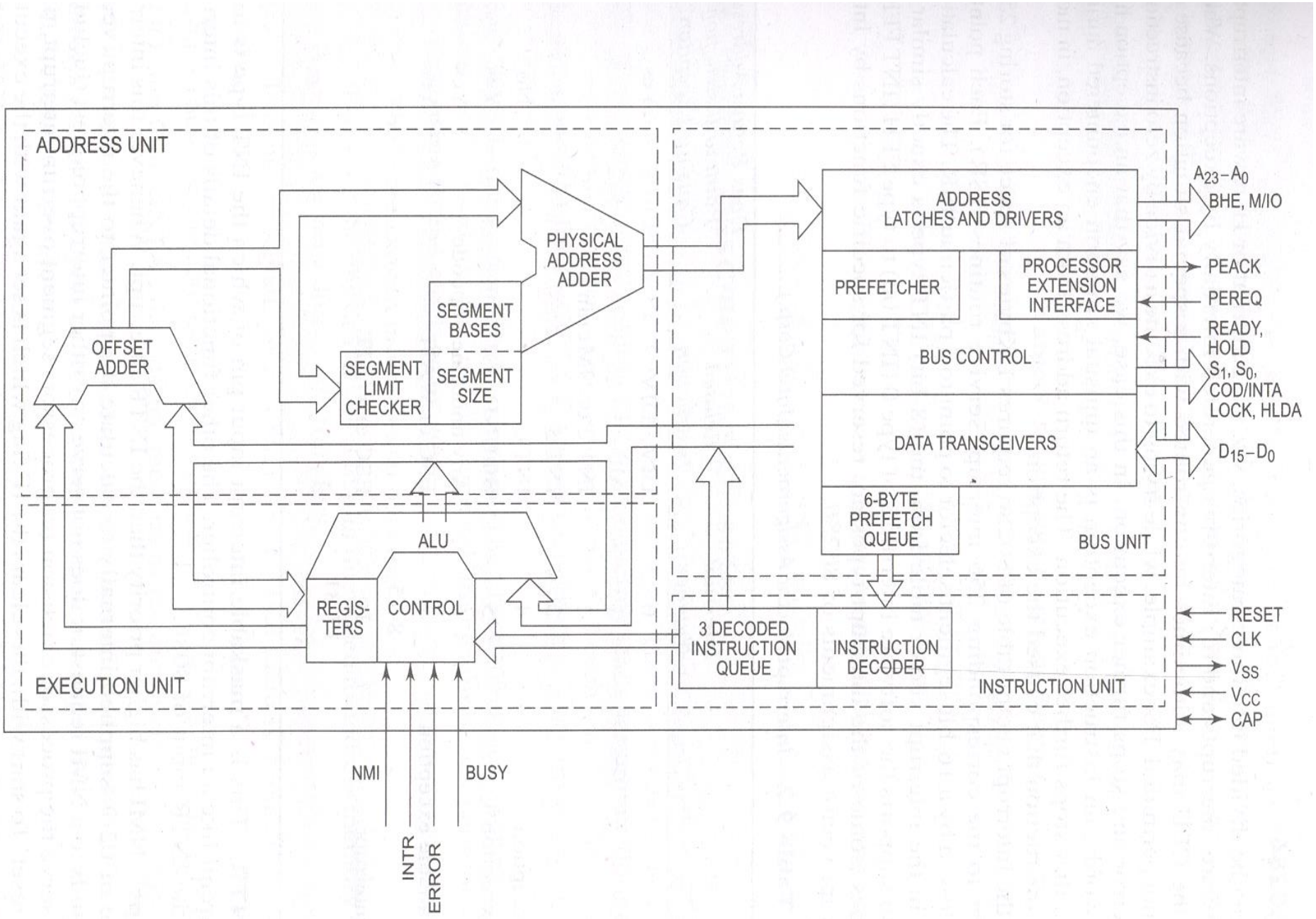
8085



8086



80286


ADDRESS UNIT
PHYSICAL ADDRESS ADDER
SEGMENT BASES
SEGMENT LIMIT CHECKER
SEGMENT SIZE
OFFSET ADDER
ALU
REGIS-TERS
CONTROL
EXECUTION UNIT
ADDRESS LATCHES AND DRIVERS
PREFETCHER
PROCESSOR EXTENSION INTERFACE
BUS CONTROL
DATA TRANSCEIVERS
6-BYTE PREFETCH QUEUE
BUS UNIT
3 DECODED INSTRUCTION QUEUE
INSTRUCTION DECODER
INSTRUCTION UNIT
A23–A0
BHE, M/IO
PEACK
PEREQ
READY, HOLD
S1, S0, COD/INTA LOCK, HLDA
D15–D0
RESET
CLK
VSS
VCC
CAP
NMI
BUSY
INTR
ERROR

Functional Parts

1. Address unit
2. Bus unit
3. Instruction unit
4. Execution unit

Address Unit

- Calculate the physical addresses of the instruction and data that the CPU want to access
- Address lines derived by this unit may be used to address different peripherals.
- Physical address computed by the address unit is handed over to the BUS unit.

Bus Unit

- Performs all memory and I/O read and write operations.
- Take care of communication between CPU and a coprocessor.
- Transmit the physical address over address bus $A_0 – A_{23}$.
- Prefetcher module in the bus unit performs this task of prefetching.
- Bus controller controls the prefetcher module.
- Fetched instructions are arranged in a 6 – byte prefetch queue.

Instruction Unit

- Receive arranged instructions from 6 byte prefetch queue.
- Instruction decoder decodes up to 3 prefetched instruction and are latched them onto a decoded instruction queue.
- Output of the decoding circuit drives a control circuit in the Execution unit.

Execution unit

- EU executes the instructions received from the decoded instruction queue sequentially.
- Contains Register Bank.
- contains one additional special register called **Machine status word (MSW)** register --- lower 4 bits are only used.
- ALU is the heart of execution unit.
- After execution ALU sends the result either over data bus or back to the register bank.

Register organization of 80286

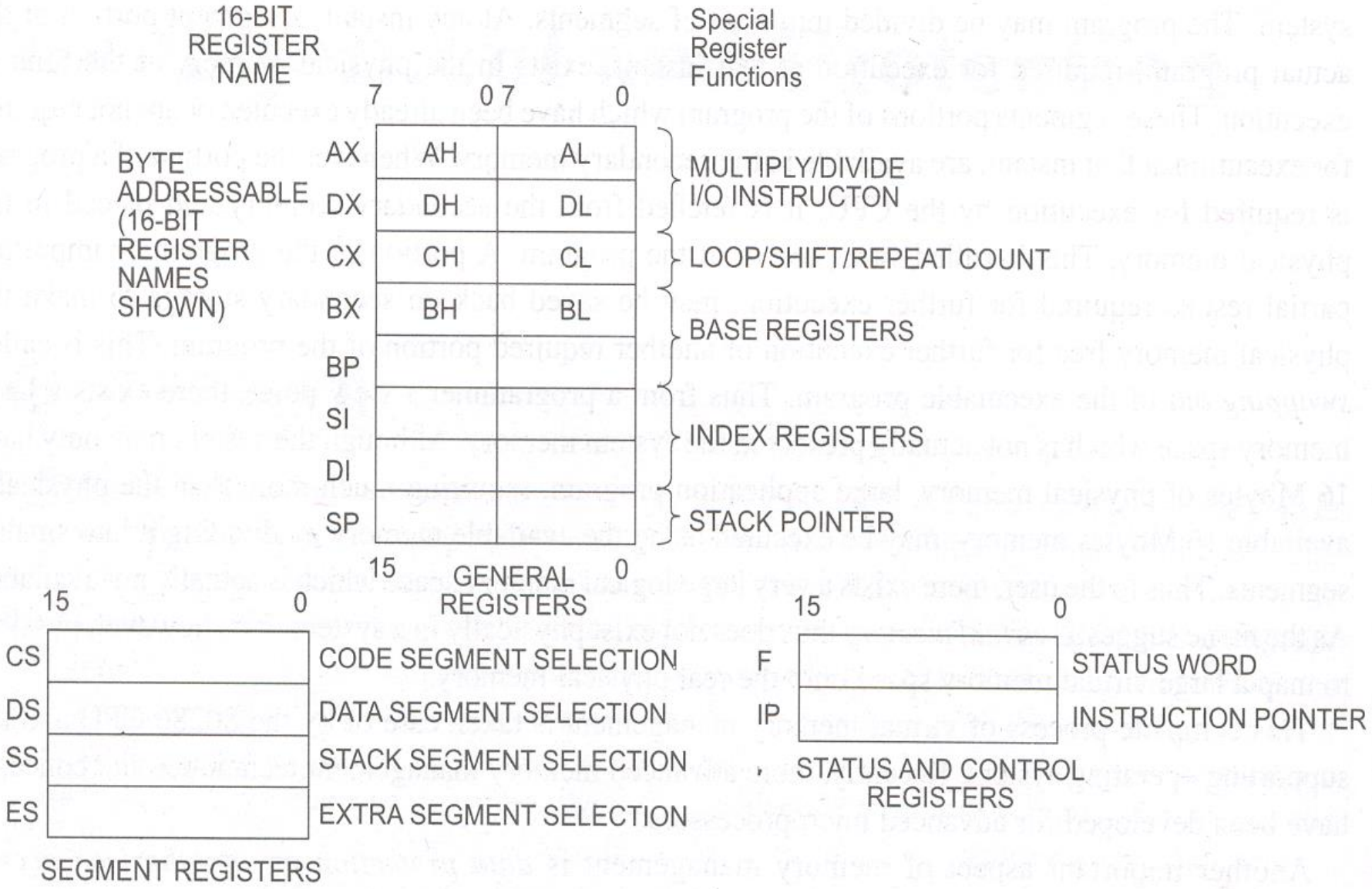
The 80286 CPU contains the same set of registers, as in 8086.

1. Eight 16-bit general purpose registers.

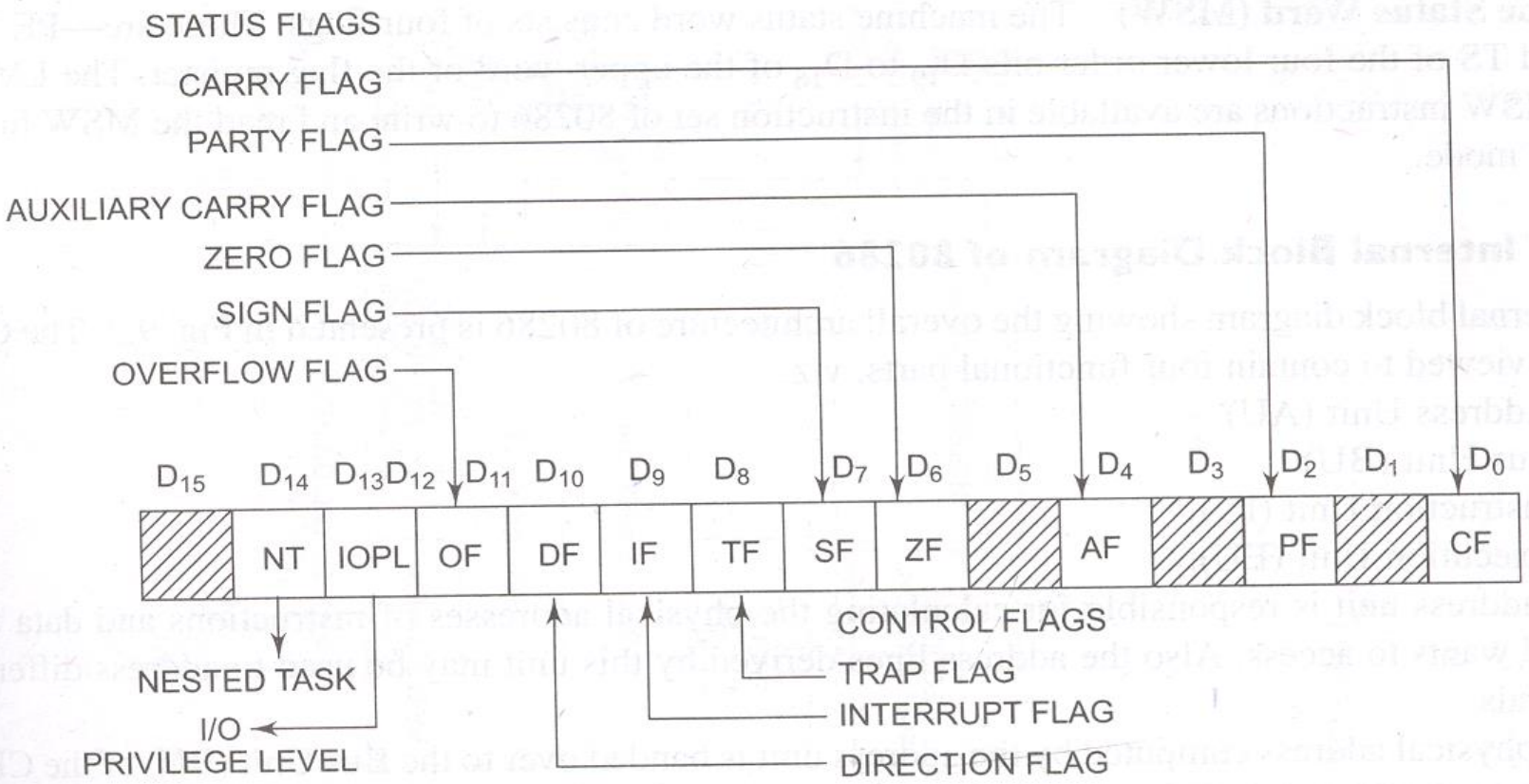
2. Four 16 bit segment registers.

3. Status and control register.

4. Instruction pointer.


16-BIT REGISTER NAME
Special Register Functions
7
0 7
0
BYTE ADDRESSABLE (16-BIT REGISTER NAMES SHOWN)
AX
AH
AL
MULTIPLY/DIVIDE I/O INSTRUCTON
DX
DH
DL
CX
CH
CL
LOOP/SHIFT/REPEAT COUNT
BX
BH
BL
BASE REGISTERS
BP
SI
INDEX REGISTERS
DI
SP
STACK POINTER
15
0
GENERAL REGISTERS
15
0
CS
CODE SEGMENT SELECTION
DS
DATA SEGMENT SELECTION
SS
STACK SEGMENT SELECTION
ES
EXTRA SEGMENT SELECTION
SEGMENT REGISTERS
15
0
F
STATUS WORD
IP
INSTRUCTION POINTER
STATUS AND CONTROL REGISTERS

Flag Registers



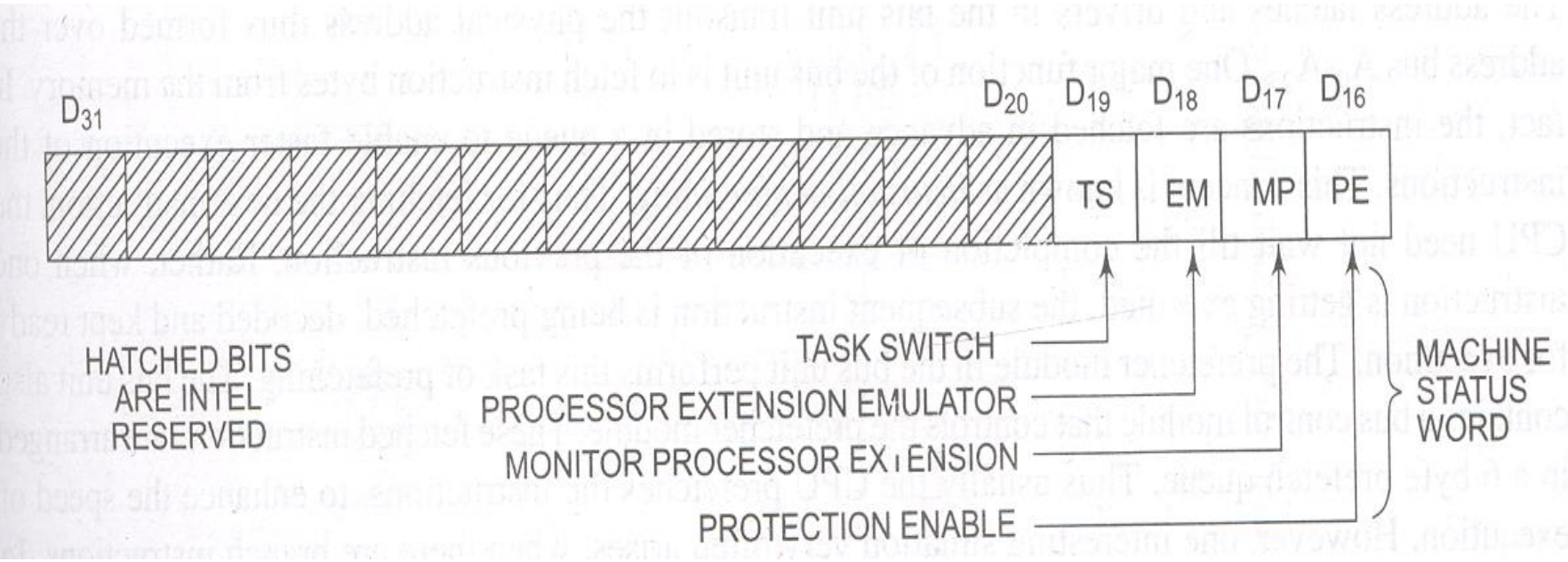
- IOPL – Input Output Privilege Level flags (bit D12 and D13)
  - IOPL is used in protected mode operation to select the privilege level for I/O devices. IF the current privilege level is higher or more trusted than the IOPL, I/O executed without hindrance. If the IOPL is lover than the current privilege level, an interrupt occurs, causing execution to suspend. Note that IPOL 00 is the highest or more trusted; and IOPL 11 is the lowest or least trusted.

- NT – Nested task flag (bit D14)
  - When set, it indicates that one system task has invoked another through a CALL instruction as opposed to a JMP. For multitasking this can be manipulated to our advantage

Machine Status Word

- Consist of four flags. These are – PE, MP, EM and TS

- LMSW & SMSW instruction are available in the instruction set of 80286 to write and read the MSW in real address mode.


D31
D20
D19
D18
D17
D16
TS
EM
MP
PE
HATCHED BITS ARE INTEL RESERVED
TASK SWITCH
PROCESSOR EXTENSION EMULATOR
MONITOR PROCESSOR EXTENSION
PROTECTION ENABLE
MACHINE STATUS WORD

- PE - Protection enable
  - Protection enable flag places the 80286 in protected mode, if set. This can only be cleared by resetting the CPU.
- MP – Monitor processor extension
  - flag allows WAIT instruction to generate a processor extension.
- EM – Emulate processor extension flag,
  - if set , causes a processor extension absent exception and permits the emulation of processor extension by CPU.
- TS – Task switch
  - if set this flag indicates the next instruction using extension will generate exception 7, permitting the CPU to test whether the current processor extension is for current task.

- **CLTS**
  - **The clear task – switched flag instruction clears the TS (Task - switched) flag bit to a logic 0.**
- **LAR**
  - **The load access rights Instruction reads the segment descriptor and place a copy of the access rights byte into a 16 bit register.**
- **LSL**
  - **The load segment limit instruction Loads a user – specified register with the segment limit.**

- **VERR**
  - **The verify for read access instruction verifies that a segment can de read.**
- **VERW**
  - **The verify for write access instruction is used to verify that a segment can be written.**
- **ARPL**
  - **The Adjust request privilege level instruction is used to test a selector so that the privilege level of the requested selector is not violated.**