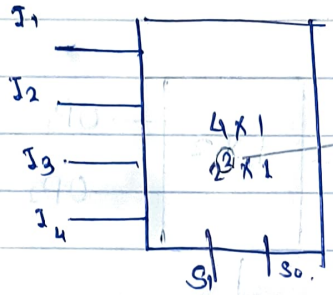
Multiplexer: $2^n : 1$ (Input : Output)

- A multiplexer is a combinational circuit that has 2^n input lines and a single output line.
- A multiplexer is an electronic ~~circuit~~ switch that connects 1 out of 'n' inputs to an output.
- It is functionally complete i.e. all Boolean functions can be realized using one multiplexer without any other gates.



0	0	I_1
0	1	I_2
1	0	I_3
1	1	I_4

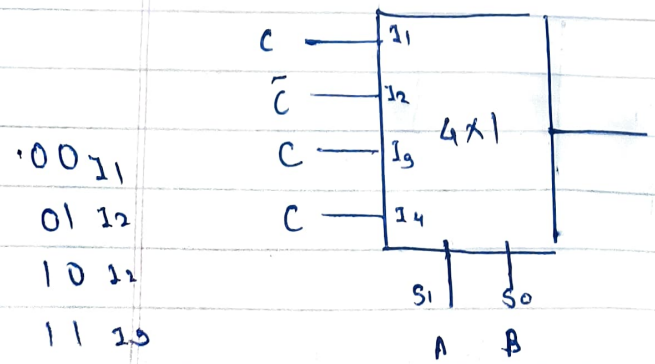
$\bar{S_1}\bar{S_0} I_1 + \bar{S_1} S_0 I_2 + S_1 \bar{S_0} I_3 + S_1 S_0 I_4$

Implementation of fun^n using MUX.

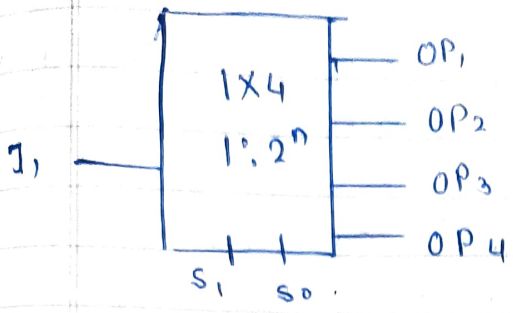
Q) $f(A,B,C) = \Sigma(1,2,5,7)$

$\bar{A}\cdot\bar{B}C + \bar{A}B\bar{C} + A\bar{B}C + ABC$

001 (I1) 010 (I2) 101 (I5) 111

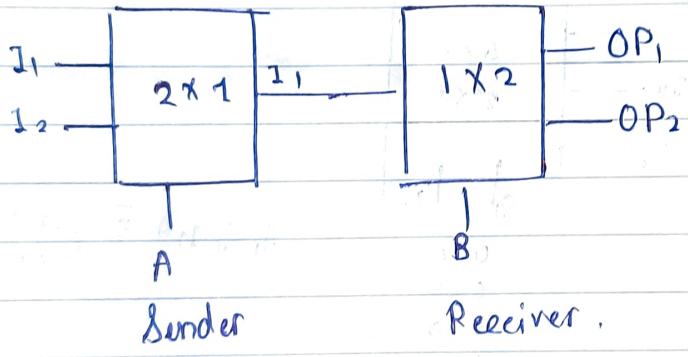


Demultiplexer. ~~$2^n - 1$~~ $1 : 2^n$.



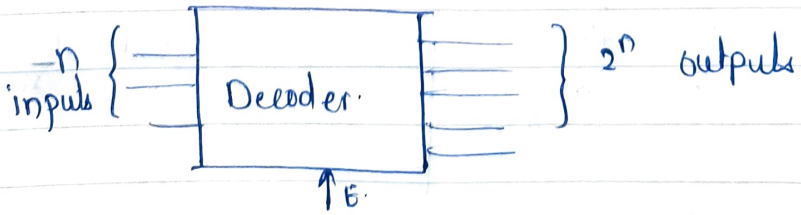
S_1	O_4	OP_1	OP_2	OP_3	OP_4
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Multiplexer ⇒ Sender's side
Demultiplexer ⇒ Receiver's side.



Decoders:

Decoder is a multi-input, multi-output logic circuit which decodes n inputs into 2^n possible outputs.



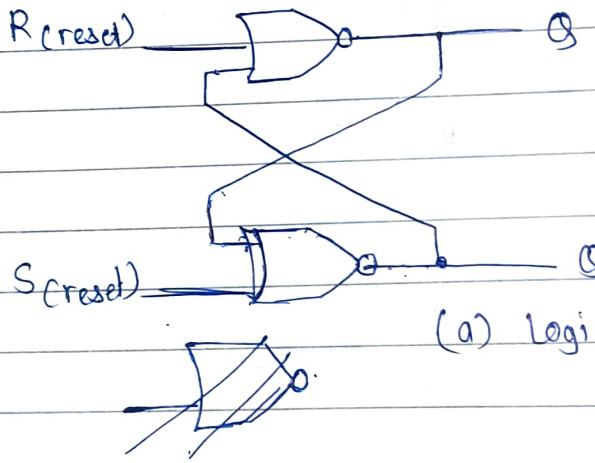
Where E: Enable < E:0 Decoder is disabled
E:1 Decoder is enabled.

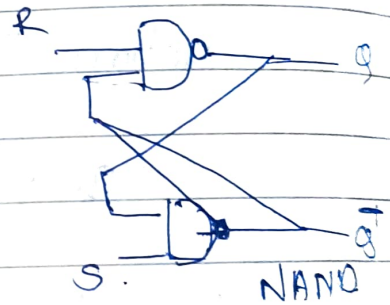
Flip Flop:

- Flip Flop is a binary cell capable of storing one bit of data.
- Flip Flop is a sequential circuit. (output = present input + past output).

① S-R Flip-flop:

The SET - RESET Flip Flop is designed with the help of two NOR gates and also two NAND gates. These Flip Flops are also called S-R Latch.





(a) Logic Diagram:

It is a Fundamental Flip-Flop.

R	S	Q	$\bar{Q}$
0	1	1	0
1	0	0	1
1	1	Invalid	→ Last state (Not valid)
0	0	Q	→ Forbidden state

Racing condition

Characteristic Table For SR Flip-Flop

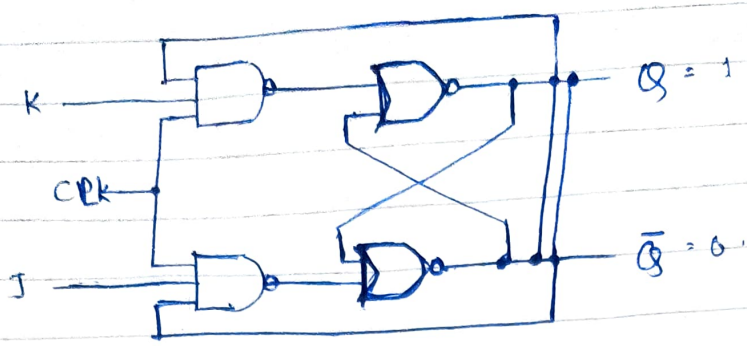
S	R	Q	Q(n+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

Excitation Table for SR :

Q	Qn+1	S	R
0	0	0	x
1	1	x	0
1	0	0	1
0	1	1	0

2] J-k Flip Flop.

In SR Flip-Flop invalid state is present when both input are one. To avoid this J-K Flip Flop is used.. Jk Flip-Flop is refinement of SR Flip-Flop.



Logic Diagram

J	k	Q(N+1)	
0	0	Q(N)	Hold
0	1	0	set to 1
1	0	1	Reset to 0.
1	1	$\bar{Q}n$	toggle

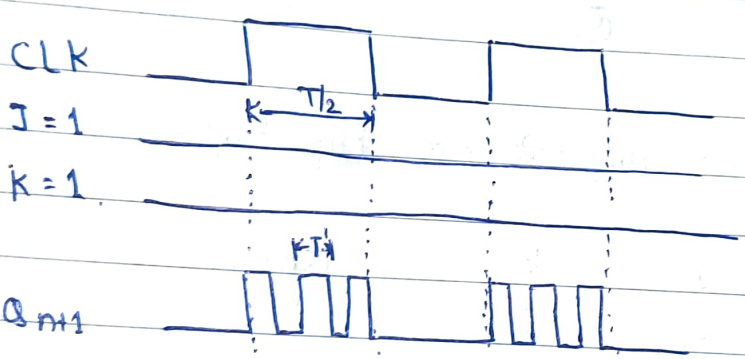
Characterstic Table For J-K Flip Flop.

Q	J	k	Qn+1
0	0	0	0
0	1	0	1
0	0	1	0
0	1	1	1
1	0	0	1
1	1	0	1
1	0	1	0
1	1	1	$\bar{Q}$

Excitation table:

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

* Race Around condition:
When J = 1 and K = 1, at that time there is possibility of race around condition.



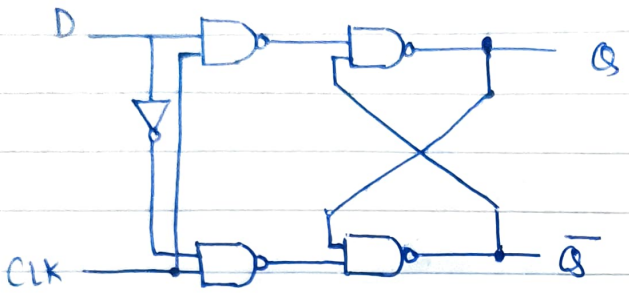
For J-K flip flop, if J = K = 1, and if clk = 1 For a long period of time, then Q_n output will toggle as long as CLK is high, which makes the output of the flip unstable or uncertain. This problem is called ~~can be avoided~~ as 'Race Around condition'.

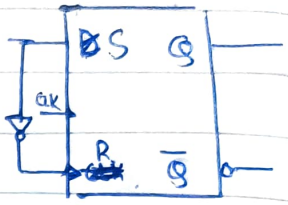
Soln:

i) $T' > T/2$ (Propogation delay greater than $T/2$) then we can avoid race around condition. which is practically not possible

2] Edge trigger
3] Master slave Flip-Flop.

D Flip-Flop (Data Flip-Flop)





Truth Table:

CLK	D	Q_{n+1}
⊖		
0	x	Q_n
1	0	0
1	1	1

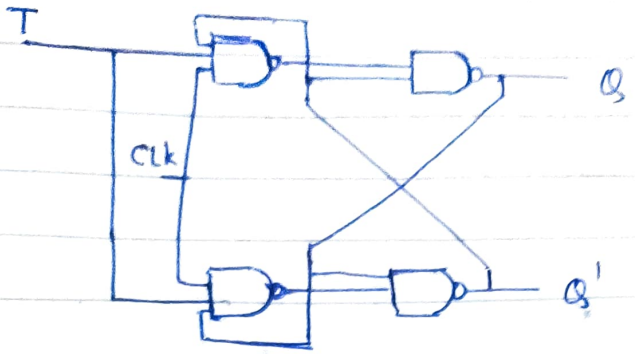
Characteristic table:

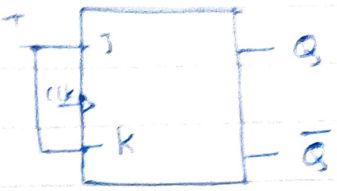
Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Excitation Table:

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

T Flip-Flop (Toggle Flip-Flop)





Truth Table:

Clk	T	Q_{n+1}
0	x	Q_n
1	0	Q_n
1	1	$\overline{Q_n}$

Characteristic Table:

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

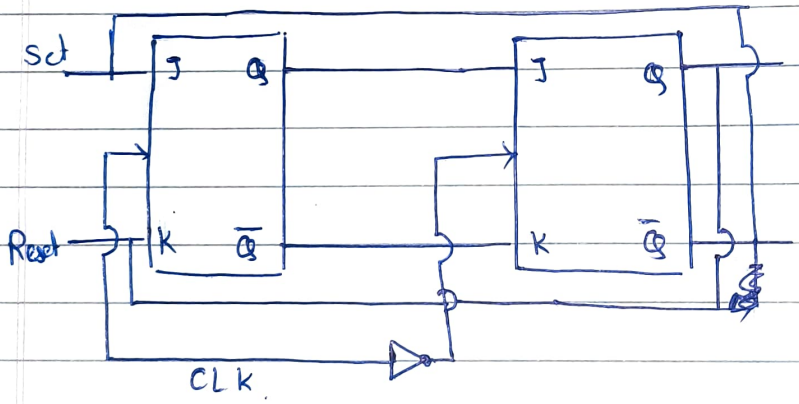
Excitation Table.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Master - Slave Flip Flop.

The master - slave Flip-Flops is basically a combination of two Jk Flip-Flops connected together in a series configuration. out of these, one act as a the 'master' and other as a "slave". The output from the master flip-flop is connected to the two inputs of the slave flip flop whose output is fed back to input of the masters flip flop.

In addition to these two flip-flops, the circuit also includes an inverter. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip flop. In other words, if CP = 0 for a master flip-flop, then CP = 1 for a slave flip-flop and vice versa.



Timing Diagram For a master Flip Flop.