

5. 80X86 Family

* 80186 Basic Features:

1. The 80186 contains 16-bit data bus.
2. The internal register structure of 80186 is virtually identical to the 8086.
3. About the only difference is that the 80186 contain additional reserved interrupt vector and some very powerful built-in I/O features.

A. Clock Generator:

The internal clock generator replaces the external 8284 A clock generator used with the 8086 microprocessors. This reduces the component count in a system.

B. Programmable Interrupt controller

The PIC arbitrates all internal and external interrupt and controls up to two external 8259A PICs. When an external 8259 is attached, the 80186 microprocessors function as the master and the 8259 functions as the slave.

C. Timers

The Timer sections contains 3 fully programmable 16 bit timers.

D. Programmable DMA Unit:

1. The programmable DMA unit contains two DMA channels, or four DMA channels in some models.

2. Each channel can transfer data between memory locations, bet' memory and IO, or between IO devices.

* Architecture of 80286

1. The 80286 microprocessor is an advanced version of the 8086 microprocessor that is designed for multiuser and multitasking environments.
2. The 80286 addresses 16 MB of physical memory and 1 GB of virtual memory by using its memory management system.
3. It contain 3 clock frequencies 12.5 MHz, 10MHz and 8MHz
4. It has 16 bit data bus and 24 bit address bus.
5. The 80286 operates in both real and protected modes.
6. In the real mode, the 80286 addresses a 1 MByte memory address space and is virtually identical to 8086
7. In the protected mode, the 80286 addresses a 16 MByte memory space.

A Functional parts of 80286

1. Address Unit

- i) calculate the physical addresses of the instruction and data that the CPU want to access.
- ii) Address lines derived by this unit may be used to address different peripherals.
- iii) Physical address computed by the address unit is handed over to the Bus unit.

B. Bus Unit

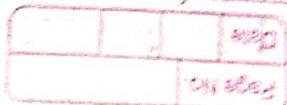
1. Performs all memory and I/O read and write operations.
2. Take care of communication between CPU and a coprocessor.
3. Transmit the physical address over address bus A₀ - A₂₃.
4. Prefetcher module in the prefetcher module.
5. Fetched instructions are arranged in a 6 byte prefetch queue.

C. Instruction Unit

1. Receive arranged instructions from 6 byte prefetch queue.
2. Instruction decoder decodes up to 3 prefetched instruction and are latched then onto a decoded instruction queue.
3. Output of the decoding circuit drives a control circuit in the Execution unit.

D. Execution Unit

1. EU executes the instructions received from the decoded instruction queue sequentially.
2. Contains Register Bank.
3. Contains one additional special register called Machine status word (MSW) register. Lower 4 bits are only used.
4. ALU is the heart of EU.
5. After execution ALU sends the result either over data bus or back to the register bank.



- The 80286 CPU contains the same set of registers, as in 8086
1. Eight 16 bit general purpose registers
 2. Four 16 bit segment registers
 3. Status and control register
 4. Instruction pointer.

* 80386 Microprocessor *

* Architecture of 80386

- * Internal Architecture of 80386 is divided into 3 sections
1. central processing unit
 - 2) Memory management unit
 - 3) Bus interface unit

* Features of 80386

1. As it is a 32 bit microprocessor.
Thus has a 32 bit ALU
2. 80386 has a data bus of 32 bit
3. It holds an address bus of 32 bit
4. It supports physical memory addressability of 4 GB and virtual memory addressability of 64 TB
5. 80386 supports a variety of operating clock frequencies, which are 16 MHz, 20 MHz, 25 MHz & 33 MHz
6. It offers 3 stage pipeline: fetch, decode and execute
7. As it supports simultaneous fetching, decoding and execution inside the system.

1. Central processing Unit (CPU)

a) Execution Unit: Reads the instruction from the instruction queue and executes the instruction

consists of 3 subunits: control, data & protection test unit

1. Control Unit: It contains microcode and special hardware allows processor to reduce time required for execution of multiply and divide instruction. It also speeds the effective address calculation.

2. Data Unit:

- 1) Responsible for data operations requested by the control unit.
- 2) It contains ALU, eight 32-bit general purpose registers and 64-bit barrel shifter.

3. Protection Test Unit:

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 checks for segmentation violations under the control of the microcode.

b) Instruction Decode Unit:

- i) Take instruction byte from the code prefetch queue and translates them into microcode.
- The decoded instructions are then stored in the instruction queue.

2. Bus control Unit:

Is the 808386 communication with the outside world. It provides a full 32 bit bidirectional data and 32 bit address bus.

Responsible for following operations:

- i) Accepts internal requests for code fetch and for data transfers from the code fetch unit and from the execution unit. It then prioritize the request and generate signals to perform bus cycles
- ii) It send address, data and control signals to communicate with memory and I/O devices
- iii) It controls the interface to external bus masters and coprocessors
- iv) It also provides the address relocation facility.

* The 80486 Microprocessor

1. 80486 math co-processor is the first processor to have built-in math coprocessor.
2. This being integrated on the chip allows it to execute math instructions 3 times faster.
3. It has 8kb code data internal cache.
4. It has five stage instruction pipeline scheme that allows it to execute instructions much faster than 80386.
5. It is 168 pin chip.
6. It is also called double clocked microprocessor.
7. Address-Bus:
 - 1) A₃₁-A₂ These are the address lines of the microprocessor, and are used for selecting memory I/O devices.
 - 2) However, for memory I/O addressing we also need another set of signals known as byte enable signals BEO-BE3.
 - 3) These active low byte enables signals (BEO# - BE3#) indicate which byte of the 32 bit data bus is active during the read or write cycle.
- 8) Data Bus- D₀-D₃₁ This is bidirectional data bus with D₀ as the least and D₃₁ as the most significant data bit.
- 9) Data Parity Group: The pins of this group of signals are extremely important, because they are used to detect the parity during the memory read & write operations.

10) DPO-DP3 : These four data parity input/output pins are used for representing the individual parity of 4 bytes (82 bits) of the data bus.

11) PCHK# : The 486 checks the parities of the data bytes read and signals on the DPO-DP3 if error is found, 486 asserts the PCHK signal.

* Bus cycle signals:

1. M/I/O# : This output pin differentiates bet' memory and I/O operations.

2. DIC# : This output pin differentiates between data control operations.

3. W/R# : This output pin differentiates bet' read and write bus cycle.

4. PLOCK# : This pseudo lock pin indicates that the current operation may require more than one bus cycle for its completion.

The bus is to be locked until then.

5. LOCK# : This output pin indicates that the current bus cycle is locked.

* Virtual m.

* Virtual mode of 80386

1. In protected mode of operation, 80386 BX provides a virtual 8086 operating environment to execute the 8086 programs.
2. The real mode can also be used to execute the 8086 programs along with the capabilities of 80386 like protections and a few additional instructions.
3. Once the 80386 enters the protected mode from the real mode, it cannot return back to the real mode without a reset operation.
4. Thus, the virtual 8086 mode of operation of 80386, offers an advantage of executing 8086 programs while in protected mode.
5. CPU Leaves V86 Mode and enters protected mode to continue executing a native 80386 program.

① The address forming mechanism in virtual 8086 mode is exactly identical with that of 8086 real mode.

② V86 Mode is known as Virtual mode of 80386

6. It can switch repeatedly & rapidly between V86 mode & protected mode.
7. To execute an 8086 program, the CPU enters in V86 Mode from protected mode.
8. In virtual mode 8086 can address 1 MB of physical memory that may be anywhere in the 4 GB address space of the protected mode of 80386.

12. Like 80386 real mode, the addresses in virtual 8086 mode lie within 1MB of memory.
13. In virtual mode, the paging mechanism and protection capabilities are available at service of the programmers.
14. The virtual mode allows the multiprogramming of 8086 applications.
15. The virtual 8086 mode executes all the programs at privilege level 3.

'Paging