Avery Wong

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Education

The University of British Columbia — Vancouver, BC
Bachelor of Applied Science, Engineering Physics - 5th Year — *Sept. 2021 – Present*

Experience

Digital Design Engineer Co-op — May 2025 - August 2025
Blue Sky Spectroscopy — *Lethbridge, AB*

- Developed a Zynq SoC based readout/sampling system for a fourier transform spectroscopy system
- Implemented AXI4-Stream protocol and interfaced with Xilinx AXI DMA IP to facilitate FPGA-CPU data transfer
- Wrote custom RTL in SystemVerilog and verified with testbenches to generate sampling logic from sensor inputs
- Interfaced with ADC and DAC board peripherals to retrieve sample data and output waveforms
- Wrote Makefile and TCL scripts to streamline project building
- Developed a python application to control the system and collect data

Research Hardware Engineer Co-op — July 2024 - December 2024
Quantum Matter Institute - UBC — *Vancouver, BC*

- Developed a timing controller and readout system for a dual-comb spectroscopy experiment using a Zynq SoC
- Wrote RTL in SystemVerilog and verified using testbenches with Vivado's simulator to control laser trigger signals
- Integrated Vivado IP and custom RTL with Zynq Processing System IP in bloack diagram
- Restructured existing repository, utilizing TCL scripts, reducing repository file size by 60%
- Created a Python GUI with 50+ elements to control experimental instruments and streamline setup

Data Analyst/Simulations Co-op — January 2023 – April 2023
Ausenco — *Burnaby, BC*

- Analyzed and processed 10,000+ client-provided raw data entries to generate simulation-ready inputs
- Contributed 10+ updates to the in-house simulation software written in Java, utilizing Git for version control
- Optimized Excel VBA macros, improving data collection speed by 20% through performance testing

Projects

Portfolio

ATLAS Hardware Neural Network Trigger (Team Capstone, In Progress) | *FPGA, HLS, Machine Learning*

- With TRIUMF, developing hardware to increase the throughput of the ATLAS particle collision sensor system
- Converting a Neural Network to HDL by writing C++ code and using HLS
- Configuring an AMD Zynq SoC in block diagram to facilitate CPU - FPGA communication over AXI
- Optimizing modules and algorithms with HLS pragmas to meet timing and FPGA resource requirements

RC4 Decrypter | *FPGA, SystemVerilog, Quartus*

- Implemented an RC4 decryption algorithm on an Altera SoC FPGA
- Developed a 'Decryption Core' that uses 5 customs FSMs with Quartus memory IP to run the algorithm
- Designed a controller to manage key scheduling for multiple 'Decryption Cores', allowing for parallel processing
- Validated functionality through RTL simulation and real-time signal analysis using Quartus Signal Tap

Alarm Clock | *FPGA, VHDL, Quartus*

- Designed an interfaceable alarm clock using an Altera SoC, featuring adjustable alarms and real-time display
- Developed counters, number converters, comparators, latches, and 7-segment display converter modules in VHDL
- Assembled the full clock in a schematic design file, routing 20+ VHDL modules and assigning 60+ pin inputs

Virtual Detective Robot | *Python, Machine Learning, Computer Vision*

- Trained a neural network using TensorFlow, achieving 97%+ text prediction accuracy on a custom dataset
- Developed a data pipeline utilizing OpenCV to automate the collection and preprocessing of training data

Technical Skills

Languages: Verilog/SystemVerilog, Python, C/C++, Java, Assembly
Software Tools: Vivado, Vitis, Quartus, Git, VS Code, Jupyter Notebook
Electrical: Oscilloscope, Logic Analyzers, Spectrum Analyzers, Soldering