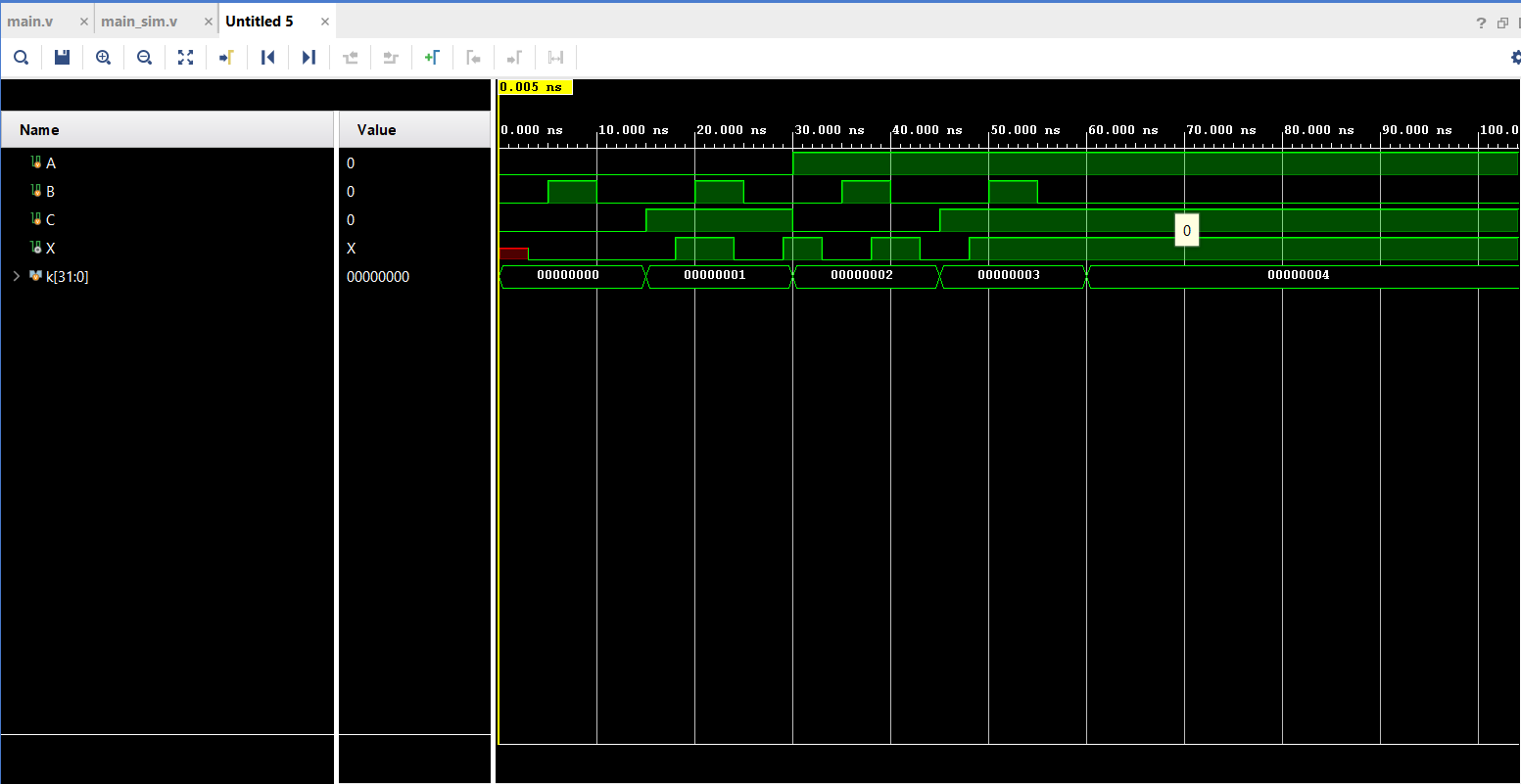
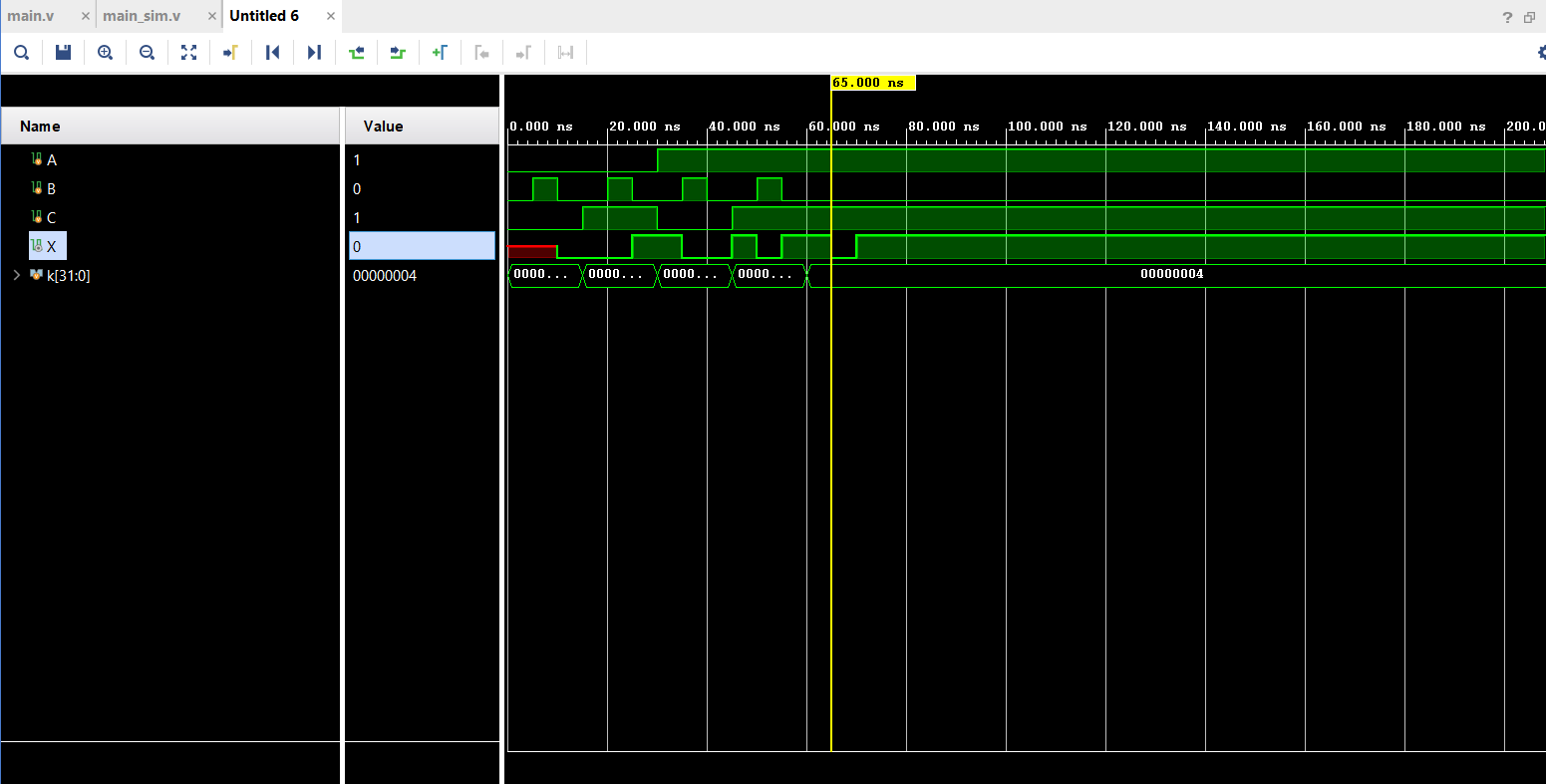
Problem 2



The 2ns delay on the OR gate ensures that the circuit will not have a glitch. This is because the output of the OR gate is delayed an extra nanosecond after the potential glitch would occur, which gives the output time to stabilize before it is read. This is reflected in the simulation which shows the 2 ns delay after C goes high.



Problem 3