TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC157AP, TC74HC157AF, TC74HC157AFN TC74HC158AP, TC74HC158AF, TC74HC158AFN

TC74HC157AP/AF/AFN QUAD 2 – CHANNEL MULTIPLEXER TC74HC158AP/AF/AFN QUAD 2 – CHANNEL MULTIPLEXER (INVERTING)

The TC74HC157A and TC74HC158A are high speed CMOS 2 - CHANNEL MULTIPLEXERs fabricated with silicon gate C2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC158A is an inverting multiplexer while the TC74HC157A is a non-inverting.

When STROBE is held high, selection of data is inhibited and all the outputs become low in the case of HC157A or high in the case of HC158A.

The SELECT decoding determines whether the A or B inputs get transferred to their corresponding Y (\overline{Y}) outputs.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed······ $t_{pd} = 10 \text{ns(typ.)}$ at $V_{CC} = 5 \text{V}$
- High Noise Immunity $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Output Drive Capability 10 LSTTL Loads
- Symmetrical Output Impedance··· | I_{OH} | = I_{OL} = 4mA(Min.)
- Balanced Propagation Delays ····· t_{pLH} ≃ t_{pHL}
- Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V~6V
- Pin and Function Compatible with 74LS157/158

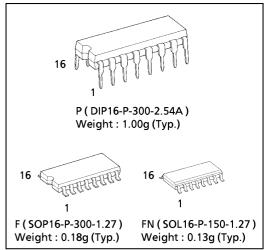
TRUTH TABLE

	INP	OUTPUTS			
ST	SELECT	Α	В	Y (157A)	₹ (158A)
Н	Х	Х	Х	L	Н
L	L	L	Х	L	Н
L	L	Н	Х	Н	L
L	Н	Х	L	L	Н
L	Н	Х	Н	Н	L

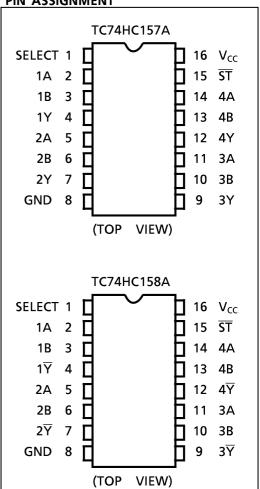
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X : Don't Care

(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



IEC LOGIC SYMBOL TC74HC157A TC74HC158A <u>s⊤</u>(15)_N ST (15) EN EΝ SELECT (1) SELECT (1) G 1 G 1 1A (2) 1B (3) 2A (5) 2B (6) 3A (11) 3B (10) 4A (13) 1A (2) 1B (3) 2A (5) 2B (6) 3A (11) 3B (10) 4A (13) <u>√(4)</u> 1<u>Y</u> <u>(4)</u> 1Y 1 MUX 1 MUX (7) 2Y (7) 2Y <u>(9)</u> 3<u>\text{Y}</u> (9) _{3Y} (12)_{4Y} (12)₄ 4B (13)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{cc}	− 0.5~7	V
DC Input Voltage	V _{IN}	$-0.5 \sim V_{CC} + 0.5$	V
DC Output Voltage	V _{OUT}	−0.5~V _{CC} + 0.5	V
Input Diode Current	I _{IK}	± 20	mA
Output Diode Current	I _{OK}	± 20	mA
DC Output Current	I _{OUT}	± 25	mA
DC V _{CC} / Ground Current	I _{cc}	± 50	mA
Power Dissipation	P _D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T _{stg}	−65~150	°C

*500mW in the range of Ta= $-40^{\circ}\text{C}\sim65^{\circ}\text{C}$. From Ta=65°C to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{cc}	2~6	V
Input Voltage	V _{IN}	0~V _{cc}	V
Output Voltage	V _{OUT}	0~V _{cc}	٧
Operating Temperature	T _{opr}	−40~85	°C
Input Rise and Fall Time	t _r , t _f	$0 \sim 1000 (V_{CC} = 2.0V)$ $0 \sim 500 (V_{CC} = 4.5V)$ $0 \sim 400 (V_{CC} = 6.0V)$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CO	NDITION Vc		Ta = 25°C			Ta = -4	UNIT	
PANAIVIETEN	STIVIBUL	TEST CONDITION		(V)	MIN.	TYP.	MAX.	MIN.	MAX.	UIVII
High - Level Input Voltage	VIH				1.50 3.15 4.20		_ _ _	1.50 3.15 4.20	 - -	V
Low - Level Input Voltage	VIL			2.0 4.5 6.0		1 1 1	0.50 1.35 1.80	_ _ _	0.50 1.35 1.80	V
High - Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	$I_{OH} = -20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9	_ _ _	V
			$I_{OH} = -4 \text{ mA}$ $I_{OH} = -5.2 \text{ mA}$	4.5 6.0	4.18 5.68	4.31 5.80	_	4.13 5.63	_	
Low - Level Output Voltage		V _{IN} = V _{IH} or V _{IL}	I _{OL} = 20μΑ	2.0 4.5 6.0	_ _ _	0.0 0.0 0.0	0.1 0.1 0.1	_ _ _	0.1 0.1 0.1	v
			$I_{OL} = 4 mA$ $I_{OL} = 5.2 mA$	4.5 6.0	_ _	0.17 0.18	0.26 0.26	_ _	0.33 0.33	
Input Leakage Current	I _{IN}	$V_{IN} = V_{CC}$ or GND		6.0	_		± 0.1	_	± 1.0	
Quiescent Supply Current	I _{cc}	$V_{IN} = V_{CC}$ or GND		6.0	_	_	4.0	_	40.0	μΑ

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AC ELECTRICAL CHARACTERISTICS ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t _{TLH} t _{THL}		_	4	8	
Propagation Delay Time (A, B $-$ Y, \overline{Y})	t _{pLH} t _{pHL}		_	10	16	ns
Propagation Delay Time (SELECT $-Y$, \overline{Y})	t _{pLH} t _{pHL}		_	13	21	113
Propagation Delay Time (STOROBE-Y, Y)	t _{pLH} t _{pHL}		_	10	19	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

DADAMETER		TEGT CONDITION			Га = 25°C	-	Ta = -4	.0~85°C	LINUT
PARAMETER	SYMBOL	TEST CONDITION	V _{cc} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
	t _{TLH}		2.0	_	30	75	_	95	
Output Transition Time	t _{THL}		4.5	_	8	15	_	19	
	LTHL		6.0	_	7	13	_	16	
Propagation Delay Time	+		2.0	_	36	100	-	125	ns
	t _{pLH}		4.5	_	12	20	-	25	113
$(A, B-Y, \overline{Y})$	t_{pHL}		6.0	_	10	17	_	21	
Dramagation Dalay Time	+		2.0	_	50	125	_	155	
Propagation Delay Time (SELECT—Y, Y)	t _{pLH}		4.5	_	16	25	_	31	
(SELECT - Y, Y)	t_{pHL}		6.0	_	14	21	_	26	
Dranagation Dalay Time	+		2.0	_	36	115	_	145	
Propagation Delay Time	t _{pLH}		4.5	_	12	23	-	29	
$(\overline{STOROBE} - Y, \ \overline{Y})$	t_{pHL}		6.0	ı	10	20	_	25	
Input Capacitance	C _{IN}		·	_	5	10	_	10	
Power Dissipation Capacitance	C _{PD} (1)	TC74HC157A			57		_	_	pF
Lissipation Capacitance	CPD (1)	TC74HC158A		-	53	_	_	_	

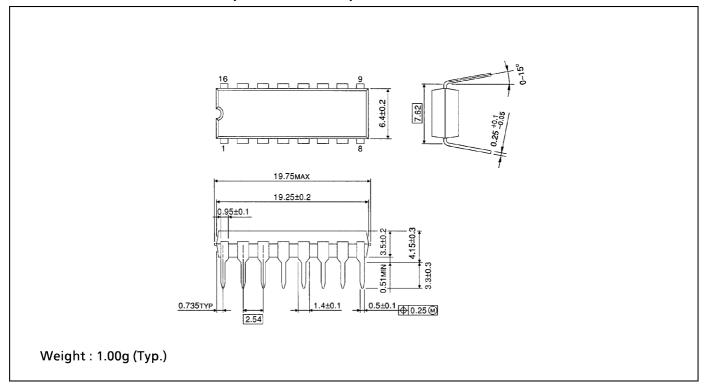
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 I_{CC} (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 4$ (per bit)

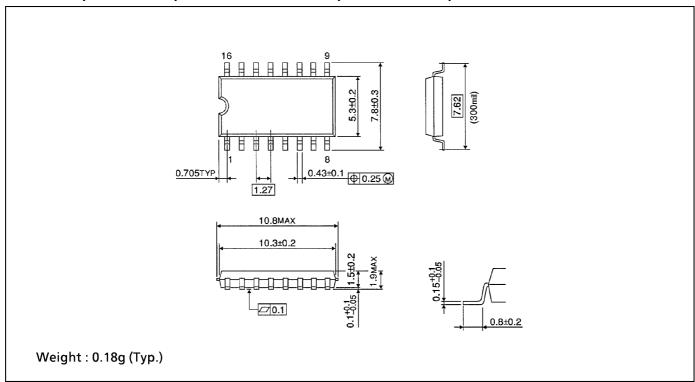
DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A)

Unit in mm



SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27)

Unit in mm

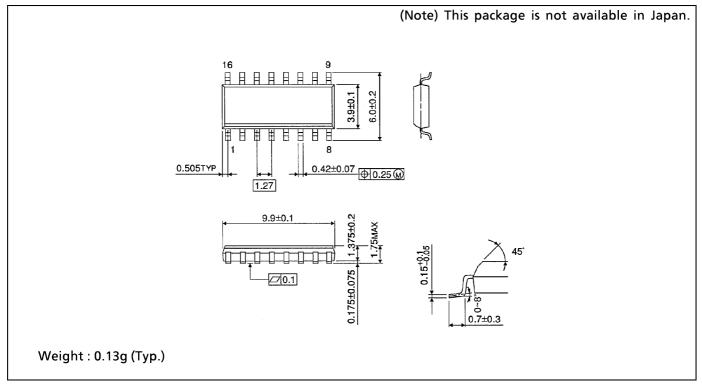


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SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27)

Unit in mm



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