COA Re-Assignment
180010011

Branch Prediction:

To reduce the impact of long pipes required for high-frequency design, the POWER4 branch invests heavily in forecasting. In each cycle, you will get eight notifications from the 64kB command in a live map capture. The branch predicts an algorithm to find two branches in each cycle. Depending on the type of branch available, different branch prediction methods can be used to predict the branch direction or branch address or both. Branch goals are not predicted for conditional branches Despite the conditional registration bit, almost all the conditional branches are approximate. Identification based on notification time Branch Target Address for PowerPC guidelines for Branch Link Registration (PLCR) and Branch Registration Count (PCDR) may be included. Evaluate the hardware-capable connection level and number using the catch method. Yours sincerely Target addresses are counted directly for full and affiliated branches part of the scanning process.

The rest of the branch instructions passed through the pipeline and eventually when determining the actual results of executive branch units and branches. Predictions are accurate and complete as directed by the branches if all the other advice seems to be wrong in the future, consult leave the available argument and start with the miscalculated suggestions.
A good way to advise POWER4 uses three branch history tables to specify the direction of the branches. The first list of so-called native prophets is similar to the traditional branch.
16K entries with the history list (BHT) branch instructions-bit is showing whether or not it shows branches. The actual route of execution to reach the branch has been identified 11-bit vector, a set of instructions in the command cache.

POWER4 has 17 pipelines designed for high frequency. It is planned to implement branch forecasting method through pipeline. POWER4 uses multi-level branch predictions, a collection of three branch history tables. The first is called local forecasting, which produces the same 1-bit forecast as the Branch History Schedule (BHT), whether it is taken or not. Taken from another so-called Global Predictor, another 1-bit branch-based forecast has been developed based on the recommendations of the previous eleven recipients. The third list, called the voter list, is used to choose between local and global estimates.

Hardware Data Prefetch :

The organizational degree of POWER4 memory consists of three levels of cache: L1-Live Map, four 32-byte zones for instructions, two-way 128-byte data collection. L2- Eight Ways, 128 bytes; L3-eight-access assistants, four 128-byte zones (for compatibility with L2catch); And main memory enhancements (DRAMS 0-16 GB) with such memories Bandwidth requires less memory access The chip runs a pre-stream system, actually eight software-activated pre-streams. This preset stream uses additional bandwidth to transmit data continuously from the L1 through memory creation. They can fly up to 20 cash routes at a time. After filling the pre-made pipes, the memory system Ecologically, central memory provides new information in every era Processor Load / Store Unit (LSU) and L2 and L3 have special arguments for implementing data subroutines. The top, bottom, or bottom of the bay is determined by the actual load address online archive missing.

To perform the present logical core load / store units (LSU) and L2 and L3 data offerings. 3. The direction of preload is determined by the address of the actual load in the line, avoiding catch. If the load address is below the line is then richer in the near direction. If the actual load address is at the top of the line, the closest direction is down. If there is an initial estimate of direction properly

configuring the next entry does not ensure that the engine is already running. Incorrectly started flow will be brought to an end. The modified flow will be installed as the new flow.