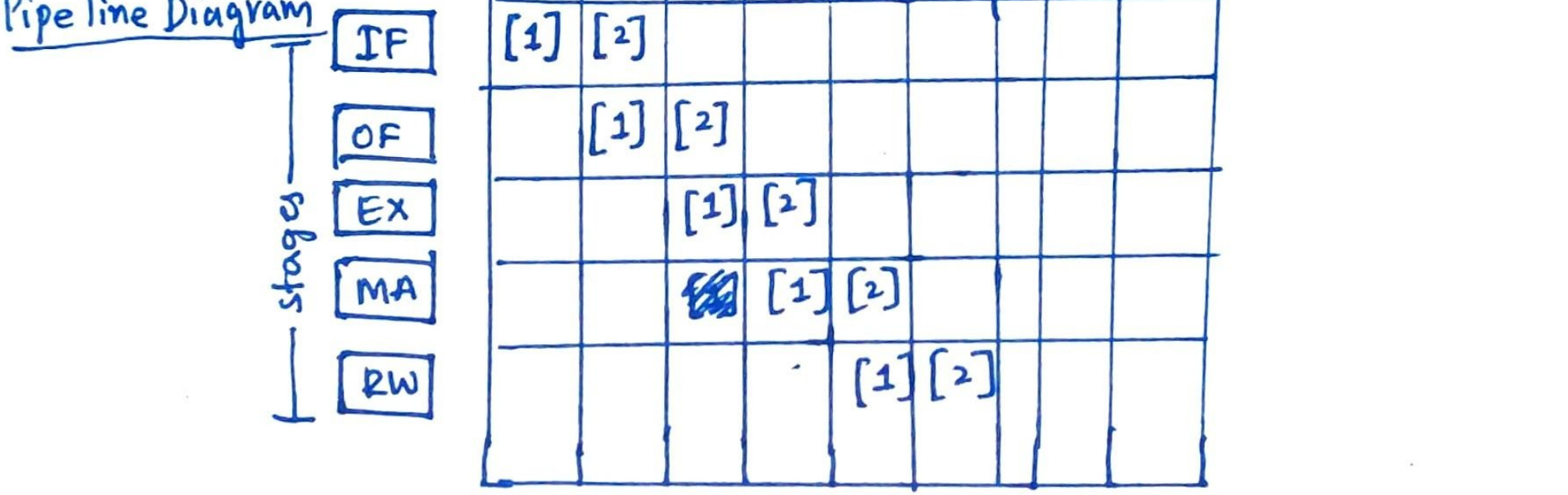
3-Ans) i) [1] st r3, 24[r1]
[2] ld r4, 24[r1]

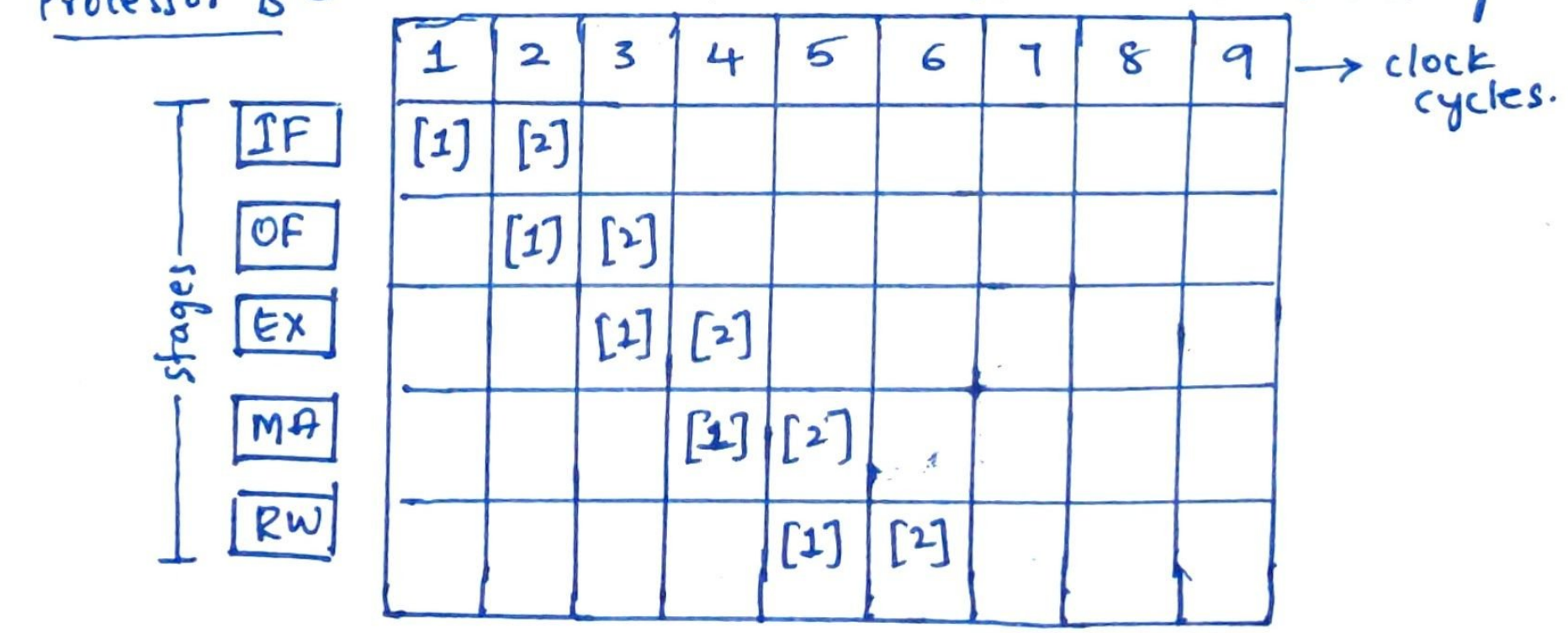
Processor A -

Pipe line Diagram



The final instruction pass through the RW stage is 6.

Processor B -



The final instruction pass through the RW stage is 6.

ii) [1] add r1, r1, r2

[2] sub r3, r1, r4

[3] add r4, r5, r6

Processor A -

data interlocks

stages	1	2	3	4	5	6	7	8	9	10 → clock cycles
IF	[1]	[2]	[3]	[3]	[3]	[3]				
OF		[1]	[2]	[2]	[2]	[2]	[3]			
EX			[1]	●	●	●	[2]	[3]		
MA				[1]	●	●	●	[2]	[3]	
RW					[1]	●	●	●	[2]	[3]

The final instruction pass through the RW stage is 10.

Processor B - data interlocks and value forwarding.

stages	1	2	3	4	5	6	7	8 → clock cycles
IF	[1]	[2]	[3]					
OF		[1]	[2]	[3]				
EX			[1]	[2]	[3]			
MA				[1]	[2]	[3]		
RW					[1]	[2]	[3]	

The final instruction pass through the RW stage is 7.