

# Assignment 11

Q 1) [5 marks] Consider a 1kB, byte-addressable, direct-mapped cache with line size of 64 bytes. Consider the following sequence of accesses (16 bit addresses in hexadecimal format):  
0x0001, 0x0002, 0x0003, 0x0041, 0x0081, 0x00A1, 0x00C1, 0x0401, 0x0402, 0x0001, 0x0002, 0x0003.

The LSB bits are used to determine the offset within the line.

How many cache hits occur? Assume the cache is entirely empty at the beginning.

Q 2) [5 marks] What if the cache in Q 1) was 2-way set associative?

Q 3) [5 marks] Consider a 128B, 4-way set associative cache, with line size 16B. The memory is byte-addressable. Can you come up with a sequence of addresses where

- The LRU replacement policy performs better than LFU
- The LFU replacement policy performs better than LRU

Q 4) [5 marks] How do your answers change if the cache is fully associative?

Q 5) [5 marks] Consider a fully associative cache following the LRU replacement scheme and consisting of only 8 words. Consider the following sequence of memory accesses (the numbers denote word address):

20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 22, 30, 21, 23, 31

Assume a line size of 2 words. Assume that we begin when the cache is empty.

- What is the hit rate?
- What are the contents of the cache at the end?

Q 6) [5 marks] What if the cache in Q 5) was 2-way associative?