

Assignment 12

Q 1) [5 marks] A processor has a baseline IPC of 0.8 for a certain program. 30% of the program's instructions are memory operations. It has two levels of caches.

The L1 instruction cache has a hit rate of 100%, and hit time of 1 cycle (part of the baseline IPC computation). The L1 data cache miss rate is 5% and the L2 miss rate is 50% for the given program. The L1 data cache hit time is 1 cycle (part of the baseline IPC computation), and the L2 hit time is 10 cycles. The L2 miss penalty is 100 cycles.

Compute the final IPC.

Q 2) [5 marks] What is the motivation behind prefetching? Intuitively, how does it work?