

08/2019						
Monday	-	5	12	19	26	
Tuesday	-	6	13	20	27	
Wednesday	-	7	14	21	28	
Thursday	1	8	15	22	29	
Friday	2	9	16	23	30	
Saturday	3	10	17	24	31	
Sunday	4	11	18	25	-	

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Wk-30 Day 203-162
MONDAY

Assignment - 5

1Ans) Hazard -

A Hazard is defined as possibility of erroneous execution of an instruction in a pipeline:

10 Data Hazards -

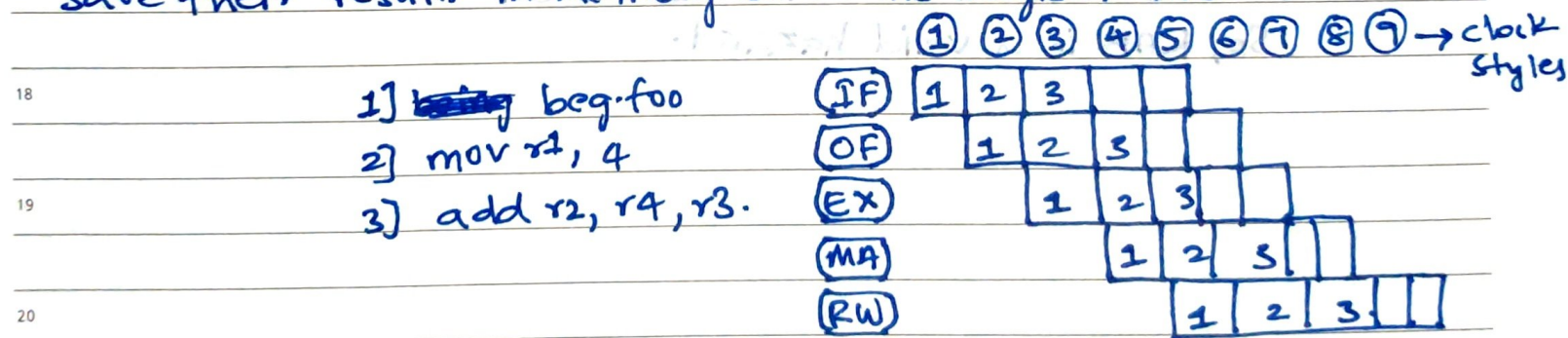
Data Hazard represents the possibility of erroneous execution because of unavailability of data, or availability of incorrect data. Instruction depends on result of prior instruction still in the pipeline.

There are three situations in which a data hazard can occur:

- 1) read after write (RAW), a true dependency
- 2) write after read (WAR), an anti-dependency
- 3) write after write (WAW), an output dependency

15 Control Hazard -

control hazard represents the possibility of erroneous execution in a pipeline because instruction in the wrong path of a branch can possibly get executed and save their results in memory or in the register file.



Structural Hazard -

A structural hazard may occur when two instructions have conflict on the same set of resources

in a cycle.

notes	*
Phone	
email	
website	

							07/2019
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8 Assume that we have an instruction that can read one operand from memory.

9 [1]: st r4, 20[r5]

[2]: sub r8, r9, r10

10 [3]: add r1, r2, 10[r3]

[3] will try to read 10[r3] in cycle 4 (OF stage)

11 [1] will try to write in 20[r5] in cycle 4 (MA stage)

12 They both try to access memory at the same time (same cycle) as the MA unit can't satisfy two operations at a time one has to wait.

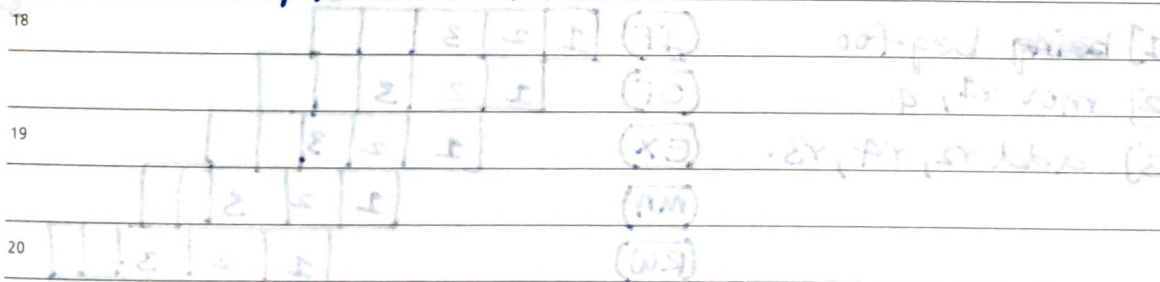
13 This doesn't happen in Simple Risc.

14 As These results to be inaccurate and to overcome these we have to spend more cycles. These degrade the performance of processing.

15 2Ans) No.

16 RAR is not a hazard as Read After Read doesn't fetch incorrect values and if data is available it is going to be available for the next instruction.

17 So, RAR is a valid hazard.



notes

Phone

email

website

* 3/10/19