

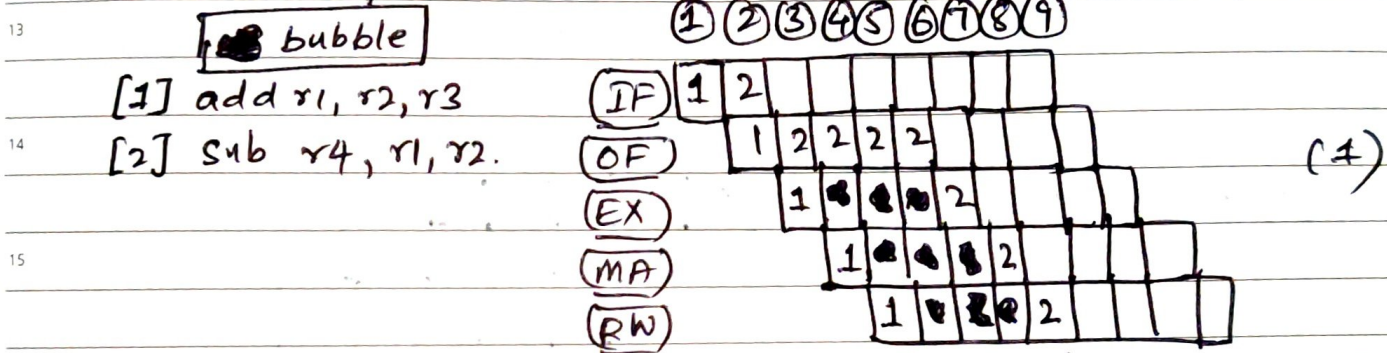
Monday	-	5	12	19	26
Tuesday	-	6	13	20	27
Wednesday	-	7	14	21	28
Thursday	1	8	15	22	29
Friday	2	9	16	23	30
Saturday	3	10	17	24	31
Sunday	4	11	18	25	-

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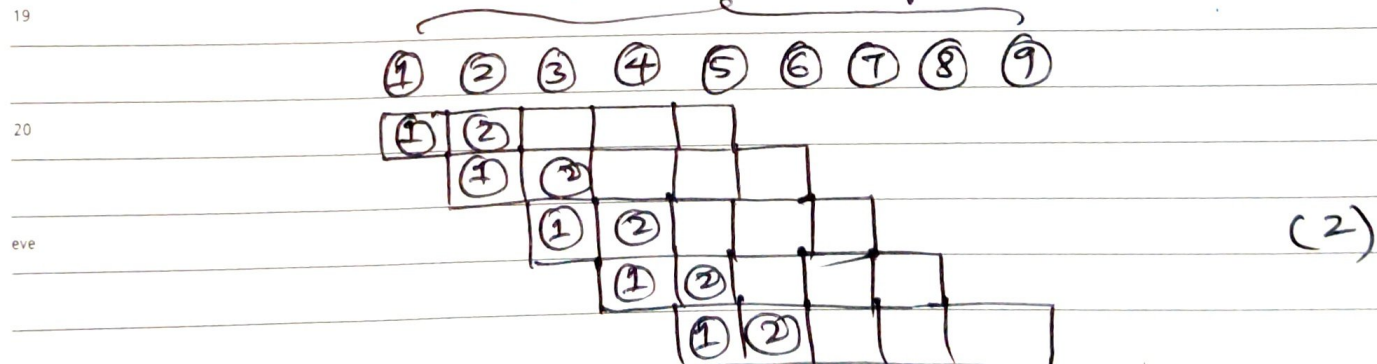
Assignment - 6

Ans) Data hazards can happen when instruction reads incorrect values.

For example - We take RAW condition. When we are in pipeline format register write happens in 5th stage, but after write operation if we have read operation the register read happens in OF stage i.e 2nd stage. So, In the pipeline when the 1st instruction is in 3rd stage, the 2nd instruction is its 2nd stage so it is reading incorrect value as updation of value in register didn't take place.

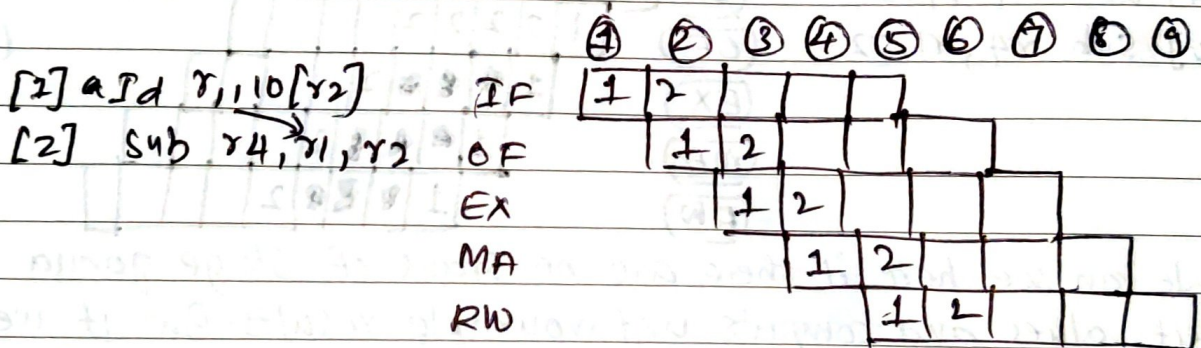


We can see here if there are no stalls of stage gonna read incorrect values and compute unfavourable results. But if we have bubbles we can see it compute correct values as it stalls until register writes takes place. So between RW stage of first instruction and OF stage of 2nd instruction we should atleast have 3 different of 3 clock cycles.



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2 Ans) We look closely at the pipeline and we see that value has to be stored for the above example. The first guidance and price required to measure the result is available at the end of cycle 3. Other suggestions will be available on cycle 4 at the beginning of the journey. So, the result has been prepared at the end of the cycle 3, and the need is on cycle 4, so you can go straight to the end of cycle 3. Send value to the x-phase of the second notification. So, we can take the next step to it. This you get the right value for registration and the delay has been reduced. Now we have reduced number of stalls in this case is 3 to zero.



So stalls needed is utmost 1 -