

# Assignment 7

Q 1) [10 marks] How can control hazards be handled through inter-locking? What is the minimum number of bubbles that need to be introduced? Explain clearly with diagrams.

Q 2) [5 marks] Is there any way to reduce the performance impact introduced through interlocking-based handling of control hazards?

Q 3) [5 marks] In pipeline forwarding, suppose an instruction has r5 as a source operand. It has just reached the OF stage. There is an instruction in MA stage that writes to r5, and similarly there is an instruction in RW stage that writes to r5. Can forwarding be done? If so, from which stage to which stage? Why?

Q 4) [5 marks] Consider a program that has 30% of its dynamic instructions as conditional branch instructions, and that 80% of these branches are not taken.

Now we have two processors P1 and P2. P1 runs at a frequency of 1GHz, while P2 runs at a frequency of 1.2GHz. P1 has a branch misprediction penalty of 2 cycles, while P2 has a penalty of 3 cycles.

Which processor gives better performance?

Assume there are no data hazards in the program. Assume that both processors have an ideal CPI of 1.