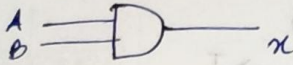


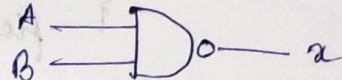
Logic gates

AND



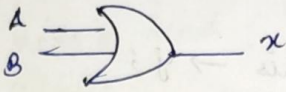
$$X = A \cdot B \\ = AB$$

NAND



$$X = (AB)'$$

OR



$$X = A + B$$

NOR



Inverter



$$X = A'$$

Buffer



$$X = A$$

XOR

K-Map

A \ B	0	1
0		
1		

A \ BC	00	01	11	10
0				
1				

AB \ CD	00	01	11	10
00	1	1	0	0
01	0	0	0	1
11	0	0	0	0
10	1	1	0	1

~~SOP~~ SOP

$$\Sigma = 0, 1, 6, 8, 9, 10$$

B'C' fixed.

AB'D'

A'B'CD'

don't care - 6, 12.

SOP

	CD 00	01	11	10
AB 00	1	1	0	1
01	0	1	0	X 1
11	X	0	0	0
10	1	1	0	1

$$B'C' + B'D' + A'C'D + A'CD' + A'CD'$$

Computer System Architecture
by Morris Mano.

	00	01	11	10
00	1	1	0	1
01	0	1	0	X 0
11	0 X	0	0	0
10	1	1	0	1

POS

	00	01	11	10
00	1	1	0	1
01	0	1	0	X 0
11	0 X	0	0	0
10	1	1	0	1

$$Y = B'C' + B'D' + A'C'D + A'CD' + A'CD' \text{ SOP}$$

$$Y = (C' + D')(A' + B')(B' + D) \text{ POS}$$

Full adder.

i/p			O/P	
x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

S: 1, 2, 4, 7.
C: 3, 5, 6, 7

sum

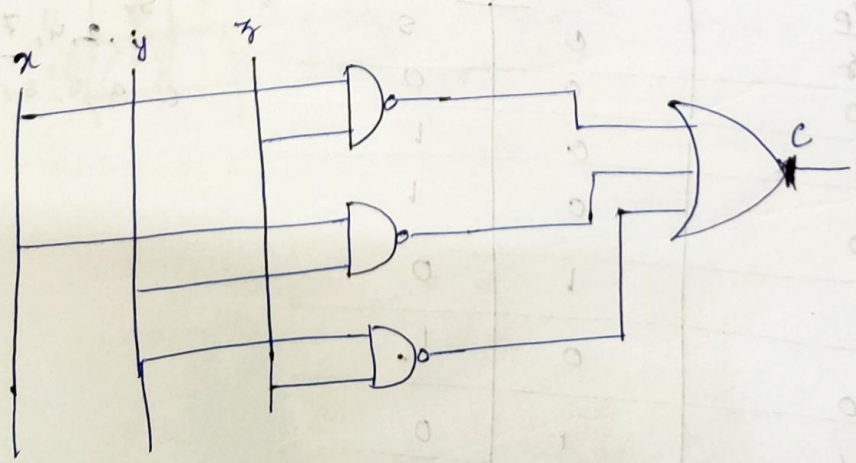
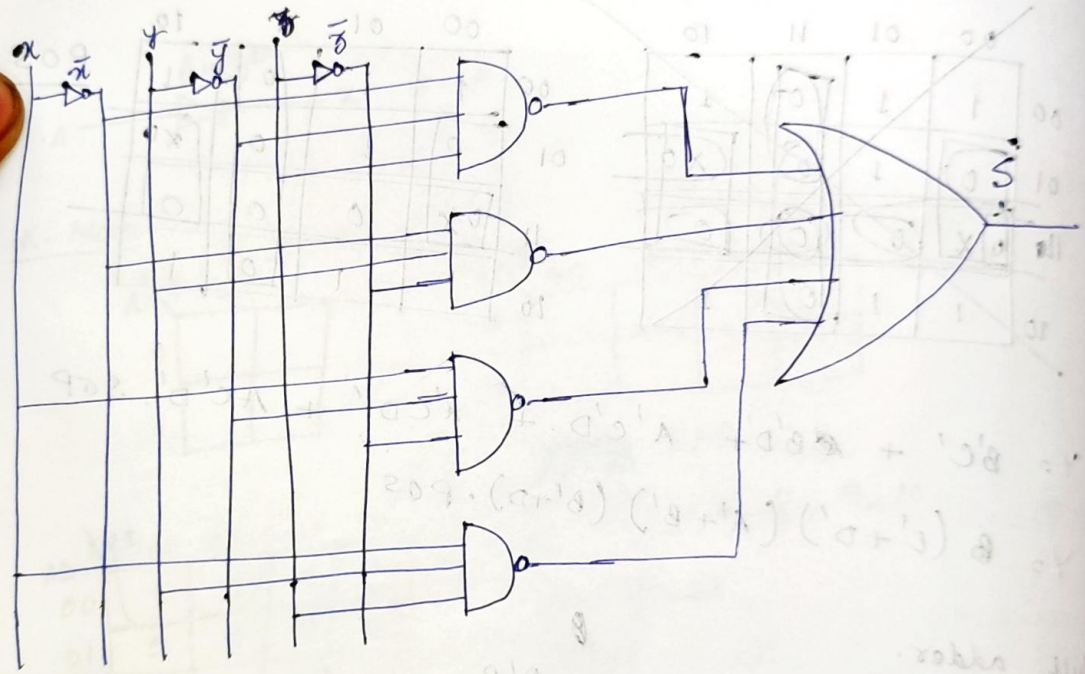
$x \backslash yz$	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$x \backslash yz$	00	01	11	10
0	0	0	1	0
1	0	1	1	1

CARRY

$$S = x'y'z + x'yz' + xy'z' + xyz$$

$$C = xz + xy + yz$$



20/10/22 ; operator.

b = 2, c = 3

a = ~~++~~(++b, ++c); precedence \rightarrow left to right.
returns right most value.

a = 4

class A

```
{  
    int x;  
    public:
```

op A operator, (A ob)

```
{
```

ob t;

t.x = ob.x;

return ob;

```
}
```

2/11/22

COCA

TTL \rightarrow Transistor Transistor Logic.

ECL \rightarrow Emitter coupled logic.

MOS \rightarrow Metal oxide semiconductor.

CMOS \rightarrow Complementary MOS.

Decoders. 3x8 decoder

O/P

enable

0

1

1

1

1

1

1

1

1

A₂ A₁ A₀

0 0 0

0 0 1

0 1 0

0 1 1

1 0 0

1 0 1

1 1 0

1 1 1

Enable

A₂ A₁ A₀

D₇ D₆ D₅ D₄ D₃

0

X X X

000

1

0 0 0

1

0 0 1

1

0 1 0

1

0 1 1

1

1 0 0

1

1 0 1

1

1 1 0

1

1 1 1

8x3 encoder Octal to binary.

FAT → 111110100111

2 | 78 - 0
2 | 39 - 1
2 | 19 - 1
2 | 9 - 1
2 | 4 - 0
2 | 2 - 0
1

1009110

(736.4)₈ = ()₁₀

478

7 3 6 . 4

$7 \times 8^2 + 3 \times 8^1 + 6 \times 8^0 + \frac{4}{8}$

478.5

64
x 7

448

24

472

6

478

$$(41.6875)_{10} = (?)_2 \quad 101001.1011$$

$$\begin{array}{r} 0.6875 \\ \times 2 \\ \hline 1.3750 \\ \times 2 \\ \hline 2.7500 \\ \times 2 \\ \hline 5.5000 \\ \times 2 \\ \hline 11.0000 \end{array}$$

$$\begin{array}{r} +13 \quad 01101 \\ +6 \quad +0110 \\ \hline 10011 \end{array}$$

-6 \Rightarrow

$$\begin{array}{r} 2 \overline{) 41 - 1} \\ 2 \overline{) 20 - 0} \\ 2 \overline{) 10 - 0} \\ 2 \overline{) 5 - 1} \\ 2 \overline{) 2 - 0} \\ \hline 1 \end{array}$$

101001.

$$\begin{aligned} \text{cat} &= \text{cat} + \log \\ \text{cat} + &= \log. \\ \text{catlog} \end{aligned}$$

6/11/22.

template <class T> // generic
void swap (<T> (T &a, T &b)

{
 T temp; temp = a; a = b; b = temp;

};

int main ()

{
 swap <int> (2, 3);
 swap <float> (1.5, 0.75);

}

template <class T, int a> // specific

int add <T> (T x).

{
 return x+a;
}

int main ()

{
 add <int, 2> (5);
 add <float, 3> (4.5);

7/11/22 String

#include <string>

string s = "Hello";

cin >> s; [A space is the end of a string].

getline (cin, s);

int → string s = s + "10"; [concatenation].

COA 10/11/22

$$\begin{array}{r} 13 \\ - 6 \\ \hline \end{array}$$

$$\begin{array}{r} 1101 \\ - 0110 \quad 2's \\ \hline \end{array} \rightarrow$$

$$\begin{array}{r} 1101 \\ 1010 \\ \hline 10111 \end{array}$$

Including sign bit.

$$\begin{array}{r} 13 \quad 01101 \\ - 6 \quad 00110 \quad 1's \rightarrow 11001 \quad 2's \rightarrow \end{array}$$

$$\begin{array}{r} 01101 \\ 11001 \\ \hline 100111 \end{array}$$

$$\begin{array}{r} 00111 \quad (7) \\ 01110 \quad -(14) \\ \hline 10001 \quad 2's \rightarrow 10001 \\ \hline 10010 \end{array}$$

$$\begin{array}{r} 00111 \\ 10010 \\ \hline 11001 \quad 1's \rightarrow 10010 \\ \hline 10111 \end{array}$$

$$\begin{array}{r} 1001 \\ \times 1001 \\ \hline \end{array}$$

$$\begin{array}{r} 1101 \\ \times 1001 \\ \hline 1101 \\ 0000X \\ 0000XX \\ 1101XXX \\ \hline 1110101 \end{array}$$

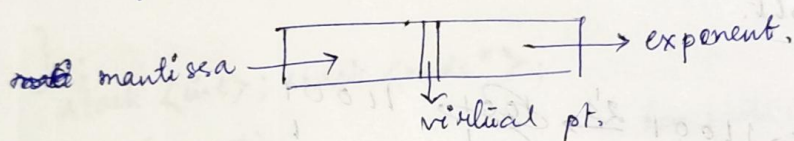
$$7) 5000 ($$

$$111) \underline{11010} (0.11$$

$$\begin{array}{r} 111 \\ - 111 \\ \hline 9900 \\ - 111 \\ \hline 101 \end{array}$$

$$\begin{array}{r|l} 70 & 01000110 \\ + 80 & 01010000 \\ \hline \end{array}$$

Use flip-flop when we have an extra bit - due to similar sign. It is outside register.



Parity bit

Odd/even parity \rightarrow Odd no. of 1s, \rightarrow odd
even " " " " even

detects error correctly.

LAB

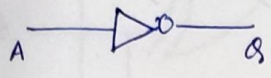
(i) Verification of universal gates

(ii) Realization of half adder

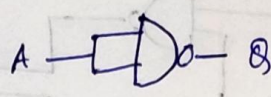
(iii) Realization of full adder using half adder.

12/11/22

NOT



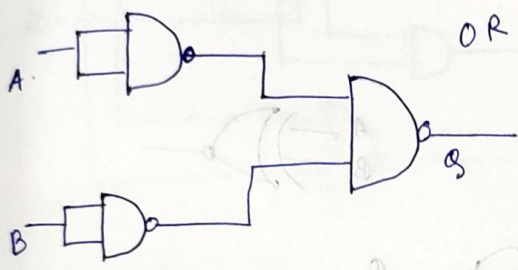
Input	Output
0	1
1	0



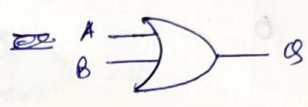
AND



Input		Output
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

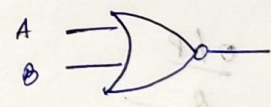
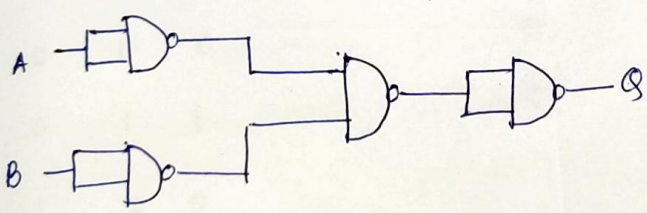


OR

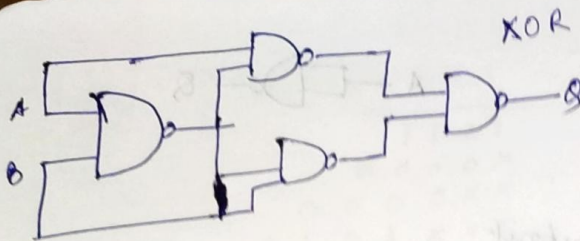


Input		Output
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

NOR

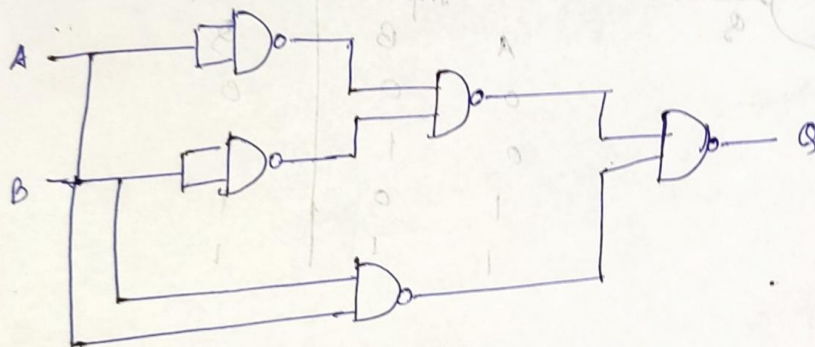


Input		Output
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0



Input		Output
A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

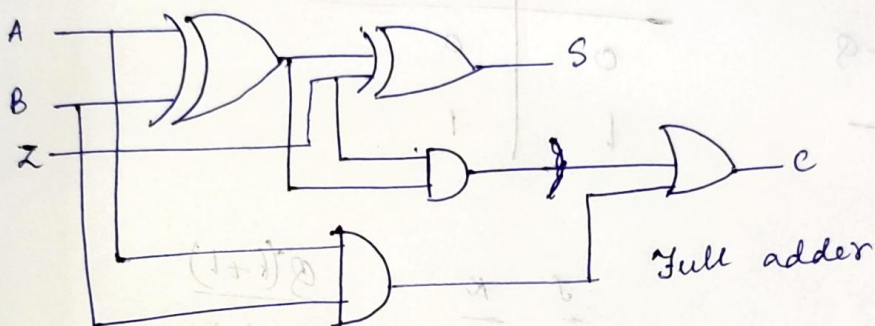
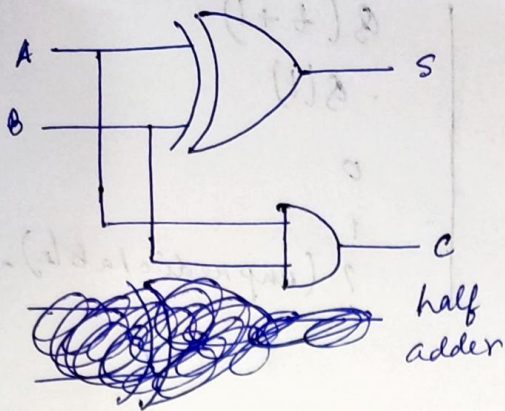
XNOR



i/P		o/P
A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

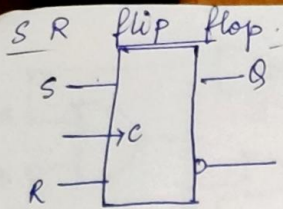
Using XOR & AND \rightarrow Half adder.

i/P		o/P	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



Half adder

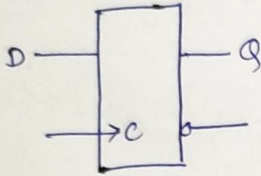
A	B	Z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



S	R
0	0
0	1
1	0
1	1

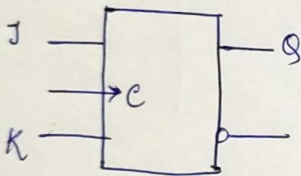
$Q(t+1)$
$Q(t)$
0
1
? (unpredictable)

D flip-flop



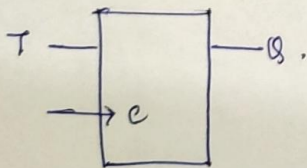
D	$Q(t+1)$
0	0
1	1

JK - Flip Flop



J	K	$Q(t+1)$
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$

T flip - flop



T	$Q(t+1)$
0	$Q(t)$
1	$Q'(t)$