ECE 6100: Project 3
Cache Coherence
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Following are the validation outputs for 4Proc, 8Proc, and 16Proc.

		4 PROC	8 PROC	16 PROC
MESI	Run Time:	123283 cycles	203059 cycles	369291 cycles
	Cache Misses:	1576 misses	2671 misses	4724 misses
	Cache Accesses:	1912 accesses	3148 accesses	5414 accesses
	Silent Upgrades:	105 upgrades	103 upgrades	116 upgrades
	$-to-$ Transfers:	375 transfers	694 transfers	1126 transfers
MOSI	Run Time:	137695 cycles	193981 cycles	280113 cycles
	Cache Misses:	1682 misses	2779 misses	4842 misses
	Cache Accesses:	1912 accesses	3148 accesses	5414 accesses
	Silent Upgrades:	0 upgrades	0 upgrades	0 upgrades
	$-to-$ Transfers:	339 transfers	895 transfers	2138 transfers
MOESIF	Run Time:	102085 cycles	105347 cycles	110591 cycles
	Cache Misses:	1576 misses	2667 misses	4725 misses
	Cache Accesses:	1912 accesses	3148 accesses	5414 accesses
	Silent Upgrades:	105 upgrades	105 upgrades	118 upgrades
	$-to-$ Transfers:	587 transfers	1667 transfers	3714 transfers

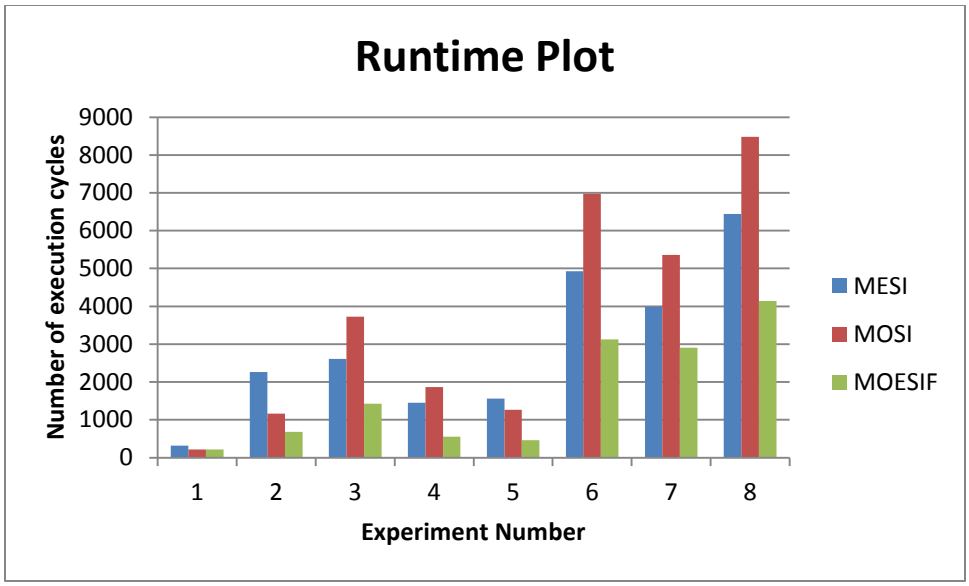
Following are the design results of the experiment trace files.

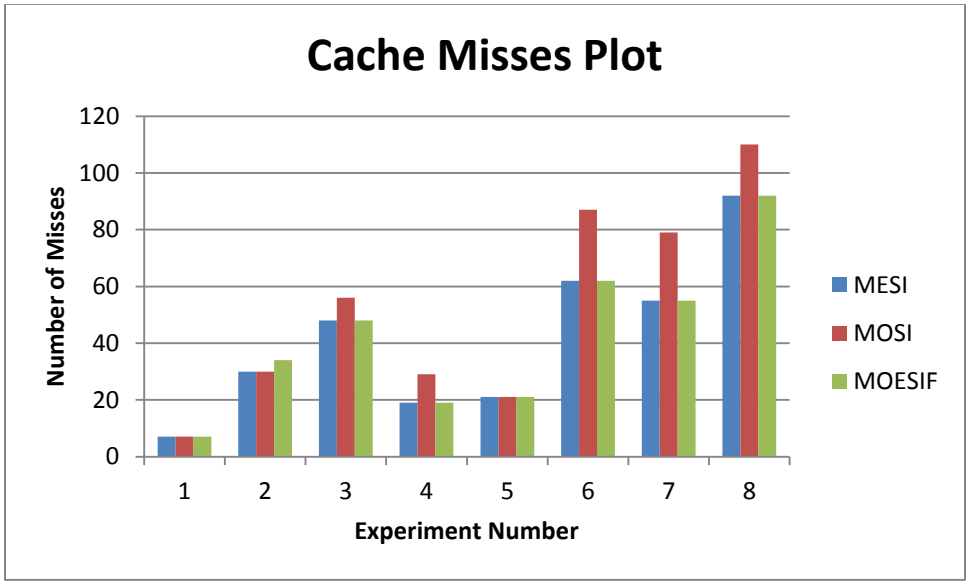
		Experiment1	**Experiment2**	**Experiment3**	**Experiment4**
MESI	Run Time:	317 cycles	2267 cycles	2607 cycles	1447 cycles
	Cache Misses:	7 misses	30 misses	48 misses	19 misses
	Cache Accesses:	12 accesses	104 accesses	200 accesses	60 accesses
	Silent Upgrades:	0 upgrades	1 upgrades	8 upgrades	3 upgrades
	$-to-$ Transfers:	4 transfers	8 transfers	23 transfers	5 transfers
MOSI	Run Time:	217 cycles	1167 cycles	3723 cycles	1869 cycles
	Cache Misses:	7 misses	30 misses	56 misses	29 misses
	Cache Accesses:	12 accesses	104 accesses	200 accesses	60 accesses

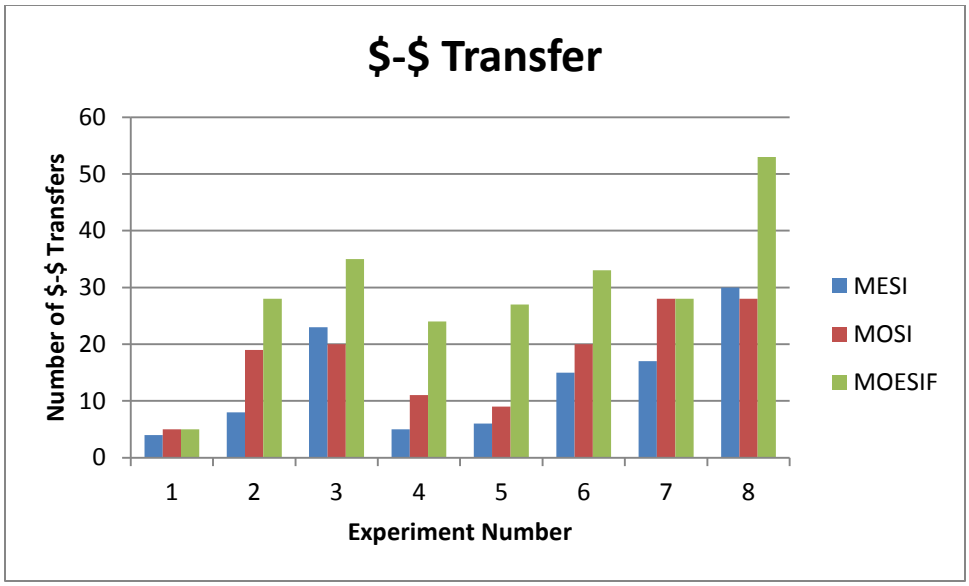
	Silent Upgrades:	0 upgrades	0 upgrades	0 upgrades	0 upgrades
	$-to-$ Transfers:	5 transfers	19 transfers	20 transfers	11 transfers
MOESIF	Run Time:	217 cycles	683 cycles	1425 cycles	551 cycles
	Cache Misses:	7 misses	34 misses	48 misses	19 misses
	Cache Accesses:	12 accesses	104 accesses	200 accesses	60 accesses
	Silent Upgrades:	0 upgrades	1 upgrades	8 upgrades	3 upgrades
	$-to-$ Transfers:	5 transfers	28 transfers	35 transfers	14 transfers

		Experiment5	**Experiment6**	**Experiment7**	**Experiment8**
MESI	Run Time:	1561 cycles	4925 cycles	3993 cycles	6441 cycles
	Cache Misses:	21 misses	62 misses	55 misses	92 misses
	Cache Accesses:	37 accesses	747 accesses	952 accesses	800 accesses
	Silent Upgrades:	0 upgrades	25 upgrades	24 upgrades	19 upgrades
	$-to-$ Transfers:	6 transfers	15 transfers	17 transfers	30 transfers
MOSI	Run Time:	1261 cycles	6975 cycles	5359 cycles	8477 cycles
	Cache Misses:	21 misses	87 misses	79 misses	110 misses
	Cache Accesses:	37 accesses	747 accesses	952 accesses	800 accesses
	Silent Upgrades:	0 upgrades	0 upgrades	0 upgrades	0 upgrades
	$-to-$ Transfers:	9 transfers	20 transfers	28 transfers	28 transfers
MOESIF	Run Time:	461 cycles	3125 cycles	2909 cycles	4141 cycles
	Cache Misses:	21 misses	62 misses	55 misses	92 misses
	Cache Accesses:	37 accesses	747 accesses	952 accesses	800 accesses
	Silent Upgrades:	0 upgrades	25 upgrades	24 upgrades	19 upgrades
	$-to-$ Transfers:	17 transfers	33 transfers	28 transfers	53 transfers

Plots:


Runtime Plot
Number of execution cycles
9000
8000
7000
6000
5000
4000
3000
2000
1000
0
1
2
3
4
5
6
7
8
Experiment Number
MESI
MOSI
MOESIF


Cache Misses Plot
Number of Misses
120
100
80
60
40
20
0
1
2
3
4
5
6
7
8
Experiment Number
MESI
MOSI
MOESIF



Observations:

1. Runtime:

We observe that for the experiments with low number of instructions (experiments 1,2,5) run time generally decreases in the order MESI > MOSI > MOESIF. But for experiments which take more number of cycles to execute (for example Experiment 6, 7 and 8) we see that the order of decreasing run time is MOSI > MESI > MOSIF. This can be explained as presence of E state in MESI which allows silent upgrade, thus reducing the memory accesses. Also, once in E state, if another cache requests for it, the cache in E state can send it via cache to cache transfer to the requesting cache. So in absence of E state, even if just one cache has a particular block, and its processor wishes to modify it, the block still has to send a get M on the bus, which has to be returned with the data block from memory. Also, in the absence of E state, the second processor that requests the same block (to share or modify) it cannot be directly shared between the caches.

We observe that MOESIF takes least number of cycles to execute in all experiments. This is clearly because of presence of F state. The forwarder state reduces the number of memory accesses drastically as everytime a cache requests for a block, it can be share on the bus if another cache has it.

2. Cache Misses:

The other statistics like number of misses are equal or almost equal for MESI and MOESIF because the additional states like O and F do not add to misses. MOSI has higher (or equal) number of cache misses in all three experiments. This can be explained as due to presence of higher coherence miss, and absence of silent upgrade. Thus, if a modified block is present in MESI, and the processor of the cache requests for it, it is a hit. In MOSI, if the processor requests for a block the cache has in O state, it must send a GetM to invalidate all other caches that have it.

3. Cache to Cache Transfer:

We see that MOESIF has significantly higher cache to cache transfer in all experiments. This Is due to presence of F state. The memory need not be accesses ache time a block is requested that is present in one of the other caches.

Thus MOESIF is the most effective protocol as it takes less cycles to complete execution, and gives favorable other statistics like lower cache to cache transfers.