Design Of a Single-Stage Differential Amplifier

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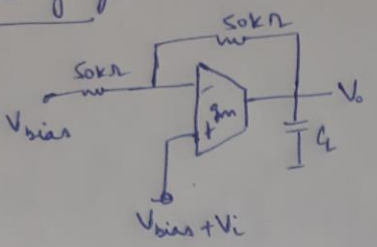
GIVEN SPECIFICATIONS:

VDD=1.8V, CL=10pF, Loop Gain= 35dB,
–3dB Bandwidth of V0/Vi (min), CMRR(@DC)=80dB

CALCULATING Gm THEORETICALLY

① Calculating gm

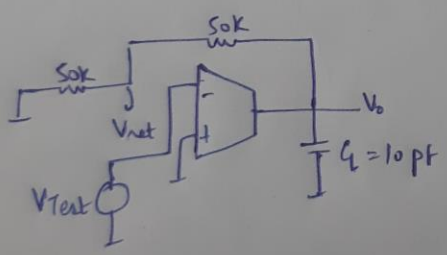


Given, open loop gain = 35dB
(LG))

$20\log|LG| = 35$

$\boxed{|LG| = 56.234}$

b) Calculating loop gain by breaking the load from that, we will calculate gm.



$$V_{test} = -g_m V_{test}(50k\Omega) \,/\, 1+(50k\Omega+50k\Omega)sC_L$$

$$|LG| = \frac{-V_{test}}{V_{test}} = \frac{g_m(50k\Omega)}{1+2sC_L(50k\Omega)}$$

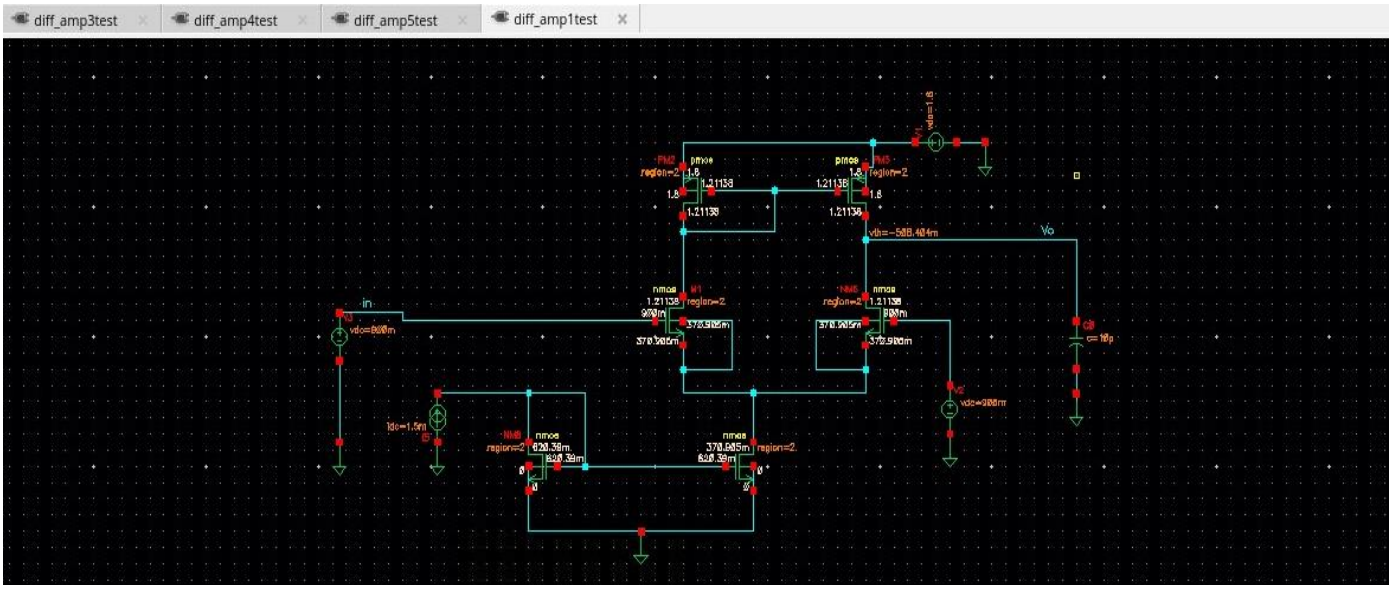
Given $\omega_{u,loop} = 2\pi \times 150 \times 10^6$ M

At $\omega_{u,loop}$, $|LG| = 1$

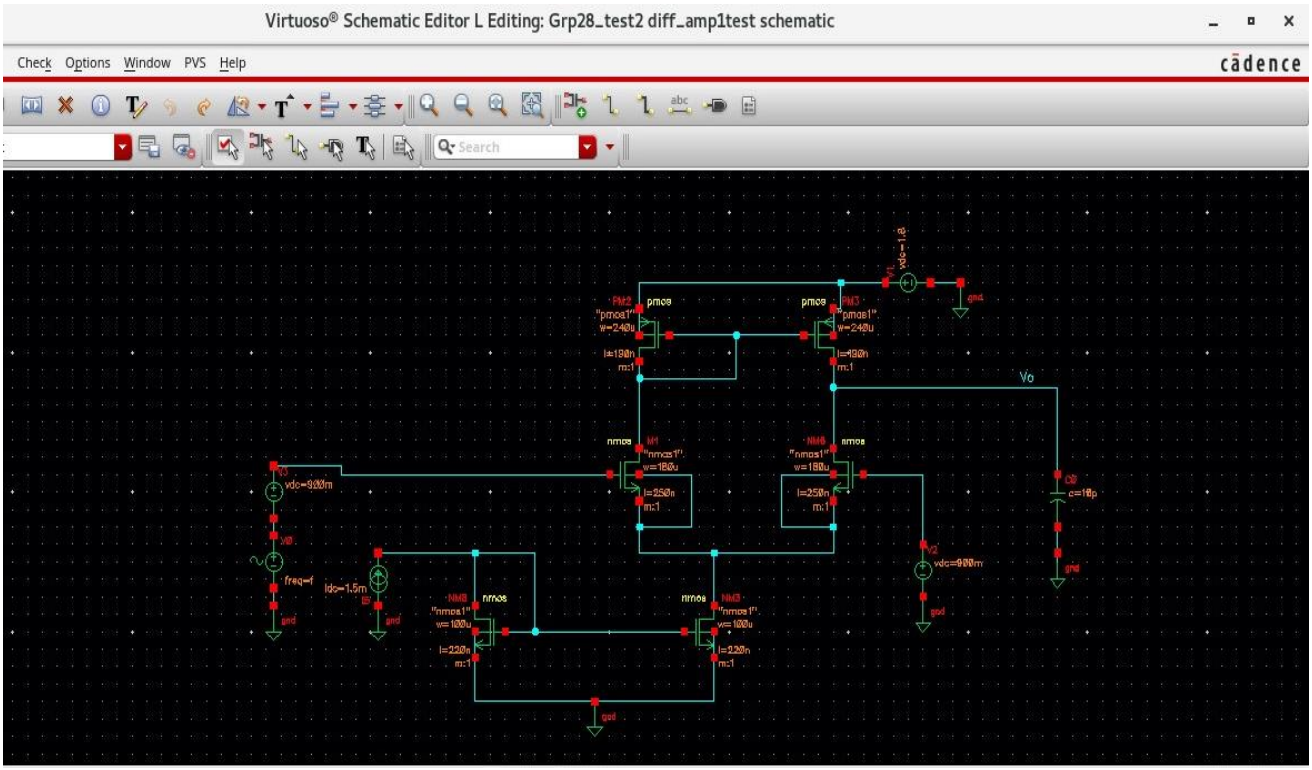
$$\Rightarrow 1 = \frac{g_m}{2\times 2\pi \times 150\times 10^6 \times 10\times 10^{-12}} \Rightarrow \boxed{g_m = 12.566\,mS}$$

OPEN LOOP GAIN AND PHASE

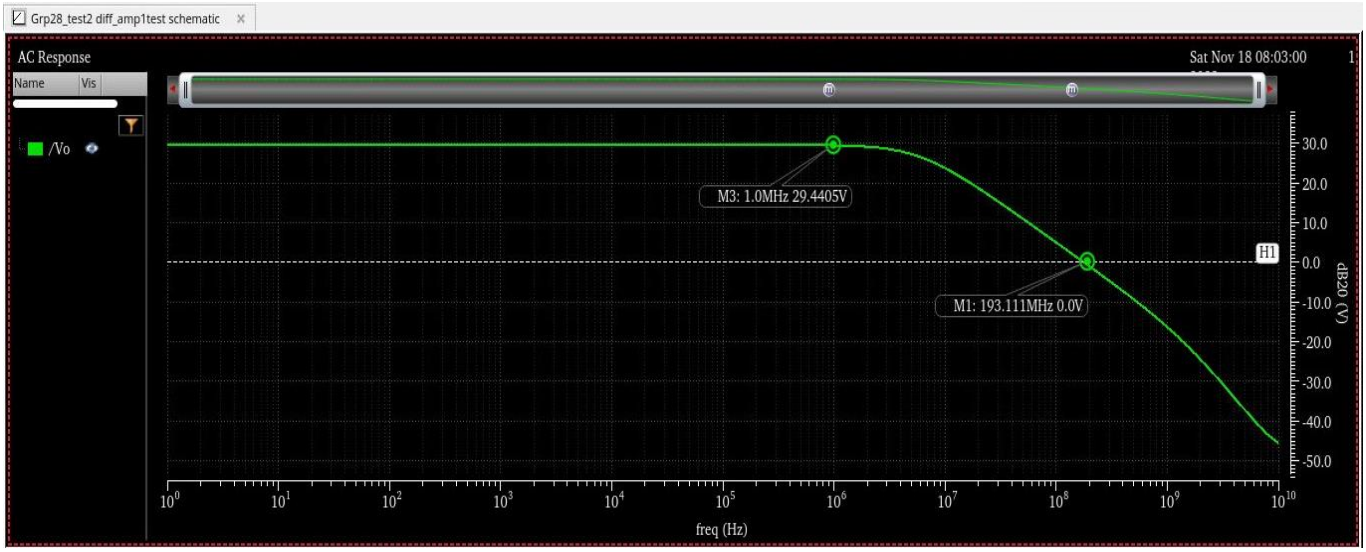
OPEN LOOP DC SCHEMATIC SHOWING REGION OF OPERATION OF EACH TRANSISTOR



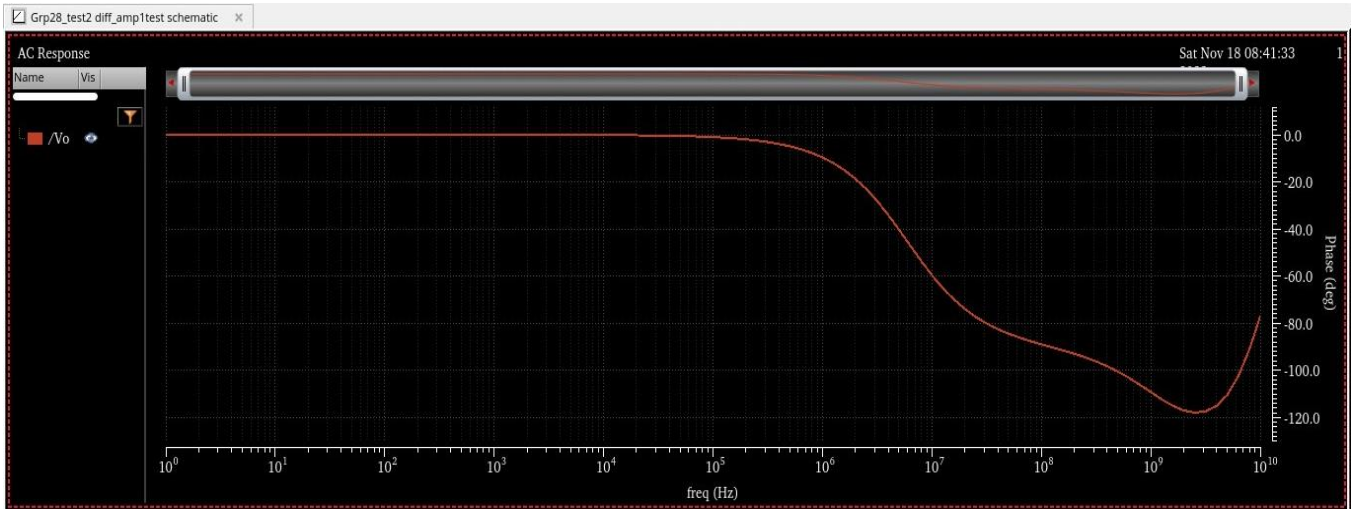
OPEN LOOP AC SCHEMATIC



OPEN LOOP GAIN PLOT

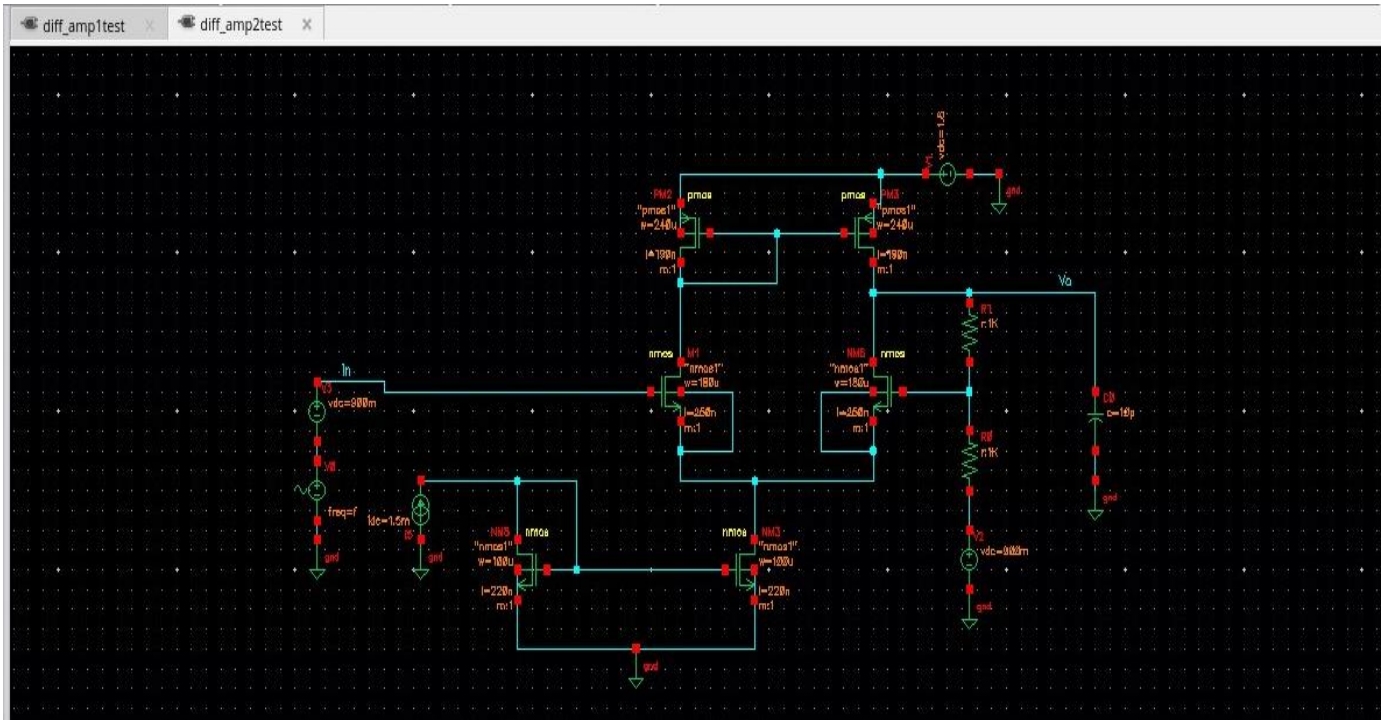


OPEN LOOP PHASE PLOT

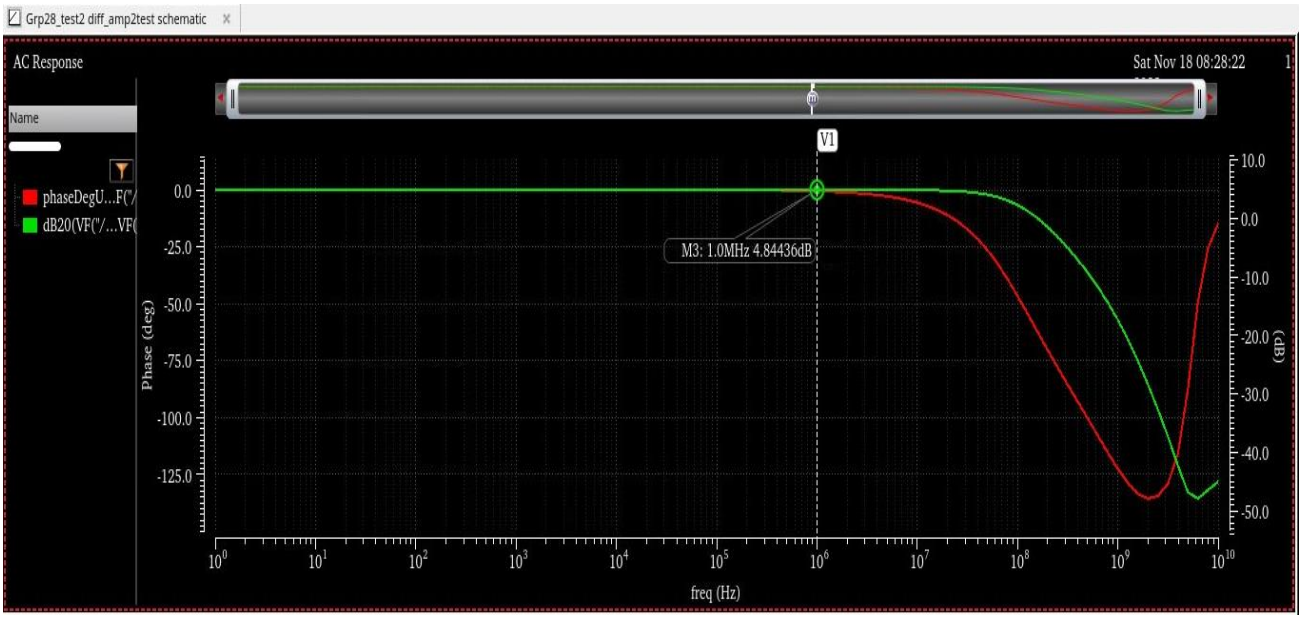


CLOSED LOOP GAIN AND PHASE

CLOSED LOOP SCHEMATIC

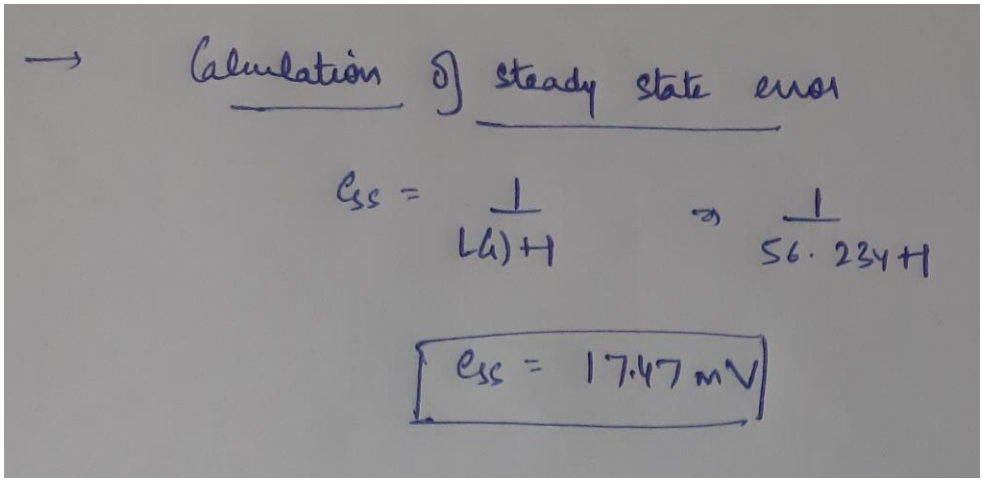


CLOSED LOOP GAIN AND PHASE PLOT

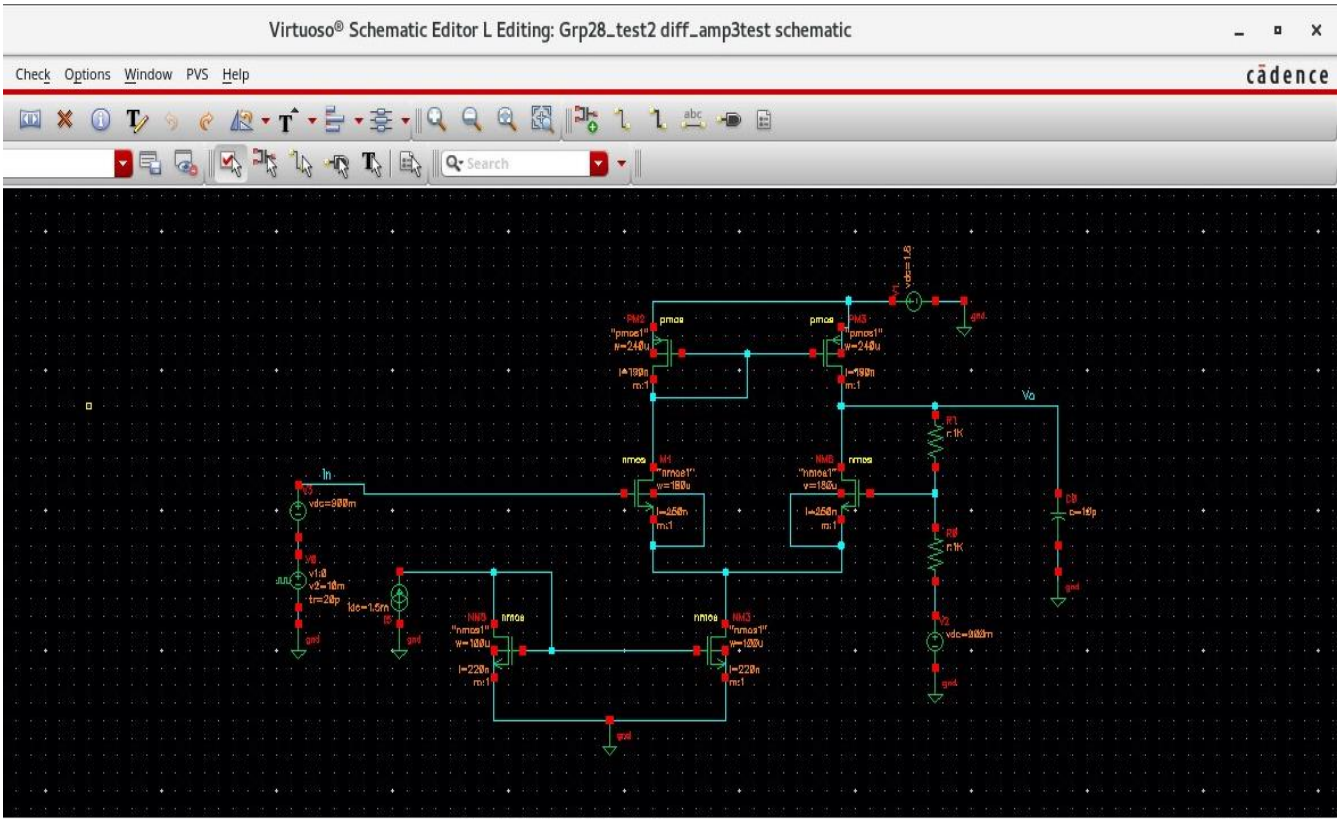


TRANSIENT RESPONSE OF THE NON-INVERTING AMPLIFIER WITH A 0.01 V STEP INPUT AT Vi

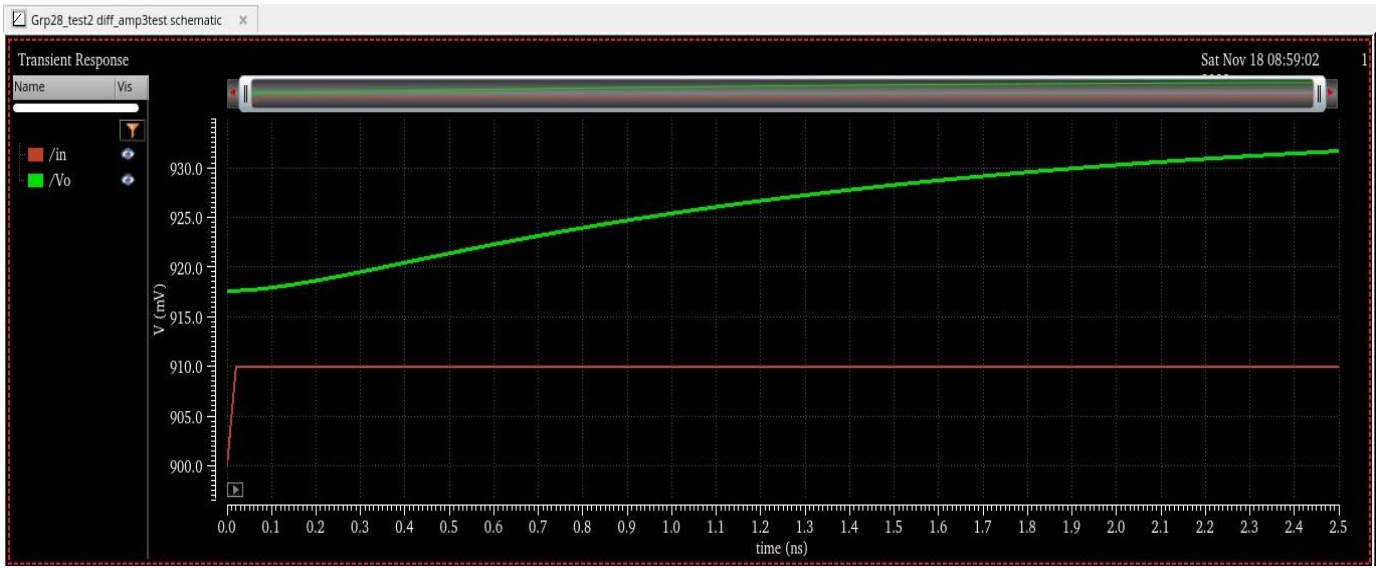
THEORETICALLY CALCULATED STEADY STATE ERROR



SCHEMATIC FOR CALCULATION OF STEADY STATE ERROR

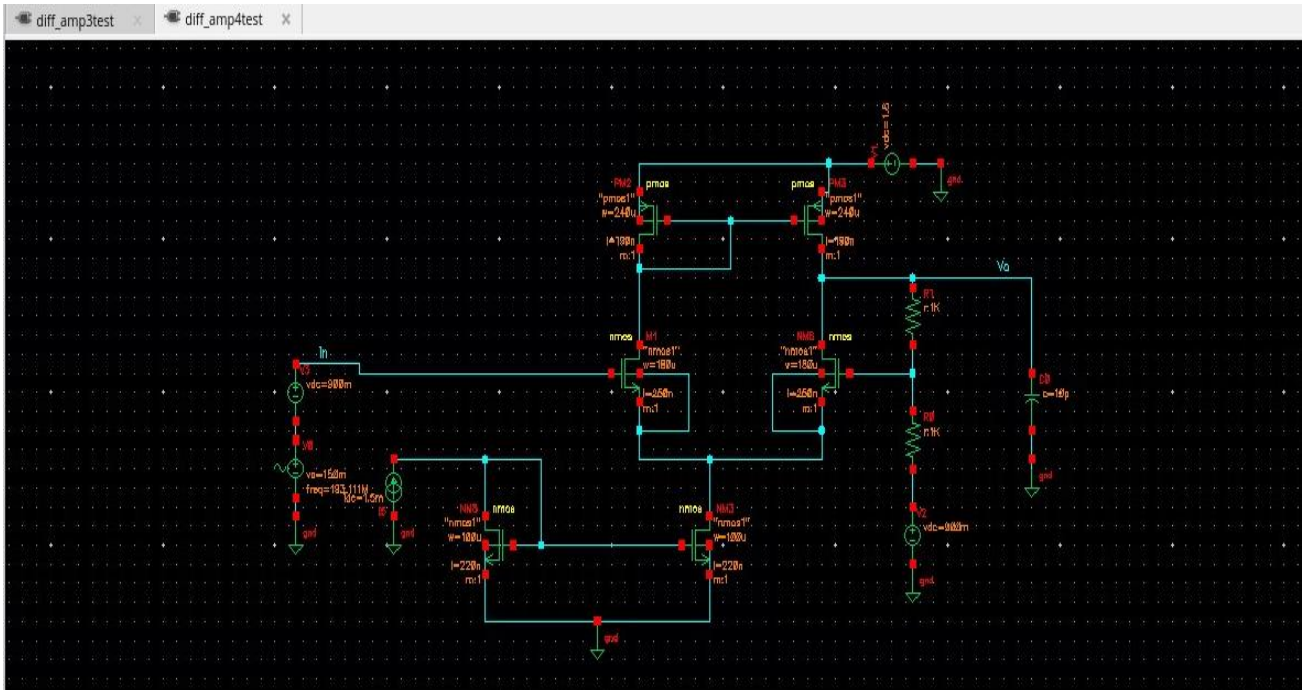


PLOT FOR TRANSIENT RESPONSE

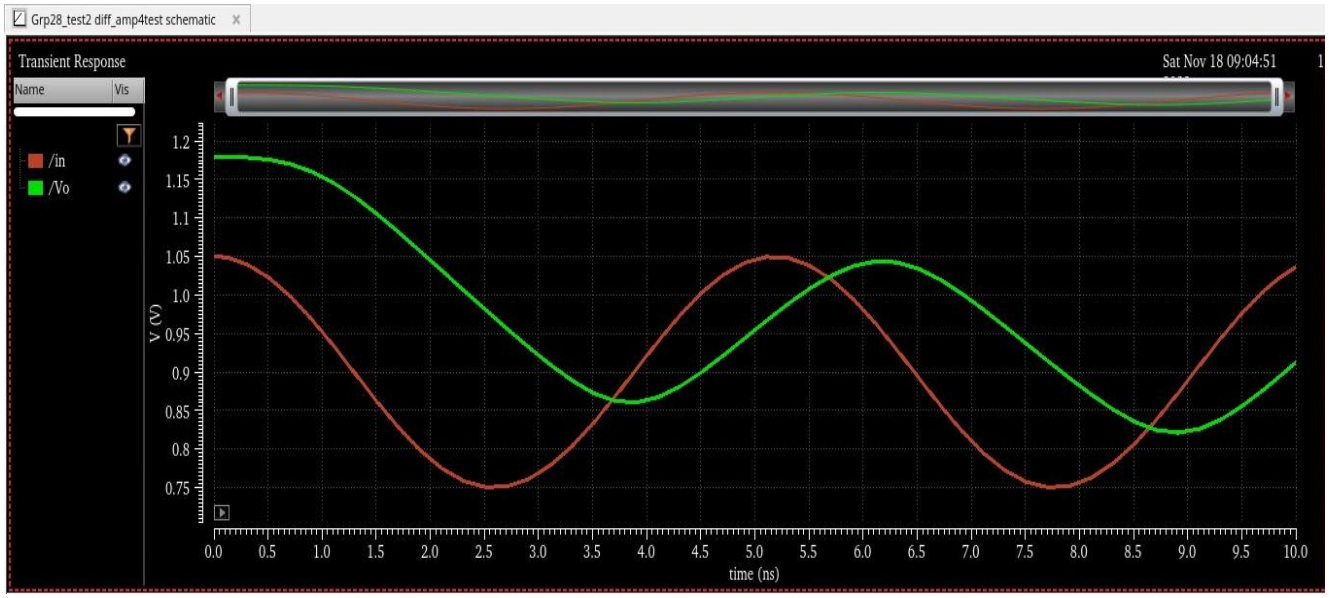


TRANSIENT RESPONSE OF THE NON-INVERTING AMPLIFIER WHEN Vi = 150 MV cos(Ω3dB T)

SCHEMATIC FOR TRANSIENT RESPONSE

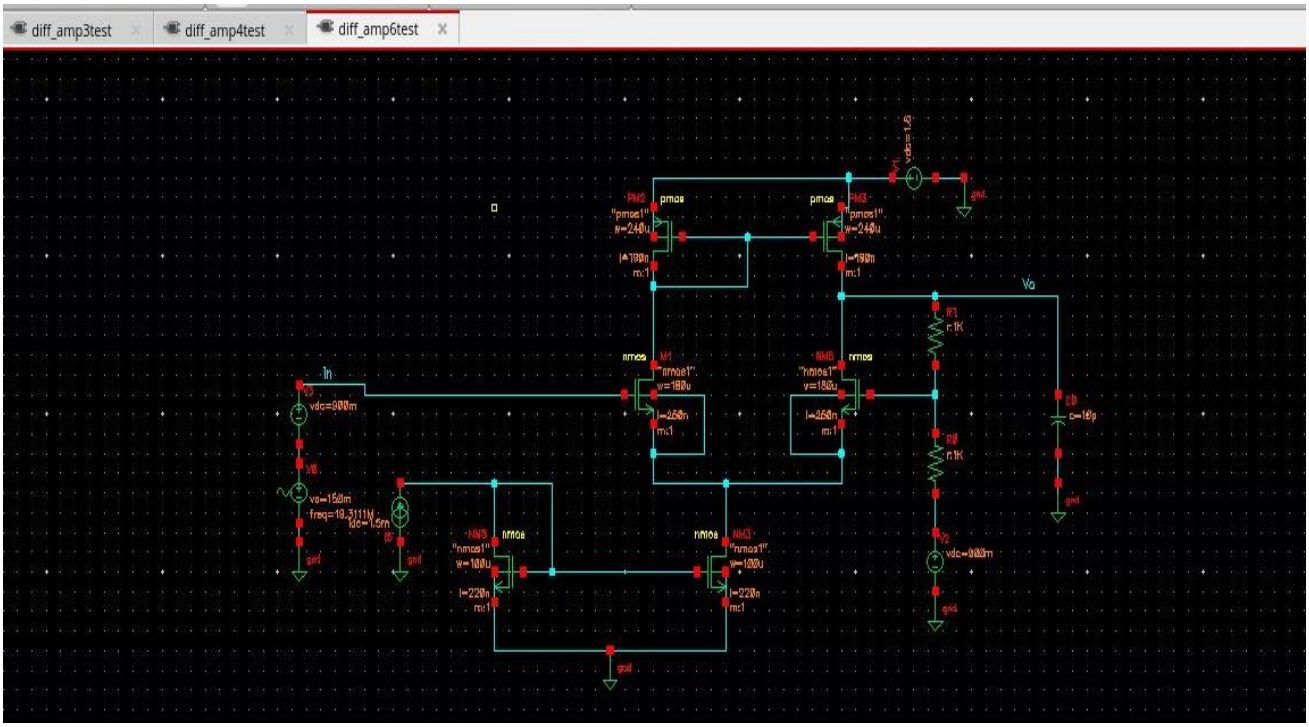


PLOT OF TRANSIENT RESPONSE

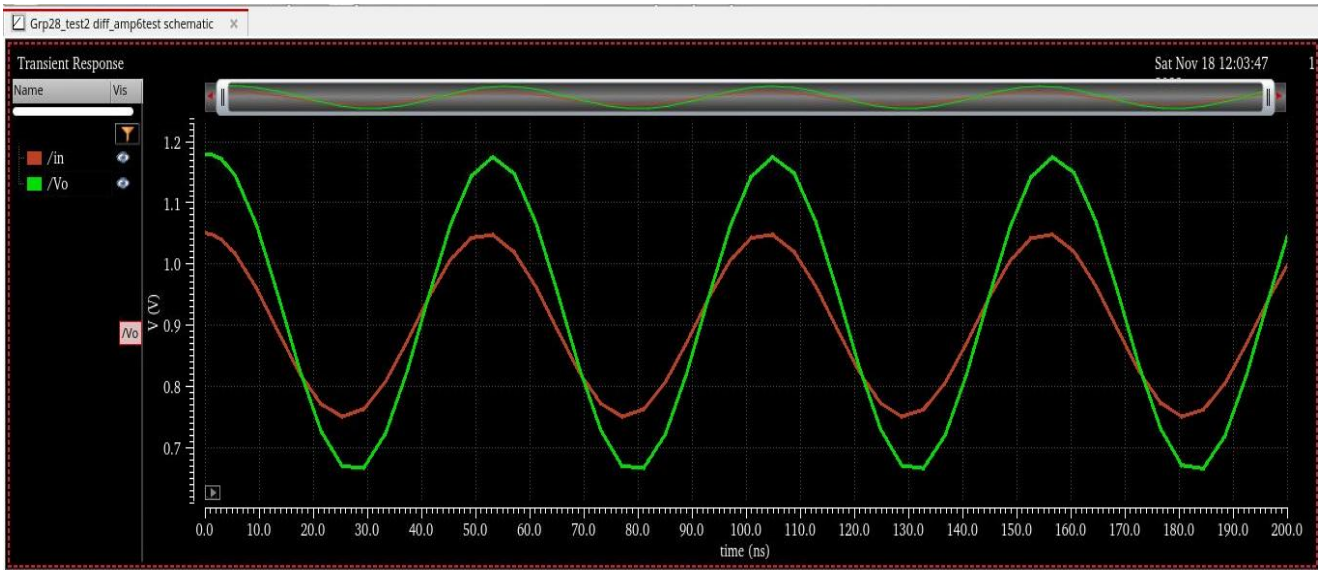


TRANSIENT RESPONSE OF THE NON-INVERTING AMPLIFIER WHEN Vi = 150 MV COS((Ω3dB/10) T)

SCHEMATIC FOR TRANSIENT RESPONSE

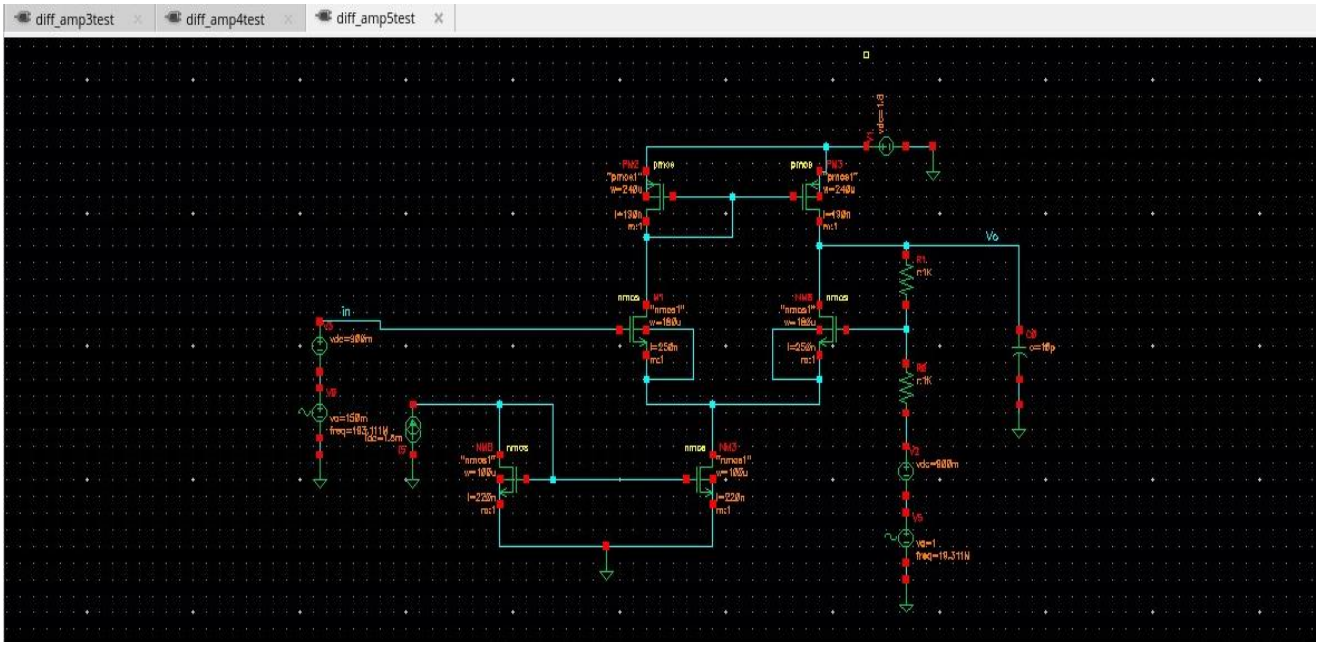


PLOT OF TRANSIENT RESPONSE

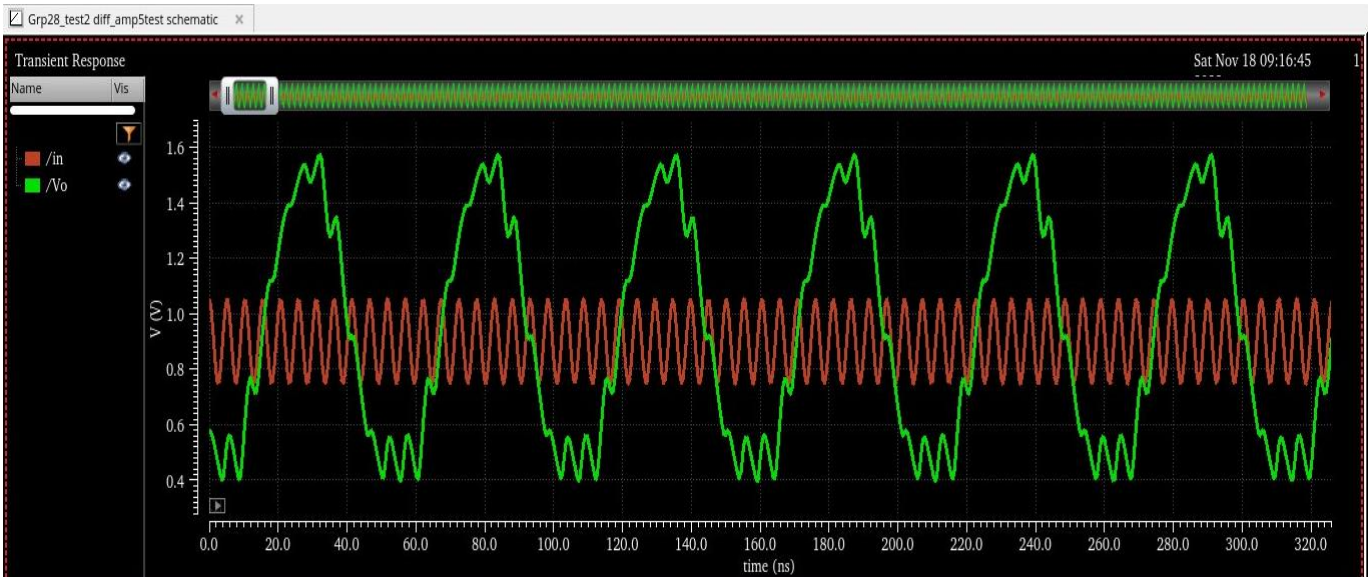


DIFFERENCE BETWEEN THE INPUT VOLTAGES OF THE DIFFAMP IN FIG. 1(A) FOR INPUTS 150 mV COS(ω3dB T) AND 150 mV COS((ω3dB/10)T).

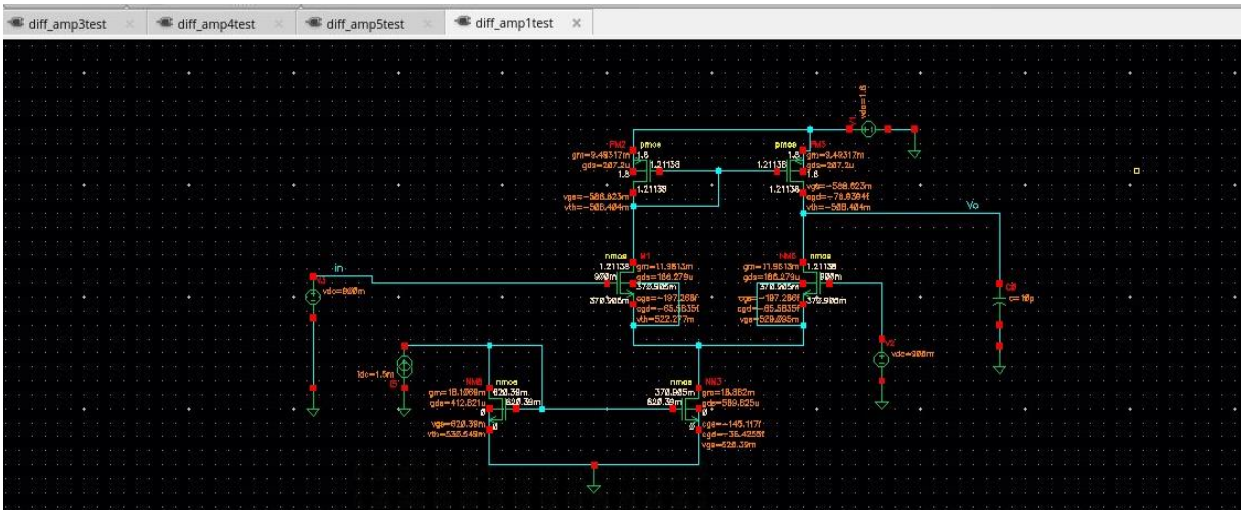
SCHEMATIC



PLOT OF THE DIFFERENCE BETWEEN THE INPUT VOLTAGES OF THE DIFFERENTIAL AMPLIFIER

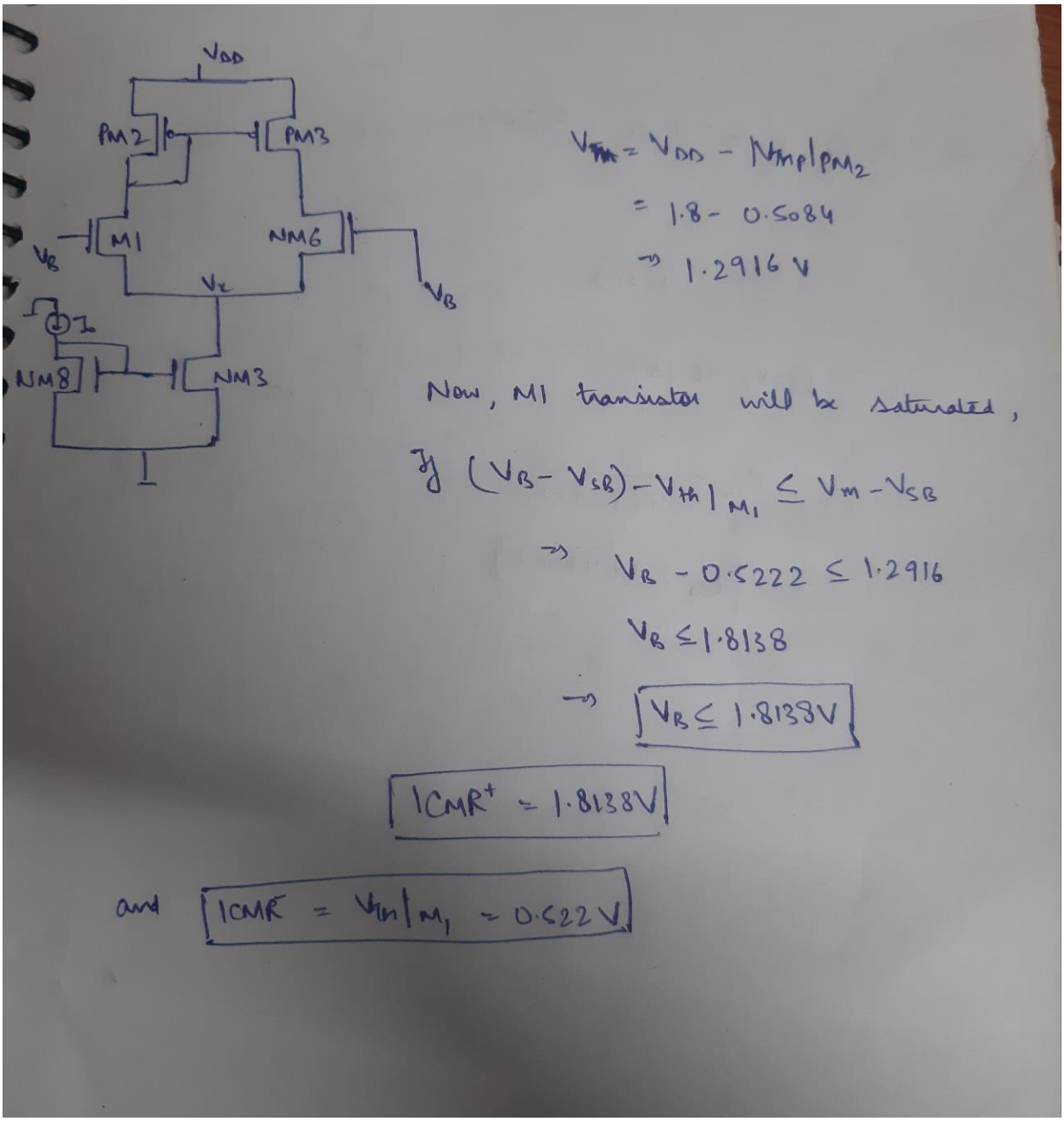


TABULATION OF Gm, Gds, Cgs, Cgd, Vov



	gm	gds	Cgs	Cgd	Vov
M1(nmos)	11.963mS	186.279uS	197.26f F	65.58f F	6.818mV
NM6(nmos)	11.963mS	186.279uS	197.26f F	65.58f F	6.818mV
PM2(pmos)	9.49317mS	207.2uS	329.603f F	76.93f F	-80.219mV
PM3(pmos)	9.49317mS	207.2uS	329.603f F	76.93f F	-80.219mV
NM8(nmos)	18.1069mS	412.821uS	144.894f F	36.354f F	89.282mV
NM3(nmos)	11.693mS	569.825uS	!45.114f F	36.354f F	89.282mV

THEOROTICAL CALCULATION OF ICMR+ AND ICMR-



$V_{th} = V_{DD} - |V_{thp}|_{PM_2}$

$= 1.8 - 0.5084$

$\Rightarrow 1.2916\ V$

Now, M1 transistor will be saturated,

If $(V_B - V_{SB}) - V_{th}|_{M_1} \leq V_m - V_{SB}$

$\Rightarrow V_B - 0.5222 \leq 1.2916$

$V_B \leq 1.8138$

$\Rightarrow \boxed{V_B \leq 1.8138V}$

$\boxed{ICMR^+ = 1.8138V}$

and $\boxed{ICMR^- = V_{th}|_{M_1} = 0.5222\ V}$