INTERNATIONAL INSTITUTE OF INFORMATION TECHNOLOGY
HYDERABAD

International Institute of Information Technology, Hyderabad

Course - VLSI Design

Date – 5/9/2019

LAB Assignment Submission Date – 15/9/2019 (23:59 IST).

Late submission will not be accepted.

LAB 2. Design ASIC (from Verilog code till GDSII File) using Cadence and Perform full FPGA Flow(from Verilog to Dumping code into FPGAs) for the following Digital Blocks.

a) MUX - 2*1 , 4*1 , 8*1
   Design 2*1 MUX using Logic gates and use it to create 4*1 MUX then use 4*1 MUX to create 8*1 MUX.
b) DEMUX - 1*4 , 1*8
   Design 1*2 DEMUX using logic gates and use it to create 1*4 DEMUX then use 1*4 DEMUX to create 1*8
c) DECODER - 2*1 , 2*4 , 3*8
   Design 2*1 DECODER using logic gates and use it to create 2*4 DECODER then use 2*4 DECODER to create 3*8 DECODER. Use enable pin also.
d) PRIORITY ENCODER - 8*3.
   Design 8*3 priority encoder using logic gates. Use enable pin also.

Write Verilog code and test benches for the above digital blocks.

Submit the following reports from Cadence:

1) Verilog code and Test bench.

2) All reports generates by genus: area, power, timing and netlist.

3) Innovus : Area, Power and Timing report (pre-place, post-place, post-rout, and sign-off).

4) Submit Snapshots: Timing Diagram (from NC launch), RTL schematic (from Genus) and Physical Design (from Innovus).

Make a report and write Truth table and Boolean expression of the output using K-MAP for the above digital blocks.

Mention Area, Power obtained from Genus and Innovus in it for above digital blocks.

FOR XILINX ISE -

1. Submit verilog code for main code, testbench and .ucf(implementation constraints file) file.

2. Submit the following snapshots from Xilinx ISE:

   a) Timing Diagram depicting clearly all possible combinations of test inputs
   b) RTL schematic depicting all logic gates present in the logic design

3. Also report Area, Power and Delay of your design.

Note: Submit reports in separate folder for each Digital Block.

Please make sure you don’t do it in the last day because the speed of server gets slow as everybody tries to access it. So start doing it from the first day and request regarding extension of deadline because of slowdown of servers won’t be accepted.

For learning Verilog and writing its test bench you can refer to the following website:

www.asic-world.com

How to submit your assignment:

1. Make a folder and rename it to your name_roll no and put rest of the folders inside it.

3. Compress that folder into .tar file and submit that folder in moodle.

NOTE: Cheating your LAB assignments from your friends is strictly prohibited though a group discussion is appreciable. Please make acknowledgements in your report if you have taken help from your friends.

If plagiarism (copying code) found strict action will be taken against you.

All The Best!!!