INTERNATIONAL INSTITUTE OF INFORMATION TECHNOLOGY
HYDERABAD

International Institute of Information Technology, Hyderabad

Course - VLSI Design

Date – 18/9/2019

LAB Assignment Submission Date – 25/8/2019 (23:59 IST).

Late submission will not be accepted.

LAB 1.

Write Verilog code and testbench for the following combinational gates :

AND, OR, NOR, NAND, XOR, NOT and XNOR

Use Xilinx ISE tool to write and simulate your code.

After that write Verilog code and test bench for the following compound combinational circuits.

a) **Y = AB + CD**
b) **Y = (ABC + DE).F**
c) **Y = ((A+B')(CD + E))'**

Write their truth table and also find their RTL schematics, Area, Power, Timing Diagram using Xilinx ISE and CADENCE.

Hint: It will be helpful if before starting your lab assignment you know the basic transistor level structure of the above gates.

For learning Verilog and writing its test bench you can refer to the following website:

www.asic-world.com

How to submit your assignment:

1. Make a folder and rename it to your name_roll no.

2. Provide your Verilog code (.v file) and test bench (.v file) inside that folder.

3. Make a report using Latex/MS word. Mention and explain your findings in it properly.

4. Compress that folder into .tar file and submit that folder in moodle.

NOTE: Cheating your LAB assignments from your friends is strictly prohibited though a group discussion is appreciable. Please make acknowledgements in your report if you have taken help from your friends.

If plagiarism (copying code) found strict action will be taken against you.

All The Best!!! ☺