INTERNATIONAL INSTITUTE OF INFORMATION TECHNOLOGY
HYDERABAD

International Institute of Information Technology, Hyderabad

Course - VLSI Design

Date – 2/10/2019

LAB Assignment Submission Date – 11/11/2019 (23:59 IST).

Late submission will not be accepted.

Design ASIC (from Verilog code till GDSII File) using Cadence and Perform full FPGA Flow(from Verilog to Dumping code into FPGAs) for the following Digital Blocks.

(1) Design 4 bit universal shift register.

(2) Design a finite state machine has one input and one output. The output becomes 1 and remains 1 thereafter when at least two 0's and two 1's have occurred as inputs, regardless of the order of appearance.

a) Assuming this is to be implemented as a Moore machine, draw a state transition diagram for the machine. Hint: You can do this in nine states.

b) Write a Verilog module that implements the machine. Your module should have the following inputs/outputs.
CLK used to clock the FSM
RESET asserted high to reset the FSM to its initial state
ONE asserted high to input a "1". Note that this signal may stay high for many cycles (eg, it's generated by a button press) before returning low. Each high period should count as a single "1" input, ie, to inputs two "1"s in series, the signal must return low in between the first and second "1".
ZERO asserted high to input a "0". This signal has the same timing protocol as ONE above.
OUT asserted high when at least two "0"s and two "1"s have occurred as inputs.
Assume that all inputs have been externally synchronized with clk.

Write Verilog code and test benches for the above digital blocks.
Submit the following inside a folder from Cadence:

1) Verilog code and Test bench.
2) All reports generates by genus: area, power, timing and netlist.
3) Innovus : Area, Power and Timing report (pre-place, post-rout, and sign-off).
4) Submit Snapshots: Timing Diagram (from NC launch), RTL schematic (from Genus) and Physical Design (from Innovus).

Make a report which will depict the area, power and delay obtained for all the above digital blocks.

FOR XILINX ISE -

1. Submit verilog code for main code, testbench and .ucf(implementation constraints file) file.
2. Submit the following snapshots from Xilinx ISE:

a) Timing Diagram depicting clearly all possible combinations of test inputs

b) RTL schematic depicting all logic gates present in the logic design

3. Also report Area, Power and Delay of your design.

Note: Submit reports in separate folder for each Digital Block.

Please make sure you don't do it in the last day because the speed of server gets slow as everybody tries to access it. So start doing it from the first day and request regarding extension of deadline because of slowdown of servers won't be accepted.

For learning Verilog and writing its test bench you can refer to the following website:

www.asic-world.com

How to submit your assignment:

1. Make a folder and rename it to your name_roll no and put rest of the folders inside it.

3. Compress that folder into .tar file and submit that folder in moodle.

NOTE: Cheating your LAB assignments from your friends is strictly prohibited though a group discussion is appreciated. Please make acknowledgements in your report if you have taken help from your friends.

If plagiarism (copying code) found strict action will be taken against you.

All The Best!!!