IE 417 - Embedded AI

All LABS

Group Name: Friendly Group

Avinash Baraiya- 202201211

Malhar Vaghasiya - 202201183

Smeet Agrawal - 202101237

Priyesh Tandel - 202101222

Samarth Panchal- 202101456

Guided By Prof. Tapas Kumar Maiti

GitHub Repo: https://github.com/AvinashB-DA/Embeded-AI

LAB 1: Voice Controlling LEDs

Edge-Impulse Trained Model:
https://studio.edgeimpulse.com/public/507931/live

LAB 2: Indoor Scene Classification

Edge-Impulse Trained Model:
https://studio.edgeimpulse.com/public/514520/live

LAB 3: Gesture-Based YouTube Controls

Edge-Impulse Trained Model:
https://studio.edgeimpulse.com/public/541977/live

LAB 4: Neural Networks for Chips

Collab File Link:
https://colab.research.google.com/drive/1KtQS5eeOSNFCWn4NqS9FsXwT2TLdUucg#scrollTo=ycV2KR2dILBT

IE417 : Embedded AI

Lab 1 - Voice Controlling LEDs with Edge Impulse

Submitted by

Avinash Baraiya- 202201211

Malhar Vaghasiya - 202201183

Smeet Agrawal - 202101237

Priyesh Tandel - 202101222

Samarth Panchal- 202101456

Submitted to

Professor Tapas Kumar Maiti

Dhirubhai Ambani Institute of Information and Communication Technology

Gandhinagar , Gujarat

Goal

In this lab, you are going to implement the following recipes:

1. Acquiring audio data with a laptop or smartphone
2. Extracting MFCC features from audio samples
3. Designing and training a neural network (NN) model
4. Tuning model performance with EON Tuner
5. Live classifications with a smartphone
6. Live classifications with the Arduino Nano
7. Continuous inferencing on the Arduino Nano

Video Link

Click below for YouTube Demo video

or Paste link in browser - https://youtu.be/Hpj7VdscqR0

Screenshots

FIGURE 1: Training

FIGURE 2: Create Impulse

FIGURE 3: Classifier

FIGURE 4: Data Acquisition

```
#define EIDSP_QUANTIZE_FILTERBANK   0

/**
   Define the number of slices per model window. E.g. a model window of 1000 ms
   with slices per model window set to 4. Results in a slice size of 250 ms.
   For more info: https://docs.edgeimpulse.com/docs/continuous-audio-sampling
*/
#define EI_CLASSIFIER_SLICES_PER_MODEL_WINDOW 3

/* Includes ---------------------------------------------------------------- */
#include <PDM.h>
#include <a2022k12111-project-1_inferencing.h>

#define RED     22
#define BLUE    24
#define GREEN   23
#define LED_PWR 25

/** Audio buffers, pointers and selectors */
typedef struct {
  signed short *buffers[2];
  unsigned char buf_select;
  unsigned char buf_ready;
  unsigned int buf_count;
  unsigned int n_samples;
} inference_t

static inference_t inference;
static bool record_ready = false;
static signed short *sample0Buffer;
static bool debug_nn = false; // Set this to true to see e.g. features generated from the raw signal
static int print_results = -(EI_CLASSIFIER_SLICES_PER_MODEL_WINDOW)

/**
  @brief      Arduino setup function
*/
void setup()
{
  pinMode(RED, OUTPUT);
  pinMode(BLUE, OUTPUT);
  pinMode(GREEN, OUTPUT);
  //pinMode(LED_PWR, OUTPUT);

  // put your setup code here, to run once:
  Serial.begin(115200);

  Serial.println("Edge Impulse Inferencing Demo");

  // summary of inferencing settings (from model_metadata.h)
  ei_printf("Inferencing settings:\n");
  ei_printf("\tInterval: %.2f ms.\n", (float)EI_CLASSIFIER_INTERVAL_MS);
  ei_printf("\tFrame size: %d\n", EI_CLASSIFIER_DSP_INPUT_FRAME_SIZE);
  ei_printf("\tSample length: %d ms.\n", EI_CLASSIFIER_RAW_SAMPLE_COUNT / 16);
  ei_printf("\tNo. of classes: %d\n", sizeof(ei_classifier_inferencing_categories) /
                  sizeof(ei_classifier_inferencing_categories[0]));

  run_classifier_init();
  if (microphone_inference_start(EI_CLASSIFIER_SLICE_SIZE) == false) {
    ei_printf("ERR: Failed to setup audio sampling\r\n");
    return;
  }
}

/**
  @brief      Arduino main function. Runs the inferencing loop.
*/
void loop()
{
  bool m = microphone_inference_record();
  if (!m) {
    ei_printf("ERR: Failed to record audio...\n");
    return;
  }

  signal_t signal;
  signal.total_length = EI_CLASSIFIER_SLICE_SIZE;
  signal.get_data = &microphone_audio_signal_get_data;
  ei_impulse_result_t result = {0};

  EI_IMPULSE_ERROR r = run_classifier_continuous(&signal, &result, debug_nn);
  if (r != EI_IMPULSE_OK) {
    ei_printf("ERR: Failed to run classifier (%d)\n", r);
    return;
  }

  if (result.classification[0].value >= 0.7) {
    digitalWrite(BLUE, LOW);
    digitalWrite(GREEN, HIGH);
    digitalWrite(RED, HIGH);
  }
  else if (result.classification[1].value >= 0.7) {
    digitalWrite(BLUE, HIGH);
    digitalWrite(GREEN, LOW);
    digitalWrite(RED, HIGH);
  }
  else if (result.classification[2].value >= 0.7) {
    digitalWrite(BLUE, HIGH);
    digitalWrite(GREEN, HIGH);
    digitalWrite(RED, HIGH);
  }
  else if (result.classification[3].value >= 0.7) {
    digitalWrite(BLUE, HIGH);
    digitalWrite(GREEN, HIGH);
    digitalWrite(RED, LOW);
  }

  if (++print_results >= (EI_CLASSIFIER_SLICES_PER_MODEL_WINDOW)) {
    // print the predictions
    ei_printf("Predictions ");
    ei_printf("(DSP: %d ms., Classification: %d ms., Anomaly: %d ms.)",
              result.timing.dsp, result.timing.classification, result.timing.anomaly);
    ei_printf(": \n");
    for (size_t ix = 0; ix < EI_CLASSIFIER_LABEL_COUNT; ix++) {
      ei_printf("    %s: %.5f\n", result.classification[ix].label,
                result.classification[ix].value);
    }
#if EI_CLASSIFIER_HAS_ANOMALY == 1
    ei_printf("    anomaly score: %.3f\n", result.anomaly);
#endif

    print_results = 0;
  }
}
```

FIGURE 5: Code first half

```
/**
 @brief      Printf function uses vsnprintf and output using Arduino Serial
 @param[in]  format     Variable argument list
*/
void ei_printf(const char *format, ...) {
  static char print_buf[1024] = { 0 };

  va_list args;
  va_start(args, format);
  int r = vsnprintf(print_buf, sizeof(print_buf), format, args);
  va_end(args);

  if (r > 0) {
    Serial.write(print_buf);
  }
}

/**
 @brief      PDM buffer full callback
             Get data and call audio thread callback
*/
static void pdm_data_ready_inference_callback(void)
{
  int bytesAvailable = PDM.available();

  // read into the sample buffer
  int bytesRead = PDM.read((char *)sampleBuffer[0], bytesAvailable);

  if (record_ready == true) {
    for (int i = 0; i<bytesRead >> 1; i++) {
      inference.buffers[inference.buf_select][inference.buf_count++] = sampleBuffer[i];

      if (inference.buf_count >= inference.n_samples) {
        inference.buf_select ^= 1;
        inference.buf_count = 0;
        inference.buf_ready = 1;
      }
    }
  }
}

/**
 @brief      Init inferencing struct and setup/start PDM
 @param[in]  n_samples  The n samples
 @return     { description_of_the_return_value }
*/
static bool microphone_inference_start(uint32_t n_samples)
{
  inference.buffers[0] = (signed short *)malloc(n_samples * sizeof(signed short));

  if (inference.buffers[0] == NULL) {
    return false;
  }

  inference.buffers[1] = (signed short *)malloc(n_samples * sizeof(signed short));

  if (inference.buffers[0] == NULL) {
    free(inference.buffers[0]);
    return false;
  }

  sampleBuffer = (signed short *)malloc((n_samples >> 1) * sizeof(signed short));

  if (sampleBuffer == NULL) {
    free(inference.buffers[0]);
    free(inference.buffers[1]);
    return false;
  }

  inference.buf_select = 0;
  inference.buf_count = 0;
  inference.n_samples = n_samples;
  inference.buf_ready = 0;

  // configure the data receive callback
  PDM.onReceive(&pdm_data_ready_inference_callback);

  PDM.setBufferSize((n_samples >> 1) * sizeof(int16_t));

  // initialize PDM with:
  // - one channel (mono mode)
  // - a 16 kHz sample rate
  if (!PDM.begin(1, EI_CLASSIFIER_FREQUENCY)) {
    ei_printf("Failed to start PDM!");
  }

  // set the gain, defaults to 20
  PDM.setGain(127);

  record_ready = true;

  return true;
}

/**
 @brief      Wait on new data
 @return     True when finished
*/
static bool microphone_inference_record(void)
{
  bool ret = true;

  if (inference.buf_ready == 1) {
    ei_printf(
      "Error sample buffer overrun. Decrease the number of slices per model window "
      "(EI_CLASSIFIER_SLICES_PER_MODEL_WINDOW)\n");
    ret = false;
  }

  while (inference.buf_ready == 0) {
    delay(1);
  }

  inference.buf_ready = 0;

  return ret;
}

/**
 Get raw audio signal data
*/
static int microphone_audio_signal_get_data(size_t offset, size_t length, float *out_ptr)
{
  numpy::int16_to_float(&inference.buffers[inference.buf_select ^ 1][offset], out_ptr, length);

  return 0;
}

/**
 @brief      Stop PDM and release buffers
*/
static void microphone_inference_end(void)
{
  PDM.end();
  free(inference.buffers[0]);
  free(inference.buffers[1]);
  free(sampleBuffer);
}

#if !defined(EI_CLASSIFIER_SENSOR) || EI_CLASSIFIER_SENSOR != EI_CLASSIFIER_SENSOR_MICROPHONE
#error "Invalid model for current sensor."
#endif
```

Figure 6: Code second half

IE417 : Embedded AI

Lab - 2 YouTube Playback Control using Gesture Code

Submitted by

Avinash Baraiya- 202201211

Malhar Vaghasiya - 202201183

Smeet Agrawal - 202101237

Priyesh Tandel - 202101222

Samarth Panchal- 202101456

Submitted to

Professor Tapas Kumar Maiti

Dhirubhai Ambani Institute of Information and Communication Technology

Gandhinagar , Gujarat

Introduction

Using an accelerometer on the Arduino Nano BLE 33 Sense, this project uses Edge Impulse for machine learning to control YouTube with gestures. Python and the PyAutoGUI module are used to simulate keyboard shortcuts so that gesture inputs can control YouTube.

Data Collection

Data was gathered using the onboard Inertial Measurement Unit (IMU) of the Arduino Nano BLE 33 Sense, which captures acceleration across three axes: X, Y, and Z. This acceleration data was sampled and subsequently processed using Edge Impulse for analysis.

Steps for Data Collection:

- **Sensor Data**: Acceleration measurements were obtained along three axes—**accX**, **accY**, and **accZ**.
- **Gestures Recorded**: Three distinct gestures were tracked: circular motion, vertical motion (up/down), and lateral motion (pan).
    - **Circle Gesture**: Represents the command to move to the next video.
    - **Up/Down Gesture**: Corresponds to the action of muting or unmuting.
    - **Pan Gesture**: Linked to the play/pause function for media control.

Figure 1 : Data Acquisition

Spectral Analysis

Figure 2 : Create Impulse

Classification

	BACKWARD	FORWARD	IDLE	PLAY-PAUSE
BACKWARD	100%	0%	0%	0%
FORWARD	71.4%	28.6%	0%	0%
IDLE	0%	0%	100%	0%
PLAY-PAUSE	0%	0%	0%	100%
F1 SCORE	0.76	0.44	1.00	1.00

Testing and Results

Once the model was trained, we tested its performance by feeding it new gesture data and verifying if it correctly classified the actions. The model's performance was satisfactory for all the gestures with minimal errors.

Code Implementation

- Reads the gesture commands from the Serial port.
- Uses the PyAutoGUI library to simulate YouTube keyboard controls:
  - "next" → right arrow key (next video)
  - "mute" → 'm' key (mute/unmute)
  - "play" → 'k' key (play/pause)

```
# if you don't have pyautogui & pyserial installed
# pip install pyserial pyautogui

# pyautogui is used for control of the mouse and keyboard, and other GUI automation
tasks
# pyserial is a python library used for working with serial ports
# time is used to create time related task in the program for delaying or early
activation of certain function

import serial
import time
import pyautogui

# Set thresholds for gesture detection or confidence threshold to make sure your
desired gesture is working
CIRCLE_THRESHOLD = 0.7
CROSS_THRESHOLD = 0.7
PAN_THRESHOLD = 0.7

def open_serial_connection():
    try:
        ser = serial.Serial('COM3', 115200) # change COM Port as per system is
showing or open arduino IDE to check which COM Port is Used
        print("Connected to the serial port")
        time.sleep(2)  # Wait for the serial connection to initialize
        return ser
    except serial.SerialException as e:
        print(f"Error connecting to serial port: {e}")
        return None

def classify_gesture(incoming):
    # Extracting gesture and confidence from the incoming data
    if 'circle' in incoming:
        confidence = float(incoming.split(':')[1].strip())
        if confidence > CIRCLE_THRESHOLD:
            print(f"Circle gesture detected with confidence {confidence}. Pressing
'm' key")
            pyautogui.press('m')
```

```
    elif 'cross' in incoming:
        confidence = float(incoming.split(':')[1].strip())
        if confidence > CROSS_THRESHOLD:
            print(f"Cross gesture detected with confidence {confidence}. Pressing
'k' key")
            pyautogui.press('k')
    elif 'pan' in incoming:
        confidence = float(incoming.split(':')[1].strip())
        if confidence > PAN_THRESHOLD:
            print(f"Pan gesture detected with confidence {confidence}. Pressing
'Shift + n' key")
            pyautogui.hotkey('shift', 'n')

def main():
    ser = open_serial_connection()
    if ser is None:
        return  # Exit if unable to connect

    try:
        while True:
            try:
                incoming = ser.readline().decode('utf-8').strip()
                print(f"Received: {incoming}")

                # Look for predictions in the incoming data
                if "Predictions" in incoming:
                    # Continue reading lines until we get the classification result
                    for _ in range(3):
                        incoming = ser.readline().decode('utf-8').strip()
                        classify_gesture(incoming)

            except serial.SerialException as e:
                print(f"Error reading from serial port: {e}")
                break
            except UnicodeDecodeError as e:
                print(f"Decoding error: {e}")
            except Exception as e:
                print(f"Unexpected error: {e}")

    finally:
        if ser is not None and ser.is_open:
            ser.close()
            print("Serial port closed.")

if __name__ == "__main__":
    main()
```

Arduino Code

```
/* Edge Impulse ingestion SDK
 * Copyright (c) 2022 EdgeImpulse Inc.
 *
 * Licensed under the Apache License, Version 2.0 (the "License");
 * you may not use this file except in compliance with the License.
 * You may obtain a copy of the License at
 * http://www.apache.org/licenses/LICENSE-2.0
 *
 * Unless required by applicable law or agreed to in writing, software
 * distributed under the License is distributed on an "AS IS" BASIS,
 * WITHOUT WARRANTIES OR CONDITIONS OF ANY KIND, either express or implied.
 * See the License for the specific language governing permissions and
 * limitations under the License.
 *
 */

/* Includes ---------------------------------------------------------------- */
#include <a202201211_Gesture_Project_inferencing.h>
#include <Arduino_LSM9DS1.h> //Click here to get the library:
https://www.arduino.cc/reference/en/libraries/arduino_lsm9ds1/

/* Constant defines -------------------------------------------------------- */
#define CONVERT_G_TO_MS2    9.80665f
#define MAX_ACCEPTED_RANGE  2.0f        // starting 03/2022, models are generated
setting range to +-2, but this example use Arudino library which set range to +-4g.
If you are using an older model, ignore this value and use 4.0f instead

/*
 ** NOTE: If you run into TFLite arena allocation issue.
 **
 ** This may be due to may dynamic memory fragmentation.
 ** Try defining "-DEI_CLASSIFIER_ALLOCATION_STATIC" in boards.local.txt (create
 ** if it doesn't exist) and copy this file to
 ** `<ARDUINO_CORE_INSTALL_PATH>/arduino/hardware/<mbed_core>/<core_version>/`.
 **
 ** See
 ** (https://support.arduino.cc/hc/en-us/articles/360012076960-Where-are-the-
installed-cores-located-)
 ** to find where Arduino installs cores on your machine.
 **
 ** If the problem persists then there's not enough memory for this model and
application.
 */

/* Private variables ------------------------------------------------------- */
```

```
static bool debug_nn = false; // Set this to true to see e.g. features generated
from the raw signal

/**
* @brief      Arduino setup function
*/
void setup()
{
    // put your setup code here, to run once:
    Serial.begin(115200);
    // comment out the below line to cancel the wait for USB connection (needed for
native USB)
    while (!Serial);
    Serial.println("Edge Impulse Inferencing Demo");

    if (!IMU.begin()) {
        ei_printf("Failed to initialize IMU!\r\n");
    }
    else {
        ei_printf("IMU initialized\r\n");
    }

    if (EI_CLASSIFIER_RAW_SAMPLES_PER_FRAME != 3) {
        ei_printf("ERR: EI_CLASSIFIER_RAW_SAMPLES_PER_FRAME should be equal to 3
(the 3 sensor axes)\n");
        return;
    }
}

/**
 * @brief Return the sign of the number
 *
 * @param number
 * @return int 1 if positive (or 0) -1 if negative
 */
float ei_get_sign(float number) {
    return (number >= 0.0) ? 1.0 : -1.0;
}

/**
* @brief      Get data and run inferencing
*
* @param[in]  debug  Get debug info if true
*/
void loop()
{
    ei_printf("\nStarting inferencing in 2 seconds...\n");
```

```
    delay(2000);

    ei_printf("Sampling...\n");

    // Allocate a buffer here for the values we'll read from the IMU
    float buffer[EI_CLASSIFIER_DSP_INPUT_FRAME_SIZE] = { 0 };

    for (size_t ix = 0; ix < EI_CLASSIFIER_DSP_INPUT_FRAME_SIZE; ix += 3) {
        // Determine the next tick (and then sleep later)
        uint64_t next_tick = micros() + (EI_CLASSIFIER_INTERVAL_MS * 1000);

        IMU.readAcceleration(buffer[ix], buffer[ix + 1], buffer[ix + 2]);

        for (int i = 0; i < 3; i++) {
            if (fabs(buffer[ix + i]) > MAX_ACCEPTED_RANGE) {
                buffer[ix + i] = ei_get_sign(buffer[ix + i]) * MAX_ACCEPTED_RANGE;
            }
        }

        buffer[ix + 0] *= CONVERT_G_TO_MS2;
        buffer[ix + 1] *= CONVERT_G_TO_MS2;
        buffer[ix + 2] *= CONVERT_G_TO_MS2;

        delayMicroseconds(next_tick - micros());
    }

    // Turn the raw buffer in a signal which we can the classify
    signal_t signal;
    int err = numpy::signal_from_buffer(buffer, EI_CLASSIFIER_DSP_INPUT_FRAME_SIZE,
&signal);
    if (err != 0) {
        ei_printf("Failed to create signal from buffer (%d)\n", err);
        return;
    }

    // Run the classifier
    ei_impulse_result_t result = { 0 };

    err = run_classifier(&signal, &result, debug_nn);
    if (err != EI_IMPULSE_OK) {
        ei_printf("ERR: Failed to run classifier (%d)\n", err);
        return;
    }

    // print the predictions
    ei_printf("Predictions ");
    ei_printf("(DSP: %d ms., Classification: %d ms., Anomaly: %d ms.)",
        result.timing.dsp, result.timing.classification, result.timing.anomaly);
```

```
    ei_printf(": \n");
    for (size_t ix = 0; ix < EI_CLASSIFIER_LABEL_COUNT; ix++) {
        ei_printf("    %s: %.5f\n", result.classification[ix].label,
result.classification[ix].value);
    }
#if EI_CLASSIFIER_HAS_ANOMALY == 1
    ei_printf("    anomaly score: %.3f\n", result.anomaly);
#endif
}

#if !defined(EI_CLASSIFIER_SENSOR) || EI_CLASSIFIER_SENSOR !=
EI_CLASSIFIER_SENSOR_ACCELEROMETER
#error "Invalid model for current sensor"
#endif
```

Practical Working Video Link

https://youtu.be/ExCY1Zeibpg?si=sdKgYLfXkwahvYO1

IE 417

Embedded AI

Lab: 03: Indoor Classification with Object Detection

Group Name: Friendly Group

Avinash Baraiya- 202201211

Malhar Vaghasiya - 202201183

Smeet Agrawal - 202101237

Priyesh Tandel - 202101222

Samarth Panchal- 202101456

Guided By Prof. Tapas Kumar Maiti

- ## Introduction

This project uses the OV7670 camera module and Arduino Nano 33 BLE Sense to classify indoor scenes, like kitchens and bathrooms, on a microcontroller. By capturing images and applying transfer learning with TensorFlow Lite for Microcontrollers, we'll deploy a compact model for recognizing indoor environments on limited hardware. This lab demonstrates how to bring basic computer vision to small devices.

- ## Data Collection

Indoor Classification with Object Detection

In this project, we use the Arduino Nano 33 BLE Sense and OV7670 camera module for indoor scene classification, focusing on detecting specific objects like a box, an Android device, and a mouse. Using TensorFlow Lite for Microcontrollers (TFLu), we apply transfer learning to classify these objects in indoor environments, enabling microcontrollers to perform basic object detection in real-world settings.

Steps for Data Collection:

- **Sensor Data**: Images were captured with the OV7670 camera module.
- **Objects Detected**: Three objects were identified for classification—box, Android device, and mouse.
    - **Box**: Identified to signal the presence of storage items.
    - **Android Device**: Detected to differentiate personal devices in a scene.
    - **Mouse**: Used to recognize workspace items, aiding in workspace classification.

This project highlights how to capture and classify indoor scenes using limited resources on microcontrollers.

- ## Impulse Creation

Learning Block: Transfer Learning(images)

Input Features: Image

Output Features: Android | Box | Mouse

- ## Classification and Testing Results

1. Mouse Sample Taken by Arduino and it correctly Predicted with value **0.87** that it is **<u>Mouse</u>**

2. Mobile Sample Taken by Arduino and it correctly Predicted with value **0.84** that is **<u>Android</u>**

3. Box Sample Taken by Arduino and it correctly Predicted with value **0.92** that is **<u>Box</u>**

4. Random Sample Taken by Arduino and it correctly Predicted **<u>Uncertain.</u>**

Android – 0.40 | Box – 0.29 | Mouse – 0.31

Testing Data:

Test data

Classify all

Set the 'expected outcome' for each sample to the desired outcome to automatically score the impulse.

SAMPLE NAME	EXPECTED OUTCOME	ACCURACY	RESULT
box.5aouulg2	box	100%	1 box
box.5aouujnr	box	100%	1 box
box.5aouug5j	box	100%	1 box
box.5aouub7c	box	100%	1 box
box.5aouuacs	box	100%	1 box
mouse.5aoutkvh	mouse	100%	1 mouse
mouse.5aoutisg	mouse	100%	1 mouse
mouse.5aoutgdr	mouse	100%	1 mouse
mouse.5aoutei4	mouse	100%	1 mouse
mouse.5aoutdkv	mouse	100%	1 mouse

Model testing output

Results

Model version: Unoptimized (float32)

ACCURACY
91.27%

Metrics for Transfer learning

METRIC	VALUE
Area under ROC Curve	1.00
Weighted average Precision	1.00
Weighted average Recall	1.00
Weighted average F1 score	1.00

Confusion matrix

	ANDROID	BOX	MOUSE	UNCERTAIN
ANDROID	100%	0%	0%	0%
BOX	0%	93%	7%	0%
MOUSE	0%	12%	88%	0%
F1 SCORE	1.00	1.00	1.00	

Confusion matrix

	ANDROID	BOX	MOUSE	UNCERTAIN
ANDROID	100%	0%	0%	0%
BOX	0%	93%	7%	0%
MOUSE	0%	12%	88%	0%
F1 SCORE	1.00	1.00	1.00	

Feature explorer

- **Code Implementation**
  https://drive.google.com/drive/folders/1WiqxxtDulSYp1AO4rWOd3ulTBMM56kAC?usp=sharing

- **Practical Video Link**

  Part 1: https://youtu.be/fFQpoj-ub_g

  Part 2: https://www.youtube.com/shorts/BTtuHPeYFQE

IE417 : Embedded AI

Lab - 4 - MISO SIMO MIMO SISO

Submitted by

Avinash Baraiya- 202201211

Malhar Vaghasiya - 202201183

Smeet Agrawal - 202101237

Priyesh Tandel - 202101222

Samarth Panchal- 202101456

Submitted to

Professor Tapas Kumar Maiti

Dhirubhai Ambani Institute of Information and Communication Technology

Gandhinagar , Gujarat

Open in Colab

Task : 1 - Single Input, Single Output (SISO)

Avinash Baraiya- 202201211

Malhar Vaghasiya - 202201183

Smeet Agrawal - 202101237

Priyesh Tandel - 202101222

Samarth Panchal- 202101456

OpenLane Colab

This Google Colab notebook will:

- Install OpenLane and its dependencies
- Run a simple design, namely a serial-parallel multiplier, through the flow and targeting the open source sky130 PDK by Google and Skywater.

Setup Nix

Nix is a package manager with an emphasis on reproducible builds, and it is the primary method for installing OpenLane 2.

This step installs the Nix package manager and enables the experimental "flakes" feature.

If you're not in a Colab, this just sets the environment variables. You will need to install Nix and enable flakes on your own following this guide.

Show code

```
---- sudo execution ------------------------------------------------------------
I am executing:

    $ sudo HOME=/root /nix/store/fsh9vmf1rfnaxv48n20nalfdavzji5sf-nix-2.25.2/bin/nix-env -i /nix/store/fsh9vmf1rfnaxv48n20nalfdavzji5sf-nix-2.25.2

to install a bootstrapping Nix in to the default profile

installing 'nix-2.25.2'
building '/nix/store/v28xaq08scl7s734iq4lbxg2l8v55z8r-user-environment.drv'...

---- sudo execution ------------------------------------------------------------
I am executing:

    $ sudo HOME=/root /nix/store/fsh9vmf1rfnaxv48n20nalfdavzji5sf-nix-2.25.2/bin/nix-env -i /nix/store/852a51xd3m7jyzifqimxc3jf3w2ipc4k-nss-cacert-3.101

to install a bootstrapping SSL certificate just for Nix in to the default profile

installing 'nss-cacert-3.101'
building '/nix/store/pw8bfl9ck7hiw1ax01pk1l1y2b6bawxn-user-environment.drv'...

---- sudo execution ------------------------------------------------------------
I am executing:

    $ sudo HOME=/root NIX_SSL_CERT_FILE=/nix/var/nix/profiles/default/etc/ssl/certs/ca-bundle.crt /nix/store/fsh9vmf1rfnaxv48n20nalfdavzji5sf-nix-2.25.2/bin/nix-channel --update nixpkgs

to update the default channel in the default profile

unpacking 1 channels...

---- sudo execution ------------------------------------------------------------
I am executing:

    $ sudo install -m 0664 /tmp/tmp.lqdqjwEBLm/nix.conf /etc/nix/nix.conf

to place the default nix daemon configuration (part 2)

Alright! We're done!
Try it! Open a new terminal, and type:
  $ sudo nix-daemon
  $ nix-shell -p nix-info --run "nix-info -m"

Thank you for using this installer. If you have any feedback or need
help, don't hesitate:

You can open an issue at
https://github.com/NixOS/nix/issues/new?labels=installer&template=installer.md

Or get in touch with the community: https://nixos.org/community

---- Reminders -----------------------------------------------------------------
[ 1 ]
Nix won't work in active shell sessions until you restart them.

[ 2 ]
I don't support your init system yet; you may want to add nix-daemon manually.

nix-daemon: no process found
```

Get OpenLane

Click the ▷ button to download and install OpenLane.

This will install OpenLane's tool dependencies using Nix, and OpenLane itself using PIP.

Note that `python3-tk` may need to be installed using your OS's package manager.

openlane_version: "version-2.1"

pdk_root: "~/.volare"

pdk: "sky130"

Show code

Downloading OpenLane…

```
  % Total    % Received % Xferd  Average Speed   Time    Time     Time  Current
                                 Dload  Upload   Total   Spent    Left  Speed
  0     0    0     0    0     0      0      0 --:--:-- --:--:-- --:--:--     0
100 9491k    0 9491k    0     0  8636k      0 --:--:--  0:00:01 --:--:-- 17.5M
```

Downloading OpenLane's dependencies…

Downloading Python dependencies using PIP…

Downloading PDK…

```
Version bdc9412b3e468c102d01b7cf6337be06ec6e9c9a not found locally, attempting to download…
Downloading common.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━  98% 0:00:01
Downloading sky130_fd_io.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━  90% 0:00:01
Downloading sky130_fd_pr.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━  52% 0:00:01
Downloading sky130_fd_sc_hd.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━  94% 0:00:01
Downloading sky130_fd_sc_hvl.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━  79% 0:00:01
Downloading sky130_ml_xx_hd.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━   0% -:--:--
Downloading sky130_sram_macros.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━  89% 0:00:01
Version bdc9412b3e468c102d01b7cf6337be06ec6e9c9a enabled for the sky130 PDK.
```

Done.

```
import openlane

print(openlane.__version__)
```

```
2.1.11
```

Creating the design

Now that OpenLane is set up, we can write a Verilog file as follows:

```
%%writefile SISO.v


module SISO(
    input [31:0] x,            // Single input
    output [63:0] y            // Single output
);

    reg [3:0] weight;
    wire [63:0] bias = 1;
    wire [63:0] neuron_output;
    wire [63:0] relu_output;

    initial begin
        weight = 4'b0101;
    end

    neuron n1 (
        .out_neuron(neuron_output),
        .input_neuron(x),
        .weight_value(weight)
    );

    ReLU r1 (
        .in(neuron_output),
        .out(relu_output)
    );

    assign y = relu_output;

endmodule

module neuron(
    output reg [63:0] out_neuron,
    input [31:0] input_neuron,
    input [3:0] weight_value
);

    wire [63:0] bias = 1;

    reg [63:0] out_mul;

    always @(*) begin
        out_mul = weight_value * input_neuron;
        out_neuron = out_mul + bias;
    end

endmodule

module ReLU(
    input signed [31:0] in,
    output reg [63:0] out
);

    always @(*) begin
        if (in < 0) begin
            out = 0;
        end else begin
            out = in;
        end
    end

endmodule
```

```
Writing SISO.v
```

Setting up the configuration

OpenLane requries you to configure any Flow before using it. This is done using the `config` module.

For colaboratories, REPLs and other interactive environments where there is no concrete Flow object, the Configuration may be initialized using `Config.interactive`, which will automatically propagate the configuration to any future steps.

You can find the documentation for `Config.interactive` here.

```
from openlane.config import Config

Config.interactive(
    "SISO",
    PDK="sky130A",
    CLOCK_PORT="clk",
    CLOCK_NET="clk",
    CLOCK_PERIOD=10,
    PRIMARY_GDSII_STREAMOUT_TOOL="klayout",
)
```

Interactive Configuration

Initial Values

```
CELL_BB_VERILOG_MODELS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/sky130_fd_sc_hd__blackbox.v
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/sky130_fd_sc_hd__blackbox_pp.v
CELL_GDS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/gds/sky130_fd_sc_hd.gds
CELL_LEFS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef
CELL_PAD_EXCLUDE:
- sky130_fd_sc_hd__tap*
- sky130_fd_sc_hd__decap*
- sky130_ef_sc_hd__decap*
- sky130_fd_sc_hd__fill*
CELL_SPICE_MODELS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__decap_12.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_12.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_4.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_8.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_fd_sc_hd.spice
CELL_VERILOG_MODELS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/primitives.v
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/sky130_fd_sc_hd.v
CLOCK_NET: clk
CLOCK_PERIOD: 10
CLOCK_PORT: clk
CLOCK_TRANSITION_CONSTRAINT: 0.15
CLOCK_UNCERTAINTY_CONSTRAINT: 0.25
CLOCK_WIRE_RC_LAYERS: null
DECAP_CELL:
- sky130_ef_sc_hd__decap_12
- sky130_fd_sc_hd__decap_8
- sky130_fd_sc_hd__decap_6
- sky130_fd_sc_hd__decap_4
- sky130_fd_sc_hd__decap_3
DEFAULT_CORNER: nom_tt_025C_1v80
DEFAULT_MAX_TRAN: null
DESIGN_DIR: .
DESIGN_NAME: SISO
DIE_AREA: null
DIODE_CELL: sky130_fd_sc_hd__diode_2/DIODE
ENDCAP_CELL: sky130_fd_sc_hd__decap_3
EXTRA_EXCLUDED_CELLS: null
EXTRA_GDS_FILES: null
EXTRA_LEFS: null
EXTRA_LIBS: null
EXTRA_SPICE_MODELS: null
EXTRA_VERILOG_MODELS: null
FALLBACK_SDC_FILE: /content/openlane_ipynb/openlane/scripts/base.sdc
FILL_CELL:
- sky130_fd_sc_hd__fill*
FP_IO_HLAYER: met3
FP_IO_VLAYER: met2
FP_TAPCELL_DIST: 13
FP_TRACKS_INFO: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tracks.info
GND_NETS: null
GND_PIN: VGND
GPIO_PADS_LEF:
- /root/.volare/sky130A/libs.ref/sky130_fd_io/lef/sky130_fd_io.lef
- /root/.volare/sky130A/libs.ref/sky130_fd_io/lef/sky130_ef_io.lef
GPIO_PADS_LEF_CORE_SIDE:
- /root/.volare/sky130A/libs.tech/openlane/custom_cells/lef/sky130_fd_io_core.lef
- /root/.volare/sky130A/libs.tech/openlane/custom_cells/lef/sky130_ef_io_core.lef
GPIO_PADS_VERILOG:
- /root/.volare/sky130A/libs.ref/sky130_fd_io/verilog/sky130_ef_io.v
GPIO_PAD_CELLS:
- sky130_fd_io*
- sky130_ef_io*
IO_DELAY_CONSTRAINT: 20
LIB:
  '*_ff_n40C_1v95':
  - /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ff_n40C_1v95.lib
  '*_ss_100C_1v60':
  - /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ss_100C_1v60.lib
  '*_tt_025C_1v80':
  - /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
MACROS: null
MAX_CAPACITANCE_CONSTRAINT: 0.2
MAX_FANOUT_CONSTRAINT: 10
MAX_TRANSITION_CONSTRAINT: 0.75
OUTPUT_CAP_LOAD: 33.442
PDK: sky130A
PDK_ROOT: /root/.volare
PLACE_SITE: unithd
PNR_EXCLUDED_CELL_FILE: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/drc_exclude.cells
PRIMARY_GDSII_STREAMOUT_TOOL: klayout
RT_MAX_LAYER: met5
RT_MIN_LAYER: met1
SCL_GROUND_PINS:
- VGND
- VNB
SCL_POWER_PINS:
- VPWR
- VPB
SIGNAL_WIRE_RC_LAYERS: null
STA_CORNERS:
- nom_tt_025C_1v80
- nom_ss_100C_1v60
- nom_ff_n40C_1v95
- min_tt_025C_1v80
- min_ss_100C_1v60
- min_ff_n40C_1v95
- max_tt_025C_1v80
- max_ss_100C_1v60
- max_ff_n40C_1v95
STD_CELL_LIBRARY: sky130_fd_sc_hd
SYNTH_BUFFER_CELL: sky130_fd_sc_hd__buf_2/A/X
SYNTH_CLK_DRIVING_CELL: null
SYNTH_DRIVING_CELL: sky130_fd_sc_hd__inv_2/Y
SYNTH_EXCLUDED_CELL_FILE: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/no_synth.cells
SYNTH_TIEHI_CELL: sky130_fd_sc_hd__conb_1/HI
SYNTH_TIELO_CELL: sky130_fd_sc_hd__conb_1/LO
TECH_LEFS:
  max_*: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__max.tlef
  min_*: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__min.tlef
  nom_*: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef
TIME_DERATING_CONSTRAINT: 5
TRISTATE_CELLS:
- sky130_fd_sc_hd__ebuf*
VDD_NETS: null
```

```
  VDD_PIN: VPWR
  VDD_PIN_VOLTAGE: 1.8
  WELLTAP_CELL: sky130_fd_sc_hd__tapvpwrvgnd_1
  WIRE_LENGTH_THRESHOLD: null
  meta:
    flow: null
    openlane_version: 2.1.11
    step: null
    substituting_steps: null
    version: 1
```

Running implementation steps

There are two ways to obtain OpenLane's built-in implementation steps:

- via directly importing from the `steps` module using its category:
  - `from openlane.steps import Yosys` then `Synthesis = Yosys.Synthesis`
- by using the step's id from the registry:
  - `from openlane.steps import Step` then `Synthesis = Step.factory.get("Yosys.Synthesis")`

You can find a full list of included steps here: https://openlane2.readthedocs.io/en/latest/reference/step_config_vars.html

```
from openlane.steps import Step
```

- First, get the step (and display its help)...

```
Synthesis = Step.factory.get("Yosys.Synthesis")

Synthesis.display_help()
```

(step-yosys-synthesis)=

Synthesis

```
Performs synthesis and technology mapping on Verilog RTL files
using Yosys and ABC, emitting a netlist.

Some metrics will also be extracted and updated, namely:

* ``design__instance__count``
* ``design__instance_unmapped__count``
* ``design__instance__area``
```

Importing

```
from openlane.steps.yosys import Synthesis

# or

from openlane.steps import Step

Synthesis = Step.factory.get("Yosys.Synthesis")
```

Inputs and Outputs

Inputs	Outputs
	Verilog Netlist (.nl.v)

(yosys.synthesis-configuration-variables)=

Configuration Variables

Variable Name	Type	Description	Default	Units
SYNTH_LATCH_MAP{#var-yosys-synthesis-synth_latch_map}^{PDK}	Path?	A path to a file containing the latch mapping for Yosys.	None	
SYNTH_TRISTATE_MAP{#var-yosys-synthesis-synth_tristate_map}^{PDK}	Path?	A path to a file containing the tri-state buffer mapping for Yosys.	None	
SYNTH_CSA_MAP{#var-yosys-synthesis-synth_csa_map}^{PDK}	Path?	A path to a file containing the carry-select adder mapping for Yosys.	None	
SYNTH_RCA_MAP{#var-yosys-synthesis-synth_rca_map}^{PDK}	Path?	A path to a file containing the ripple-carry adder mapping for Yosys.	None	
SYNTH_FA_MAP{#var-yosys-synthesis-synth_fa_map}^{PDK}	Path?	A path to a file containing the full adder mapping for Yosys.	None	
SYNTH_MUX_MAP{#var-yosys-synthesis-synth_mux_map}^{PDK}	Path?	A path to a file containing the mux mapping for Yosys.	None	
SYNTH_MUX4_MAP{#var-yosys-synthesis-synth_mux4_map}^{PDK}	Path?	A path to a file containing the mux4 mapping for Yosys.	None	
USE_LIGHTER{#var-yosys-synthesis-use_lighter}	bool	Activates Lighter, an experimental plugin that attempts to optimize clock-gated flip-flops.	False	
LIGHTER_DFF_MAP{#var-yosys-synthesis-lighter_dff_map}	Path?	An override to the custom DFF map file provided for the given SCL by Lighter.	None	
YOSYS_LOG_LEVEL{#var-yosys-synthesis-yosys_log_level}	'ALL' | 'WARNING' | 'ERROR'	Which log level for Yosys. At WARNING or higher, the initialization splash is also disabled.	ALL	
SYNTH_CHECKS_ALLOW_TRISTATE{#var-yosys-synthesis-synth_checks_allow_tristate}	bool	Ignore multiple-driver warnings if they are connected to tri-state buffers on a best-effort basis.	True	
SYNTH_AUTONAME{#var-yosys-synthesis-synth_autoname}	bool	Generates names for netlist instances. This results in instance names that can be extremely long, but are more human-readable.	False	
SYNTH_STRATEGY{#var-yosys-synthesis-synth_strategy}	'AREA 0' | 'AREA 1' | 'AREA 2' | 'AREA 3' | 'DELAY 0' | 'DELAY 1' | 'DELAY 2' | 'DELAY 3' | 'DELAY 4'	Strategies for abc logic synthesis and technology mapping. AREA strategies usually result in a more compact design, while DELAY strategies usually result in a design that runs at a higher frequency. Please note that there is no way to know which strategy is the best before trying them.	AREA 0	
SYNTH_ABC_BUFFERING{#var-yosys-synthesis-synth_abc_buffering}	bool	Enables `abc` cell buffering.	False	
SYNTH_ABC_LEGACY_REFACTOR{#var-yosys-synthesis-synth_abc_legacy_refactor}	bool	Replaces the ABC command `drf -l` with `refactor` which matches older versions of OpenLane but is more unstable.	False	
SYNTH_ABC_LEGACY_REWRITE{#var-yosys-synthesis-synth_abc_legacy_rewrite}	bool	Replaces the ABC command `drw -l` with `rewrite` which matches older versions of OpenLane but is more unstable.	False	
SYNTH_DIRECT_WIRE_BUFFERING{#var-yosys-synthesis-synth_direct_wire_buffering}	bool	Enables inserting buffer cells for directly connected wires.	True	
SYNTH_SPLITNETS{#var-yosys-synthesis-synth_splitnets}	bool	Splits multi-bit nets into single-bit nets. Easier to trace but may not be supported by all tools.	True	
SYNTH_SIZING{#var-yosys-synthesis-synth_sizing}	bool	Enables `abc` cell sizing (instead of buffering).	False	
SYNTH_NO_FLAT{#var-yosys-synthesis-synth_no_flat}	bool	A flag that disables flattening the hierarchy during synthesis, only flattening it after synthesis, mapping and optimizations.	False	
SYNTH_SHARE_RESOURCES{#var-yosys-synthesis-synth_share_resources}	bool	A flag that enables yosys to reduce the number of cells by determining shareable resources and merging them.	True	
SYNTH_ADDER_TYPE{#var-yosys-synthesis-synth_adder_type}	'YOSYS' | 'FA' | 'RCA' | 'CSA'	Adder type to which the $addand$sub operators are mapped to. Possible values are `YOSYS/FA/RCA/CSA`; where `YOSYS` refers to using Yosys internal adder definition, `FA` refers to full-adder structure, `RCA` refers to ripple carry adder structure, and `CSA` refers to carry select adder.	YOSYS	
SYNTH_EXTRA_MAPPING_FILE{#var-yosys-synthesis-synth_extra_mapping_file}	Path?	Points to an extra techmap file for yosys that runs right after yosys `synth` before generic techmap.	None	
SYNTH_PARAMETERS{#var-yosys-synthesis-synth_parameters}	List[str]?	Key-value pairs to be `chparam`ed in Yosys, in the format `key1=value1`.	None	
SYNTH_ELABORATE_ONLY{#var-yosys-synthesis-synth_elaborate_only}	bool	"Elaborate" the design only without attempting any logic mapping. Useful when dealing with structural Verilog netlists.	False	
SYNTH_ELABORATE_FLATTEN{#var-yosys-synthesis-synth_elaborate_flatten}	bool	If `SYNTH_ELABORATE_ONLY` is specified, this variable controls whether or not the top level should be flattened.	True	
VERILOG_FILES{#var-yosys-synthesis-verilog_files}	List[Path]	The paths of the design's Verilog files.	None	
VERILOG_DEFINES{#var-yosys-synthesis-verilog_defines}	List[str]?	Preprocessor defines for input Verilog files.	None	

VERILOG_POWER_DEFINE{#var-yosys-synthesis-verilog_power_define}	str	Specifies the name of the define used to guard power and ground connections in the input RTL.	USE_POWER_PINS
VERILOG_INCLUDE_DIRS{#var-yosys-synthesis-verilog_include_dirs}	List[str]?	Specifies the Verilog `include` directories.	None
USE_SYNLIG{#var-yosys-synthesis-use_synlig}	bool	Use the Synlig plugin to process files, which has better SystemVerilog parsing capabilities but may not be compatible with all Yosys commands and attributes.	False
SYNLIG_DEFER{#var-yosys-synthesis-synlig_defer}	bool	Uses -defer flag when reading files the Synlig plugin, which may improve performance by reading each file separately, but is experimental.	False

- Then run it. Note you can pass step-specific configs using Python keyword arguments.

Synthesis

We need to start by converting our high-level Verilog to one that just shows the connections between small silicon patterns called "standard cells" in process called Synthesis. We can do this by passing the Verilog files as a configuration variable to `Yosys.Synthesis` as follows, then running it.

As this is the first step, we need to create an empty state and pass it to it.

```
from openlane.state import State

synthesis = Synthesis(
    VERILOG_FILES=["./SISO.v"],
    state_in=State(),
)
synthesis.start()
```

```
──────────────────────────────────────────────────────── Synthesis ────────────────────────────────────────────────────────
[14:46:34] VERBOSE  Running 'Yosys.Synthesis'…                                                          step.py:1088
[14:46:34] VERBOSE  Logging subprocess to openlane_run/1-yosys-synthesis/yosys-synthesis.log…           step.py:1268

/-------------------------------------------------------------------------\
|                                                                         |
|  yosys -- Yosys Open SYnthesis Suite                                    |
|                                                                         |
|  Copyright (C) 2012 - 2020  Claire Xenia Wolf <claire@yosyshq.com>      |
|                                                                         |
|  Permission to use, copy, modify, and/or distribute this software for any |
|  purpose with or without fee is hereby granted, provided that the above |
|  copyright notice and this permission notice appear in all copies.      |
|                                                                         |
|  THE SOFTWARE IS PROVIDED "AS IS" AND THE AUTHOR DISCLAIMS ALL WARRANTIES |
|  WITH REGARD TO THIS SOFTWARE INCLUDING ALL IMPLIED WARRANTIES OF       |
|  MERCHANTABILITY AND FITNESS. IN NO EVENT SHALL THE AUTHOR BE LIABLE FOR |
|  ANY SPECIAL, DIRECT, INDIRECT, OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES |
|  WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN  |
|  ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF |
|  OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.         |
|                                                                         |
\-------------------------------------------------------------------------/

Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)

Loaded SDC plugin
[TCL: yosys -import] Command name collision: found pre-existing command `cd' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `eval' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `exec' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `read' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `trace' -> skip.

1. Executing Liberty frontend: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
Imported 428 cell types from liberty file.

2. Executing Verilog-2005 frontend: ./SISO.v
Parsing SystemVerilog input from `./SISO.v' to AST representation.
Generating RTLIL representation for module `\SISO'.
Generating RTLIL representation for module `\neuron'.
Generating RTLIL representation for module `\ReLU'.
Successfully finished Verilog frontend.

3. Executing HIERARCHY pass (managing design hierarchy).

3.1. Analyzing design hierarchy..
Top module:  \SISO
Used module:     \ReLU
Used module:     \neuron

3.2. Analyzing design hierarchy..
Top module:  \SISO
Used module:     \ReLU
Used module:     \neuron
Removed 0 unused modules.
Warning: Resizing cell port SISO.r1.in from 64 bits to 32 bits.
Renaming module SISO to SISO.

4. Generating Graphviz representation of design.
Writing dot description to `/content/openlane_run/1-yosys-synthesis/hierarchy.dot'.
Dumping module SISO to page 1.

5. Executing TRIBUF pass.

6. Executing HIERARCHY pass (managing design hierarchy).

6.1. Analyzing design hierarchy..
Top module:  \SISO
Used module:     \ReLU
Used module:     \neuron

6.2. Analyzing design hierarchy..
Top module:  \SISO
Used module:     \ReLU
Used module:     \neuron
Removed 0 unused modules.

7. Executing PROC_CLEAN pass (remove empty switches from decision trees).
Cleaned up 0 empty switches.

8. Executing PROC_RMDEAD pass (remove dead branches from decision trees).
Marked 1 switch rules as full_case in process $proc$./SISO.v:54$5 in module ReLU.
Removed a total of 0 dead cases.

9. Executing PROC_PRUNE pass (remove redundant assignments in processes).
Removed 0 redundant assignments.
Promoted 4 assignments to connections.

10. Executing PROC_INIT pass (extract init attributes).

11. Executing PROC_ARST pass (detect async resets in processes).

12. Executing PROC_ROM pass (convert switches to ROMs).
Converted 0 switches.
<suppressed ~1 debug messages>

13. Executing PROC_MUX pass (convert decision trees to multiplexers).
Creating decoders for process `\SISO.$proc$./SISO.v:0$1'.
Creating decoders for process `\neuron.$proc$./SISO.v:42$2'.
Creating decoders for process `\ReLU.$proc$./SISO.v:54$5'.
1/1: $1\out[63:0]

14. Executing PROC_DLATCH pass (convert process syncs to latches).
No latch inferred for signal `\SISO.\weight' from process `\SISO.$proc$./SISO.v:0$1'.
No latch inferred for signal `\neuron.\out_neuron' from process `\neuron.$proc$./SISO.v:42$2'.
No latch inferred for signal `\neuron.\out_mul' from process `\neuron.$proc$./SISO.v:42$2'.
No latch inferred for signal `\ReLU.\out' from process `\ReLU.$proc$./SISO.v:54$5'.

15. Executing PROC_DFF pass (convert process syncs to FFs).

16. Executing PROC_MEMWR pass (convert process memory writes to cells).

17. Executing PROC_CLEAN pass (remove empty switches from decision trees).
Removing empty process `SISO.$proc$./SISO.v:0$1'.
Removing empty process `neuron.$proc$./SISO.v:42$2'.
Found and cleaned up 1 empty switch in `\ReLU.$proc$./SISO.v:54$5'.
Removing empty process `ReLU.$proc$./SISO.v:54$5'.
Cleaned up 1 empty switch.

18. Executing CHECK pass (checking for obvious problems).
Checking module SISO...
Checking module neuron...
Checking module ReLU...
Found and reported 0 problems.

19. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.
```

```
Optimizing module neuron.
Optimizing module ReLU.

20. Executing FLATTEN pass (flatten design).
Deleting now unused module neuron.
Deleting now unused module ReLU.
<suppressed ~2 debug messages>

21. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

22. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..
Removed 0 unused cells and 9 unused wires.
<suppressed ~1 debug messages>

23. Executing OPT pass (performing simple optimizations).

23.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

23.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

23.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~1 debug messages>

23.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Performed a total of 0 changes.

23.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

23.6. Executing OPT_DFF pass (perform DFF optimizations).

23.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

23.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

23.9. Finished OPT passes. (There is nothing left to do.)

24. Executing FSM pass (extract and optimize FSM).

24.1. Executing FSM_DETECT pass (finding FSMs in design).

24.2. Executing FSM_EXTRACT pass (extracting FSM from design).

24.3. Executing FSM_OPT pass (simple optimizations of FSMs).

24.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

24.5. Executing FSM_OPT pass (simple optimizations of FSMs).

24.6. Executing FSM_RECODE pass (re-assigning FSM state encoding).

24.7. Executing FSM_INFO pass (dumping all available information on FSM cells).

24.8. Executing FSM_MAP pass (mapping FSMs to basic logic).

25. Executing OPT pass (performing simple optimizations).

25.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

25.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

25.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~1 debug messages>

25.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Performed a total of 0 changes.

25.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

25.6. Executing OPT_DFF pass (perform DFF optimizations).

25.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

25.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

25.9. Finished OPT passes. (There is nothing left to do.)

26. Executing WREDUCE pass (reducing word size of cells).
Removed top 63 bits (of 64) from port B of cell SISO.$flatten\n1.$add$./SISO.v:44$4 ($add).
Removed top 32 bits (of 64) from port Y of cell SISO.$flatten\n1.$add$./SISO.v:44$4 ($add).
Removed top 32 bits (of 64) from port A of cell SISO.$flatten\n1.$add$./SISO.v:44$4 ($add).
Removed top 1 bits (of 4) from port A of cell SISO.$flatten\n1.$mul$./SISO.v:43$3 ($mul).
Removed top 32 bits (of 64) from port Y of cell SISO.$flatten\n1.$mul$./SISO.v:43$3 ($mul).
Removed top 31 bits (of 32) from port B of cell SISO.$flatten\r1.$lt$./SISO.v:55$6 ($lt).

27. Executing PEEPOPT pass (run peephole optimizers).

28. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

29. Executing ALUMACC pass (create $alu and $macc cells).
Extracting $alu and $macc cells in module SISO:
creating $macc model for $flatten\n1.$add$./SISO.v:44$4 ($add).
creating $macc model for $flatten\n1.$mul$./SISO.v:43$3 ($mul).
merging $macc model for $flatten\n1.$mul$./SISO.v:43$3 into $flatten\n1.$add$./SISO.v:44$4.
creating $macc cell for $flatten\n1.$add$./SISO.v:44$4: $auto$alumacc.cc:365:replace_macc$10
creating $alu model for $flatten\r1.$lt$./SISO.v:55$6 ($lt): new $alu
creating $alu cell for $flatten\r1.$lt$./SISO.v:55$6: $auto$alumacc.cc:485:replace_alu$12
created 1 $alu and 1 $macc cells.
```

```
30. Executing SHARE pass (SAT-based resource sharing).

31. Executing OPT pass (performing simple optimizations).

31.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.
<suppressed ~1 debug messages>

31.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

31.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~1 debug messages>

31.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Performed a total of 0 changes.

31.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

31.6. Executing OPT_DFF pass (perform DFF optimizations).

31.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..
Removed 2 unused cells and 3 unused wires.
<suppressed ~4 debug messages>

31.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

31.9. Rerunning OPT passes. (Maybe there is more to do..)

31.10. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~1 debug messages>

31.11. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Performed a total of 0 changes.

31.12. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

31.13. Executing OPT_DFF pass (perform DFF optimizations).

31.14. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

31.15. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

31.16. Finished OPT passes. (There is nothing left to do.)

32. Executing MEMORY pass.

32.1. Executing OPT_MEM pass (optimize memories).
Performed a total of 0 transformations.

32.2. Executing OPT_MEM_PRIORITY pass (removing unnecessary memory write priority relations).
Performed a total of 0 transformations.

32.3. Executing OPT_MEM_FEEDBACK pass (finding memory read-to-write feedback paths).

32.4. Executing MEMORY_BMUX2ROM pass (converting muxes to ROMs).

32.5. Executing MEMORY_DFF pass (merging $dff cells to $memrd).

32.6. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

32.7. Executing MEMORY_SHARE pass (consolidating $memrd/$memwr cells).

32.8. Executing OPT_MEM_WIDEN pass (optimize memories where all ports are wide).
Performed a total of 0 transformations.

32.9. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

32.10. Executing MEMORY_COLLECT pass (generating $mem cells).

33. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

34. Executing OPT pass (performing simple optimizations).

34.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.
<suppressed ~6 debug messages>

34.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

34.3. Executing OPT_DFF pass (perform DFF optimizations).

34.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

34.5. Finished fast OPT passes.

35. Executing MEMORY_MAP pass (converting memories to logic and flip-flops).

36. Executing OPT pass (performing simple optimizations).

36.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

36.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

36.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
```

```
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~1 debug messages>

36.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Consolidated identical input bits for $mux cell $flatten\r1.$procmux$8:
Old ports: A=64'0000000000000000000000000000000000000000000000000000000000000000, B={ \r1.in [31] \r1.in [31]
\r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in
[31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31]
\r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in
[31] \r1.in [31] \r1.in }, Y=\y
New ports: A=0, B=\r1.in, Y=\y [31:0]
New connections: \y [63:32] = { \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y
[31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y
[31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] }
Optimizing cells in module \SISO.
Performed a total of 1 changes.

36.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

36.6. Executing OPT_SHARE pass.

36.7. Executing OPT_DFF pass (perform DFF optimizations).

36.8. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

36.9. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

36.10. Rerunning OPT passes. (Maybe there is more to do..)

36.11. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~1 debug messages>

36.12. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Performed a total of 0 changes.

36.13. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

36.14. Executing OPT_SHARE pass.

36.15. Executing OPT_DFF pass (perform DFF optimizations).

36.16. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

36.17. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

36.18. Finished OPT passes. (There is nothing left to do.)

37. Executing TECHMAP pass (map to technology primitives).

37.1. Executing Verilog-2005 frontend:
/nix/store/sx2v0i73mn1ih2z1nk61pm9n5gjgpidy-yosys/bin/../share/yosys/techmap.v
Parsing Verilog input from `/nix/store/sx2v0i73mn1ih2z1nk61pm9n5gjgpidy-yosys/bin/../share/yosys/techmap.v' to AST
representation.
Generating RTLIL representation for module `\_90_simplemap_bool_ops'.
Generating RTLIL representation for module `\_90_simplemap_reduce_ops'.
Generating RTLIL representation for module `\_90_simplemap_logic_ops'.
Generating RTLIL representation for module `\_90_simplemap_compare_ops'.
Generating RTLIL representation for module `\_90_simplemap_various'.
Generating RTLIL representation for module `\_90_simplemap_registers'.
Generating RTLIL representation for module `\_90_shift_ops_shr_shl_sshl_sshr'.
Generating RTLIL representation for module `\_90_shift_shiftx'.
Generating RTLIL representation for module `\_90_fa'.
Generating RTLIL representation for module `\_90_lcu'.
Generating RTLIL representation for module `\_90_alu'.
Generating RTLIL representation for module `\_90_macc'.
Generating RTLIL representation for module `\_90_alumacc'.
Generating RTLIL representation for module `\$__div_mod_u'.
Generating RTLIL representation for module `\$__div_mod_trunc'.
Generating RTLIL representation for module `\_90_div'.
Generating RTLIL representation for module `\_90_mod'.
Generating RTLIL representation for module `\$__div_mod_floor'.
Generating RTLIL representation for module `\_90_divfloor'.
Generating RTLIL representation for module `\_90_modfloor'.
Generating RTLIL representation for module `\_90_pow'.
Generating RTLIL representation for module `\_90_pmux'.
Generating RTLIL representation for module `\_90_demux'.
Generating RTLIL representation for module `\_90_lut'.
Successfully finished Verilog frontend.

37.2. Continuing TECHMAP pass.
Using extmapper simplemap for cells of type $reduce_and.
Using extmapper simplemap for cells of type $xor.
Using extmapper simplemap for cells of type $or.
Using template $paramod$7b00947614a4c48e09c066dca449366ddfa907a5\_90_alu for cells of type $alu.
Using extmapper maccmap for cells of type $macc.
add \x * 3'101 (32x3 bits, unsigned)
add 1 (32 bits, unsigned)
packed 1 (1) bits / 1 words into adder tree
Using extmapper simplemap for cells of type $mux.
Using extmapper simplemap for cells of type $and.
Using template $paramod\_90_lcu\WIDTH=32'00000000000000000000000000100000 for cells of type $lcu.
Using extmapper simplemap for cells of type $pos.
Using extmapper simplemap for cells of type $not.
Using template $paramod\_90_fa\WIDTH=32'00000000000000000000000000100000 for cells of type $fa.
Using template $paramod$fbc7873bff55778c0b3173955b7e4bce1d9d6834\_90_alu for cells of type $alu.
No more expansions possible.
<suppressed ~576 debug messages>

38. Executing OPT pass (performing simple optimizations).

38.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.
<suppressed ~430 debug messages>

38.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
<suppressed ~96 debug messages>
Removed a total of 32 cells.

38.3. Executing OPT_DFF pass (perform DFF optimizations).
```

```
38.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..
Removed 97 unused cells and 199 unused wires.
<suppressed ~98 debug messages>

38.5. Finished fast OPT passes.

39. Executing ABC pass (technology mapping using ABC).

39.1. Extracting gate netlist of module `\SISO' to `<abc-temp-dir>/input.blif'..
Extracted 372 gates and 405 wires to a netlist network with 32 inputs and 32 outputs.

39.1.1. Executing ABC.
Running ABC command: "/nix/store/wq2q0njg3sx8wvj2akz7x1qxwyrv9xlr-yosys-abc/bin/abc" -s -f
<abc-temp-dir>/abc.script 2>&1
ABC: ABC command line: "source <abc-temp-dir>/abc.script".
ABC:
ABC: + read_blif <abc-temp-dir>/input.blif
ABC: + read_library <abc-temp-dir>/stdcells.genlib
ABC: Entered genlib library with 13 gates from file "<abc-temp-dir>/stdcells.genlib".
ABC: + strash
ABC: + dretime
ABC: + map
ABC: + write_blif <abc-temp-dir>/output.blif

39.1.2. Re-integrating ABC results.
ABC RESULTS:               AND cells:       30
ABC RESULTS:              XNOR cells:       23
ABC RESULTS:             ORNOT cells:       28
ABC RESULTS:              NAND cells:       13
ABC RESULTS:                OR cells:       28
ABC RESULTS:               NOR cells:       33
ABC RESULTS:               XOR cells:       67
ABC RESULTS:            ANDNOT cells:      111
ABC RESULTS:        internal signals:      341
ABC RESULTS:           input signals:       32
ABC RESULTS:          output signals:       32
Removing temp directory.

40. Executing OPT pass (performing simple optimizations).

40.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

40.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
<suppressed ~3 debug messages>
Removed a total of 1 cells.

40.3. Executing OPT_DFF pass (perform DFF optimizations).

40.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..
Removed 0 unused cells and 172 unused wires.
<suppressed ~1 debug messages>

40.5. Finished fast OPT passes.

41. Executing HIERARCHY pass (managing design hierarchy).

41.1. Analyzing design hierarchy..
Top module:  \SISO

41.2. Analyzing design hierarchy..
Top module:  \SISO
Removed 0 unused modules.

42. Printing statistics.

=== SISO ===

Number of wires:                 312
Number of wire bits:             852
Number of public wires:           12
Number of public wire bits:      552
Number of memories:                0
Number of memory bits:             0
Number of processes:               0
Number of cells:                 332
$_ANDNOT_                      111
$_AND_                          30
$_NAND_                         12
$_NOR_                          33
$_ORNOT_                        28
$_OR_                           28
$_XNOR_                         23
$_XOR_                          67

43. Executing CHECK pass (checking for obvious problems).
Checking module SISO...
Found and reported 0 problems.

44. Generating Graphviz representation of design.
Writing dot description to `/content/openlane_run/1-yosys-synthesis/primitive_techmap.dot'.
Dumping module SISO to page 1.

45. Executing OPT pass (performing simple optimizations).

45.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

45.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

45.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
No muxes found in this module.
Removed 0 multiplexer ports.

45.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Performed a total of 0 changes.

45.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

45.6. Executing OPT_DFF pass (perform DFF optimizations).

45.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

45.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

45.9. Finished OPT passes. (There is nothing left to do.)
```

```
46. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..
Removed 0 unused cells and 10 unused wires.
<suppressed ~10 debug messages>
{
"creator": "Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)",
"invocation": "stat -json -liberty /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib ",
"modules": {
"\\SISO": {
"num_wires":         302,
"num_wire_bits":     396,
"num_pub_wires":     2,
"num_pub_wire_bits": 96,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         332,
"num_cells_by_type": {
"$_ANDNOT_": 111,
"$_AND_": 30,
"$_NAND_": 12,
"$_NOR_": 33,
"$_ORNOT_": 28,
"$_OR_": 28,
"$_XNOR_": 23,
"$_XOR_": 67
}
}
},
"design": {
"num_wires":         302,
"num_wire_bits":     396,
"num_pub_wires":     2,
"num_pub_wire_bits": 96,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         332,
"num_cells_by_type": {
"$_ANDNOT_": 111,
"$_AND_": 30,
"$_NAND_": 12,
"$_NOR_": 33,
"$_ORNOT_": 28,
"$_OR_": 28,
"$_XNOR_": 23,
"$_XOR_": 67
}
}
}

47. Printing statistics.

=== SISO ===

   Number of wires:                302
   Number of wire bits:            396
   Number of public wires:           2
   Number of public wire bits:      96
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                332
     $_ANDNOT_                     111
     $_AND_                         30
     $_NAND_                        12
     $_NOR_                         33
     $_ORNOT_                       28
     $_OR_                          28
     $_XNOR_                        23
     $_XOR_                         67

   Area for cell type $_AND_ is unknown!
   Area for cell type $_NAND_ is unknown!
   Area for cell type $_OR_ is unknown!
   Area for cell type $_NOR_ is unknown!
   Area for cell type $_XOR_ is unknown!
   Area for cell type $_XNOR_ is unknown!
   Area for cell type $_ANDNOT_ is unknown!
   Area for cell type $_ORNOT_ is unknown!

mapping tbuf
[INFO] Applying tri-state buffer mapping from
'/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tribuff_map.v'...

48. Executing TECHMAP pass (map to technology primitives).

48.1. Executing Verilog-2005 frontend: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tribuff_map.v
Parsing Verilog input from `/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tribuff_map.v' to AST
representation.
Generating RTLIL representation for module `\$_TBUF_'.
Successfully finished Verilog frontend.

48.2. Continuing TECHMAP pass.
No more expansions possible.
<suppressed ~3 debug messages>

49. Executing SIMPLEMAP pass (map simple cells to gate primitives).
[INFO] Applying latch mapping from '/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/latch_map.v'...

50. Executing TECHMAP pass (map to technology primitives).

50.1. Executing Verilog-2005 frontend: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/latch_map.v
Parsing Verilog input from `/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/latch_map.v' to AST
representation.
Generating RTLIL representation for module `\$_DLATCH_P_'.
Generating RTLIL representation for module `\$_DLATCH_N_'.
Successfully finished Verilog frontend.

50.2. Continuing TECHMAP pass.
No more expansions possible.
<suppressed ~4 debug messages>

51. Executing SIMPLEMAP pass (map simple cells to gate primitives).

52. Executing DFFLIBMAP pass (mapping DFF cells to sequential cells from liberty file).
cell sky130_fd_sc_hd__dfxtp_2 (noninv, pins=3, area=21.27) is a direct match for cell type $_DFF_P_.
cell sky130_fd_sc_hd__dfrtp_2 (noninv, pins=4, area=26.28) is a direct match for cell type $_DFF_PN0_.
cell sky130_fd_sc_hd__dfstp_2 (noninv, pins=4, area=26.28) is a direct match for cell type $_DFF_PN1_.
cell sky130_fd_sc_hd__dfbbn_2 (noninv, pins=6, area=35.03) is a direct match for cell type $_DFFSR_NNN_.
final dff cell mappings:
unmapped dff cell: $_DFF_N_
\sky130_fd_sc_hd__dfxtp_2 _DFF_P_ (.CLK( C), .D( D), .Q( Q));
unmapped dff cell: $_DFF_NN0_
unmapped dff cell: $_DFF_NN1_
unmapped dff cell: $_DFF_NP0_
unmapped dff cell: $_DFF_NP1_
```

```
unmapped dff cell: $_DFF_NP1_
\sky130_fd_sc_hd__dfrtp_2 _DFF_PN0_ (.CLK( C), .D( D), .Q( Q), .RESET_B( R));
\sky130_fd_sc_hd__dfstp_2 _DFF_PN1_ (.CLK( C), .D( D), .Q( Q), .SET_B( R));
unmapped dff cell: $_DFF_PP0_
unmapped dff cell: $_DFF_PP1_
\sky130_fd_sc_hd__dfbbn_2 _DFFSR_NNN_ (.CLK_N( C), .D( D), .Q( Q), .Q_N(~Q), .RESET_B( R), .SET_B( S));
unmapped dff cell: $_DFFSR_NNP_
unmapped dff cell: $_DFFSR_NPN_
unmapped dff cell: $_DFFSR_NPP_
unmapped dff cell: $_DFFSR_PNN_
unmapped dff cell: $_DFFSR_PNP_
unmapped dff cell: $_DFFSR_PPN_
unmapped dff cell: $_DFFSR_PPP_

52.1. Executing DFFLEGALIZE pass (convert FFs to types supported by the target).
Mapping DFF cells in module `\SISO':
{
"creator": "Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)",
"invocation": "stat -json -liberty /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib ",
"modules": {
"\\SISO": {
"num_wires":         302,
"num_wire_bits":     396,
"num_pub_wires":     2,
"num_pub_wire_bits": 96,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         332,
"num_cells_by_type": {
"$_ANDNOT_": 111,
"$_AND_": 30,
"$_NAND_": 12,
"$_NOR_": 33,
"$_ORNOT_": 28,
"$_OR_": 28,
"$_XNOR_": 23,
"$_XOR_": 67
}
}
},
"design": {
"num_wires":         302,
"num_wire_bits":     396,
"num_pub_wires":     2,
"num_pub_wire_bits": 96,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         332,
"num_cells_by_type": {
"$_ANDNOT_": 111,
"$_AND_": 30,
"$_NAND_": 12,
"$_NOR_": 33,
"$_ORNOT_": 28,
"$_OR_": 28,
"$_XNOR_": 23,
"$_XOR_": 67
}
}
}

53. Printing statistics.

=== SISO ===

   Number of wires:                302
   Number of wire bits:            396
   Number of public wires:           2
   Number of public wire bits:      96
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                332
     $_ANDNOT_                     111
     $_AND_                         30
     $_NAND_                        12
     $_NOR_                         33
     $_ORNOT_                       28
     $_OR_                          28
     $_XNOR_                        23
     $_XOR_                         67

   Area for cell type $_AND_ is unknown!
   Area for cell type $_NAND_ is unknown!
   Area for cell type $_OR_ is unknown!
   Area for cell type $_NOR_ is unknown!
   Area for cell type $_XOR_ is unknown!
   Area for cell type $_XNOR_ is unknown!
   Area for cell type $_ANDNOT_ is unknown!
   Area for cell type $_ORNOT_ is unknown!

[INFO] Using strategy "AREA 0"...

54. Executing ABC pass (technology mapping using ABC).

54.1. Extracting gate netlist of module `\SISO' to `/tmp/yosys-abc-TE4VR1/input.blif'..
Extracted 332 gates and 364 wires to a netlist network with 32 inputs and 32 outputs.

54.1.1. Executing ABC.
Running ABC command: "/nix/store/wq2q0njg3sx8wvj2akz7x1qxwyrv9xlr-yosys-abc/bin/abc" -s -f
/tmp/yosys-abc-TE4VR1/abc.script 2>&1
ABC: ABC command line: "source /tmp/yosys-abc-TE4VR1/abc.script".
ABC:
ABC: + read_blif /tmp/yosys-abc-TE4VR1/input.blif
ABC: + read_lib -w /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib
ABC: Parsing finished successfully.  Parsing time =     0.44 sec
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfbbn_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfrbp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfrtp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfrtp_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfsbp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfstp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfstp_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfxbp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfxtp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfxtp_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtn_1".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtn_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtn_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtp_1".
ABC: Scl_LibertyReadGenlib() skipped three-state cell "sky130_fd_sc_hd__ebufn_2".
ABC: Scl_LibertyReadGenlib() skipped three-state cell "sky130_fd_sc_hd__ebufn_4".
ABC: Scl_LibertyReadGenlib() skipped three-state cell "sky130_fd_sc_hd__ebufn_8".
ABC: Library "sky130_fd_sc_hd__tt_025C_1v80" from "/content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib"
has 175 cells (17 skipped: 14 seq; 3 tri-state; 0 no func; 0 dont_use).  Time =     0.77 sec
ABC: Memory =    9.54 MB. Time =     0.77 sec
```

```
ABC: Warning: Detected 2 multi-output gates (for example, "sky130_fd_sc_hd__fa_1").
ABC: + read_constr -v /content/openlane_run/1-yosys-synthesis/synthesis.sdc
ABC: Setting driving cell to be "sky130_fd_sc_hd__inv_2/Y".
ABC: Setting output load to be 33.442001.
ABC: + read_constr /content/openlane_run/1-yosys-synthesis/synthesis.sdc
ABC: + fx
ABC: + mfs
ABC: + strash
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + retime -D -D 10000 -M 5
ABC: + scleanup
ABC: Error: The network is combinational.
ABC: + fraig_store
ABC: + balance
ABC: + fraig_store
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + fraig_store
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + fraig_store
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + fraig_store
ABC: + fraig_restore
ABC: + amap -m -Q 0.1 -F 20 -A 20 -C 5000
ABC: + retime -D -D 10000
ABC: + &get -n
ABC: + &st
ABC: + &dch
ABC: + &nf
ABC: + &put
ABC: +
ABC: + stime -p
ABC: Cannot find the default PI driving cell (sky130_fd_sc_hd__inv_2/Y) in the library.
ABC: WireLoad = "none"  Gates =    261 (  2.7 %)   Cap = 11.8 ff (  0.9 %)   Area =     2501.15 ( 95.8 %)   Delay =
3615.36 ps  (  7.3 %)
ABC: Path  0 --      10 : 0    6 pi                        A =   0.00  Df =   0.0   -0.0 ps  S =   0.0 ps  Cin =
0.0 ff  Cout =  22.6 ff  Cmax =   0.0 ff  G =    0
ABC: Path  1 --     151 : 2    2 sky130_fd_sc_hd__or2_2    A =   6.26  Df = 285.7 -193.4 ps  S =  64.1 ps  Cin =
1.5 ff  Cout =   6.2 ff  Cmax = 299.4 ff  G =  400
ABC: Path  2 --     152 : 4    4 sky130_fd_sc_hd__and4_2   A =  10.01  Df = 551.9 -193.5 ps  S = 103.0 ps  Cin =
1.5 ff  Cout =  13.4 ff  Cmax = 300.3 ff  G =  830
ABC: Path  3 --     154 : 2    4 sky130_fd_sc_hd__or2_2    A =   6.26  Df = 872.8 -316.4 ps  S =  73.1 ps  Cin =
1.5 ff  Cout =   9.6 ff  Cmax = 299.4 ff  G =  626
ABC: Path  4 --     163 : 3    2 sky130_fd_sc_hd__or3_2    A =   7.51  Df =1328.2 -661.0 ps  S =  80.7 ps  Cin =
1.5 ff  Cout =   4.1 ff  Cmax = 310.4 ff  G =  257
ABC: Path  5 --     175 : 2    2 sky130_fd_sc_hd__or2_2    A =   6.26  Df =1638.0 -620.3 ps  S =  61.4 ps  Cin =
1.5 ff  Cout =   5.1 ff  Cmax = 299.4 ff  G =  330
ABC: Path  6 --     184 : 5    2 sky130_fd_sc_hd__a2111o_2 A =  12.51  Df =2054.4 -563.0 ps  S =  75.3 ps  Cin =
2.4 ff  Cout =   7.0 ff  Cmax = 324.1 ff  G =  281
ABC: Path  7 --     213 : 3    2 sky130_fd_sc_hd__a21o_2   A =   8.76  Df =2261.1 -644.7 ps  S =  49.8 ps  Cin =
2.4 ff  Cout =   7.0 ff  Cmax = 309.5 ff  G =  288
ABC: Path  8 --     227 : 3    2 sky130_fd_sc_hd__a21o_2   A =   8.76  Df =2452.4 -715.4 ps  S =  45.5 ps  Cin =
2.4 ff  Cout =   6.1 ff  Cmax = 309.5 ff  G =  249
ABC: Path  9 --     229 : 4    5 sky130_fd_sc_hd__a31oi_2  A =  12.51  Df =2736.5 -868.0 ps  S = 299.3 ps  Cin =
4.4 ff  Cout =  18.2 ff  Cmax = 118.1 ff  G =  390
ABC: Path 10 --     232 : 3    4 sky130_fd_sc_hd__nor3_2   A =  10.01  Df =2865.8 -652.5 ps  S = 351.4 ps  Cin =
4.4 ff  Cout =  18.5 ff  Cmax =  92.5 ff  G =  400
ABC: Path 11 --     315 : 4    1 sky130_fd_sc_hd__nor4b_2  A =  15.01  Df =3615.4 -534.4 ps  S = 822.2 ps  Cin =
3.7 ff  Cout =  33.4 ff  Cmax =  65.0 ff  G =  915
ABC: Start-point = pi9 (\x [22]).  End-point = po26 (\y [26]).
ABC: + print_stats -m
ABC: netlist                       : i/o =   32/   32  lat =    0  nd =   261  edge =    673  area =2501.79  delay
=11.00  lev = 11
ABC: + write_blif /tmp/yosys-abc-TE4VR1/output.blif

54.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__a32o_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a221o_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__and4bb_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__or4b_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a22oi_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a2111o_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o2bb2a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o32a_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__nand4_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a22o_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__nand3_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__inv_2 cells:        7
ABC RESULTS:   sky130_fd_sc_hd__or4_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o31a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o221a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a31oi_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__or3_2 cells:        6
ABC RESULTS:   sky130_fd_sc_hd__and3b_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o2111a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__and4b_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__nor2_2 cells:        6
ABC RESULTS:   sky130_fd_sc_hd__and2_2 cells:        12
ABC RESULTS:   sky130_fd_sc_hd__a31o_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__o21ai_2 cells:        5
ABC RESULTS:   sky130_fd_sc_hd__a21bo_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__nand2b_2 cells:        3
```

```
ABC RESULTS:   sky130_fd_sc_hd__and2b_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__o21bai_2 cells:        4
ABC RESULTS:   sky130_fd_sc_hd__a211o_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__or2_2 cells:       21
ABC RESULTS:   sky130_fd_sc_hd__nand2_2 cells:       43
ABC RESULTS:   sky130_fd_sc_hd__a21boi_2 cells:        4
ABC RESULTS:   sky130_fd_sc_hd__nor3_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__o21a_2 cells:        5
ABC RESULTS:   sky130_fd_sc_hd__o22a_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__xnor2_2 cells:       31
ABC RESULTS:   sky130_fd_sc_hd__or3b_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__nor4b_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a21oi_2 cells:        7
ABC RESULTS:   sky130_fd_sc_hd__o211a_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__a21o_2 cells:        9
ABC RESULTS:   sky130_fd_sc_hd__xor2_2 cells:       20
ABC RESULTS:   sky130_fd_sc_hd__and3_2 cells:       28
ABC RESULTS:   sky130_fd_sc_hd__and4_2 cells:        6
ABC RESULTS:   sky130_fd_sc_hd__nor4_2 cells:        3
ABC RESULTS:          _const0_ cells:        1
ABC RESULTS:        internal signals:      300
ABC RESULTS:           input signals:       32
ABC RESULTS:          output signals:       32
Removing temp directory.

55. Executing SETUNDEF pass (replace undef values with defined constants).

56. Executing HILOMAP pass (mapping to constant drivers).

57. Executing SPLITNETS pass (splitting up multi-bit signals).

58. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..
Removed 0 unused cells and 365 unused wires.
<suppressed ~1 debug messages>

59. Executing INSBUF pass (insert buffer cells for connected wires).
Add SISO/$auto$insbuf.cc:97:execute$1842: \y [63] -> \y [31]
Add SISO/$auto$insbuf.cc:97:execute$1843: \y [63] -> \y [32]
Add SISO/$auto$insbuf.cc:97:execute$1844: \y [63] -> \y [33]
Add SISO/$auto$insbuf.cc:97:execute$1845: \y [63] -> \y [34]
Add SISO/$auto$insbuf.cc:97:execute$1846: \y [63] -> \y [35]
Add SISO/$auto$insbuf.cc:97:execute$1847: \y [63] -> \y [36]
Add SISO/$auto$insbuf.cc:97:execute$1848: \y [63] -> \y [37]
Add SISO/$auto$insbuf.cc:97:execute$1849: \y [63] -> \y [38]
Add SISO/$auto$insbuf.cc:97:execute$1850: \y [63] -> \y [39]
Add SISO/$auto$insbuf.cc:97:execute$1851: \y [63] -> \y [40]
Add SISO/$auto$insbuf.cc:97:execute$1852: \y [63] -> \y [41]
Add SISO/$auto$insbuf.cc:97:execute$1853: \y [63] -> \y [42]
Add SISO/$auto$insbuf.cc:97:execute$1854: \y [63] -> \y [43]
Add SISO/$auto$insbuf.cc:97:execute$1855: \y [63] -> \y [44]
Add SISO/$auto$insbuf.cc:97:execute$1856: \y [63] -> \y [45]
Add SISO/$auto$insbuf.cc:97:execute$1857: \y [63] -> \y [46]
Add SISO/$auto$insbuf.cc:97:execute$1858: \y [63] -> \y [47]
Add SISO/$auto$insbuf.cc:97:execute$1859: \y [63] -> \y [48]
Add SISO/$auto$insbuf.cc:97:execute$1860: \y [63] -> \y [49]
Add SISO/$auto$insbuf.cc:97:execute$1861: \y [63] -> \y [50]
Add SISO/$auto$insbuf.cc:97:execute$1862: \y [63] -> \y [51]
Add SISO/$auto$insbuf.cc:97:execute$1863: \y [63] -> \y [52]
Add SISO/$auto$insbuf.cc:97:execute$1864: \y [63] -> \y [53]
Add SISO/$auto$insbuf.cc:97:execute$1865: \y [63] -> \y [54]
Add SISO/$auto$insbuf.cc:97:execute$1866: \y [63] -> \y [55]
Add SISO/$auto$insbuf.cc:97:execute$1867: \y [63] -> \y [56]
Add SISO/$auto$insbuf.cc:97:execute$1868: \y [63] -> \y [57]
Add SISO/$auto$insbuf.cc:97:execute$1869: \y [63] -> \y [58]
Add SISO/$auto$insbuf.cc:97:execute$1870: \y [63] -> \y [59]
Add SISO/$auto$insbuf.cc:97:execute$1871: \y [63] -> \y [60]
Add SISO/$auto$insbuf.cc:97:execute$1872: \y [63] -> \y [61]
Add SISO/$auto$insbuf.cc:97:execute$1873: \y [63] -> \y [62]

60. Executing CHECK pass (checking for obvious problems).
Checking module SISO...
Found and reported 0 problems.
{
"creator": "Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)",
"invocation": "stat -json -liberty /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib ",
"modules": {
"\\SISO": {
"num_wires":         231,
"num_wire_bits":     325,
"num_pub_wires":     2,
"num_pub_wire_bits": 96,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         293,
"area":              2665.056000,
"num_cells_by_type": {
"sky130_fd_sc_hd__a2111o_2": 1,
"sky130_fd_sc_hd__a211o_2": 1,
"sky130_fd_sc_hd__a21bo_2": 2,
"sky130_fd_sc_hd__a21boi_2": 4,
"sky130_fd_sc_hd__a21o_2": 9,
"sky130_fd_sc_hd__a21oi_2": 7,
"sky130_fd_sc_hd__a221o_2": 1,
"sky130_fd_sc_hd__a22o_2": 1,
"sky130_fd_sc_hd__a22oi_2": 1,
"sky130_fd_sc_hd__a31o_2": 3,
"sky130_fd_sc_hd__a31oi_2": 1,
"sky130_fd_sc_hd__a32o_2": 1,
"sky130_fd_sc_hd__and2_2": 12,
"sky130_fd_sc_hd__and2b_2": 3,
"sky130_fd_sc_hd__and3_2": 28,
"sky130_fd_sc_hd__and3b_2": 1,
"sky130_fd_sc_hd__and4_2": 6,
"sky130_fd_sc_hd__and4b_2": 2,
"sky130_fd_sc_hd__and4bb_2": 1,
"sky130_fd_sc_hd__buf_2": 32,
"sky130_fd_sc_hd__conb_1": 1,
"sky130_fd_sc_hd__inv_2": 7,
"sky130_fd_sc_hd__nand2_2": 43,
"sky130_fd_sc_hd__nand2b_2": 3,
"sky130_fd_sc_hd__nand3_2": 1,
"sky130_fd_sc_hd__nand4_2": 1,
"sky130_fd_sc_hd__nor2_2": 6,
"sky130_fd_sc_hd__nor3_2": 2,
"sky130_fd_sc_hd__nor4_2": 3,
"sky130_fd_sc_hd__nor4b_2": 1,
"sky130_fd_sc_hd__o2111a_2": 1,
"sky130_fd_sc_hd__o211a_2": 3,
"sky130_fd_sc_hd__o21a_2": 5,
"sky130_fd_sc_hd__o21ai_2": 5,
"sky130_fd_sc_hd__o21bai_2": 4,
"sky130_fd_sc_hd__o221a_2": 1,
"sky130_fd_sc_hd__o22a_2": 2,
"sky130_fd_sc_hd__o2bb2a_2": 1,
"sky130_fd_sc_hd__o31a_2": 1,
```

```
"sky130_fd_sc_hd__o32a_2": 3,
"sky130_fd_sc_hd__or2_2": 21,
"sky130_fd_sc_hd__or3_2": 6,
"sky130_fd_sc_hd__or3b_2": 2,
"sky130_fd_sc_hd__or4_2": 1,
"sky130_fd_sc_hd__or4b_2": 1,
"sky130_fd_sc_hd__xnor2_2": 31,
"sky130_fd_sc_hd__xor2_2": 20
}
}
},
"design": {
"num_wires":         231,
"num_wire_bits":     325,
"num_pub_wires":     2,
"num_pub_wire_bits": 96,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         293,
"area":              2665.056000,
"num_cells_by_type": {
"sky130_fd_sc_hd__a2111o_2": 1,
"sky130_fd_sc_hd__a211o_2": 1,
"sky130_fd_sc_hd__a21bo_2": 2,
"sky130_fd_sc_hd__a21boi_2": 4,
"sky130_fd_sc_hd__a21o_2": 9,
"sky130_fd_sc_hd__a21oi_2": 7,
"sky130_fd_sc_hd__a221o_2": 1,
"sky130_fd_sc_hd__a22o_2": 1,
"sky130_fd_sc_hd__a22oi_2": 1,
"sky130_fd_sc_hd__a31o_2": 3,
"sky130_fd_sc_hd__a31oi_2": 1,
"sky130_fd_sc_hd__a32o_2": 1,
"sky130_fd_sc_hd__and2_2": 12,
"sky130_fd_sc_hd__and2b_2": 3,
"sky130_fd_sc_hd__and3_2": 28,
"sky130_fd_sc_hd__and3b_2": 1,
"sky130_fd_sc_hd__and4_2": 6,
"sky130_fd_sc_hd__and4b_2": 2,
"sky130_fd_sc_hd__and4bb_2": 1,
"sky130_fd_sc_hd__buf_2": 32,
"sky130_fd_sc_hd__conb_1": 1,
"sky130_fd_sc_hd__inv_2": 7,
"sky130_fd_sc_hd__nand2_2": 43,
"sky130_fd_sc_hd__nand2b_2": 3,
"sky130_fd_sc_hd__nand3_2": 1,
"sky130_fd_sc_hd__nand4_2": 1,
"sky130_fd_sc_hd__nor2_2": 6,
"sky130_fd_sc_hd__nor3_2": 2,
"sky130_fd_sc_hd__nor4_2": 3,
"sky130_fd_sc_hd__nor4b_2": 1,
"sky130_fd_sc_hd__o2111a_2": 1,
"sky130_fd_sc_hd__o211a_2": 3,
"sky130_fd_sc_hd__o21a_2": 5,
"sky130_fd_sc_hd__o21ai_2": 5,
"sky130_fd_sc_hd__o21bai_2": 4,
"sky130_fd_sc_hd__o221a_2": 1,
"sky130_fd_sc_hd__o22a_2": 2,
"sky130_fd_sc_hd__o2bb2a_2": 1,
"sky130_fd_sc_hd__o31a_2": 1,
"sky130_fd_sc_hd__o32a_2": 3,
"sky130_fd_sc_hd__or2_2": 21,
"sky130_fd_sc_hd__or3_2": 6,
"sky130_fd_sc_hd__or3b_2": 2,
"sky130_fd_sc_hd__or4_2": 1,
"sky130_fd_sc_hd__or4b_2": 1,
"sky130_fd_sc_hd__xnor2_2": 31,
"sky130_fd_sc_hd__xor2_2": 20
}
}
}
```

```
display(synthesis)
```

Time Elapsed: 15.89s

Views updated:

- Verilog Netlist

Floorplanning

Floorplanning does two things:

- Determines the dimensions of the final chip.
- Creates the "cell placement grid" which placed cells must be aligned to.
  - Each cell in the grid is called a "site." Cells can occupy multiple sites, with the overwhelming majority of cells occupying multiple sites by width, and some standard cell libraries supporting varying heights as well.

> Don't forget- you may call `display_help()` on any Step class to get a full list of configuration variables.

```
Floorplan = Step.factory.get("OpenROAD.Floorplan")

floorplan = Floorplan(state_in=synthesis.state_out)
floorplan.start()
```

```
─────────────────────────────────────── Floorplan Initialization ───────────────────────────────────────
[14:46:50] VERBOSE  Running 'OpenROAD.Floorplan'…                                          step.py:1088
[14:46:50] VERBOSE  Logging subprocess to openlane_run/2-openroad-floorplan/openroad-floorplan.log…  step.py:1268
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading technology LEF file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef'…
[INFO ODB-0227] LEF file: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef, created
13 layers, 25 vias
Reading cell LEF file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef'…
The NOWIREEXTENSIONATPIN statement will be ignored. See file
/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef at line 2.

[INFO ODB-0227] LEF file: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef, created 4 library
cells
Reading cell LEF file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef'…
The NOWIREEXTENSIONATPIN statement will be ignored. See file
/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef at line 2.

[INFO ODB-0227] LEF file: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef, created 437
library cells
Reading top-level netlist at '/content/openlane_run/1-yosys-synthesis/SISO.nl.v'…
Linking design 'SISO' from netlist…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:46:54] WARNING  [STA-0366] port 'clk' not found.                                        openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:46:54] WARNING  [STA-0366] port 'clk' not found.                                        openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:46:54] WARNING  [STA-0419] transition time can not be specified for virtual clocks.      openroad.py:235
[INFO] Setting timing derate to: 5%
[14:46:54] WARNING  [STA-0450] virtual clock clk can not be propagated.                     openroad.py:235
Using site height: 2.72 and site width: 0.46…
[INFO] Using relative sizing for the floorplan.
[INFO IFP-0001] Added 26 rows of 158 site unithd.
[INFO IFP-0030] Inserted 0 tiecells using sky130_fd_sc_hd__conb_1/LO.
[INFO IFP-0030] Inserted 0 tiecells using sky130_fd_sc_hd__conb_1/HI.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 84.045 94.765 (µm).
[INFO] Floorplanned on a core area of 5.52 10.88 78.2 81.6 (µm).
Writing metric design__die__bbox: 0.0 0.0 84.045 94.765
Writing metric design__core__bbox: 5.52 10.88 78.2 81.6
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/2-openroad-floorplan/SISO.odb'…
Writing netlist to '/content/openlane_run/2-openroad-floorplan/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/2-openroad-floorplan/SISO.pnl.v'…
Writing layout to '/content/openlane_run/2-openroad-floorplan/SISO.def'…
Writing timing constraints to '/content/openlane_run/2-openroad-floorplan/SISO.sdc'…
```

Format	Path
nl	openlane_run/2-openroad-floorplan/SISO.nl.v
pnl	openlane_run/2-openroad-floorplan/SISO.pnl.v
def	openlane_run/2-openroad-floorplan/SISO.def

```
display(floorplan)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[14:46:54] VERBOSE  Running 'KLayout.Render'…                                                  step.py:1088
[14:46:54] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_1yic76_q/klayout-render.log…  step.py:1268
```

Time Elapsed: 4.43s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Tap/Endcap Cell Insertion

This places two kinds of cells on the floorplan:

- End cap/boundary cells: Added at the beginning and end of each row. True to their name, they "cap off" the core area of a design.
- Tap cells: Placed in a polka dot-ish fashion across the rows. Tap cells connect VDD to the nwell and the psubstrate to VSS, which the majority of cells do not do themselves to save area- but if you go long enough without one such connection you end up with the cell "latching-up"; i.e.; refusing to switch back to LO from HI.

  There is a maximum distance between tap cells enforced as part of every foundry process.

```
TapEndcapInsertion = Step.factory.get("OpenROAD.TapEndcapInsertion")

tdi = TapEndcapInsertion(state_in=floorplan.state_out)
tdi.start()
```

```
──────────────────────────────────────────────────────────── Tap/Decap Insertion ────────────────────────────────────────────────────────────
[14:46:55] VERBOSE  Running 'OpenROAD.TapEndcapInsertion'…                                                                    step.py:1088
[14:46:55] VERBOSE  Logging subprocess to                                                                                      step.py:1268
                    openlane_run/3-openroad-tapendcapinsertion/openroad-tapendcapinsertion.log…
Reading OpenROAD database at '/content/openlane_run/2-openroad-floorplan/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:46:56] WARNING  [STA-0366] port 'clk' not found.                                                                          openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:46:56] WARNING  [STA-0366] port 'clk' not found.                                                                          openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:46:56] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                        openroad.py:235
[INFO] Setting timing derate to: 5%
[14:46:57] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                       openroad.py:235
[INFO TAP-0004] Inserted 52 endcaps.
[INFO TAP-0005] Inserted 70 tapcells.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/3-openroad-tapendcapinsertion/SISO.odb'…
Writing netlist to '/content/openlane_run/3-openroad-tapendcapinsertion/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/3-openroad-tapendcapinsertion/SISO.pnl.v'…
Writing layout to '/content/openlane_run/3-openroad-tapendcapinsertion/SISO.def'…
Writing timing constraints to '/content/openlane_run/3-openroad-tapendcapinsertion/SISO.sdc'…
```

Format	Path
nl	openlane_run/3-openroad-tapendcapinsertion/SISO.nl.v
pnl	openlane_run/3-openroad-tapendcapinsertion/SISO.pnl.v
def	openlane_run/3-openroad-tapendcapinsertion/SISO.def
odb	openlane_run/3-openroad-tapendcapinsertion/SISO.odb

```
display(tdi)
```

```
──────────────────────────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────────────────────
[14:46:57] VERBOSE  Running 'KLayout.Render'…                                                                                  step.py:1088
[14:46:57] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_3ex61j4t/klayout-render.log…                            step.py:1268
```

Time Elapsed: 1.44s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

I/O Placement

This places metal pins at the edges of the design corresponding to the top level inputs and outputs for your design. These pins act as the interface with other designs when you integrate it with other designs.

```
IOPlacement = Step.factory.get("OpenROAD.IOPlacement")

ioplace = IOPlacement(state_in=tdi.state_out)
ioplace.start()
```

```
I/O Placement
[14:46:58] VERBOSE  Running 'OpenROAD.IOPlacement'…                                   step.py:1088
[14:46:58] VERBOSE  Logging subprocess to                                             step.py:1268
                    openlane_run/4-openroad-ioplacement/openroad-ioplacement.log…
Reading OpenROAD database at '/content/openlane_run/3-openroad-tapendcapinsertion/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:46:59] WARNING  [STA-0366] port 'clk' not found.                                  openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:46:59] WARNING  [STA-0366] port 'clk' not found.                                  openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:46:59] WARNING  [STA-0419] transition time can not be specified for virtual clocks.  openroad.py:235
[INFO] Setting timing derate to: 5%
[14:46:59] WARNING  [STA-0450] virtual clock clk can not be propagated.                openroad.py:235
[INFO] place_pins args: -min_distance 3
Found 0 macro blocks.
[INFO PPL-0010] Tentative 0 to set up sections.
[INFO PPL-0001] Number of slots          108
[INFO PPL-0002] Number of I/O            96
[INFO PPL-0003] Number of I/O w/sink     96
[INFO PPL-0004] Number of I/O w/o sink   0
[INFO PPL-0005] Slots per section        200
[INFO PPL-0006] Slots increase factor    0.01
[INFO PPL-0008] Successfully assigned pins to sections.
[INFO PPL-0012] I/O nets HPWL: 6283.33 um.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/4-openroad-ioplacement/SISO.odb'…
Writing netlist to '/content/openlane_run/4-openroad-ioplacement/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/4-openroad-ioplacement/SISO.pnl.v'…
Writing layout to '/content/openlane_run/4-openroad-ioplacement/SISO.def'…
Writing timing constraints to '/content/openlane_run/4-openroad-ioplacement/SISO.sdc'…
```

Format	Path
nl	openlane_run/4-openroad-ioplacement/SISO.nl.v
pnl	openlane_run/4-openroad-ioplacement/SISO.pnl.v
def	openlane_run/4-openroad-ioplacement/SISO.def
odb	openlane_run/4-openroad-ioplacement/SISO.odb

```
display(ioplace)
```

```
Render Image (w/ KLayout)
[14:46:59] VERBOSE  Running 'KLayout.Render'…                                         step.py:1088
[14:46:59] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_g1efz2fo/klayout-render.log…  step.py:1268
```

Time Elapsed: 1.44s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Generating the Power Distribution Network (PDN)

This creates the power distribution network for your design, which is essentially a plaid pattern of horizontal and vertical "straps" across the design that is then connected to the rails' VDD and VSS (via the tap cells.)

You can find an explanation of how the power distribution network works at this link: https://openlane2.readthedocs.io/en/latest/usage/hardening_macros.html#pdn-generation

While we typically don't need to mess with the PDN too much, the SPM is a small design, so we're going to need to make the plaid pattern formed by the PDN a bit smaller.

```
GeneratePDN = Step.factory.get("OpenROAD.GeneratePDN")

pdn = GeneratePDN(
    state_in=ioplace.state_out,
    FP_PDN_VWIDTH=2,
    FP_PDN_HWIDTH=2,
    FP_PDN_VPITCH=30,
    FP_PDN_HPITCH=30,
)
pdn.start()
```

```
─────────────────────────────────── Power Distribution Network Generation ───────────────────────────────────
[14:47:00] VERBOSE  Running 'OpenROAD.GeneratePDN'…                                                  step.py:1088
[14:47:00] INFO     'FP_PDN_CFG' not explicitly set, setting it to                                openroad.py:1174
                    /content/openlane_ipynb/openlane/scripts/openroad/common/pdn_cfg.tcl…
[14:47:00] VERBOSE  Logging subprocess to                                                            step.py:1268
                    openlane_run/5-openroad-generatepdn/openroad-generatepdn.log…
Reading OpenROAD database at '/content/openlane_run/4-openroad-ioplacement/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:47:01] WARNING  [STA-0366] port 'clk' not found.                                                 openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:47:01] WARNING  [STA-0366] port 'clk' not found.                                                 openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:47:02] WARNING  [STA-0419] transition time can not be specified for virtual clocks.               openroad.py:235
[INFO] Setting timing derate to: 5%
[14:47:02] WARNING  [STA-0450] virtual clock clk can not be propagated.                              openroad.py:235
[INFO] Setting global connections...
[INFO PDN-0001] Inserting grid: stdcell_grid
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/5-openroad-generatepdn/SISO.odb'…
Writing netlist to '/content/openlane_run/5-openroad-generatepdn/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/5-openroad-generatepdn/SISO.pnl.v'…
Writing layout to '/content/openlane_run/5-openroad-generatepdn/SISO.def'…
Writing timing constraints to '/content/openlane_run/5-openroad-generatepdn/SISO.sdc'…
[INFO PSM-0040] All shapes on net VPWR are connected.
[INFO PSM-0040] All shapes on net VGND are connected.
```

Format	Path
nl	openlane_run/5-openroad-generatepdn/SISO.nl.v
pnl	openlane_run/5-openroad-generatepdn/SISO.pnl.v
def	openlane_run/5-openroad-generatepdn/SISO.def
odb	openlane_run/5-openroad-generatepdn/SISO.odb

```
display(pdn)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[14:47:02] VERBOSE  Running 'KLayout.Render'…                                                  step.py:1088
[14:47:02] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_2gzz3i3e/klayout-render.log…  step.py:1268
```

Time Elapsed: 1.44s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Global Placement

Global Placement is deciding on a fuzzy, non-final location for each of the cells, with the aim of minimizing the distance between cells that are connected together (more specifically, the total length of the not-yet-created wires that will connect them).

As you will see in the `.display()` in the second cell below, the placement is considered "illegal", i.e., not properly aligned with the cell placement grid. This is addressed by "Detailed Placement", also referred to as "placement legalization", which is the next step.

```
GlobalPlacement = Step.factory.get("OpenROAD.GlobalPlacement")

gpl = GlobalPlacement(state_in=pdn.state_out)
gpl.start()
```

```
──────────────────────────────────────────────────────────── Global Placement ────────────────────────────────────────────────────────────
[14:47:03] VERBOSE  Running 'OpenROAD.GlobalPlacement'…                                                                    step.py:1088
[14:47:03] INFO     'PL_TARGET_DENSITY_PCT' not explicitly set, using dynamically calculated                            openroad.py:1260
                    target density: 63.55400…
[14:47:03] VERBOSE  Logging subprocess to                                                                                  step.py:1268
                    openlane_run/6-openroad-globalplacement/openroad-globalplacement.log…
Reading OpenROAD database at '/content/openlane_run/5-openroad-generatepdn/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:47:04] WARNING  [STA-0366] port 'clk' not found.                                                                       openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:47:04] WARNING  [STA-0366] port 'clk' not found.                                                                       openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:47:04] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                    openroad.py:235
[INFO] Setting timing derate to: 5%
[14:47:04] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                    openroad.py:235
[INFO] Setting RC values…
[INFO] Setting signal min routing layer to: met1 and clock min routing layer to met1.
[INFO] Setting signal max routing layer to: met5 and clock max routing layer to met5.
[INFO GPL-0002] DBU: 1000
[INFO GPL-0003] SiteSize: (  0.460  2.720 ) um
[INFO GPL-0004] CoreBBox: (  5.520 10.880 ) ( 78.200 81.600 ) um
[INFO GPL-0006] NumInstances:               415
[INFO GPL-0007] NumPlaceInstances:          293
[INFO GPL-0008] NumFixedInstances:          122
[INFO GPL-0009] NumDummyInstances:            0
[INFO GPL-0010] NumNets:                    325
[INFO GPL-0011] NumPins:                   1094
[INFO GPL-0012] DieBBox:  (  0.000  0.000 ) ( 84.045 94.765 ) um
[INFO GPL-0013] CoreBBox: (  5.520 10.880 ) ( 78.200 81.600 ) um
[INFO GPL-0016] CoreArea:              5139.930 um^2
[INFO GPL-0017] NonPlaceInstsArea:      282.771 um^2
[INFO GPL-0018] PlaceInstsArea:        2665.056 um^2
[INFO GPL-0019] Util:                    54.869 %
[INFO GPL-0020] StdInstsArea:          2665.056 um^2
[INFO GPL-0021] MacroInstsArea:           0.000 um^2
[InitialPlace]  Iter: 1 CG residual: 0.00000010 HPWL: 10984720
[InitialPlace]  Iter: 2 CG residual: 0.00000010 HPWL: 7240658
[InitialPlace]  Iter: 3 CG residual: 0.00000010 HPWL: 6595639
[InitialPlace]  Iter: 4 CG residual: 0.00000011 HPWL: 6574643
[InitialPlace]  Iter: 5 CG residual: 0.00000009 HPWL: 6560245
[INFO GPL-0031] FillerInit:NumGCells:       340
[INFO GPL-0032] FillerInit:NumGNets:        325
[INFO GPL-0033] FillerInit:NumGPins:       1094
[INFO GPL-0023] TargetDensity:            0.636
[INFO GPL-0024] AvrgPlaceInstArea:        9.096 um^2
[INFO GPL-0025] IdealBinArea:            14.312 um^2
[INFO GPL-0026] IdealBinCnt:                359
[INFO GPL-0027] TotalBinArea:          5139.930 um^2
[INFO GPL-0028] BinCnt:        16     16
[INFO GPL-0029] BinSize: (  4.543  4.420 )
[INFO GPL-0030] NumBins: 256
[NesterovSolve] Iter:    1 overflow: 0.703 HPWL: 5494123
[INFO GPL-0100] worst slack 2.51e-09
[INFO GPL-0103] Weighted 29 nets.
[INFO GPL-0100] worst slack 2.48e-09
[INFO GPL-0103] Weighted 29 nets.
[NesterovSolve] Snapshot saved at iter = 3
[NesterovSolve] Iter:   10 overflow: 0.526 HPWL: 5927586
[NesterovSolve] Iter:   20 overflow: 0.524 HPWL: 5898256
[NesterovSolve] Iter:   30 overflow: 0.522 HPWL: 5892824
[NesterovSolve] Iter:   40 overflow: 0.523 HPWL: 5893540
[NesterovSolve] Iter:   50 overflow: 0.524 HPWL: 5894015
[NesterovSolve] Iter:   60 overflow: 0.523 HPWL: 5894909
[NesterovSolve] Iter:   70 overflow: 0.523 HPWL: 5895107
[NesterovSolve] Iter:   80 overflow: 0.523 HPWL: 5894031
[NesterovSolve] Iter:   90 overflow: 0.523 HPWL: 5893681
[NesterovSolve] Iter:  100 overflow: 0.523 HPWL: 5894881
[NesterovSolve] Iter:  110 overflow: 0.522 HPWL: 5895901
[NesterovSolve] Iter:  120 overflow: 0.522 HPWL: 5895926
[NesterovSolve] Iter:  130 overflow: 0.521 HPWL: 5896003
[NesterovSolve] Iter:  140 overflow: 0.519 HPWL: 5897195
[NesterovSolve] Iter:  150 overflow: 0.517 HPWL: 5899558
[NesterovSolve] Iter:  160 overflow: 0.513 HPWL: 5901736
[NesterovSolve] Iter:  170 overflow: 0.509 HPWL: 5904488
[NesterovSolve] Iter:  180 overflow: 0.503 HPWL: 5910052
[NesterovSolve] Iter:  190 overflow: 0.491 HPWL: 5913349
[INFO GPL-0100] worst slack 2.47e-09
[INFO GPL-0103] Weighted 29 nets.
[NesterovSolve] Iter:  200 overflow: 0.467 HPWL: 5902360
[NesterovSolve] Iter:  210 overflow: 0.438 HPWL: 5847206
[NesterovSolve] Iter:  220 overflow: 0.403 HPWL: 5770373
[NesterovSolve] Iter:  230 overflow: 0.370 HPWL: 5723600
[NesterovSolve] Iter:  240 overflow: 0.344 HPWL: 5721253
[NesterovSolve] Iter:  250 overflow: 0.316 HPWL: 5711731
[NesterovSolve] Iter:  260 overflow: 0.289 HPWL: 5716790
[INFO GPL-0100] worst slack 2.38e-09
[INFO GPL-0103] Weighted 29 nets.
[NesterovSolve] Iter:  270 overflow: 0.264 HPWL: 5742151
[NesterovSolve] Iter:  280 overflow: 0.242 HPWL: 5759494
[NesterovSolve] Iter:  290 overflow: 0.220 HPWL: 5778022
[INFO GPL-0100] worst slack 2.3e-09
[INFO GPL-0103] Weighted 29 nets.
[NesterovSolve] Iter:  300 overflow: 0.201 HPWL: 5802950
[INFO GPL-0075] Routability numCall: 1 inflationIterCnt: 1 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      12   13
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 156
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0
[INFO GPL-0065] OverflowTileCnt2: 0
[INFO GPL-0066] 0.5%RC: 1.0000
[INFO GPL-0067] 1.0%RC: 1.0000
[INFO GPL-0068] 2.0%RC: 1.0000
[INFO GPL-0069] 5.0%RC: 0.9591
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0000
[INFO GPL-0078] FinalRC lower than minRC (1e+30), min RC updated.
[INFO GPL-0045] InflatedAreaDelta:        0.000 um^2
[INFO GPL-0046] TargetDensity:            0.636
[INFO GPL-0049] WhiteSpaceArea:        4857.158 um^2
[INFO GPL-0050] NesterovInstsArea:     2665.056 um^2
[INFO GPL-0051] TotalFillerArea:        421.863 um^2
[INFO GPL-0052] TotalGCellsArea:       3086.919 um^2
[INFO GPL-0053] ExpectedGCellsArea:    3086.919 um^2
[INFO GPL-0054] NewTargetDensity:         0.636
[INFO GPL-0055] NewWhiteSpaceArea:     4857.158 um^2
[INFO GPL-0056] MovableArea:           3086.919 um^2
[INFO GPL-0057] NewNesterovInstArea:   2665.056 um^2
```

```
[INFO GPL-0058] NewTotalFillerArea:     421.863 um^2
[INFO GPL-0059] NewTotalGCellsArea:    3086.919 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter:  310 overflow: 0.523 HPWL: 5872113
[NesterovSolve] Iter:  320 overflow: 0.515 HPWL: 5847346
[NesterovSolve] Iter:  330 overflow: 0.518 HPWL: 5839385
[NesterovSolve] Iter:  340 overflow: 0.519 HPWL: 5845360
[NesterovSolve] Iter:  350 overflow: 0.517 HPWL: 5844672
[NesterovSolve] Iter:  360 overflow: 0.517 HPWL: 5841758
[NesterovSolve] Iter:  370 overflow: 0.518 HPWL: 5841458
[NesterovSolve] Iter:  380 overflow: 0.518 HPWL: 5842074
[NesterovSolve] Iter:  390 overflow: 0.517 HPWL: 5841996
[NesterovSolve] Iter:  400 overflow: 0.517 HPWL: 5841511
[NesterovSolve] Iter:  410 overflow: 0.517 HPWL: 5841986
[NesterovSolve] Iter:  420 overflow: 0.517 HPWL: 5842356
[NesterovSolve] Iter:  430 overflow: 0.516 HPWL: 5841580
[NesterovSolve] Iter:  440 overflow: 0.516 HPWL: 5841206
[NesterovSolve] Iter:  450 overflow: 0.516 HPWL: 5841962
[NesterovSolve] Iter:  460 overflow: 0.514 HPWL: 5842613
[NesterovSolve] Iter:  470 overflow: 0.513 HPWL: 5843282
[NesterovSolve] Iter:  480 overflow: 0.511 HPWL: 5843867
[NesterovSolve] Iter:  490 overflow: 0.509 HPWL: 5844726
[NesterovSolve] Iter:  500 overflow: 0.505 HPWL: 5842983
[NesterovSolve] Iter:  510 overflow: 0.497 HPWL: 5835551
[NesterovSolve] Iter:  520 overflow: 0.488 HPWL: 5826159
[NesterovSolve] Iter:  530 overflow: 0.479 HPWL: 5815501
[NesterovSolve] Iter:  540 overflow: 0.467 HPWL: 5801815
[NesterovSolve] Iter:  550 overflow: 0.449 HPWL: 5785749
[NesterovSolve] Iter:  560 overflow: 0.423 HPWL: 5735741
[NesterovSolve] Iter:  570 overflow: 0.396 HPWL: 5682331
[NesterovSolve] Iter:  580 overflow: 0.378 HPWL: 5669610
[NesterovSolve] Iter:  590 overflow: 0.355 HPWL: 5662115
[NesterovSolve] Iter:  600 overflow: 0.328 HPWL: 5649687
[NesterovSolve] Iter:  610 overflow: 0.302 HPWL: 5657538
[NesterovSolve] Iter:  620 overflow: 0.278 HPWL: 5679598
[NesterovSolve] Iter:  630 overflow: 0.258 HPWL: 5706224
[NesterovSolve] Iter:  640 overflow: 0.233 HPWL: 5720087
[NesterovSolve] Iter:  650 overflow: 0.215 HPWL: 5754183
[INFO GPL-0075] Routability numCall: 2 inflationIterCnt: 2 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      12   13
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 156
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0
[INFO GPL-0065] OverflowTileCnt2: 0
[INFO GPL-0066] 0.5%RC: 1.0000
[INFO GPL-0067] 1.0%RC: 1.0000
[INFO GPL-0068] 2.0%RC: 0.9889
[INFO GPL-0069] 5.0%RC: 0.9386
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0000
[INFO GPL-0079] MinRC (1) violation occurred, total count: 1.
[INFO GPL-0045] InflatedAreaDelta:        0.000 um^2
[INFO GPL-0046] TargetDensity:            0.636
[INFO GPL-0049] WhiteSpaceArea:        4857.158 um^2
[INFO GPL-0050] NesterovInstsArea:     2665.056 um^2
[INFO GPL-0051] TotalFillerArea:        421.863 um^2
[INFO GPL-0052] TotalGCellsArea:       3086.919 um^2
[INFO GPL-0053] ExpectedGCellsArea:    3086.919 um^2
[INFO GPL-0054] NewTargetDensity:         0.636
[INFO GPL-0055] NewWhiteSpaceArea:     4857.158 um^2
[INFO GPL-0056] MovableArea:           3086.919 um^2
[INFO GPL-0057] NewNesterovInstArea:   2665.056 um^2
[INFO GPL-0058] NewTotalFillerArea:     421.863 um^2
[INFO GPL-0059] NewTotalGCellsArea:    3086.919 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter:  660 overflow: 0.535 HPWL: 5973975
[NesterovSolve] Iter:  670 overflow: 0.520 HPWL: 5853490
[NesterovSolve] Iter:  680 overflow: 0.516 HPWL: 5838952
[NesterovSolve] Iter:  690 overflow: 0.520 HPWL: 5838857
[NesterovSolve] Iter:  700 overflow: 0.518 HPWL: 5843701
[NesterovSolve] Iter:  710 overflow: 0.517 HPWL: 5842741
[NesterovSolve] Iter:  720 overflow: 0.518 HPWL: 5840770
[NesterovSolve] Iter:  730 overflow: 0.518 HPWL: 5840981
[NesterovSolve] Iter:  740 overflow: 0.517 HPWL: 5841943
[NesterovSolve] Iter:  750 overflow: 0.517 HPWL: 5841280
[NesterovSolve] Iter:  760 overflow: 0.517 HPWL: 5841217
[NesterovSolve] Iter:  770 overflow: 0.517 HPWL: 5841740
[NesterovSolve] Iter:  780 overflow: 0.517 HPWL: 5841573
[NesterovSolve] Iter:  790 overflow: 0.516 HPWL: 5840480
[NesterovSolve] Iter:  800 overflow: 0.516 HPWL: 5840297
[NesterovSolve] Iter:  810 overflow: 0.515 HPWL: 5840933
[NesterovSolve] Iter:  820 overflow: 0.514 HPWL: 5840916
[NesterovSolve] Iter:  830 overflow: 0.513 HPWL: 5840673
[NesterovSolve] Iter:  840 overflow: 0.511 HPWL: 5840888
[NesterovSolve] Iter:  850 overflow: 0.508 HPWL: 5841242
[NesterovSolve] Iter:  860 overflow: 0.503 HPWL: 5838654
[NesterovSolve] Iter:  870 overflow: 0.494 HPWL: 5829441
[NesterovSolve] Iter:  880 overflow: 0.486 HPWL: 5819330
[NesterovSolve] Iter:  890 overflow: 0.475 HPWL: 5807768
[NesterovSolve] Iter:  900 overflow: 0.464 HPWL: 5796692
[NesterovSolve] Iter:  910 overflow: 0.443 HPWL: 5768619
[NesterovSolve] Iter:  920 overflow: 0.414 HPWL: 5717789
[NesterovSolve] Iter:  930 overflow: 0.390 HPWL: 5672429
[NesterovSolve] Iter:  940 overflow: 0.371 HPWL: 5667287
[NesterovSolve] Iter:  950 overflow: 0.347 HPWL: 5656782
[NesterovSolve] Iter:  960 overflow: 0.321 HPWL: 5653017
[NesterovSolve] Iter:  970 overflow: 0.294 HPWL: 5660951
[NesterovSolve] Iter:  980 overflow: 0.273 HPWL: 5682496
[NesterovSolve] Iter:  990 overflow: 0.252 HPWL: 5710917
[NesterovSolve] Iter: 1000 overflow: 0.227 HPWL: 5724906
[NesterovSolve] Iter: 1010 overflow: 0.209 HPWL: 5763050
[INFO GPL-0075] Routability numCall: 3 inflationIterCnt: 3 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      12   13
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 156
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0
[INFO GPL-0065] OverflowTileCnt2: 0
[INFO GPL-0066] 0.5%RC: 1.0000
[INFO GPL-0067] 1.0%RC: 1.0000
[INFO GPL-0068] 2.0%RC: 0.9889
[INFO GPL-0069] 5.0%RC: 0.9386
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0000
[INFO GPL-0079] MinRC (1) violation occurred, total count: 2.
[INFO GPL-0045] InflatedAreaDelta:        0.000 um^2
[INFO GPL-0046] TargetDensity:            0.636
[INFO GPL-0049] WhiteSpaceArea:        4857.158 um^2
[INFO GPL-0050] NesterovInstsArea:     2665.056 um^2
```

```
[INFO GPL-0051] TotalFillerArea:        421.863 um^2
[INFO GPL-0052] TotalGCellsArea:       3086.919 um^2
[INFO GPL-0053] ExpectedGCellsArea:    3086.919 um^2
[INFO GPL-0054] NewTargetDensity:         0.636
[INFO GPL-0055] NewWhiteSpaceArea:     4857.158 um^2
[INFO GPL-0056] MovableArea:           3086.919 um^2
[INFO GPL-0057] NewNesterovInstArea:   2665.056 um^2
[INFO GPL-0058] NewTotalFillerArea:     421.863 um^2
[INFO GPL-0059] NewTotalGCellsArea:    3086.919 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter: 1020 overflow: 0.521 HPWL: 5925600
[NesterovSolve] Iter: 1030 overflow: 0.517 HPWL: 5854950
[NesterovSolve] Iter: 1040 overflow: 0.517 HPWL: 5839530
[NesterovSolve] Iter: 1050 overflow: 0.520 HPWL: 5843892
[NesterovSolve] Iter: 1060 overflow: 0.518 HPWL: 5845493
[NesterovSolve] Iter: 1070 overflow: 0.517 HPWL: 5842872
[NesterovSolve] Iter: 1080 overflow: 0.518 HPWL: 5841330
[NesterovSolve] Iter: 1090 overflow: 0.518 HPWL: 5841766
[NesterovSolve] Iter: 1100 overflow: 0.517 HPWL: 5842235
[NesterovSolve] Iter: 1110 overflow: 0.517 HPWL: 5841584
[NesterovSolve] Iter: 1120 overflow: 0.517 HPWL: 5841699
[NesterovSolve] Iter: 1130 overflow: 0.517 HPWL: 5842332
[NesterovSolve] Iter: 1140 overflow: 0.516 HPWL: 5841975
[NesterovSolve] Iter: 1150 overflow: 0.516 HPWL: 5841170
[NesterovSolve] Iter: 1160 overflow: 0.516 HPWL: 5841595
[NesterovSolve] Iter: 1170 overflow: 0.515 HPWL: 5842439
[NesterovSolve] Iter: 1180 overflow: 0.514 HPWL: 5842978
[NesterovSolve] Iter: 1190 overflow: 0.512 HPWL: 5843372
[NesterovSolve] Iter: 1200 overflow: 0.510 HPWL: 5844514
[NesterovSolve] Iter: 1210 overflow: 0.507 HPWL: 5844212
[NesterovSolve] Iter: 1220 overflow: 0.500 HPWL: 5839553
[NesterovSolve] Iter: 1230 overflow: 0.492 HPWL: 5829843
[NesterovSolve] Iter: 1240 overflow: 0.483 HPWL: 5819255
[NesterovSolve] Iter: 1250 overflow: 0.472 HPWL: 5805943
[NesterovSolve] Iter: 1260 overflow: 0.459 HPWL: 5796319
[NesterovSolve] Iter: 1270 overflow: 0.434 HPWL: 5758446
[NesterovSolve] Iter: 1280 overflow: 0.405 HPWL: 5701832
[NesterovSolve] Iter: 1290 overflow: 0.385 HPWL: 5667659
[NesterovSolve] Iter: 1300 overflow: 0.365 HPWL: 5664282
[NesterovSolve] Iter: 1310 overflow: 0.338 HPWL: 5654438
[NesterovSolve] Iter: 1320 overflow: 0.312 HPWL: 5655942
[NesterovSolve] Iter: 1330 overflow: 0.288 HPWL: 5669394
[NesterovSolve] Iter: 1340 overflow: 0.267 HPWL: 5692861
[NesterovSolve] Iter: 1350 overflow: 0.242 HPWL: 5716796
[NesterovSolve] Iter: 1360 overflow: 0.221 HPWL: 5739099
[NesterovSolve] Iter: 1370 overflow: 0.203 HPWL: 5773801
[INFO GPL-0075] Routability numCall: 4 inflationIterCnt: 4 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      12   13
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 156
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0
[INFO GPL-0065] OverflowTileCnt2: 0
[INFO GPL-0066] 0.5%RC: 1.0000
[INFO GPL-0067] 1.0%RC: 1.0000
[INFO GPL-0068] 2.0%RC: 0.9889
[INFO GPL-0069] 5.0%RC: 0.9364
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0000
[INFO GPL-0079] MinRC (1) violation occurred, total count: 3.
[INFO GPL-0045] InflatedAreaDelta:        0.000 um^2
[INFO GPL-0046] TargetDensity:            0.636
Revert Routability Procedure. Target density higher than max, or minRC max violations.
[INFO GPL-0080] minRcViolatedCnt: 3
[INFO GPL-0047] SavedMinRC: 1.0000
[INFO GPL-0048] SavedTargetDensity: 0.6355
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter: 1380 overflow: 0.521 HPWL: 5873273
[NesterovSolve] Iter: 1390 overflow: 0.515 HPWL: 5844760
[NesterovSolve] Iter: 1400 overflow: 0.518 HPWL: 5836387
[NesterovSolve] Iter: 1410 overflow: 0.519 HPWL: 5843121
[NesterovSolve] Iter: 1420 overflow: 0.517 HPWL: 5843366
[NesterovSolve] Iter: 1430 overflow: 0.517 HPWL: 5841554
[NesterovSolve] Iter: 1440 overflow: 0.518 HPWL: 5840667
[NesterovSolve] Iter: 1450 overflow: 0.518 HPWL: 5841802
[NesterovSolve] Iter: 1460 overflow: 0.517 HPWL: 5841620
[NesterovSolve] Iter: 1470 overflow: 0.517 HPWL: 5841148
[NesterovSolve] Iter: 1480 overflow: 0.517 HPWL: 5841469
[NesterovSolve] Iter: 1490 overflow: 0.517 HPWL: 5841774
[NesterovSolve] Iter: 1500 overflow: 0.516 HPWL: 5840955
[NesterovSolve] Iter: 1510 overflow: 0.516 HPWL: 5840204
[NesterovSolve] Iter: 1520 overflow: 0.516 HPWL: 5840662
[NesterovSolve] Iter: 1530 overflow: 0.514 HPWL: 5840981
[NesterovSolve] Iter: 1540 overflow: 0.513 HPWL: 5840821
[NesterovSolve] Iter: 1550 overflow: 0.512 HPWL: 5840679
[NesterovSolve] Iter: 1560 overflow: 0.509 HPWL: 5841205
[NesterovSolve] Iter: 1570 overflow: 0.505 HPWL: 5840322
[NesterovSolve] Iter: 1580 overflow: 0.498 HPWL: 5833822
[NesterovSolve] Iter: 1590 overflow: 0.489 HPWL: 5823627
[NesterovSolve] Iter: 1600 overflow: 0.480 HPWL: 5812783
[NesterovSolve] Iter: 1610 overflow: 0.468 HPWL: 5799940
[NesterovSolve] Iter: 1620 overflow: 0.452 HPWL: 5786200
[NesterovSolve] Iter: 1630 overflow: 0.425 HPWL: 5739269
[NesterovSolve] Iter: 1640 overflow: 0.399 HPWL: 5683577
[NesterovSolve] Iter: 1650 overflow: 0.381 HPWL: 5667059
[NesterovSolve] Iter: 1660 overflow: 0.358 HPWL: 5661713
[NesterovSolve] Iter: 1670 overflow: 0.331 HPWL: 5649790
[NesterovSolve] Iter: 1680 overflow: 0.304 HPWL: 5655514
[NesterovSolve] Iter: 1690 overflow: 0.281 HPWL: 5676007
[NesterovSolve] Iter: 1700 overflow: 0.261 HPWL: 5700535
[NesterovSolve] Iter: 1710 overflow: 0.236 HPWL: 5715523
[NesterovSolve] Iter: 1720 overflow: 0.216 HPWL: 5748367
[NesterovSolve] Iter: 1730 overflow: 0.196 HPWL: 5779845
[NesterovSolve] Iter: 1740 overflow: 0.174 HPWL: 5798781
[NesterovSolve] Iter: 1750 overflow: 0.155 HPWL: 5827150
```

```
display(gpl)
```

```
────────────────────────────────────────── Render Image (w/ KLayout) ──────────────────────────────────────────
[14:47:08] VERBOSE  Running 'KLayout.Render'…                                                          step.py:1088
[14:47:08] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_9koircp2/klayout-render.log…     step.py:1268
```

Time Elapsed: 4.56s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Detailed Placement

This aligns the fuzzy placement from before with the grid, "legalizing" it.

```
DetailedPlacement = Step.factory.get("OpenROAD.DetailedPlacement")

dpl = DetailedPlacement(state_in=gpl.state_out)
dpl.start()
```

```
────────────────────────────────────────────────────────────── Detailed Placement ──────────────────────────────────────────────────────────────
[14:47:09] VERBOSE  Running 'OpenROAD.DetailedPlacement'…                                                                          step.py:1088
[14:47:09] VERBOSE  Logging subprocess to                                                                                           step.py:1268
                    openlane_run/7-openroad-detailedplacement/openroad-detailedplacement.log…
Reading OpenROAD database at '/content/openlane_run/6-openroad-globalplacement/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:47:10] WARNING  [STA-0366] port 'clk' not found.                                                                              openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:47:10] WARNING  [STA-0366] port 'clk' not found.                                                                              openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:47:10] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                            openroad.py:235
[INFO] Setting timing derate to: 5%
[14:47:10] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                           openroad.py:235
Placement Analysis
---------------------------------
total displacement        625.7 u
average displacement        1.5 u
max displacement            7.6 u
original HPWL            5934.9 u
legalized HPWL           6534.3 u
delta HPWL                   10 %

[INFO DPL-0020] Mirrored 84 instances
[INFO DPL-0021] HPWL before            6534.3 u
[INFO DPL-0022] HPWL after             6411.8 u
[INFO DPL-0023] HPWL delta               -1.9 %
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/7-openroad-detailedplacement/SISO.odb'…
Writing netlist to '/content/openlane_run/7-openroad-detailedplacement/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/7-openroad-detailedplacement/SISO.pnl.v'…
Writing layout to '/content/openlane_run/7-openroad-detailedplacement/SISO.def'…
Writing timing constraints to '/content/openlane_run/7-openroad-detailedplacement/SISO.sdc'…
```

Format	Path
nl	openlane_run/7-openroad-detailedplacement/SISO.nl.v
pnl	openlane_run/7-openroad-detailedplacement/SISO.pnl.v
def	openlane_run/7-openroad-detailedplacement/SISO.def
odb	openlane_run/7-openroad-detailedplacement/SISO.odb

```
display(dpl)
```

```
────────────────────────────────────────────────────────────── Render Image (w/ KLayout) ──────────────────────────────────────────────────────────────
[14:47:10] VERBOSE  Running 'KLayout.Render'…                                                                                       step.py:1088
[14:47:10] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_92a99_cv/klayout-render.log…                                  step.py:1268
```

Time Elapsed: 1.33s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Clock Tree Synthesis (CTS)

With the cells now having a final placement, we can go ahead and create what is known as the clock tree, i.e., the hierarchical set of buffers used for clock signal to minimize what is known as "clock skew"- variable delay of the clock cycle from register to register because of factors such as metal wire length, clock load (number of gates connected to the same clock buffer,) et cetera.

The CTS step creates the cells and places the between the gaps in the detailed placement above.

```
CTS = Step.factory.get("OpenROAD.CTS")

cts = CTS(state_in=dpl.state_out)
cts.start()
```

```
────────────────────────────────────────────────────────── Clock Tree Synthesis ──────────────────────────────────────────────────────────
[14:47:11] VERBOSE  Running 'OpenROAD.CTS'…                                                                                    step.py:1088
[14:47:11] VERBOSE  Logging subprocess to openlane_run/8-openroad-cts/openroad-cts.log…                                        step.py:1268
Reading timing models for corner nom_tt_025C_1v80…
Reading timing library for the 'nom_tt_025C_1v80' corner at
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading timing models for corner nom_ff_n40C_1v95…
Reading timing library for the 'nom_ff_n40C_1v95' corner at
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ff_n40C_1v95.lib'…
Reading timing models for corner nom_ss_100C_1v60…
Reading timing library for the 'nom_ss_100C_1v60' corner at
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ss_100C_1v60.lib'…
Reading OpenROAD database at '/content/openlane_run/7-openroad-detailedplacement/SISO.odb'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:47:15] WARNING  [STA-0366] port 'clk' not found.                                                                            openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:47:15] WARNING  [STA-0366] port 'clk' not found.                                                                            openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:47:15] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                          openroad.py:235
[INFO] Setting timing derate to: 5%
[14:47:15] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                         openroad.py:235
[INFO] Setting RC values…
[INFO] Configuring cts characterization…
[INFO] Performing clock tree synthesis…
[INFO] Looking for the following net(s): clk
[INFO] Running Clock Tree Synthesis…
[INFO CTS-0050] Root buffer is sky130_fd_sc_hd__clkbuf_16.
[INFO CTS-0051] Sink buffer is sky130_fd_sc_hd__clkbuf_8.
[INFO CTS-0052] The following clock buffers will be used for CTS:
sky130_fd_sc_hd__clkbuf_2
sky130_fd_sc_hd__clkbuf_4
sky130_fd_sc_hd__clkbuf_8
[INFO CTS-0049] Characterization buffer is sky130_fd_sc_hd__clkbuf_8.
[14:47:22] WARNING  [CTS-0083] No clock nets have been found.                                                                   openroad.py:235
[INFO CTS-0008] TritonCTS found 0 clock nets.
[14:47:22] WARNING  [CTS-0082] No valid clock nets in the design.                                                               openroad.py:235
[14:47:22] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                         openroad.py:235
[INFO] Repairing long wires on clock nets…
[INFO RSZ-0058] Using max wire length 6335um.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/8-openroad-cts/SISO.odb'…
Writing netlist to '/content/openlane_run/8-openroad-cts/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/8-openroad-cts/SISO.pnl.v'…
Writing layout to '/content/openlane_run/8-openroad-cts/SISO.def'…
Writing timing constraints to '/content/openlane_run/8-openroad-cts/SISO.sdc'…
[INFO] Legalizing…
Placement Analysis
---------------------------------
total displacement          0.0 u
average displacement        0.0 u
max displacement            0.0 u
original HPWL            6411.8 u
legalized HPWL           6534.3 u
delta HPWL                    2 %

[INFO DPL-0020] Mirrored 84 instances
[INFO DPL-0021] HPWL before            6534.3 u
[INFO DPL-0022] HPWL after             6411.8 u
[INFO DPL-0023] HPWL delta               -1.9 %
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/8-openroad-cts/SISO.odb'…
Writing netlist to '/content/openlane_run/8-openroad-cts/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/8-openroad-cts/SISO.pnl.v'…
Writing layout to '/content/openlane_run/8-openroad-cts/SISO.def'…
Writing timing constraints to '/content/openlane_run/8-openroad-cts/SISO.sdc'…
```

Format	Path
nl	openlane_run/8-openroad-cts/SISO.nl.v
pnl	openlane_run/8-openroad-cts/SISO.pnl.v

```
display(cts)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[14:47:23] VERBOSE  Running 'KLayout.Render'…                                                  step.py:1088
[14:47:23] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_xku0qhhp/klayout-render.log…  step.py:1268
```

Time Elapsed: 12.02s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Global Routing

Global routing "plans" the routes the wires between two gates (or gates and I/O pins/the PDN) will take. The results of global routing (which are called "routing guides") are stored in internal data structures and have no effect on the actual design, so there is no `display()` statement.

```
GlobalRouting = Step.factory.get("OpenROAD.GlobalRouting")

grt = GlobalRouting(state_in=cts.state_out)
grt.start()
```

```
──────────────────────────────────────────────────────── Global Routing ────────────────────────────────────────────────────────
[14:47:24] VERBOSE  Running 'OpenROAD.GlobalRouting'…                                                          step.py:1088
[14:47:24] VERBOSE  Logging subprocess to                                                                      step.py:1268
                    openlane_run/9-openroad-globalrouting/openroad-globalrouting.log…
Reading OpenROAD database at '/content/openlane_run/8-openroad-cts/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:47:25] WARNING  [STA-0366] port 'clk' not found.                                                        openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:47:25] WARNING  [STA-0366] port 'clk' not found.                                                        openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.1499999999999999944488848768742172978818416595458984375
[14:47:25] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                      openroad.py:235
[INFO] Setting timing derate to: 5%
[14:47:25] WARNING  [STA-0450] virtual clock clk can not be propagated.                                     openroad.py:235
[14:47:25] WARNING  [STA-0450] virtual clock clk can not be propagated.                                     openroad.py:235
[INFO] Setting signal min routing layer to: met1 and clock min routing layer to met1.
[INFO] Setting signal max routing layer to: met5 and clock max routing layer to met5.
-congestion_iterations 50 -verbose
[INFO GRT-0020] Min routing layer: met1
[INFO GRT-0021] Max routing layer: met5
[INFO GRT-0022] Global adjustment: 30%
[INFO GRT-0023] Grid origin: (0, 0)
[INFO GRT-0043] No OR_DEFAULT vias defined.
[INFO GRT-0088] Layer li1     Track-Pitch = 0.4600  line-2-Via Pitch: 0.3400
[INFO GRT-0088] Layer met1    Track-Pitch = 0.3400  line-2-Via Pitch: 0.3400
[INFO GRT-0088] Layer met2    Track-Pitch = 0.4600  line-2-Via Pitch: 0.3500
[INFO GRT-0088] Layer met3    Track-Pitch = 0.6800  line-2-Via Pitch: 0.6150
[INFO GRT-0088] Layer met4    Track-Pitch = 0.9200  line-2-Via Pitch: 1.0400
[INFO GRT-0088] Layer met5    Track-Pitch = 3.4000  line-2-Via Pitch: 3.1100
[INFO GRT-0019] Found 0 clock nets.
[INFO GRT-0001] Minimum degree: 2
[INFO GRT-0002] Maximum degree: 34
[INFO GRT-0003] Macros: 0
[INFO GRT-0043] No OR_DEFAULT vias defined.
[INFO GRT-0004] Blockages: 255

[INFO GRT-0053] Routing resources analysis:
Routing      Original      Derated      Resource
Layer     Direction    Resources     Resources    Reduction (%)
-------------------------------------------------------------
li1        Vertical            0             0          0.00%
met1       Horizontal       3280          1619          50.64%
met2       Vertical         2381          1430          39.94%
met3       Horizontal       1634           965          40.94%
met4       Vertical          968           498          48.55%
met5       Horizontal        322           132          59.01%
-------------------------------------------------------------

[INFO GRT-0197] Via related to pin nodes: 1652
[INFO GRT-0198] Via related Steiner nodes: 15
[INFO GRT-0199] Via filling finished.
[INFO GRT-0111] Final number of vias: 2033
[INFO GRT-0112] Final usage 3D: 7006

[INFO GRT-0096] Final congestion report:
Layer         Resource        Demand        Usage (%)    Max H / Max V / Total Overflow
---------------------------------------------------------------------------------------
li1                  0             0            0.00%             0 /  0 /  0
met1              1619           385           23.78%             0 /  0 /  0
met2              1430           422           29.51%             0 /  0 /  0
met3               965            88            9.12%             0 /  0 /  0
met4               498            12            2.41%             0 /  0 /  0
met5               132             0            0.00%             0 /  0 /  0
---------------------------------------------------------------------------------------
Total             4644           907           19.53%             0 /  0 /  0

[INFO GRT-0018] Total wirelength: 11681 um
[INFO GRT-0014] Routed nets: 325
[INFO] Setting RC values…
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/9-openroad-globalrouting/SISO.odb'…
Writing layout to '/content/openlane_run/9-openroad-globalrouting/SISO.def'…
```

Format	Path
nl	openlane_run/8-openroad-cts/SISO.nl.v
pnl	openlane_run/8-openroad-cts/SISO.pnl.v

Detailed Routing

Detailed routing uses the guides from Global Routing to actually create wires on the metal layers and connect the gates, making the connections finally physical.

This is typically the longest step in the flow.

```
DetailedRouting = Step.factory.get("OpenROAD.DetailedRouting")

drt = DetailedRouting(state_in=grt.state_out)
drt.start()
```

```
Detailed Routing
[14:47:26] VERBOSE  Running 'OpenROAD.DetailedRouting'…                                   step.py:1088
[14:47:26] INFO     Running TritonRoute with 2 threads…                                  openroad.py:1619
[14:47:26] VERBOSE  Logging subprocess to                                                 step.py:1268
                    openlane_run/10-openroad-detailedrouting/openroad-detailedrouting.log…
Reading OpenROAD database at '/content/openlane_run/9-openroad-globalrouting/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:47:27] WARNING  [STA-0366] port 'clk' not found.                                      openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:47:27] WARNING  [STA-0366] port 'clk' not found.                                      openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:47:27] WARNING  [STA-0419] transition time can not be specified for virtual clocks.    openroad.py:235
[INFO] Setting timing derate to: 5%
[14:47:27] WARNING  [STA-0450] virtual clock clk can not be propagated.                   openroad.py:235
[INFO ORD-0030] Using 2 thread(s).
[INFO DRT-0149] Reading tech and libs.
[14:47:27] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer mcon
[14:47:27] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer mcon
[14:47:27] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via
[14:47:27] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via
[14:47:27] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via2
[14:47:27] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via2
[14:47:27] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via3
[14:47:27] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via3
[14:47:27] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via4
[14:47:27] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via4

Units:                1000
Number of layers:     13
Number of macros:     441
Number of vias:       29
Number of viarulegen: 25

[INFO DRT-0150] Reading design.

Design:                   SISO
Die area:                 ( 0 0 ) ( 84045 94765 )
Number of track patterns: 12
Number of DEF vias:       0
Number of components:     415
Number of terminals:      98
Number of snets:          2
Number of nets:           325

[INFO DRT-0167] List of default vias:
Layer via
default via: M1M2_PR
Layer via2
default via: M2M3_PR
Layer via3
default via: M3M4_PR
Layer via4
default via: M4M5_PR
[INFO DRT-0162] Library cell analysis.
[INFO DRT-0163] Instance analysis.
[INFO DRT-0164] Number of unique instances = 110.
[INFO DRT-0168] Init region query.
[INFO DRT-0024]   Complete FR_MASTERSLICE.
[INFO DRT-0024]   Complete Fr_VIA.
[INFO DRT-0024]   Complete li1.
[INFO DRT-0024]   Complete mcon.
[INFO DRT-0024]   Complete met1.
[INFO DRT-0024]   Complete via.
[INFO DRT-0024]   Complete met2.
[INFO DRT-0024]   Complete via2.
[INFO DRT-0024]   Complete met3.
[INFO DRT-0024]   Complete via3.
[INFO DRT-0024]   Complete met4.
[INFO DRT-0024]   Complete via4.
[INFO DRT-0024]   Complete met5.
[INFO DRT-0033] FR_MASTERSLICE shape region query size = 0.
[INFO DRT-0033] FR_VIA shape region query size = 0.
[INFO DRT-0033] li1 shape region query size = 8401.
[INFO DRT-0033] mcon shape region query size = 0.
[INFO DRT-0033] met1 shape region query size = 1164.
[INFO DRT-0033] via shape region query size = 324.
[INFO DRT-0033] met2 shape region query size = 148.
[INFO DRT-0033] via2 shape region query size = 270.
[INFO DRT-0033] met3 shape region query size = 218.
[INFO DRT-0033] via3 shape region query size = 270.
[INFO DRT-0033] met4 shape region query size = 70.
[INFO DRT-0033] via4 shape region query size = 8.
[INFO DRT-0033] met5 shape region query size = 16.
[INFO DRT-0165] Start pin access.
[INFO DRT-0078]   Complete 407 pins.
[INFO DRT-0079]   Complete 100 unique inst patterns.
[INFO DRT-0081]   Complete 104 unique inst patterns.
[INFO DRT-0084]   Complete 200 groups.
#scanned instances     = 415
#unique  instances     = 110
#stdCellGenAp          = 2810
#stdCellValidPlanarAp  = 28
#stdCellValidViaAp     = 2224
#stdCellPinNoAp        = 0
#stdCellPinCnt         = 998
#instTermValidViaApCnt = 0
#macroGenAp            = 0
#macroValidPlanarAp    = 0
#macroValidViaAp       = 0
#macroNoAp             = 0
[INFO DRT-0166] Complete pin access.
[INFO DRT-0267] cpu time = 00:00:18, elapsed time = 00:00:10, memory = 115.75 (MB), peak = 255.95 (MB)

Number of guides:     2119

[INFO DRT-0169] Post process guides.
[INFO DRT-0176] GCELLGRID X 0 DO 12 STEP 6900 ;
[INFO DRT-0177] GCELLGRID Y 0 DO 13 STEP 6900 ;
[INFO DRT-0028]   Complete FR_MASTERSLICE.
[INFO DRT-0028]   Complete Fr_VIA.
[INFO DRT-0028]   Complete li1.
[INFO DRT-0028]   Complete mcon.
```

```
[INFO DRT-0028]   Complete met1.
[INFO DRT-0028]   Complete via.
[INFO DRT-0028]   Complete met2.
[INFO DRT-0028]   Complete via2.
[INFO DRT-0028]   Complete met3.
[INFO DRT-0028]   Complete via3.
[INFO DRT-0028]   Complete met4.
[INFO DRT-0028]   Complete via4.
[INFO DRT-0028]   Complete met5.
[INFO DRT-0178] Init guide query.
[INFO DRT-0035]   Complete FR_MASTERSLICE (guide).
[INFO DRT-0035]   Complete Fr_VIA (guide).
[INFO DRT-0035]   Complete li1 (guide).
[INFO DRT-0035]   Complete mcon (guide).
[INFO DRT-0035]   Complete met1 (guide).
[INFO DRT-0035]   Complete via (guide).
[INFO DRT-0035]   Complete met2 (guide).
[INFO DRT-0035]   Complete via2 (guide).
[INFO DRT-0035]   Complete met3 (guide).
[INFO DRT-0035]   Complete via3 (guide).
[INFO DRT-0035]   Complete met4 (guide).
[INFO DRT-0035]   Complete via4 (guide).
[INFO DRT-0035]   Complete met5 (guide).
[INFO DRT-0036] FR_MASTERSLICE guide region query size = 0.
[INFO DRT-0036] FR_VIA guide region query size = 0.
[INFO DRT-0036] li1 guide region query size = 726.
[INFO DRT-0036] mcon guide region query size = 0.
[INFO DRT-0036] met1 guide region query size = 554.
[INFO DRT-0036] via guide region query size = 0.
[INFO DRT-0036] met2 guide region query size = 318.
[INFO DRT-0036] via2 guide region query size = 0.
[INFO DRT-0036] met3 guide region query size = 60.
[INFO DRT-0036] via3 guide region query size = 0.
[INFO DRT-0036] met4 guide region query size = 2.
[INFO DRT-0036] via4 guide region query size = 0.
[INFO DRT-0036] met5 guide region query size = 0.
[INFO DRT-0179] Init gr pin query.
[INFO DRT-0245] skipped writing guide updates to database.
[INFO DRT-0185] Post process initialize RPin region query.
[INFO DRT-0181] Start track assignment.
[INFO DRT-0184] Done with 1046 vertical wires in 1 frboxes and 614 horizontal wires in 1 frboxes.
[INFO DRT-0186] Done with 94 vertical wires in 1 frboxes and 133 horizontal wires in 1 frboxes.
[INFO DRT-0182] Complete track assignment.
[INFO DRT-0267] cpu time = 00:00:00, elapsed time = 00:00:00, memory = 120.84 (MB), peak = 255.95 (MB)
[INFO DRT-0187] Start routing data preparation.
[INFO DRT-0267] cpu time = 00:00:00, elapsed time = 00:00:00, memory = 120.84 (MB), peak = 255.95 (MB)
[INFO DRT-0194] Start detail routing.
[INFO DRT-0195] Start 0th optimization iteration.
Completing 10% with 0 violations.
elapsed time = 00:00:01, memory = 128.92 (MB).
Completing 20% with 15 violations.
elapsed time = 00:00:02, memory = 137.73 (MB).
Completing 30% with 30 violations.
elapsed time = 00:00:04, memory = 150.62 (MB).
Completing 40% with 52 violations.
elapsed time = 00:00:05, memory = 150.62 (MB).
[INFO DRT-0199]   Number of violations = 83.
Viol/Layer         li1   met1   met2
Metal Spacing        2     23      1
Recheck              1      8      6
Short                0     28     14
[INFO DRT-0267] cpu time = 00:00:05, elapsed time = 00:00:06, memory = 496.67 (MB), peak = 496.67 (MB)
Total wire length = 6947 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 2752 um.
Total wire length on LAYER met2 = 3178 um.
Total wire length on LAYER met3 = 945 um.
Total wire length on LAYER met4 = 70 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 2024.
Up-via summary (total 2024):

-----------------------
FR_MASTERSLICE       0
li1     979
met1     980
met2      61
met3       4
met4       0
-----------------------
2024


[INFO DRT-0195] Start 1st optimization iteration.
Completing 10% with 83 violations.
elapsed time = 00:00:00, memory = 496.67 (MB).
Completing 20% with 83 violations.
elapsed time = 00:00:00, memory = 496.67 (MB).
Completing 30% with 83 violations.
elapsed time = 00:00:01, memory = 501.62 (MB).
Completing 40% with 76 violations.
elapsed time = 00:00:01, memory = 501.62 (MB).
Completing 50% with 76 violations.
elapsed time = 00:00:01, memory = 501.62 (MB).
Completing 60% with 50 violations.
elapsed time = 00:00:02, memory = 501.62 (MB).
[INFO DRT-0199]   Number of violations = 7.
Viol/Layer        met1   met2
Metal Spacing        4      1
Recheck              2      0
[INFO DRT-0267] cpu time = 00:00:03, elapsed time = 00:00:02, memory = 501.62 (MB), peak = 501.62 (MB)
Total wire length = 6858 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 2719 um.
Total wire length on LAYER met2 = 3127 um.
Total wire length on LAYER met3 = 941 um.
Total wire length on LAYER met4 = 70 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 1990.
Up-via summary (total 1990):

-----------------------
FR_MASTERSLICE       0
li1     978
met1     945
met2      63
met3       4
met4       0
-----------------------
1990


[INFO DRT-0195] Start 2nd optimization iteration.
Completing 10% with 7 violations.
elapsed time = 00:00:00, memory = 501.62 (MB).
Completing 20% with 7 violations.
elapsed time = 00:00:00, memory = 501.62 (MB).
Completing 30% with 7 violations.
```

```
elapsed time = 00:00:00, memory = 501.62 (MB).
Completing 40% with 7 violations.
elapsed time = 00:00:00, memory = 501.62 (MB).
Completing 50% with 7 violations.
elapsed time = 00:00:00, memory = 501.62 (MB).
Completing 60% with 7 violations.
elapsed time = 00:00:00, memory = 501.62 (MB).
Completing 70% with 7 violations.
elapsed time = 00:00:00, memory = 501.62 (MB).
Completing 80% with 7 violations.
elapsed time = 00:00:00, memory = 501.62 (MB).
Completing 90% with 2 violations.
elapsed time = 00:00:02, memory = 501.62 (MB).
Completing 100% with 2 violations.
elapsed time = 00:00:02, memory = 501.62 (MB).
[INFO DRT-0199]   Number of violations = 2.
Viol/Layer        met1   met2
Metal Spacing        1      1
[INFO DRT-0267] cpu time = 00:00:02, elapsed time = 00:00:02, memory = 501.62 (MB), peak = 501.62 (MB)
Total wire length = 6841 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 2705 um.
Total wire length on LAYER met2 = 3122 um.
Total wire length on LAYER met3 = 942 um.
Total wire length on LAYER met4 = 70 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 1987.
Up-via summary (total 1987):

-----------------------
FR_MASTERSLICE       0
li1     978
met1     942
met2      63
met3       4
met4       0
-----------------------
1987


[INFO DRT-0195] Start 3rd optimization iteration.
Completing 10% with 2 violations.
elapsed time = 00:00:00, memory = 501.62 (MB).
Completing 20% with 0 violations.
elapsed time = 00:00:00, memory = 501.62 (MB).
Completing 30% with 0 violations.
elapsed time = 00:00:00, memory = 501.62 (MB).
Completing 40% with 0 violations.
elapsed time = 00:00:00, memory = 501.62 (MB).
[INFO DRT-0199]   Number of violations = 0.
[INFO DRT-0267] cpu time = 00:00:00, elapsed time = 00:00:00, memory = 501.62 (MB), peak = 501.62 (MB)
Total wire length = 6835 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 2696 um.
Total wire length on LAYER met2 = 3125 um.
Total wire length on LAYER met3 = 942 um.
Total wire length on LAYER met4 = 70 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 1988.
Up-via summary (total 1988):

-----------------------
FR_MASTERSLICE       0
li1     978
met1     943
met2      63
met3       4
met4       0
-----------------------
1988


[INFO DRT-0198] Complete detail routing.
Total wire length = 6835 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 2696 um.
Total wire length on LAYER met2 = 3125 um.
Total wire length on LAYER met3 = 942 um.
Total wire length on LAYER met4 = 70 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 1988.
Up-via summary (total 1988):

-----------------------
FR_MASTERSLICE       0
li1     978
met1     943
met2      63
met3       4
met4       0
-----------------------
```

Start coding or generate with AI.

Double-click (or enter) to edit

```
display(drt)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[14:47:52] VERBOSE  Running 'KLayout.Render'…                                                    step.py:1088
[14:47:52] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_pd97p_9_/klayout-render.log…  step.py:1268
```

Time Elapsed: 25.90s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Fill Insertion

Finally, as we're done placing all the essential cells, the only thing left to do is fill in the gaps.

We prioritize the use of decap (decoupling capacitor) cells, which further supports the power distribution network, but when there aren't any small enough cells, we just use regular fill cells.

```
FillInsertion = Step.factory.get("OpenROAD.FillInsertion")
fill = FillInsertion(state_in=drt.state_out)
fill.start()
```

```
──────────────────────────────────────────────────────── Fill Insertion ────────────────────────────────────────────────────────
[14:47:53] VERBOSE  Running 'OpenROAD.FillInsertion'…                                                          step.py:1088
[14:47:53] VERBOSE  Logging subprocess to                                                                      step.py:1268
                    openlane_run/11-openroad-fillinsertion/openroad-fillinsertion.log…
Reading OpenROAD database at '/content/openlane_run/10-openroad-detailedrouting/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:47:53] WARNING  [STA-0366] port 'clk' not found.                                                        openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:47:53] WARNING  [STA-0366] port 'clk' not found.                                                        openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:47:53] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                      openroad.py:235
[INFO] Setting timing derate to: 5%
[14:47:53] WARNING  [STA-0450] virtual clock clk can not be propagated.                                     openroad.py:235
sky130_ef_sc_hd__decap_12 sky130_fd_sc_hd__decap_8 sky130_fd_sc_hd__decap_6 sky130_fd_sc_hd__decap_4
sky130_fd_sc_hd__decap_3 sky130_fd_sc_hd__fill*
[INFO DPL-0001] Placed 362 filler instances.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/11-openroad-fillinsertion/SISO.odb'…
Writing netlist to '/content/openlane_run/11-openroad-fillinsertion/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/11-openroad-fillinsertion/SISO.pnl.v'…
Writing layout to '/content/openlane_run/11-openroad-fillinsertion/SISO.def'…
Writing timing constraints to '/content/openlane_run/11-openroad-fillinsertion/SISO.sdc'…
```

Format	Path
nl	openlane_run/11-openroad-fillinsertion/SISO.nl.v
pnl	openlane_run/11-openroad-fillinsertion/SISO.pnl.v
def	openlane_run/11-openroad-fillinsertion/SISO.def
odb	openlane_run/11-openroad-fillinsertion/SISO.odb

```
display(fill)
```

```
──────────────────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────────────────
[14:47:53] VERBOSE  Running 'KLayout.Render'…                                                                  step.py:1088
[14:47:53] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_8kqpu82f/klayout-render.log…            step.py:1268
```

Time Elapsed: 0.93s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Parasitics Extraction a.k.a. Resistance/Capacitance Extraction (RCX)

This step does not alter the design- rather, it computes the Parasitic elements of the circuit, which have an effect of timing, as we prepare to do the final timing analysis.

The parasitic elements are saved in the **Standard Parasitics Exchange Format**, or SPEF. OpenLane creates a SPEF file for each interconnect corner as described in the Corners and STA section of the documentation.

```
RCX = Step.factory.get("OpenROAD.RCX")

rcx = RCX(state_in=fill.state_out)
rcx.start()
```

```
─────────────────────────────── Parasitic Resistance/Capacitance Extraction ───────────────────────────────
[14:47:54] VERBOSE  Running 'OpenROAD.RCX'…                                                    step.py:1088
[14:47:54] INFO     Running RCX for corners matching min_*                                   openroad.py:1748
                    (/content/openlane_run/12-openroad-rcx/min/rcx.log)…
[14:47:54] INFO     Running RCX for corners matching nom_*                                   openroad.py:1748
                    (/content/openlane_run/12-openroad-rcx/nom/rcx.log)…
[14:47:55] VERBOSE  Logging subprocess to openlane_run/12-openroad-rcx/min/rcx.log…             step.py:1268
[14:47:55] VERBOSE  Logging subprocess to openlane_run/12-openroad-rcx/nom/rcx.log…             step.py:1268
[14:47:56] INFO     Finished RCX for corners matching min_*.                                 openroad.py:1757
[14:47:56] INFO     Running RCX for corners matching max_*                                   openroad.py:1748
                    (/content/openlane_run/12-openroad-rcx/max/rcx.log)…
[14:47:56] VERBOSE  Logging subprocess to openlane_run/12-openroad-rcx/max/rcx.log…             step.py:1268
[14:47:56] INFO     Finished RCX for corners matching nom_*.                                 openroad.py:1757
[14:47:56] INFO     Finished RCX for corners matching max_*.                                 openroad.py:1757
```

Format	Path
nl	openlane_run/11-openroad-fillinsertion/SISO.nl.v
pnl	openlane_run/11-openroad-fillinsertion/SISO.pnl.v
def	openlane_run/11-openroad-fillinsertion/SISO.def
odb	openlane_run/11-openroad-fillinsertion/SISO.odb
sdc	openlane_run/11-openroad-fillinsertion/SISO.sdc
spef	nom_* openlane_run/12-openroad-rcx/nom/SISO.nom.spef min_* openlane_run/12-openroad-rcx/min/SISO.min.spef max_* openlane_run/12-openroad-rcx/max/SISO.max.spef

Static Timing Analysis (Post-PnR)

STA is a process that verifies that a chip meets certain constraints on clock and data timings to run at its rated clock speed. See Corners and STA in the documentation for more info.

This step generates two kinds of files:

- `.lib` : Liberty™-compatible Library files. Can be used to do static timing analysis when creating a design with this design as a sub-macro.
- `.sdf` : Standard Delay Format. Can be used with certain simulation software to do *dynamic* timing analysis.

Unfortunately, the `.lib` files coming out of OpenLane right now are not super reliable for timing purposes and are only provided for completeness. When using OpenLane-created macros withing other designs, it is best to use the macro's final netlist and extracted parasitics instead.

```
STAPostPNR = Step.factory.get("OpenROAD.STAPostPNR")

sta_post_pnr = STAPostPNR(state_in=rcx.state_out)
sta_post_pnr.start()
```

```
──────────────────────────────────────── Static Timing Analysis (Post-PnR) ────────────────────────────────────────
[14:47:57] VERBOSE  Running 'OpenROAD.STAPostPNR'…                                                   step.py:1088
[14:47:57] INFO     Starting STA for the nom_tt_025C_1v80 timing corner…                           openroad.py:561
[14:47:57] INFO     Starting STA for the nom_ss_100C_1v60 timing corner…                           openroad.py:561
[14:47:57] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/nom_tt_025C_1v80/sta.log…
[14:47:57] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/nom_ss_100C_1v60/sta.log…
[14:47:58] INFO     Finished STA for the nom_ss_100C_1v60 timing corner.                           openroad.py:576
[14:47:58] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/nom_ss_100C_1v60/filter_unannotated.log…
[14:47:59] INFO     Finished STA for the nom_tt_025C_1v80 timing corner.                           openroad.py:576
[14:47:59] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/nom_tt_025C_1v80/filter_unannotated.log…
[14:48:00] INFO     Starting STA for the nom_ff_n40C_1v95 timing corner…                           openroad.py:561
[14:48:00] INFO     Starting STA for the min_tt_025C_1v80 timing corner…                           openroad.py:561
[14:48:00] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/min_tt_025C_1v80/sta.log…
[14:48:00] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/nom_ff_n40C_1v95/sta.log…
[14:48:01] INFO     Finished STA for the min_tt_025C_1v80 timing corner.                           openroad.py:576
[14:48:01] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/min_tt_025C_1v80/filter_unannotated.log…
[14:48:02] INFO     Finished STA for the nom_ff_n40C_1v95 timing corner.                           openroad.py:576
[14:48:02] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/nom_ff_n40C_1v95/filter_unannotated.log…
[14:48:02] INFO     Starting STA for the min_ss_100C_1v60 timing corner…                           openroad.py:561
[14:48:02] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/min_ss_100C_1v60/sta.log…
[14:48:03] INFO     Starting STA for the min_ff_n40C_1v95 timing corner…                           openroad.py:561
[14:48:03] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/min_ff_n40C_1v95/sta.log…
[14:48:04] INFO     Finished STA for the min_ss_100C_1v60 timing corner.                           openroad.py:576
[14:48:04] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/min_ss_100C_1v60/filter_unannotated.log…
[14:48:05] INFO     Starting STA for the max_tt_025C_1v80 timing corner…                           openroad.py:561
[14:48:05] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/max_tt_025C_1v80/sta.log…
[14:48:06] INFO     Finished STA for the min_ff_n40C_1v95 timing corner.                           openroad.py:576
[14:48:06] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/min_ff_n40C_1v95/filter_unannotated.log…
[14:48:06] INFO     Finished STA for the max_tt_025C_1v80 timing corner.                           openroad.py:576
[14:48:06] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/max_tt_025C_1v80/filter_unannotated.log…
[14:48:07] INFO     Starting STA for the max_ss_100C_1v60 timing corner…                           openroad.py:561
[14:48:07] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/max_ss_100C_1v60/sta.log…
[14:48:07] INFO     Starting STA for the max_ff_n40C_1v95 timing corner…                           openroad.py:561
[14:48:07] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/max_ff_n40C_1v95/sta.log…
[14:48:08] INFO     Finished STA for the max_ss_100C_1v60 timing corner.                           openroad.py:576
[14:48:08] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/max_ss_100C_1v60/filter_unannotated.log…
[14:48:11] INFO     Finished STA for the max_ff_n40C_1v95 timing corner.                           openroad.py:576
[14:48:11] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/13-openroad-stapostpnr/max_ff_n40C_1v95/filter_unannotated.log…
```

Corner/Group	Hold Worst Slack	Reg to Reg Paths	Hold TNS	Hold Vio Count	of whi… reg to reg	Setup Worst Slack	Reg to Reg Pat…	Setup TNS	Set… Vio Cou…	of which reg to reg	Max Cap Vio…	Max Slew Viol…
Overall	4.02…	N/A	0.0…	0	0	-2.4…	N/A	-64.…	93	0	5	36
nom_tt_025C_1v80	4.18…	N/A	0.0…	0	0	1.72…	N/A	0.00…	0	0	0	36
nom_ss_100C_1v60	4.59…	N/A	0.0…	0	0	-2.3…	N/A	-62.…	31	0	5	36
nom_ff_n40C_1v95	4.02…	N/A	0.0…	0	0	3.26…	N/A	0.00…	0	0	0	4
min_tt_025C_1v80	4.17…	N/A	0.0…	0	0	1.76…	N/A	0.00…	0	0	0	36
min_ss_100C_1v60	4.58…	N/A	0.0…	0	0	-2.2…	N/A	-60.…	31	0	3	36
min_ff_n40C_1v95	4.02…	N/A	0.0…	0	0	3.29…	N/A	0.00…	0	0	0	2
max_tt_025C_1v80	4.18…	N/A	0.0…	0	0	1.68…	N/A	0.00…	0	0	0	36
max_ss_100C_1v60	4.60…	N/A	0.0…	0	0	-2.4…	N/A	-64.…	31	0	5	36
max_ff_n40C_1v95	4.03…	N/A	0.0…	0	0	3.23…	N/A	0.00…	0	0	0	4

Corner/Group	Hold Worst Slack	Reg to Reg Paths	Hold TNS	Hold Vio Count	of which reg to reg	Setup Worst Slack	Reg to Reg Paths	Setup TNS	Setup Vio Count	of which reg to reg	Max Cap Violatio…	Max Slew Violati…
Overall	4.0245	N/A	0.0000	0	0	-2.4145	N/A	-64.1156	93	0	5	36
nom_tt_025C_1v80	4.1817	N/A	0.0000	0	0	1.7292	N/A	0.0000	0	0	0	36
nom_ss_100C_1v60	4.5913	N/A	0.0000	0	0	-2.3454	N/A	-62.0659	31	0	5	36
nom_ff_n40C_1v95	4.0279	N/A	0.0000	0	0	3.2657	N/A	0.0000	0	0	0	4
min_tt_025C_1v80	4.1751	N/A	0.0000	0	0	1.7661	N/A	0.0000	0	0	0	36
min_ss_100C_1v60	4.5837	N/A	0.0000	0	0	-2.2977	N/A	-60.4811	31	0	3	36
min_ff_n40C_1v95	4.0245	N/A	0.0000	0	0	3.2913	N/A	0.0000	0	0	0	2
max_tt_025C_1v80	4.1888	N/A	0.0000	0	0	1.6889	N/A	0.0000	0	0	0	36
max_ss_100C_1v60	4.6011	N/A	0.0000	0	0	-2.4145	N/A	-64.1156	31	0	5	36
max_ff_n40C_1v95	4.0325	N/A	0.0000	0	0	3.2373	N/A	0.0000	0	0	0	4

Format	Path	
nl	openlane_run/11-openroad-fillinsertion/SISO.nl.v	
pnl	openlane_run/11-openroad-fillinsertion/SISO.pnl.v	
def	openlane_run/11-openroad-fillinsertion/SISO.def	
odb	openlane_run/11-openroad-fillinsertion/SISO.odb	
sdc	openlane_run/11-openroad-fillinsertion/SISO.sdc	
sdf	nom_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/nom_tt_025C_1v80/SISO__nom_tt_025C_1v80.sdf
	nom_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/nom_ss_100C_1v60/SISO__nom_ss_100C_1v60.sdf
	nom_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/nom_ff_n40C_1v95/SISO__nom_ff_n40C_1v95.sdf
	min_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/min_tt_025C_1v80/SISO__min_tt_025C_1v80.sdf
	min_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/min_ss_100C_1v60/SISO__min_ss_100C_1v60.sdf
	min_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/min_ff_n40C_1v95/SISO__min_ff_n40C_1v95.sdf
	max_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/max_tt_025C_1v80/SISO__max_tt_025C_1v80.sdf
	max_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/max_ss_100C_1v60/SISO__max_ss_100C_1v60.sdf
	max_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/max_ff_n40C_1v95/SISO__max_ff_n40C_1v95.sdf
spef	nom_*	openlane_run/12-openroad-rcx/nom/SISO.nom.spef
	min_*	openlane_run/12-openroad-rcx/min/SISO.min.spef
	max_*	openlane_run/12-openroad-rcx/max/SISO.max.spef
lib	nom_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/nom_tt_025C_1v80/SISO__nom_tt_025C_1v80.lib
	nom_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/nom_ss_100C_1v60/SISO__nom_ss_100C_1v60.lib
	nom_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/nom_ff_n40C_1v95/SISO__nom_ff_n40C_1v95.lib
	min_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/min_tt_025C_1v80/SISO__min_tt_025C_1v80.lib
	min_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/min_ss_100C_1v60/SISO__min_ss_100C_1v60.lib

Stream-out

Stream-out is the process of converting the designs from the abstract formats using during floorplanning, placement and routing into a concrete format called GDSII (lit. Graphic Design System 2), which is the final file that is then sent for fabrication.

```
StreamOut = Step.factory.get("KLayout.StreamOut")

gds = StreamOut(state_in=sta_post_pnr.state_out)
gds.start()
```

```
──────────────────────────────────────── GDSII Stream Out (KLayout) ────────────────────────────────────────
[14:48:12] VERBOSE  Running 'KLayout.StreamOut'…                                                  step.py:1088
[14:48:12] VERBOSE  Logging subprocess to openlane_run/14-klayout-streamout/klayout-streamout.log…  step.py:1268
[INFO] Clearing cells…
[INFO] Merging GDS files…
[INFO] Copying top level cell 'SISO'…
[INFO] Checking for missing GDS…
[INFO] All LEF cells have matching GDS cells.
[INFO] Writing out GDS '/content/openlane_run/14-klayout-streamout/SISO.klayout.gds'…
[INFO] Done.
```

Format	Path	
nl	openlane_run/11-openroad-fillinsertion/SISO.nl.v	
pnl	openlane_run/11-openroad-fillinsertion/SISO.pnl.v	
def	openlane_run/11-openroad-fillinsertion/SISO.def	
odb	openlane_run/11-openroad-fillinsertion/SISO.odb	
sdc	openlane_run/11-openroad-fillinsertion/SISO.sdc	
sdf	nom_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/nom_tt_025C_1v80/SISO__nom_tt_025C_1v80.sdf
	nom_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/nom_ss_100C_1v60/SISO__nom_ss_100C_1v60.sdf
	nom_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/nom_ff_n40C_1v95/SISO__nom_ff_n40C_1v95.sdf
	min_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/min_tt_025C_1v80/SISO__min_tt_025C_1v80.sdf
	min_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/min_ss_100C_1v60/SISO__min_ss_100C_1v60.sdf
	min_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/min_ff_n40C_1v95/SISO__min_ff_n40C_1v95.sdf
	max_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/max_tt_025C_1v80/SISO__max_tt_025C_1v80.sdf
	max_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/max_ss_100C_1v60/SISO__max_ss_100C_1v60.sdf
	max_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/max_ff_n40C_1v95/SISO__max_ff_n40C_1v95.sdf
spef	nom_*	openlane_run/12-openroad-rcx/nom/SISO.nom.spef
	min_*	openlane_run/12-openroad-rcx/min/SISO.min.spef
	max_*	openlane_run/12-openroad-rcx/max/SISO.max.spef
lib	nom_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/nom_tt_025C_1v80/SISO__nom_tt_025C_1v80.lib
	nom_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/nom_ss_100C_1v60/SISO__nom_ss_100C_1v60.lib
	nom_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/nom_ff_n40C_1v95/SISO__nom_ff_n40C_1v95.lib
	min_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/min_tt_025C_1v80/SISO__min_tt_025C_1v80.lib
	min_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/min_ss_100C_1v60/SISO__min_ss_100C_1v60.lib
	min_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/min_ff_n40C_1v95/SISO__min_ff_n40C_1v95.lib
	max_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/max_tt_025C_1v80/SISO__max_tt_025C_1v80.lib
	max_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/max_ss_100C_1v60/SISO__max_ss_100C_1v60.lib
	max_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/max_ff_n40C_1v95/SISO__max_ff_n40C_1v95.lib
gds	openlane_run/14-klayout-streamout/SISO.gds	
klayout_gds	openlane_run/14-klayout-streamout/SISO.klayout.gds	

```
display(gds)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[14:48:13] VERBOSE  Running 'KLayout.Render'…                                                   step.py:1088
[14:48:13] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_eh6yd3h5/klayout-render.log…  step.py:1268
```

Time Elapsed: 0.62s

Views updated:

- GDSII Stream
- GDSII Stream (KLayout)

Preview:

Design Rule Checks (DRC)

DRC determines that the final layout does not violate any of the rules set by the foundry to ensure the design is actually manufacturable- for example, not enough space between two wires, *too much* space between tap cells, and so on.

A design not passing DRC will typically be rejected by the foundry, who also run DRC on their side.

```
DRC = Step.factory.get("Magic.DRC")

drc = DRC(state_in=gds.state_out)
drc.start()
```

```
──────────────────────────────────────────────────────── Design Rule Checks ────────────────────────────────────────────────────────
[14:48:14] VERBOSE  Running 'Magic.DRC'…                                                                                  step.py:1088
[14:48:14] VERBOSE  Logging subprocess to openlane_run/15-magic-drc/magic-drc.log…                                         step.py:1268

Magic 8.3 revision 483 - Compiled on Sun Jun  2 18:57:41 UTC 2024.
Starting magic under Tcl interpreter
Using the terminal as the console.
Using NULL graphics device.
Processing system .magicrc file
Sourcing design .magicrc for technology sky130A ...
2 Magic internal units = 1 Lambda
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
ubm
Scaled tech values by 2 / 1 to match internal grid scaling
Loading sky130A Device Generator Menu ...
Loading "/content/openlane_ipynb/openlane/scripts/magic/wrapper.tcl" from command line.
Warning: Calma reading is not undoable!  I hope that's OK.
Library written using GDS-II Release 6.0
Library name: LIB
Reading "VIA_M3M4_PR".
Reading "VIA_M2M3_PR".
Reading "VIA_M1M2_PR_MR".
Reading "VIA_M1M2_PR".
Reading "VIA_L1M1_PR_MR".
Reading "VIA_via2_3_2000_480_1_6_320_320".
Reading "VIA_via3_4_2000_480_1_5_400_400".
Reading "VIA_via4_5_2000_480_1_5_400_400".
Reading "VIA_via5_6_2000_2000_1_1_1600_1600".
Reading "sky130_fd_sc_hd__buf_2".
Reading "sky130_fd_sc_hd__conb_1".
Reading "sky130_fd_sc_hd__nor4b_2".
Reading "sky130_fd_sc_hd__a211o_2".
Reading "sky130_fd_sc_hd__nor4_2".
Reading "sky130_fd_sc_hd__and4b_2".
Reading "sky130_fd_sc_hd__o2111a_2".
Reading "sky130_fd_sc_hd__and3b_2".
Reading "sky130_fd_sc_hd__nor3_2".
Reading "sky130_fd_sc_hd__a31oi_2".
Reading "sky130_fd_sc_hd__o221a_2".
Reading "sky130_fd_sc_hd__o31a_2".
Reading "sky130_fd_sc_hd__or4_2".
Reading "sky130_fd_sc_hd__nand3_2".
Reading "sky130_fd_sc_hd__a22o_2".
Reading "sky130_fd_sc_hd__nand4_2".
Reading "sky130_fd_sc_hd__o211a_2".
Reading "sky130_fd_sc_hd__o22a_2".
Reading "sky130_fd_sc_hd__o21bai_2".
Reading "sky130_fd_sc_hd__o2bb2a_2".
Reading "sky130_fd_sc_hd__a2111o_2".
Reading "sky130_fd_sc_hd__a21bo_2".
Reading "sky130_fd_sc_hd__or3b_2".
Reading "sky130_fd_sc_hd__nand2b_2".
Reading "sky130_fd_sc_hd__a22oi_2".
Reading "sky130_fd_sc_hd__a21o_2".
Reading "sky130_fd_sc_hd__a21boi_2".
Reading "sky130_fd_sc_hd__o32a_2".
Reading "sky130_fd_sc_hd__or4b_2".
Reading "sky130_fd_sc_hd__a31o_2".
Reading "sky130_fd_sc_hd__and4bb_2".
Reading "sky130_fd_sc_hd__a221o_2".
Reading "sky130_fd_sc_hd__and4_2".
Reading "sky130_fd_sc_hd__o21a_2".
Reading "sky130_fd_sc_hd__and2b_2".
Reading "sky130_fd_sc_hd__o21ai_2".
Reading "sky130_fd_sc_hd__a32o_2".
Reading "sky130_fd_sc_hd__or3_2".
Reading "sky130_fd_sc_hd__nor2_2".
Reading "sky130_fd_sc_hd__xnor2_2".
Reading "sky130_fd_sc_hd__xor2_2".
Reading "sky130_fd_sc_hd__a21oi_2".
Reading "sky130_fd_sc_hd__and3_2".
Reading "sky130_fd_sc_hd__and2_2".
Reading "sky130_fd_sc_hd__or2_2".
Reading "sky130_fd_sc_hd__nand2_2".
Reading "sky130_fd_sc_hd__inv_2".
Reading "sky130_fd_sc_hd__tapvpwrvgnd_1".
Reading "sky130_fd_sc_hd__decap_3".
Reading "sky130_fd_sc_hd__decap_8".
Reading "sky130_fd_sc_hd__decap_4".
Reading "sky130_ef_sc_hd__decap_12".
Reading "sky130_fd_sc_hd__decap_6".
Reading "sky130_fd_sc_hd__fill_2".
Reading "sky130_fd_sc_hd__fill_1".
Reading "SISO".
[INFO] Loading SISO

DRC style is now "drc(full)"
Loading DRC CIF style.
No errors found.
[INFO] COUNT: 0
[INFO] Should be divided by 3 or 4
[INFO] DRC Checking DONE (/content/openlane_run/15-magic-drc/reports/drc_violations.magic.rpt)
[INFO] Saving mag view with DRC errors (/content/openlane_run/15-magic-drc/views/SISO.drc.mag)
[INFO] Saved
```

Format	Path	
nl	openlane_run/11-openroad-fillinsertion/SISO.nl.v	
pnl	openlane_run/11-openroad-fillinsertion/SISO.pnl.v	
def	openlane_run/11-openroad-fillinsertion/SISO.def	
odb	openlane_run/11-openroad-fillinsertion/SISO.odb	
sdc	openlane_run/11-openroad-fillinsertion/SISO.sdc	
sdf	nom_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/nom_tt_025C_1v80/SISO__nom_tt_025C_1v80.sdf
	nom_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/nom_ss_100C_1v60/SISO__nom_ss_100C_1v60.sdf
	nom_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/nom_ff_n40C_1v95/SISO__nom_ff_n40C_1v95.sdf
	min_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/min_tt_025C_1v80/SISO__min_tt_025C_1v80.sdf
	min_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/min_ss_100C_1v60/SISO__min_ss_100C_1v60.sdf
	min_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/min_ff_n40C_1v95/SISO__min_ff_n40C_1v95.sdf
	max_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/max_tt_025C_1v80/SISO__max_tt_025C_1v80.sdf
	max_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/max_ss_100C_1v60/SISO__max_ss_100C_1v60.sdf
	max_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/max_ff_n40C_1v95/SISO__max_ff_n40C_1v95.sdf
spef	nom_*	openlane_run/12-openroad-rcx/nom/SISO.nom.spef
	min_*	openlane_run/12-openroad-rcx/min/SISO.min.spef
	max_*	openlane_run/12-openroad-rcx/max/SISO.max.spef
lib	nom_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/nom_tt_025C_1v80/SISO__nom_tt_025C_1v80.lib
	nom_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/nom_ss_100C_1v60/SISO__nom_ss_100C_1v60.lib
	nom_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/nom_ff_n40C_1v95/SISO__nom_ff_n40C_1v95.lib
	min_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/min_tt_025C_1v80/SISO__min_tt_025C_1v80.lib
	min_ss_100C_1v60	openlane_run/13-openroad-stapostpnr/min_ss_100C_1v60/SISO__min_ss_100C_1v60.lib
	min_ff_n40C_1v95	openlane_run/13-openroad-stapostpnr/min_ff_n40C_1v95/SISO__min_ff_n40C_1v95.lib
	max_tt_025C_1v80	openlane_run/13-openroad-stapostpnr/max_tt_025C_1v80/SISO__max_tt_025C_1v80.lib

SPICE Extraction for Layout vs. Schematic Check

This step tries to reconstruct a SPICE netlist from the GDSII file, so it can later be used for the **Layout vs. Schematic** (LVS) check.

```
SpiceExtraction = Step.factory.get("Magic.SpiceExtraction")

spx = SpiceExtraction(state_in=drc.state_out)
spx.start()
```

```
──────────────────────────────────────────── SPICE Model Extraction ────────────────────────────────────────────
[14:48:16] VERBOSE  Running 'Magic.SpiceExtraction'…                                                  step.py:1088
[14:48:16] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/16-magic-spiceextraction/magic-spiceextraction.log…

Magic 8.3 revision 483 - Compiled on Sun Jun  2 18:57:41 UTC 2024.
Starting magic under Tcl interpreter
Using the terminal as the console.
Using NULL graphics device.
Processing system .magicrc file
Sourcing design .magicrc for technology sky130A ...
2 Magic internal units = 1 Lambda
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
ubm
Scaled tech values by 2 / 1 to match internal grid scaling
Loading sky130A Device Generator Menu ...
Loading "/content/openlane_ipynb/openlane/scripts/magic/wrapper.tcl" from command line.
> lef read /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef
Reading LEF data from file /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef.
This action cannot be undone.
LEF read, Line 78 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 79 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 112 (Message): Unknown keyword "MINENCLOSEDAREA" in LEF file; ignoring.
LEF read, Line 114 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 115 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 121 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 122 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 123 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 156 (Message): Unknown keyword "MINENCLOSEDAREA" in LEF file; ignoring.
LEF read, Line 164 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 165 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 167 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 168 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 169 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 206 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 207 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 209 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 210 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 211 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 248 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 249 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 251 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 252 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 253 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 290 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 291 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read: Processed 797 lines.
```

Layout vs. Schematic (LVS)

A comparison between the final Verilog netlist (from PnR) and the final SPICE netlist (extracted.)

This check effectively compares the physically implemented circuit to the final Verilog netlist output by OpenROAD.

The idea is, if there are any disconnects, shorts or other mismatches in the physical implementation that do not exist in the logical view of the design, they would be caught at this step.

Common issues that result in LVS violations include:

Open in Colab

Task : 2 - Single Input, Multiple Output (SIMO)

Avinash Baraiya- 202201211

Malhar Vaghasiya - 202201183

Smeet Agrawal - 202101237

Priyesh Tandel - 202101222

Samarth Panchal- 202101456

OpenLane Colab

This Google Colab notebook will:

- Install OpenLane and its dependencies
- Run a simple design, namely a serial-parallel multiplier, through the flow and targeting the open source sky130 PDK by Google and Skywater.

Setup Nix

Nix is a package manager with an emphasis on reproducible builds, and it is the primary method for installing OpenLane 2.

This step installs the Nix package manager and enables the experimental "flakes" feature.

If you're not in a Colab, this just sets the environment variables. You will need to install Nix and enable flakes on your own following this guide.

Show code

Get OpenLane

Click the ▷ button to download and install OpenLane.

This will install OpenLane's tool dependencies using Nix, and OpenLane itself using PIP.

Note that `python3-tk` may need to be installed using your OS's package manager.

openlane_version: "version-2.1"

pdk_root: "~/.volare"

pdk: "sky130"

Show code

Downloading OpenLane…

```
  % Total    % Received % Xferd  Average Speed   Time    Time     Time  Current
                                 Dload  Upload   Total   Spent    Left  Speed
  0     0    0     0    0     0      0      0 --:--:-- --:--:-- --:--:--     0
100 9491k    0 9491k    0     0  7352k      0 --:--:--  0:00:01 --:--:-- 13.2M
```

Downloading OpenLane's dependencies…

Downloading Python dependencies using PIP…

Downloading PDK…

```
Version bdc9412b3e468c102d01b7cf6337be06ec6e9c9a enabled for the sky130 PDK.
```

Done.

```
import openlane

print(openlane.__version__)
```

```
2.1.11
```

Creating the design

Now that OpenLane is set up, we can write a Verilog file as follows:

```
%%writefile SIMO.v

module SIMO(
    input [31:0] x,            // Single input
    output [63:0] y1,          // First output
    output [63:0] y2,          // Second output
    output [63:0] y3           // Third output
);

    // Weight declaration
    reg [3:0] w [2:0];

    // Intermediate outputs from neuron modules
    wire [63:0] o1, o2, o3;

    // ReLU outputs
    wire [63:0] out1, out2, out3;

    // Initialize weights
    initial begin
        w[0] = 4'b0001;   // Weight for y1
        w[1] = 4'b0111;   // Weight for y2
        w[2] = 4'b0011;   // Weight for y3
    end

    // Instantiate neuron modules for each output
    neuron n1 (.out_neuron(o1), .input_neuron(x), .weight_value(w[0]));
    neuron n2 (.out_neuron(o2), .input_neuron(x), .weight_value(w[1]));
```

```
    neuron n3 (.out_neuron(o3), .input_neuron(x), .weight_value(w[2]));

    // Apply ReLU activation to each neuron's output
    ReLU r1 (.in(o1), .out(out1));
    ReLU r2 (.in(o2), .out(out2));
    ReLU r3 (.in(o3), .out(out3));

    // Assign outputs
    assign y1 = out1;
    assign y2 = out2;
    assign y3 = out3;

endmodule

module neuron(
    output reg [63:0] out_neuron,
    input [31:0] input_neuron,
    input [3:0] weight_value
);

    // Bias constant
    wire [63:0] bias = 1;

    // Intermediate multiplication result
    reg [63:0] out_mul;

    // Compute neuron output
    always @(*) begin
        out_mul = weight_value * input_neuron;
        out_neuron = out_mul + bias;
    end

endmodule

module ReLU(
    input signed [63:0] in,
    output reg [63:0] out
);

    always @(*) begin
        if (in < 0) begin
            out = 0;
        end else begin
            out = in;
        end
    end

endmodule
```

```
Writing SIMO.v
```

Setting up the configuration

OpenLane requries you to configure any Flow before using it. This is done using the `config` module.

For colaboratories, REPLs and other interactive environments where there is no concrete Flow object, the Configuration may be initialized using `Config.interactive`, which will automatically propagate the configuration to any future steps.

You can find the documentation for `Config.interactive` here.

```
from openlane.config import Config

Config.interactive(
    "SISO",
    PDK="sky130A",
    CLOCK_PORT="clk",
    CLOCK_NET="clk",
    CLOCK_PERIOD=10,
    PRIMARY_GDSII_STREAMOUT_TOOL="klayout",
)
```

Interactive Configuration

Initial Values

```
CELL_BB_VERILOG_MODELS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/sky130_fd_sc_hd__blackbox.v
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/sky130_fd_sc_hd__blackbox_pp.v
CELL_GDS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/gds/sky130_fd_sc_hd.gds
CELL_LEFS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef
CELL_PAD_EXCLUDE:
- sky130_fd_sc_hd__tap*
- sky130_fd_sc_hd__decap*
- sky130_ef_sc_hd__decap*
- sky130_fd_sc_hd__fill*
CELL_SPICE_MODELS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__decap_12.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_12.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_4.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_8.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_fd_sc_hd.spice
CELL_VERILOG_MODELS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/primitives.v
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/sky130_fd_sc_hd.v
CLOCK_NET: clk
CLOCK_PERIOD: 10
CLOCK_PORT: clk
CLOCK_TRANSITION_CONSTRAINT: 0.15
CLOCK_UNCERTAINTY_CONSTRAINT: 0.25
CLOCK_WIRE_RC_LAYERS: null
DECAP_CELL:
- sky130_ef_sc_hd__decap_12
- sky130_fd_sc_hd__decap_8
- sky130_fd_sc_hd__decap_6
- sky130_fd_sc_hd__decap_4
- sky130_fd_sc_hd__decap_3
DEFAULT_CORNER: nom_tt_025C_1v80
DEFAULT_MAX_TRAN: null
DESIGN_DIR: .
DESIGN_NAME: SISO
DIE_AREA: null
DIODE_CELL: sky130_fd_sc_hd__diode_2/DIODE
ENDCAP_CELL: sky130_fd_sc_hd__decap_3
EXTRA_EXCLUDED_CELLS: null
EXTRA_GDS_FILES: null
EXTRA_LEFS: null
EXTRA_LIBS: null
EXTRA_SPICE_MODELS: null
EXTRA_VERILOG_MODELS: null
FALLBACK_SDC_FILE: /content/openlane_ipynb/openlane/scripts/base.sdc
FILL_CELL:
- sky130_fd_sc_hd__fill*
FP_IO_HLAYER: met3
FP_IO_VLAYER: met2
FP_TAPCELL_DIST: 13
FP_TRACKS_INFO: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tracks.info
GND_NETS: null
GND_PIN: VGND
GPIO_PADS_LEF:
- /root/.volare/sky130A/libs.ref/sky130_fd_io/lef/sky130_fd_io.lef
- /root/.volare/sky130A/libs.ref/sky130_fd_io/lef/sky130_ef_io.lef
GPIO_PADS_LEF_CORE_SIDE:
- /root/.volare/sky130A/libs.tech/openlane/custom_cells/lef/sky130_fd_io_core.lef
- /root/.volare/sky130A/libs.tech/openlane/custom_cells/lef/sky130_ef_io_core.lef
GPIO_PADS_VERILOG:
- /root/.volare/sky130A/libs.ref/sky130_fd_io/verilog/sky130_ef_io.v
GPIO_PAD_CELLS:
- sky130_fd_io*
- sky130_ef_io*
IO_DELAY_CONSTRAINT: 20
LIB:
  '*_ff_n40C_1v95':
  - /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ff_n40C_1v95.lib
  '*_ss_100C_1v60':
  - /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ss_100C_1v60.lib
  '*_tt_025C_1v80':
  - /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
MACROS: null
MAX_CAPACITANCE_CONSTRAINT: 0.2
MAX_FANOUT_CONSTRAINT: 10
MAX_TRANSITION_CONSTRAINT: 0.75
OUTPUT_CAP_LOAD: 33.442
PDK: sky130A
PDK_ROOT: /root/.volare
PLACE_SITE: unithd
PNR_EXCLUDED_CELL_FILE: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/drc_exclude.cells
PRIMARY_GDSII_STREAMOUT_TOOL: klayout
RT_MAX_LAYER: met5
RT_MIN_LAYER: met1
SCL_GROUND_PINS:
- VGND
- VNB
SCL_POWER_PINS:
- VPWR
- VPB
SIGNAL_WIRE_RC_LAYERS: null
STA_CORNERS:
- nom_tt_025C_1v80
- nom_ss_100C_1v60
- nom_ff_n40C_1v95
- min_tt_025C_1v80
- min_ss_100C_1v60
- min_ff_n40C_1v95
- max_tt_025C_1v80
- max_ss_100C_1v60
- max_ff_n40C_1v95
STD_CELL_LIBRARY: sky130_fd_sc_hd
SYNTH_BUFFER_CELL: sky130_fd_sc_hd__buf_2/A/X
SYNTH_CLK_DRIVING_CELL: null
SYNTH_DRIVING_CELL: sky130_fd_sc_hd__inv_2/Y
SYNTH_EXCLUDED_CELL_FILE: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/no_synth.cells
SYNTH_TIEHI_CELL: sky130_fd_sc_hd__conb_1/HI
SYNTH_TIELO_CELL: sky130_fd_sc_hd__conb_1/LO
TECH_LEFS:
  max_*: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__max.tlef
  min_*: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__min.tlef
  nom_*: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef
TIME_DERATING_CONSTRAINT: 5
TRISTATE_CELLS:
- sky130_fd_sc_hd__ebuf*
VDD_NETS: null
```

```
  VDD_PIN: VPWR
  VDD_PIN_VOLTAGE: 1.8
  WELLTAP_CELL: sky130_fd_sc_hd__tapvpwrvgnd_1
  WIRE_LENGTH_THRESHOLD: null
  meta:
    flow: null
    openlane_version: 2.1.11
    step: null
    substituting_steps: null
    version: 1
```

Running implementation steps

There are two ways to obtain OpenLane's built-in implementation steps:

- via directly importing from the `steps` module using its category:
  - `from openlane.steps import Yosys` then `Synthesis = Yosys.Synthesis`
- by using the step's id from the registry:
  - `from openlane.steps import Step` then `Synthesis = Step.factory.get("Yosys.Synthesis")`

You can find a full list of included steps here: https://openlane2.readthedocs.io/en/latest/reference/step_config_vars.html

```
from openlane.steps import Step
```

- First, get the step (and display its help)...

```
Synthesis = Step.factory.get("Yosys.Synthesis")

Synthesis.display_help()
```

(step-yosys-synthesis)=

Synthesis

```
Performs synthesis and technology mapping on Verilog RTL files
using Yosys and ABC, emitting a netlist.

Some metrics will also be extracted and updated, namely:

* ``design__instance__count``
* ``design__instance_unmapped__count``
* ``design__instance__area``
```

Importing

```
from openlane.steps.yosys import Synthesis

# or

from openlane.steps import Step

Synthesis = Step.factory.get("Yosys.Synthesis")
```

Inputs and Outputs

Inputs	Outputs
	Verilog Netlist (.nl.v)

(yosys.synthesis-configuration-variables)=

Configuration Variables

Variable Name	Type	Description	Default	Units
SYNTH_LATCH_MAP{#var-yosys-synthesis-synth_latch_map}^{PDK}	Path?	A path to a file containing the latch mapping for Yosys.	None	
SYNTH_TRISTATE_MAP{#var-yosys-synthesis-synth_tristate_map}^{PDK}	Path?	A path to a file containing the tri-state buffer mapping for Yosys.	None	
SYNTH_CSA_MAP{#var-yosys-synthesis-synth_csa_map}^{PDK}	Path?	A path to a file containing the carry-select adder mapping for Yosys.	None	
SYNTH_RCA_MAP{#var-yosys-synthesis-synth_rca_map}^{PDK}	Path?	A path to a file containing the ripple-carry adder mapping for Yosys.	None	
SYNTH_FA_MAP{#var-yosys-synthesis-synth_fa_map}^{PDK}	Path?	A path to a file containing the full adder mapping for Yosys.	None	
SYNTH_MUX_MAP{#var-yosys-synthesis-synth_mux_map}^{PDK}	Path?	A path to a file containing the mux mapping for Yosys.	None	
SYNTH_MUX4_MAP{#var-yosys-synthesis-synth_mux4_map}^{PDK}	Path?	A path to a file containing the mux4 mapping for Yosys.	None	
USE_LIGHTER{#var-yosys-synthesis-use_lighter}	bool	Activates Lighter, an experimental plugin that attempts to optimize clock-gated flip-flops.	False	
LIGHTER_DFF_MAP{#var-yosys-synthesis-lighter_dff_map}	Path?	An override to the custom DFF map file provided for the given SCL by Lighter.	None	
YOSYS_LOG_LEVEL{#var-yosys-synthesis-yosys_log_level}	'ALL' | 'WARNING' | 'ERROR'	Which log level for Yosys. At WARNING or higher, the initialization splash is also disabled.	ALL	
SYNTH_CHECKS_ALLOW_TRISTATE{#var-yosys-synthesis-synth_checks_allow_tristate}	bool	Ignore multiple-driver warnings if they are connected to tri-state buffers on a best-effort basis.	True	
SYNTH_AUTONAME{#var-yosys-synthesis-synth_autoname}	bool	Generates names for netlist instances. This results in instance names that can be extremely long, but are more human-readable.	False	
SYNTH_STRATEGY{#var-yosys-synthesis-synth_strategy}	'AREA 0' | 'AREA 1' | 'AREA 2' | 'AREA 3' | 'DELAY 0' | 'DELAY 1' | 'DELAY 2' | 'DELAY 3' | 'DELAY 4'	Strategies for abc logic synthesis and technology mapping. AREA strategies usually result in a more compact design, while DELAY strategies usually result in a design that runs at a higher frequency. Please note that there is no way to know which strategy is the best before trying them.	AREA 0	
SYNTH_ABC_BUFFERING{#var-yosys-synthesis-synth_abc_buffering}	bool	Enables `abc` cell buffering.	False	
SYNTH_ABC_LEGACY_REFACTOR{#var-yosys-synthesis-synth_abc_legacy_refactor}	bool	Replaces the ABC command `drf -l` with `refactor` which matches older versions of OpenLane but is more unstable.	False	
SYNTH_ABC_LEGACY_REWRITE{#var-yosys-synthesis-synth_abc_legacy_rewrite}	bool	Replaces the ABC command `drw -l` with `rewrite` which matches older versions of OpenLane but is more unstable.	False	
SYNTH_DIRECT_WIRE_BUFFERING{#var-yosys-synthesis-synth_direct_wire_buffering}	bool	Enables inserting buffer cells for directly connected wires.	True	
SYNTH_SPLITNETS{#var-yosys-synthesis-synth_splitnets}	bool	Splits multi-bit nets into single-bit nets. Easier to trace but may not be supported by all tools.	True	
SYNTH_SIZING{#var-yosys-synthesis-synth_sizing}	bool	Enables `abc` cell sizing (instead of buffering).	False	
SYNTH_NO_FLAT{#var-yosys-synthesis-synth_no_flat}	bool	A flag that disables flattening the hierarchy during synthesis, only flattening it after synthesis, mapping and optimizations.	False	
SYNTH_SHARE_RESOURCES{#var-yosys-synthesis-synth_share_resources}	bool	A flag that enables yosys to reduce the number of cells by determining shareable resources and merging them.	True	
SYNTH_ADDER_TYPE{#var-yosys-synthesis-synth_adder_type}	'YOSYS' | 'FA' | 'RCA' | 'CSA'	Adder type to which the $addand$sub operators are mapped to. Possible values are `YOSYS/FA/RCA/CSA`; where `YOSYS` refers to using Yosys internal adder definition, `FA` refers to full-adder structure, `RCA` refers to ripple carry adder structure, and `CSA` refers to carry select adder.	YOSYS	
SYNTH_EXTRA_MAPPING_FILE{#var-yosys-synthesis-synth_extra_mapping_file}	Path?	Points to an extra techmap file for yosys that runs right after yosys `synth` before generic techmap.	None	
SYNTH_PARAMETERS{#var-yosys-synthesis-synth_parameters}	List[str]?	Key-value pairs to be `chparam`ed in Yosys, in the format `key1=value1`.	None	
SYNTH_ELABORATE_ONLY{#var-yosys-synthesis-synth_elaborate_only}	bool	"Elaborate" the design only without attempting any logic mapping. Useful when dealing with structural Verilog netlists.	False	
SYNTH_ELABORATE_FLATTEN{#var-yosys-synthesis-synth_elaborate_flatten}	bool	If `SYNTH_ELABORATE_ONLY` is specified, this variable controls whether or not the top level should be flattened.	True	
VERILOG_FILES{#var-yosys-synthesis-verilog_files}	List[Path]	The paths of the design's Verilog files.	None	
VERILOG_DEFINES{#var-yosys-synthesis-verilog_defines}	List[str]?	Preprocessor defines for input Verilog files.	None	

VERILOG_POWER_DEFINE{#var-yosys-synthesis-verilog_power_define}	str	Specifies the name of the define used to guard power and ground connections in the input RTL.	USE_POWER_PINS
VERILOG_INCLUDE_DIRS{#var-yosys-synthesis-verilog_include_dirs}	List[str]?	Specifies the Verilog `include` directories.	None
USE_SYNLIG{#var-yosys-synthesis-use_synlig}	bool	Use the Synlig plugin to process files, which has better SystemVerilog parsing capabilities but may not be compatible with all Yosys commands and attributes.	False
SYNLIG_DEFER{#var-yosys-synthesis-synlig_defer}	bool	Uses -defer flag when reading files the Synlig plugin, which may improve performance by reading each file separately, but is experimental.	False

- Then run it. Note you can pass step-specific configs using Python keyword arguments.

Synthesis

We need to start by converting our high-level Verilog to one that just shows the connections between small silicon patterns called "standard cells" in process called Synthesis. We can do this by passing the Verilog files as a configuration variable to `Yosys.Synthesis` as follows, then running it.

As this is the first step, we need to create an empty state and pass it to it.

```
from openlane.state import State

synthesis = Synthesis(
    VERILOG_FILES=["./SISO.v"],
    state_in=State(),
)
synthesis.start()
```

```
──────────────────────────────────────────────────────── Synthesis ────────────────────────────────────────────────────────
[14:57:10] VERBOSE  Running 'Yosys.Synthesis'…                                                                  step.py:1088
[14:57:10] VERBOSE  Logging subprocess to openlane_run/18-yosys-synthesis/yosys-synthesis.log…                   step.py:1268

/-----------------------------------------------------------------------------\
|                                                                             |
|  yosys -- Yosys Open SYnthesis Suite                                        |
|                                                                             |
|  Copyright (C) 2012 - 2020  Claire Xenia Wolf <claire@yosyshq.com>          |
|                                                                             |
|  Permission to use, copy, modify, and/or distribute this software for any  |
|  purpose with or without fee is hereby granted, provided that the above    |
|  copyright notice and this permission notice appear in all copies.          |
|                                                                             |
|  THE SOFTWARE IS PROVIDED "AS IS" AND THE AUTHOR DISCLAIMS ALL WARRANTIES  |
|  WITH REGARD TO THIS SOFTWARE INCLUDING ALL IMPLIED WARRANTIES OF           |
|  MERCHANTABILITY AND FITNESS. IN NO EVENT SHALL THE AUTHOR BE LIABLE FOR    |
|  ANY SPECIAL, DIRECT, INDIRECT, OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES     |
|  WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN      |
|  ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF    |
|  OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.             |
|                                                                             |
\-----------------------------------------------------------------------------/

Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)

Loaded SDC plugin
[TCL: yosys -import] Command name collision: found pre-existing command `cd' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `eval' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `exec' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `read' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `trace' -> skip.

1. Executing Liberty frontend: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
Imported 428 cell types from liberty file.

2. Executing Verilog-2005 frontend: ./SISO.v
Parsing SystemVerilog input from `./SISO.v' to AST representation.
Generating RTLIL representation for module `\SISO'.
Generating RTLIL representation for module `\neuron'.
Generating RTLIL representation for module `\ReLU'.
Successfully finished Verilog frontend.

3. Executing HIERARCHY pass (managing design hierarchy).

3.1. Analyzing design hierarchy..
Top module:  \SISO
Used module:     \ReLU
Used module:     \neuron

3.2. Analyzing design hierarchy..
Top module:  \SISO
Used module:     \ReLU
Used module:     \neuron
Removed 0 unused modules.
Warning: Resizing cell port SISO.r1.in from 64 bits to 32 bits.
Renaming module SISO to SISO.

4. Generating Graphviz representation of design.
Writing dot description to `/content/openlane_run/18-yosys-synthesis/hierarchy.dot'.
Dumping module SISO to page 1.

5. Executing TRIBUF pass.

6. Executing HIERARCHY pass (managing design hierarchy).

6.1. Analyzing design hierarchy..
Top module:  \SISO
Used module:     \ReLU
Used module:     \neuron

6.2. Analyzing design hierarchy..
Top module:  \SISO
Used module:     \ReLU
Used module:     \neuron
Removed 0 unused modules.

7. Executing PROC_CLEAN pass (remove empty switches from decision trees).
Cleaned up 0 empty switches.

8. Executing PROC_RMDEAD pass (remove dead branches from decision trees).
Marked 1 switch rules as full_case in process $proc$./SISO.v:54$5 in module ReLU.
Removed a total of 0 dead cases.

9. Executing PROC_PRUNE pass (remove redundant assignments in processes).
Removed 0 redundant assignments.
Promoted 4 assignments to connections.

10. Executing PROC_INIT pass (extract init attributes).

11. Executing PROC_ARST pass (detect async resets in processes).

12. Executing PROC_ROM pass (convert switches to ROMs).
Converted 0 switches.
<suppressed ~1 debug messages>

13. Executing PROC_MUX pass (convert decision trees to multiplexers).
Creating decoders for process `\SISO.$proc$./SISO.v:0$1'.
Creating decoders for process `\neuron.$proc$./SISO.v:42$2'.
Creating decoders for process `\ReLU.$proc$./SISO.v:54$5'.
1/1: $1\out[63:0]

14. Executing PROC_DLATCH pass (convert process syncs to latches).
No latch inferred for signal `\SISO.\weight' from process `\SISO.$proc$./SISO.v:0$1'.
No latch inferred for signal `\neuron.\out_neuron' from process `\neuron.$proc$./SISO.v:42$2'.
No latch inferred for signal `\neuron.\out_mul' from process `\neuron.$proc$./SISO.v:42$2'.
No latch inferred for signal `\ReLU.\out' from process `\ReLU.$proc$./SISO.v:54$5'.

15. Executing PROC_DFF pass (convert process syncs to FFs).

16. Executing PROC_MEMWR pass (convert process memory writes to cells).

17. Executing PROC_CLEAN pass (remove empty switches from decision trees).
Removing empty process `SISO.$proc$./SISO.v:0$1'.
Removing empty process `neuron.$proc$./SISO.v:42$2'.
Found and cleaned up 1 empty switch in `\ReLU.$proc$./SISO.v:54$5'.
Removing empty process `ReLU.$proc$./SISO.v:54$5'.
Cleaned up 1 empty switch.

18. Executing CHECK pass (checking for obvious problems).
Checking module SISO...
Checking module neuron...
Checking module ReLU...
Found and reported 0 problems.

19. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.
```

```
Optimizing module neuron.
Optimizing module ReLU.

20. Executing FLATTEN pass (flatten design).
Deleting now unused module neuron.
Deleting now unused module ReLU.
<suppressed ~2 debug messages>

21. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

22. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..
Removed 0 unused cells and 9 unused wires.
<suppressed ~1 debug messages>

23. Executing OPT pass (performing simple optimizations).

23.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

23.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

23.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~1 debug messages>

23.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Performed a total of 0 changes.

23.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

23.6. Executing OPT_DFF pass (perform DFF optimizations).

23.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

23.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

23.9. Finished OPT passes. (There is nothing left to do.)

24. Executing FSM pass (extract and optimize FSM).

24.1. Executing FSM_DETECT pass (finding FSMs in design).

24.2. Executing FSM_EXTRACT pass (extracting FSM from design).

24.3. Executing FSM_OPT pass (simple optimizations of FSMs).

24.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

24.5. Executing FSM_OPT pass (simple optimizations of FSMs).

24.6. Executing FSM_RECODE pass (re-assigning FSM state encoding).

24.7. Executing FSM_INFO pass (dumping all available information on FSM cells).

24.8. Executing FSM_MAP pass (mapping FSMs to basic logic).

25. Executing OPT pass (performing simple optimizations).

25.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

25.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

25.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~1 debug messages>

25.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Performed a total of 0 changes.

25.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

25.6. Executing OPT_DFF pass (perform DFF optimizations).

25.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

25.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

25.9. Finished OPT passes. (There is nothing left to do.)

26. Executing WREDUCE pass (reducing word size of cells).
Removed top 63 bits (of 64) from port B of cell SISO.$flatten\n1.$add$./SISO.v:44$4 ($add).
Removed top 32 bits (of 64) from port Y of cell SISO.$flatten\n1.$add$./SISO.v:44$4 ($add).
Removed top 32 bits (of 64) from port A of cell SISO.$flatten\n1.$add$./SISO.v:44$4 ($add).
Removed top 1 bits (of 4) from port A of cell SISO.$flatten\n1.$mul$./SISO.v:43$3 ($mul).
Removed top 32 bits (of 64) from port Y of cell SISO.$flatten\n1.$mul$./SISO.v:43$3 ($mul).
Removed top 31 bits (of 32) from port B of cell SISO.$flatten\r1.$lt$./SISO.v:55$6 ($lt).

27. Executing PEEPOPT pass (run peephole optimizers).

28. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

29. Executing ALUMACC pass (create $alu and $macc cells).
Extracting $alu and $macc cells in module SISO:
creating $macc model for $flatten\n1.$add$./SISO.v:44$4 ($add).
creating $macc model for $flatten\n1.$mul$./SISO.v:43$3 ($mul).
merging $macc model for $flatten\n1.$mul$./SISO.v:43$3 into $flatten\n1.$add$./SISO.v:44$4.
creating $macc cell for $flatten\n1.$add$./SISO.v:44$4: $auto$alumacc.cc:365:replace_macc$10
creating $alu model for $flatten\r1.$lt$./SISO.v:55$6 ($lt): new $alu
creating $alu cell for $flatten\r1.$lt$./SISO.v:55$6: $auto$alumacc.cc:485:replace_alu$12
created 1 $alu and 1 $macc cells.
```

```
30. Executing SHARE pass (SAT-based resource sharing).

31. Executing OPT pass (performing simple optimizations).

31.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.
<suppressed ~1 debug messages>

31.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

31.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~1 debug messages>

31.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Performed a total of 0 changes.

31.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

31.6. Executing OPT_DFF pass (perform DFF optimizations).

31.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..
Removed 2 unused cells and 3 unused wires.
<suppressed ~4 debug messages>

31.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

31.9. Rerunning OPT passes. (Maybe there is more to do..)

31.10. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~1 debug messages>

31.11. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Performed a total of 0 changes.

31.12. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

31.13. Executing OPT_DFF pass (perform DFF optimizations).

31.14. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

31.15. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

31.16. Finished OPT passes. (There is nothing left to do.)

32. Executing MEMORY pass.

32.1. Executing OPT_MEM pass (optimize memories).
Performed a total of 0 transformations.

32.2. Executing OPT_MEM_PRIORITY pass (removing unnecessary memory write priority relations).
Performed a total of 0 transformations.

32.3. Executing OPT_MEM_FEEDBACK pass (finding memory read-to-write feedback paths).

32.4. Executing MEMORY_BMUX2ROM pass (converting muxes to ROMs).

32.5. Executing MEMORY_DFF pass (merging $dff cells to $memrd).

32.6. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

32.7. Executing MEMORY_SHARE pass (consolidating $memrd/$memwr cells).

32.8. Executing OPT_MEM_WIDEN pass (optimize memories where all ports are wide).
Performed a total of 0 transformations.

32.9. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

32.10. Executing MEMORY_COLLECT pass (generating $mem cells).

33. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

34. Executing OPT pass (performing simple optimizations).

34.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.
<suppressed ~6 debug messages>

34.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

34.3. Executing OPT_DFF pass (perform DFF optimizations).

34.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

34.5. Finished fast OPT passes.

35. Executing MEMORY_MAP pass (converting memories to logic and flip-flops).

36. Executing OPT pass (performing simple optimizations).

36.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

36.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

36.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
```

```
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~1 debug messages>

36.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Consolidated identical input bits for $mux cell $flatten\r1.$procmux$8:
Old ports: A=64'0000000000000000000000000000000000000000000000000000000000000000, B={ \r1.in [31] \r1.in [31]
\r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in
[31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31]
\r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in [31] \r1.in
[31] \r1.in [31] \r1.in }, Y=\y
New ports: A=0, B=\r1.in, Y=\y [31:0]
New connections: \y [63:32] = { \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y
[31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y
[31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] \y [31] }
Optimizing cells in module \SISO.
Performed a total of 1 changes.

36.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

36.6. Executing OPT_SHARE pass.

36.7. Executing OPT_DFF pass (perform DFF optimizations).

36.8. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

36.9. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

36.10. Rerunning OPT passes. (Maybe there is more to do..)

36.11. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~1 debug messages>

36.12. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Performed a total of 0 changes.

36.13. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

36.14. Executing OPT_SHARE pass.

36.15. Executing OPT_DFF pass (perform DFF optimizations).

36.16. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

36.17. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

36.18. Finished OPT passes. (There is nothing left to do.)

37. Executing TECHMAP pass (map to technology primitives).

37.1. Executing Verilog-2005 frontend:
/nix/store/sx2v0i73mn1ih2z1nk61pm9n5gjgpidy-yosys/bin/../share/yosys/techmap.v
Parsing Verilog input from `/nix/store/sx2v0i73mn1ih2z1nk61pm9n5gjgpidy-yosys/bin/../share/yosys/techmap.v' to AST
representation.
Generating RTLIL representation for module `\_90_simplemap_bool_ops'.
Generating RTLIL representation for module `\_90_simplemap_reduce_ops'.
Generating RTLIL representation for module `\_90_simplemap_logic_ops'.
Generating RTLIL representation for module `\_90_simplemap_compare_ops'.
Generating RTLIL representation for module `\_90_simplemap_various'.
Generating RTLIL representation for module `\_90_simplemap_registers'.
Generating RTLIL representation for module `\_90_shift_ops_shr_shl_sshl_sshr'.
Generating RTLIL representation for module `\_90_shift_shiftx'.
Generating RTLIL representation for module `\_90_fa'.
Generating RTLIL representation for module `\_90_lcu'.
Generating RTLIL representation for module `\_90_alu'.
Generating RTLIL representation for module `\_90_macc'.
Generating RTLIL representation for module `\_90_alumacc'.
Generating RTLIL representation for module `\$__div_mod_u'.
Generating RTLIL representation for module `\$__div_mod_trunc'.
Generating RTLIL representation for module `\_90_div'.
Generating RTLIL representation for module `\_90_mod'.
Generating RTLIL representation for module `\$__div_mod_floor'.
Generating RTLIL representation for module `\_90_divfloor'.
Generating RTLIL representation for module `\_90_modfloor'.
Generating RTLIL representation for module `\_90_pow'.
Generating RTLIL representation for module `\_90_pmux'.
Generating RTLIL representation for module `\_90_demux'.
Generating RTLIL representation for module `\_90_lut'.
Successfully finished Verilog frontend.

37.2. Continuing TECHMAP pass.
Using extmapper simplemap for cells of type $reduce_and.
Using extmapper simplemap for cells of type $xor.
Using extmapper simplemap for cells of type $or.
Using template $paramod$7b00947614a4c48e09c066dca449366ddfa907a5\_90_alu for cells of type $alu.
Using extmapper maccmap for cells of type $macc.
add \x * 3'101 (32x3 bits, unsigned)
add 1 (32 bits, unsigned)
packed 1 (1) bits / 1 words into adder tree
Using extmapper simplemap for cells of type $mux.
Using extmapper simplemap for cells of type $and.
Using template $paramod\_90_lcu\WIDTH=32'00000000000000000000000000100000 for cells of type $lcu.
Using extmapper simplemap for cells of type $pos.
Using extmapper simplemap for cells of type $not.
Using template $paramod\_90_fa\WIDTH=32'00000000000000000000000000100000 for cells of type $fa.
Using template $paramod$fbc7873bff55778c0b3173955b7e4bce1d9d6834\_90_alu for cells of type $alu.
No more expansions possible.
<suppressed ~576 debug messages>

38. Executing OPT pass (performing simple optimizations).

38.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.
<suppressed ~430 debug messages>

38.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
<suppressed ~96 debug messages>
Removed a total of 32 cells.

38.3. Executing OPT_DFF pass (perform DFF optimizations).
```

```
38.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..
Removed 97 unused cells and 199 unused wires.
<suppressed ~98 debug messages>

38.5. Finished fast OPT passes.

39. Executing ABC pass (technology mapping using ABC).

39.1. Extracting gate netlist of module `\SISO' to `<abc-temp-dir>/input.blif'..
Extracted 372 gates and 405 wires to a netlist network with 32 inputs and 32 outputs.

39.1.1. Executing ABC.
Running ABC command: "/nix/store/wq2q0njg3sx8wvj2akz7x1qxwyrv9xlr-yosys-abc/bin/abc" -s -f
<abc-temp-dir>/abc.script 2>&1
ABC: ABC command line: "source <abc-temp-dir>/abc.script".
ABC:
ABC: + read_blif <abc-temp-dir>/input.blif
ABC: + read_library <abc-temp-dir>/stdcells.genlib
ABC: Entered genlib library with 13 gates from file "<abc-temp-dir>/stdcells.genlib".
ABC: + strash
ABC: + dretime
ABC: + map
ABC: + write_blif <abc-temp-dir>/output.blif

39.1.2. Re-integrating ABC results.
ABC RESULTS:               AND cells:       30
ABC RESULTS:              XNOR cells:       23
ABC RESULTS:             ORNOT cells:       28
ABC RESULTS:              NAND cells:       13
ABC RESULTS:                OR cells:       28
ABC RESULTS:               NOR cells:       33
ABC RESULTS:               XOR cells:       67
ABC RESULTS:            ANDNOT cells:      111
ABC RESULTS:        internal signals:      341
ABC RESULTS:           input signals:       32
ABC RESULTS:          output signals:       32
Removing temp directory.

40. Executing OPT pass (performing simple optimizations).

40.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

40.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
<suppressed ~3 debug messages>
Removed a total of 1 cells.

40.3. Executing OPT_DFF pass (perform DFF optimizations).

40.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..
Removed 0 unused cells and 172 unused wires.
<suppressed ~1 debug messages>

40.5. Finished fast OPT passes.

41. Executing HIERARCHY pass (managing design hierarchy).

41.1. Analyzing design hierarchy..
Top module:  \SISO

41.2. Analyzing design hierarchy..
Top module:  \SISO
Removed 0 unused modules.

42. Printing statistics.

=== SISO ===

   Number of wires:                 312
   Number of wire bits:             852
   Number of public wires:           12
   Number of public wire bits:      552
   Number of memories:                0
   Number of memory bits:             0
   Number of processes:               0
   Number of cells:                 332
     $_ANDNOT_                      111
     $_AND_                          30
     $_NAND_                         12
     $_NOR_                          33
     $_ORNOT_                        28
     $_OR_                           28
     $_XNOR_                         23
     $_XOR_                          67

43. Executing CHECK pass (checking for obvious problems).
Checking module SISO...
Found and reported 0 problems.

44. Generating Graphviz representation of design.
Writing dot description to `/content/openlane_run/18-yosys-synthesis/primitive_techmap.dot'.
Dumping module SISO to page 1.

45. Executing OPT pass (performing simple optimizations).

45.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

45.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

45.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \SISO..
Creating internal representation of mux trees.
No muxes found in this module.
Removed 0 multiplexer ports.

45.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \SISO.
Performed a total of 0 changes.

45.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\SISO'.
Removed a total of 0 cells.

45.6. Executing OPT_DFF pass (perform DFF optimizations).

45.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..

45.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module SISO.

45.9. Finished OPT passes. (There is nothing left to do.)
```

```
46. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..
Removed 0 unused cells and 10 unused wires.
<suppressed ~10 debug messages>
{
"creator": "Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)",
"invocation": "stat -json -liberty /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib ",
"modules": {
"\\SISO": {
"num_wires":         302,
"num_wire_bits":     396,
"num_pub_wires":     2,
"num_pub_wire_bits": 96,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         332,
"num_cells_by_type": {
"$_ANDNOT_": 111,
"$_AND_": 30,
"$_NAND_": 12,
"$_NOR_": 33,
"$_ORNOT_": 28,
"$_OR_": 28,
"$_XNOR_": 23,
"$_XOR_": 67
}
}
},
"design": {
"num_wires":         302,
"num_wire_bits":     396,
"num_pub_wires":     2,
"num_pub_wire_bits": 96,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         332,
"num_cells_by_type": {
"$_ANDNOT_": 111,
"$_AND_": 30,
"$_NAND_": 12,
"$_NOR_": 33,
"$_ORNOT_": 28,
"$_OR_": 28,
"$_XNOR_": 23,
"$_XOR_": 67
}
}
}

47. Printing statistics.

=== SISO ===

   Number of wires:                302
   Number of wire bits:            396
   Number of public wires:           2
   Number of public wire bits:      96
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                332
     $_ANDNOT_                     111
     $_AND_                         30
     $_NAND_                        12
     $_NOR_                         33
     $_ORNOT_                       28
     $_OR_                          28
     $_XNOR_                        23
     $_XOR_                         67

   Area for cell type $_AND_ is unknown!
   Area for cell type $_NAND_ is unknown!
   Area for cell type $_OR_ is unknown!
   Area for cell type $_NOR_ is unknown!
   Area for cell type $_XOR_ is unknown!
   Area for cell type $_XNOR_ is unknown!
   Area for cell type $_ANDNOT_ is unknown!
   Area for cell type $_ORNOT_ is unknown!

mapping tbuf
[INFO] Applying tri-state buffer mapping from
'/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tribuff_map.v'...

48. Executing TECHMAP pass (map to technology primitives).

48.1. Executing Verilog-2005 frontend: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tribuff_map.v
Parsing Verilog input from `/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tribuff_map.v' to AST
representation.
Generating RTLIL representation for module `\$_TBUF_'.
Successfully finished Verilog frontend.

48.2. Continuing TECHMAP pass.
No more expansions possible.
<suppressed ~3 debug messages>

49. Executing SIMPLEMAP pass (map simple cells to gate primitives).
[INFO] Applying latch mapping from '/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/latch_map.v'...

50. Executing TECHMAP pass (map to technology primitives).

50.1. Executing Verilog-2005 frontend: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/latch_map.v
Parsing Verilog input from `/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/latch_map.v' to AST
representation.
Generating RTLIL representation for module `\$_DLATCH_P_'.
Generating RTLIL representation for module `\$_DLATCH_N_'.
Successfully finished Verilog frontend.

50.2. Continuing TECHMAP pass.
No more expansions possible.
<suppressed ~4 debug messages>

51. Executing SIMPLEMAP pass (map simple cells to gate primitives).

52. Executing DFFLIBMAP pass (mapping DFF cells to sequential cells from liberty file).
cell sky130_fd_sc_hd__dfxtp_2 (noninv, pins=3, area=21.27) is a direct match for cell type $_DFF_P_.
cell sky130_fd_sc_hd__dfrtp_2 (noninv, pins=4, area=26.28) is a direct match for cell type $_DFF_PN0_.
cell sky130_fd_sc_hd__dfstp_2 (noninv, pins=4, area=26.28) is a direct match for cell type $_DFF_PN1_.
cell sky130_fd_sc_hd__dfbbn_2 (noninv, pins=6, area=35.03) is a direct match for cell type $_DFFSR_NNN_.
final dff cell mappings:
unmapped dff cell: $_DFF_N_
\sky130_fd_sc_hd__dfxtp_2 _DFF_P_ (.CLK( C), .D( D), .Q( Q));
unmapped dff cell: $_DFF_NN0_
unmapped dff cell: $_DFF_NN1_
unmapped dff cell: $_DFF_NP0_
unmapped dff cell: $_DFF_NP1_
```

```
unmapped dff cell: $_DFF_NP1_
\sky130_fd_sc_hd__dfrtp_2 _DFF_PN0_ (.CLK( C), .D( D), .Q( Q), .RESET_B( R));
\sky130_fd_sc_hd__dfstp_2 _DFF_PN1_ (.CLK( C), .D( D), .Q( Q), .SET_B( R));
unmapped dff cell: $_DFF_PP0_
unmapped dff cell: $_DFF_PP1_
\sky130_fd_sc_hd__dfbbn_2 _DFFSR_NNN_ (.CLK_N( C), .D( D), .Q( Q), .Q_N(~Q), .RESET_B( R), .SET_B( S));
unmapped dff cell: $_DFFSR_NNP_
unmapped dff cell: $_DFFSR_NPN_
unmapped dff cell: $_DFFSR_NPP_
unmapped dff cell: $_DFFSR_PNN_
unmapped dff cell: $_DFFSR_PNP_
unmapped dff cell: $_DFFSR_PPN_
unmapped dff cell: $_DFFSR_PPP_

52.1. Executing DFFLEGALIZE pass (convert FFs to types supported by the target).
Mapping DFF cells in module `\SISO':
{
"creator": "Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)",
"invocation": "stat -json -liberty /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib ",
"modules": {
"\\SISO": {
"num_wires":         302,
"num_wire_bits":     396,
"num_pub_wires":     2,
"num_pub_wire_bits": 96,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         332,
"num_cells_by_type": {
"$_ANDNOT_": 111,
"$_AND_": 30,
"$_NAND_": 12,
"$_NOR_": 33,
"$_ORNOT_": 28,
"$_OR_": 28,
"$_XNOR_": 23,
"$_XOR_": 67
}
}
},
"design": {
"num_wires":         302,
"num_wire_bits":     396,
"num_pub_wires":     2,
"num_pub_wire_bits": 96,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         332,
"num_cells_by_type": {
"$_ANDNOT_": 111,
"$_AND_": 30,
"$_NAND_": 12,
"$_NOR_": 33,
"$_ORNOT_": 28,
"$_OR_": 28,
"$_XNOR_": 23,
"$_XOR_": 67
}
}
}

53. Printing statistics.

=== SISO ===

   Number of wires:                302
   Number of wire bits:            396
   Number of public wires:           2
   Number of public wire bits:      96
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                332
     $_ANDNOT_                     111
     $_AND_                         30
     $_NAND_                        12
     $_NOR_                         33
     $_ORNOT_                       28
     $_OR_                          28
     $_XNOR_                        23
     $_XOR_                         67

   Area for cell type $_AND_ is unknown!
   Area for cell type $_NAND_ is unknown!
   Area for cell type $_OR_ is unknown!
   Area for cell type $_NOR_ is unknown!
   Area for cell type $_XOR_ is unknown!
   Area for cell type $_XNOR_ is unknown!
   Area for cell type $_ANDNOT_ is unknown!
   Area for cell type $_ORNOT_ is unknown!

[INFO] Using strategy "AREA 0"...

54. Executing ABC pass (technology mapping using ABC).

54.1. Extracting gate netlist of module `\SISO' to `/tmp/yosys-abc-zigPZC/input.blif'..
Extracted 332 gates and 364 wires to a netlist network with 32 inputs and 32 outputs.

54.1.1. Executing ABC.
Running ABC command: "/nix/store/wq2q0njg3sx8wvj2akz7x1qxwyrv9xlr-yosys-abc/bin/abc" -s -f
/tmp/yosys-abc-zigPZC/abc.script 2>&1
ABC: ABC command line: "source /tmp/yosys-abc-zigPZC/abc.script".
ABC:
ABC: + read_blif /tmp/yosys-abc-zigPZC/input.blif
ABC: + read_lib -w /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib
ABC: Parsing finished successfully.  Parsing time =     0.21 sec
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfbbn_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfrbp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfrtp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfrtp_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfsbp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfstp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfstp_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfxbp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfxtp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfxtp_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtn_1".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtn_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtn_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtp_1".
ABC: Scl_LibertyReadGenlib() skipped three-state cell "sky130_fd_sc_hd__ebufn_2".
ABC: Scl_LibertyReadGenlib() skipped three-state cell "sky130_fd_sc_hd__ebufn_4".
ABC: Scl_LibertyReadGenlib() skipped three-state cell "sky130_fd_sc_hd__ebufn_8".
ABC: Library "sky130_fd_sc_hd__tt_025C_1v80" from "/content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib"
has 175 cells (17 skipped: 14 seq; 3 tri-state; 0 no func; 0 dont_use).  Time =     0.35 sec
ABC: Memory =    9.54 MB. Time =     0.35 sec
```

```
ABC: Warning: Detected 2 multi-output gates (for example, "sky130_fd_sc_hd__fa_1").
ABC: + read_constr -v /content/openlane_run/18-yosys-synthesis/synthesis.sdc
ABC: Setting driving cell to be "sky130_fd_sc_hd__inv_2/Y".
ABC: Setting output load to be 33.442001.
ABC: + read_constr /content/openlane_run/18-yosys-synthesis/synthesis.sdc
ABC: + fx
ABC: + mfs
ABC: + strash
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + retime -D -D 10000 -M 5
ABC: + scleanup
ABC: Error: The network is combinational.
ABC: + fraig_store
ABC: + balance
ABC: + fraig_store
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + fraig_store
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + fraig_store
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + fraig_store
ABC: + fraig_restore
ABC: + amap -m -Q 0.1 -F 20 -A 20 -C 5000
ABC: + retime -D -D 10000
ABC: + &get -n
ABC: + &st
ABC: + &dch
ABC: + &nf
ABC: + &put
ABC: +
ABC: + stime -p
ABC: Cannot find the default PI driving cell (sky130_fd_sc_hd__inv_2/Y) in the library.
ABC: WireLoad = "none"  Gates =    261 (  2.7 %)   Cap = 11.8 ff (  0.9 %)   Area =     2501.15 ( 95.8 %)   Delay =
3615.36 ps  (  7.3 %)
ABC: Path  0 --      10 : 0    6 pi                        A =   0.00  Df =   0.0   -0.0 ps  S =   0.0 ps  Cin =
0.0 ff  Cout =  22.6 ff  Cmax =   0.0 ff  G =    0
ABC: Path  1 --     151 : 2    2 sky130_fd_sc_hd__or2_2    A =   6.26  Df = 285.7 -193.4 ps  S =  64.1 ps  Cin =
1.5 ff  Cout =   6.2 ff  Cmax = 299.4 ff  G =  400
ABC: Path  2 --     152 : 4    4 sky130_fd_sc_hd__and4_2   A =  10.01  Df = 551.9 -193.5 ps  S = 103.0 ps  Cin =
1.5 ff  Cout =  13.4 ff  Cmax = 300.3 ff  G =  830
ABC: Path  3 --     154 : 2    4 sky130_fd_sc_hd__or2_2    A =   6.26  Df = 872.8 -316.4 ps  S =  73.1 ps  Cin =
1.5 ff  Cout =   9.6 ff  Cmax = 299.4 ff  G =  626
ABC: Path  4 --     163 : 3    2 sky130_fd_sc_hd__or3_2    A =   7.51  Df =1328.2 -661.0 ps  S =  80.7 ps  Cin =
1.5 ff  Cout =   4.1 ff  Cmax = 310.4 ff  G =  257
ABC: Path  5 --     175 : 2    2 sky130_fd_sc_hd__or2_2    A =   6.26  Df =1638.0 -620.3 ps  S =  61.4 ps  Cin =
1.5 ff  Cout =   5.1 ff  Cmax = 299.4 ff  G =  330
ABC: Path  6 --     184 : 5    2 sky130_fd_sc_hd__a2111o_2 A =  12.51  Df =2054.4 -563.0 ps  S =  75.3 ps  Cin =
2.4 ff  Cout =   7.0 ff  Cmax = 324.1 ff  G =  281
ABC: Path  7 --     213 : 3    2 sky130_fd_sc_hd__a21o_2   A =   8.76  Df =2261.1 -644.7 ps  S =  49.8 ps  Cin =
2.4 ff  Cout =   7.0 ff  Cmax = 309.5 ff  G =  288
ABC: Path  8 --     227 : 3    2 sky130_fd_sc_hd__a21o_2   A =   8.76  Df =2452.4 -715.4 ps  S =  45.5 ps  Cin =
2.4 ff  Cout =   6.1 ff  Cmax = 309.5 ff  G =  249
ABC: Path  9 --     229 : 4    5 sky130_fd_sc_hd__a31oi_2  A =  12.51  Df =2736.5 -868.0 ps  S = 299.3 ps  Cin =
4.4 ff  Cout =  18.2 ff  Cmax = 118.1 ff  G =  390
ABC: Path 10 --     232 : 3    4 sky130_fd_sc_hd__nor3_2   A =  10.01  Df =2865.8 -652.5 ps  S = 351.4 ps  Cin =
4.4 ff  Cout =  18.5 ff  Cmax =  92.5 ff  G =  400
ABC: Path 11 --     315 : 4    1 sky130_fd_sc_hd__nor4b_2  A =  15.01  Df =3615.4 -534.4 ps  S = 822.2 ps  Cin =
3.7 ff  Cout =  33.4 ff  Cmax =  65.0 ff  G =  915
ABC: Start-point = pi9 (\x [22]).  End-point = po26 (\y [26]).
ABC: + print_stats -m
ABC: netlist                       : i/o =   32/   32  lat =    0  nd =   261  edge =    673  area =2501.79  delay
=11.00  lev = 11
ABC: + write_blif /tmp/yosys-abc-zigPZC/output.blif

54.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__a32o_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a221o_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__and4bb_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__or4b_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a22oi_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a2111o_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o2bb2a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o32a_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__nand4_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a22o_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__nand3_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__inv_2 cells:        7
ABC RESULTS:   sky130_fd_sc_hd__or4_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o31a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o221a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a31oi_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__or3_2 cells:        6
ABC RESULTS:   sky130_fd_sc_hd__and3b_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o2111a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__and4b_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__nor2_2 cells:        6
ABC RESULTS:   sky130_fd_sc_hd__and2_2 cells:        12
ABC RESULTS:   sky130_fd_sc_hd__a31o_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__o21ai_2 cells:        5
ABC RESULTS:   sky130_fd_sc_hd__a21bo_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__nand2b_2 cells:        3
```

```
ABC RESULTS:   sky130_fd_sc_hd__and2b_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__o21bai_2 cells:        4
ABC RESULTS:   sky130_fd_sc_hd__a211o_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__or2_2 cells:       21
ABC RESULTS:   sky130_fd_sc_hd__nand2_2 cells:       43
ABC RESULTS:   sky130_fd_sc_hd__a21boi_2 cells:        4
ABC RESULTS:   sky130_fd_sc_hd__nor3_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__o21a_2 cells:        5
ABC RESULTS:   sky130_fd_sc_hd__o22a_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__xnor2_2 cells:       31
ABC RESULTS:   sky130_fd_sc_hd__or3b_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__nor4b_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a21oi_2 cells:        7
ABC RESULTS:   sky130_fd_sc_hd__o211a_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__a21o_2 cells:        9
ABC RESULTS:   sky130_fd_sc_hd__xor2_2 cells:       20
ABC RESULTS:   sky130_fd_sc_hd__and3_2 cells:       28
ABC RESULTS:   sky130_fd_sc_hd__and4_2 cells:        6
ABC RESULTS:   sky130_fd_sc_hd__nor4_2 cells:        3
ABC RESULTS:          _const0_ cells:        1
ABC RESULTS:        internal signals:      300
ABC RESULTS:           input signals:       32
ABC RESULTS:          output signals:       32
Removing temp directory.

55. Executing SETUNDEF pass (replace undef values with defined constants).

56. Executing HILOMAP pass (mapping to constant drivers).

57. Executing SPLITNETS pass (splitting up multi-bit signals).

58. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \SISO..
Removed 0 unused cells and 365 unused wires.
<suppressed ~1 debug messages>

59. Executing INSBUF pass (insert buffer cells for connected wires).
Add SISO/$auto$insbuf.cc:97:execute$1842: \y [63] -> \y [31]
Add SISO/$auto$insbuf.cc:97:execute$1843: \y [63] -> \y [32]
Add SISO/$auto$insbuf.cc:97:execute$1844: \y [63] -> \y [33]
Add SISO/$auto$insbuf.cc:97:execute$1845: \y [63] -> \y [34]
Add SISO/$auto$insbuf.cc:97:execute$1846: \y [63] -> \y [35]
Add SISO/$auto$insbuf.cc:97:execute$1847: \y [63] -> \y [36]
Add SISO/$auto$insbuf.cc:97:execute$1848: \y [63] -> \y [37]
Add SISO/$auto$insbuf.cc:97:execute$1849: \y [63] -> \y [38]
Add SISO/$auto$insbuf.cc:97:execute$1850: \y [63] -> \y [39]
Add SISO/$auto$insbuf.cc:97:execute$1851: \y [63] -> \y [40]
Add SISO/$auto$insbuf.cc:97:execute$1852: \y [63] -> \y [41]
Add SISO/$auto$insbuf.cc:97:execute$1853: \y [63] -> \y [42]
Add SISO/$auto$insbuf.cc:97:execute$1854: \y [63] -> \y [43]
Add SISO/$auto$insbuf.cc:97:execute$1855: \y [63] -> \y [44]
Add SISO/$auto$insbuf.cc:97:execute$1856: \y [63] -> \y [45]
Add SISO/$auto$insbuf.cc:97:execute$1857: \y [63] -> \y [46]
Add SISO/$auto$insbuf.cc:97:execute$1858: \y [63] -> \y [47]
Add SISO/$auto$insbuf.cc:97:execute$1859: \y [63] -> \y [48]
Add SISO/$auto$insbuf.cc:97:execute$1860: \y [63] -> \y [49]
Add SISO/$auto$insbuf.cc:97:execute$1861: \y [63] -> \y [50]
Add SISO/$auto$insbuf.cc:97:execute$1862: \y [63] -> \y [51]
Add SISO/$auto$insbuf.cc:97:execute$1863: \y [63] -> \y [52]
Add SISO/$auto$insbuf.cc:97:execute$1864: \y [63] -> \y [53]
Add SISO/$auto$insbuf.cc:97:execute$1865: \y [63] -> \y [54]
Add SISO/$auto$insbuf.cc:97:execute$1866: \y [63] -> \y [55]
Add SISO/$auto$insbuf.cc:97:execute$1867: \y [63] -> \y [56]
Add SISO/$auto$insbuf.cc:97:execute$1868: \y [63] -> \y [57]
Add SISO/$auto$insbuf.cc:97:execute$1869: \y [63] -> \y [58]
Add SISO/$auto$insbuf.cc:97:execute$1870: \y [63] -> \y [59]
Add SISO/$auto$insbuf.cc:97:execute$1871: \y [63] -> \y [60]
Add SISO/$auto$insbuf.cc:97:execute$1872: \y [63] -> \y [61]
Add SISO/$auto$insbuf.cc:97:execute$1873: \y [63] -> \y [62]

60. Executing CHECK pass (checking for obvious problems).
Checking module SISO...
Found and reported 0 problems.
{
"creator": "Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)",
"invocation": "stat -json -liberty /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib ",
"modules": {
"\\SISO": {
"num_wires":         231,
"num_wire_bits":     325,
"num_pub_wires":     2,
"num_pub_wire_bits": 96,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         293,
"area":              2665.056000,
"num_cells_by_type": {
"sky130_fd_sc_hd__a2111o_2": 1,
"sky130_fd_sc_hd__a211o_2": 1,
"sky130_fd_sc_hd__a21bo_2": 2,
"sky130_fd_sc_hd__a21boi_2": 4,
"sky130_fd_sc_hd__a21o_2": 9,
"sky130_fd_sc_hd__a21oi_2": 7,
"sky130_fd_sc_hd__a221o_2": 1,
"sky130_fd_sc_hd__a22o_2": 1,
"sky130_fd_sc_hd__a22oi_2": 1,
"sky130_fd_sc_hd__a31o_2": 3,
"sky130_fd_sc_hd__a31oi_2": 1,
"sky130_fd_sc_hd__a32o_2": 1,
"sky130_fd_sc_hd__and2_2": 12,
"sky130_fd_sc_hd__and2b_2": 3,
"sky130_fd_sc_hd__and3_2": 28,
"sky130_fd_sc_hd__and3b_2": 1,
"sky130_fd_sc_hd__and4_2": 6,
"sky130_fd_sc_hd__and4b_2": 2,
"sky130_fd_sc_hd__and4bb_2": 1,
"sky130_fd_sc_hd__buf_2": 32,
"sky130_fd_sc_hd__conb_1": 1,
"sky130_fd_sc_hd__inv_2": 7,
"sky130_fd_sc_hd__nand2_2": 43,
"sky130_fd_sc_hd__nand2b_2": 3,
"sky130_fd_sc_hd__nand3_2": 1,
"sky130_fd_sc_hd__nand4_2": 1,
"sky130_fd_sc_hd__nor2_2": 6,
"sky130_fd_sc_hd__nor3_2": 2,
"sky130_fd_sc_hd__nor4_2": 3,
"sky130_fd_sc_hd__nor4b_2": 1,
"sky130_fd_sc_hd__o2111a_2": 1,
"sky130_fd_sc_hd__o211a_2": 3,
"sky130_fd_sc_hd__o21a_2": 5,
"sky130_fd_sc_hd__o21ai_2": 5,
"sky130_fd_sc_hd__o21bai_2": 4,
"sky130_fd_sc_hd__o221a_2": 1,
"sky130_fd_sc_hd__o22a_2": 2,
"sky130_fd_sc_hd__o2bb2a_2": 1,
"sky130_fd_sc_hd__o31a_2": 1,
```

```
"sky130_fd_sc_hd__o32a_2": 3,
"sky130_fd_sc_hd__or2_2": 21,
"sky130_fd_sc_hd__or3_2": 6,
"sky130_fd_sc_hd__or3b_2": 2,
"sky130_fd_sc_hd__or4_2": 1,
"sky130_fd_sc_hd__or4b_2": 1,
"sky130_fd_sc_hd__xnor2_2": 31,
"sky130_fd_sc_hd__xor2_2": 20
}
}
},
"design": {
"num_wires":         231,
"num_wire_bits":     325,
"num_pub_wires":     2,
"num_pub_wire_bits": 96,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         293,
"area":              2665.056000,
"num_cells_by_type": {
"sky130_fd_sc_hd__a2111o_2": 1,
"sky130_fd_sc_hd__a211o_2": 1,
"sky130_fd_sc_hd__a21bo_2": 2,
"sky130_fd_sc_hd__a21boi_2": 4,
"sky130_fd_sc_hd__a21o_2": 9,
"sky130_fd_sc_hd__a21oi_2": 7,
"sky130_fd_sc_hd__a221o_2": 1,
"sky130_fd_sc_hd__a22o_2": 1,
"sky130_fd_sc_hd__a22oi_2": 1,
"sky130_fd_sc_hd__a31o_2": 3,
"sky130_fd_sc_hd__a31oi_2": 1,
"sky130_fd_sc_hd__a32o_2": 1,
"sky130_fd_sc_hd__and2_2": 12,
"sky130_fd_sc_hd__and2b_2": 3,
"sky130_fd_sc_hd__and3_2": 28,
"sky130_fd_sc_hd__and3b_2": 1,
"sky130_fd_sc_hd__and4_2": 6,
"sky130_fd_sc_hd__and4b_2": 2,
"sky130_fd_sc_hd__and4bb_2": 1,
"sky130_fd_sc_hd__buf_2": 32,
"sky130_fd_sc_hd__conb_1": 1,
"sky130_fd_sc_hd__inv_2": 7,
"sky130_fd_sc_hd__nand2_2": 43,
"sky130_fd_sc_hd__nand2b_2": 3,
"sky130_fd_sc_hd__nand3_2": 1,
"sky130_fd_sc_hd__nand4_2": 1,
"sky130_fd_sc_hd__nor2_2": 6,
"sky130_fd_sc_hd__nor3_2": 2,
"sky130_fd_sc_hd__nor4_2": 3,
"sky130_fd_sc_hd__nor4b_2": 1,
"sky130_fd_sc_hd__o2111a_2": 1,
"sky130_fd_sc_hd__o211a_2": 3,
"sky130_fd_sc_hd__o21a_2": 5,
"sky130_fd_sc_hd__o21ai_2": 5,
"sky130_fd_sc_hd__o21bai_2": 4,
"sky130_fd_sc_hd__o221a_2": 1,
"sky130_fd_sc_hd__o22a_2": 2,
"sky130_fd_sc_hd__o2bb2a_2": 1,
"sky130_fd_sc_hd__o31a_2": 1,
"sky130_fd_sc_hd__o32a_2": 3,
"sky130_fd_sc_hd__or2_2": 21,
"sky130_fd_sc_hd__or3_2": 6,
"sky130_fd_sc_hd__or3b_2": 2,
"sky130_fd_sc_hd__or4_2": 1,
"sky130_fd_sc_hd__or4b_2": 1,
"sky130_fd_sc_hd__xnor2_2": 31,
"sky130_fd_sc_hd__xor2_2": 20
}
}
}
```

```
display(synthesis)
```

Time Elapsed: 14.76s

Views updated:

- Verilog Netlist

Floorplanning

Floorplanning does two things:

- Determines the dimensions of the final chip.
- Creates the "cell placement grid" which placed cells must be aligned to.
  - Each cell in the grid is called a "site." Cells can occupy multiple sites, with the overwhelming majority of cells occupying multiple sites by width, and some standard cell libraries supporting varying heights as well.

> Don't forget- you may call `display_help()` on any Step class to get a full list of configuration variables.

```
Floorplan = Step.factory.get("OpenROAD.Floorplan")

floorplan = Floorplan(state_in=synthesis.state_out)
floorplan.start()
```

```
─────────────────────────────────────── Floorplan Initialization ───────────────────────────────────────
[14:57:25] VERBOSE  Running 'OpenROAD.Floorplan'…                                          step.py:1088
[14:57:25] VERBOSE  Logging subprocess to openlane_run/19-openroad-floorplan/openroad-floorplan.log…  step.py:1268
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading technology LEF file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef'…
[INFO ODB-0227] LEF file: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef, created
13 layers, 25 vias
Reading cell LEF file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef'…
The NOWIREEXTENSIONATPIN statement will be ignored. See file
/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef at line 2.

[INFO ODB-0227] LEF file: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef, created 4 library
cells
Reading cell LEF file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef'…
The NOWIREEXTENSIONATPIN statement will be ignored. See file
/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef at line 2.

[INFO ODB-0227] LEF file: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef, created 437
library cells
Reading top-level netlist at '/content/openlane_run/18-yosys-synthesis/SISO.nl.v'…
Linking design 'SISO' from netlist…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:57:27] WARNING  [STA-0366] port 'clk' not found.                                        openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:57:27] WARNING  [STA-0366] port 'clk' not found.                                        openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:57:28] WARNING  [STA-0419] transition time can not be specified for virtual clocks.      openroad.py:235
[INFO] Setting timing derate to: 5%
[14:57:28] WARNING  [STA-0450] virtual clock clk can not be propagated.                     openroad.py:235
Using site height: 2.72 and site width: 0.46…
[INFO] Using relative sizing for the floorplan.
[INFO IFP-0001] Added 26 rows of 158 site unithd.
[INFO IFP-0030] Inserted 0 tiecells using sky130_fd_sc_hd__conb_1/LO.
[INFO IFP-0030] Inserted 0 tiecells using sky130_fd_sc_hd__conb_1/HI.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 84.045 94.765 (µm).
[INFO] Floorplanned on a core area of 5.52 10.88 78.2 81.6 (µm).
Writing metric design__die__bbox: 0.0 0.0 84.045 94.765
Writing metric design__core__bbox: 5.52 10.88 78.2 81.6
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/19-openroad-floorplan/SISO.odb'…
Writing netlist to '/content/openlane_run/19-openroad-floorplan/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/19-openroad-floorplan/SISO.pnl.v'…
Writing layout to '/content/openlane_run/19-openroad-floorplan/SISO.def'…
Writing timing constraints to '/content/openlane_run/19-openroad-floorplan/SISO.sdc'…
```

Format	Path
nl	openlane_run/19-openroad-floorplan/SISO.nl.v
pnl	openlane_run/19-openroad-floorplan/SISO.pnl.v
def	openlane_run/19-openroad-floorplan/SISO.def

```
display(floorplan)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[14:57:28] VERBOSE  Running 'KLayout.Render'…                                                    step.py:1088
[14:57:28] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_pugukkgj/klayout-render.log…  step.py:1268
```

Time Elapsed: 3.34s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Tap/Endcap Cell Insertion

This places two kinds of cells on the floorplan:

- End cap/boundary cells: Added at the beginning and end of each row. True to their name, they "cap off" the core area of a design.
- Tap cells: Placed in a polka dot-ish fashion across the rows. Tap cells connect VDD to the nwell and the psubstrate to VSS, which the majority of cells do not do themselves to save area- but if you go long enough without one such connection you end up with the cell "latching-up"; i.e.; refusing to switch back to LO from HI.

  There is a maximum distance between tap cells enforced as part of every foundry process.

```
TapEndcapInsertion = Step.factory.get("OpenROAD.TapEndcapInsertion")

tdi = TapEndcapInsertion(state_in=floorplan.state_out)
tdi.start()
```

```
──────────────────────────────────────────────────────────── Tap/Decap Insertion ────────────────────────────────────────────────────────────
[14:57:31] VERBOSE  Running 'OpenROAD.TapEndcapInsertion'…                                                                    step.py:1088
[14:57:31] VERBOSE  Logging subprocess to                                                                                      step.py:1268
                    openlane_run/20-openroad-tapendcapinsertion/openroad-tapendcapinsertion.log…
Reading OpenROAD database at '/content/openlane_run/19-openroad-floorplan/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:57:32] WARNING  [STA-0366] port 'clk' not found.                                                                          openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:57:32] WARNING  [STA-0366] port 'clk' not found.                                                                          openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:57:32] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                       openroad.py:235
[INFO] Setting timing derate to: 5%
[14:57:32] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                       openroad.py:235
[INFO TAP-0004] Inserted 52 endcaps.
[INFO TAP-0005] Inserted 70 tapcells.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/20-openroad-tapendcapinsertion/SISO.odb'…
Writing netlist to '/content/openlane_run/20-openroad-tapendcapinsertion/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/20-openroad-tapendcapinsertion/SISO.pnl.v'…
Writing layout to '/content/openlane_run/20-openroad-tapendcapinsertion/SISO.def'…
Writing timing constraints to '/content/openlane_run/20-openroad-tapendcapinsertion/SISO.sdc'…
```

Format	Path
nl	openlane_run/20-openroad-tapendcapinsertion/SISO.nl.v
pnl	openlane_run/20-openroad-tapendcapinsertion/SISO.pnl.v
def	openlane_run/20-openroad-tapendcapinsertion/SISO.def
odb	openlane_run/20-openroad-tapendcapinsertion/SISO.odb

```
display(tdi)
```

```
──────────────────────────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────────────────────
[14:57:32] VERBOSE  Running 'KLayout.Render'…                                                                                  step.py:1088
[14:57:32] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_svsulh8a/klayout-render.log…                            step.py:1268
```

Time Elapsed: 1.52s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

I/O Placement

This places metal pins at the edges of the design corresponding to the top level inputs and outputs for your design. These pins act as the interface with other designs when you integrate it with other designs.

```
IOPlacement = Step.factory.get("OpenROAD.IOPlacement")

ioplace = IOPlacement(state_in=tdi.state_out)
ioplace.start()
```

```
──────────────
```

This creates the power distribution network for your design, which is essentially a plaid pattern of horizontal and vertical "straps" across the design that is then connected to the rails' VDD and VSS (via the tap cells.)

You can find an explanation of how the power distribution network works at this link: https://openlane2.readthedocs.io/en/latest/usage/hardening_macros.html#pdn-generation

While we typically don't need to mess with the PDN too much, the SPM is a small design, so we're going to need to make the plaid pattern formed by the PDN a bit smaller.

```
GeneratePDN = Step.factory.get("OpenROAD.GeneratePDN")

pdn = GeneratePDN(
    state_in=ioplace.state_out,
    FP_PDN_VWIDTH=2,
    FP_PDN_HWIDTH=2,
    FP_PDN_VPITCH=30,
    FP_PDN_HPITCH=30,
)
pdn.start()
```

```
─────────────────────────────────── Power Distribution Network Generation ───────────────────────────────────
[14:57:36] VERBOSE  Running 'OpenROAD.GeneratePDN'…                                                  step.py:1088
[14:57:36] INFO     'FP_PDN_CFG' not explicitly set, setting it to                                openroad.py:1174
                    /content/openlane_ipynb/openlane/scripts/openroad/common/pdn_cfg.tcl…
[14:57:36] VERBOSE  Logging subprocess to                                                            step.py:1268
                    openlane_run/22-openroad-generatepdn/openroad-generatepdn.log…
Reading OpenROAD database at '/content/openlane_run/21-openroad-ioplacement/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:57:37] WARNING  [STA-0366] port 'clk' not found.                                                 openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:57:37] WARNING  [STA-0366] port 'clk' not found.                                                 openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:57:37] WARNING  [STA-0419] transition time can not be specified for virtual clocks.               openroad.py:235
[INFO] Setting timing derate to: 5%
[14:57:37] WARNING  [STA-0450] virtual clock clk can not be propagated.                              openroad.py:235
[INFO] Setting global connections...
[INFO PDN-0001] Inserting grid: stdcell_grid
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/22-openroad-generatepdn/SISO.odb'…
Writing netlist to '/content/openlane_run/22-openroad-generatepdn/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/22-openroad-generatepdn/SISO.pnl.v'…
Writing layout to '/content/openlane_run/22-openroad-generatepdn/SISO.def'…
Writing timing constraints to '/content/openlane_run/22-openroad-generatepdn/SISO.sdc'…
[INFO PSM-0040] All shapes on net VPWR are connected.
[INFO PSM-0040] All shapes on net VGND are connected.
```

Format	Path
nl	openlane_run/22-openroad-generatepdn/SISO.nl.v
pnl	openlane_run/22-openroad-generatepdn/SISO.pnl.v
def	openlane_run/22-openroad-generatepdn/SISO.def
odb	openlane_run/22-openroad-generatepdn/SISO.odb

```
display(pdn)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[14:57:37] VERBOSE  Running 'KLayout.Render'…                                                   step.py:1088
[14:57:37] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_6qahcnyv/klayout-render.log…  step.py:1268
```

Time Elapsed: 1.44s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Global Placement

Global Placement is deciding on a fuzzy, non-final location for each of the cells, with the aim of minimizing the distance between cells that are connected together (more specifically, the total length of the not-yet-created wires that will connect them).

As you will see in the `.display()` in the second cell below, the placement is considered "illegal", i.e., not properly aligned with the cell placement grid. This is addressed by "Detailed Placement", also referred to as "placement legalization", which is the next step.

```
GlobalPlacement = Step.factory.get("OpenROAD.GlobalPlacement")

gpl = GlobalPlacement(state_in=pdn.state_out)
gpl.start()
```

```
──────────────────────────────────────────────────────────── Global Placement ────────────────────────────────────────────────────────────
[14:57:38] VERBOSE  Running 'OpenROAD.GlobalPlacement'…                                                                          step.py:1088
[14:57:38] INFO     'PL_TARGET_DENSITY_PCT' not explicitly set, using dynamically calculated                                  openroad.py:1260
                    target density: 63.55400…
[14:57:38] VERBOSE  Logging subprocess to                                                                                        step.py:1268
                    openlane_run/23-openroad-globalplacement/openroad-globalplacement.log…
Reading OpenROAD database at '/content/openlane_run/22-openroad-generatepdn/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:57:39] WARNING  [STA-0366] port 'clk' not found.                                                                             openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:57:39] WARNING  [STA-0366] port 'clk' not found.                                                                             openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:57:39] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                          openroad.py:235
[INFO] Setting timing derate to: 5%
[14:57:39] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                          openroad.py:235
[INFO] Setting RC values…
[INFO] Setting signal min routing layer to: met1 and clock min routing layer to met1.
[INFO] Setting signal max routing layer to: met5 and clock max routing layer to met5.
[INFO GPL-0002] DBU: 1000
[INFO GPL-0003] SiteSize: (  0.460  2.720 ) um
[INFO GPL-0004] CoreBBox: (  5.520 10.880 ) ( 78.200 81.600 ) um
[INFO GPL-0006] NumInstances:               415
[INFO GPL-0007] NumPlaceInstances:          293
[INFO GPL-0008] NumFixedInstances:          122
[INFO GPL-0009] NumDummyInstances:            0
[INFO GPL-0010] NumNets:                    325
[INFO GPL-0011] NumPins:                   1094
[INFO GPL-0012] DieBBox:  (  0.000  0.000 ) ( 84.045 94.765 ) um
[INFO GPL-0013] CoreBBox: (  5.520 10.880 ) ( 78.200 81.600 ) um
[INFO GPL-0016] CoreArea:              5139.930 um^2
[INFO GPL-0017] NonPlaceInstsArea:      282.771 um^2
[INFO GPL-0018] PlaceInstsArea:        2665.056 um^2
[INFO GPL-0019] Util:                    54.869 %
[INFO GPL-0020] StdInstsArea:          2665.056 um^2
[INFO GPL-0021] MacroInstsArea:           0.000 um^2
[InitialPlace]  Iter: 1 CG residual: 0.00000010 HPWL: 10984720
[InitialPlace]  Iter: 2 CG residual: 0.00000010 HPWL: 7240658
[InitialPlace]  Iter: 3 CG residual: 0.00000010 HPWL: 6595639
[InitialPlace]  Iter: 4 CG residual: 0.00000011 HPWL: 6574643
[InitialPlace]  Iter: 5 CG residual: 0.00000009 HPWL: 6560245
[INFO GPL-0031] FillerInit:NumGCells:       340
[INFO GPL-0032] FillerInit:NumGNets:        325
[INFO GPL-0033] FillerInit:NumGPins:       1094
[INFO GPL-0023] TargetDensity:            0.636
[INFO GPL-0024] AvrgPlaceInstArea:        9.096 um^2
[INFO GPL-0025] IdealBinArea:            14.312 um^2
[INFO GPL-0026] IdealBinCnt:                359
[INFO GPL-0027] TotalBinArea:          5139.930 um^2
[INFO GPL-0028] BinCnt:        16     16
[INFO GPL-0029] BinSize: (  4.543  4.420 )
[INFO GPL-0030] NumBins: 256
[NesterovSolve] Iter:    1 overflow: 0.703 HPWL: 5494123
[INFO GPL-0100] worst slack 2.51e-09
[INFO GPL-0103] Weighted 29 nets.
[INFO GPL-0100] worst slack 2.48e-09
[INFO GPL-0103] Weighted 29 nets.
[NesterovSolve] Snapshot saved at iter = 3
[NesterovSolve] Iter:   10 overflow: 0.526 HPWL: 5927586
[NesterovSolve] Iter:   20 overflow: 0.524 HPWL: 5898256
[NesterovSolve] Iter:   30 overflow: 0.522 HPWL: 5892824
[NesterovSolve] Iter:   40 overflow: 0.523 HPWL: 5893540
[NesterovSolve] Iter:   50 overflow: 0.524 HPWL: 5894015
[NesterovSolve] Iter:   60 overflow: 0.523 HPWL: 5894909
[NesterovSolve] Iter:   70 overflow: 0.523 HPWL: 5895107
[NesterovSolve] Iter:   80 overflow: 0.523 HPWL: 5894031
[NesterovSolve] Iter:   90 overflow: 0.523 HPWL: 5893681
[NesterovSolve] Iter:  100 overflow: 0.523 HPWL: 5894881
[NesterovSolve] Iter:  110 overflow: 0.522 HPWL: 5895901
[NesterovSolve] Iter:  120 overflow: 0.522 HPWL: 5895926
[NesterovSolve] Iter:  130 overflow: 0.521 HPWL: 5896003
[NesterovSolve] Iter:  140 overflow: 0.519 HPWL: 5897195
[NesterovSolve] Iter:  150 overflow: 0.517 HPWL: 5899558
[NesterovSolve] Iter:  160 overflow: 0.513 HPWL: 5901736
[NesterovSolve] Iter:  170 overflow: 0.509 HPWL: 5904488
[NesterovSolve] Iter:  180 overflow: 0.503 HPWL: 5910052
[NesterovSolve] Iter:  190 overflow: 0.491 HPWL: 5913349
[INFO GPL-0100] worst slack 2.47e-09
[INFO GPL-0103] Weighted 29 nets.
[NesterovSolve] Iter:  200 overflow: 0.467 HPWL: 5902360
[NesterovSolve] Iter:  210 overflow: 0.438 HPWL: 5847206
[NesterovSolve] Iter:  220 overflow: 0.403 HPWL: 5770373
[NesterovSolve] Iter:  230 overflow: 0.370 HPWL: 5723600
[NesterovSolve] Iter:  240 overflow: 0.344 HPWL: 5721253
[NesterovSolve] Iter:  250 overflow: 0.316 HPWL: 5711731
[NesterovSolve] Iter:  260 overflow: 0.289 HPWL: 5716790
[INFO GPL-0100] worst slack 2.38e-09
[INFO GPL-0103] Weighted 29 nets.
[NesterovSolve] Iter:  270 overflow: 0.264 HPWL: 5742151
[NesterovSolve] Iter:  280 overflow: 0.242 HPWL: 5759494
[NesterovSolve] Iter:  290 overflow: 0.220 HPWL: 5778022
[INFO GPL-0100] worst slack 2.3e-09
[INFO GPL-0103] Weighted 29 nets.
[NesterovSolve] Iter:  300 overflow: 0.201 HPWL: 5802950
[INFO GPL-0075] Routability numCall: 1 inflationIterCnt: 1 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      12   13
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 156
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0
[INFO GPL-0065] OverflowTileCnt2: 0
[INFO GPL-0066] 0.5%RC: 1.0000
[INFO GPL-0067] 1.0%RC: 1.0000
[INFO GPL-0068] 2.0%RC: 1.0000
[INFO GPL-0069] 5.0%RC: 0.9591
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0000
[INFO GPL-0078] FinalRC lower than minRC (1e+30), min RC updated.
[INFO GPL-0045] InflatedAreaDelta:        0.000 um^2
[INFO GPL-0046] TargetDensity:            0.636
[INFO GPL-0049] WhiteSpaceArea:        4857.158 um^2
[INFO GPL-0050] NesterovInstsArea:     2665.056 um^2
[INFO GPL-0051] TotalFillerArea:        421.863 um^2
[INFO GPL-0052] TotalGCellsArea:       3086.919 um^2
[INFO GPL-0053] ExpectedGCellsArea:    3086.919 um^2
[INFO GPL-0054] NewTargetDensity:         0.636
[INFO GPL-0055] NewWhiteSpaceArea:     4857.158 um^2
[INFO GPL-0056] MovableArea:           3086.919 um^2
[INFO GPL-0057] NewNesterovInstArea:   2665.056 um^2
```

```
[INFO GPL-0058] NewTotalFillerArea:     421.863 um^2
[INFO GPL-0059] NewTotalGCellsArea:    3086.919 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter:  310 overflow: 0.523 HPWL: 5872113
[NesterovSolve] Iter:  320 overflow: 0.515 HPWL: 5847346
[NesterovSolve] Iter:  330 overflow: 0.518 HPWL: 5839385
[NesterovSolve] Iter:  340 overflow: 0.519 HPWL: 5845360
[NesterovSolve] Iter:  350 overflow: 0.517 HPWL: 5844672
[NesterovSolve] Iter:  360 overflow: 0.517 HPWL: 5841758
[NesterovSolve] Iter:  370 overflow: 0.518 HPWL: 5841458
[NesterovSolve] Iter:  380 overflow: 0.518 HPWL: 5842074
[NesterovSolve] Iter:  390 overflow: 0.517 HPWL: 5841996
[NesterovSolve] Iter:  400 overflow: 0.517 HPWL: 5841511
[NesterovSolve] Iter:  410 overflow: 0.517 HPWL: 5841986
[NesterovSolve] Iter:  420 overflow: 0.517 HPWL: 5842356
[NesterovSolve] Iter:  430 overflow: 0.516 HPWL: 5841580
[NesterovSolve] Iter:  440 overflow: 0.516 HPWL: 5841206
[NesterovSolve] Iter:  450 overflow: 0.516 HPWL: 5841962
[NesterovSolve] Iter:  460 overflow: 0.514 HPWL: 5842613
[NesterovSolve] Iter:  470 overflow: 0.513 HPWL: 5843282
[NesterovSolve] Iter:  480 overflow: 0.511 HPWL: 5843867
[NesterovSolve] Iter:  490 overflow: 0.509 HPWL: 5844726
[NesterovSolve] Iter:  500 overflow: 0.505 HPWL: 5842983
[NesterovSolve] Iter:  510 overflow: 0.497 HPWL: 5835551
[NesterovSolve] Iter:  520 overflow: 0.488 HPWL: 5826159
[NesterovSolve] Iter:  530 overflow: 0.479 HPWL: 5815501
[NesterovSolve] Iter:  540 overflow: 0.467 HPWL: 5801815
[NesterovSolve] Iter:  550 overflow: 0.449 HPWL: 5785749
[NesterovSolve] Iter:  560 overflow: 0.423 HPWL: 5735741
[NesterovSolve] Iter:  570 overflow: 0.396 HPWL: 5682331
[NesterovSolve] Iter:  580 overflow: 0.378 HPWL: 5669610
[NesterovSolve] Iter:  590 overflow: 0.355 HPWL: 5662115
[NesterovSolve] Iter:  600 overflow: 0.328 HPWL: 5649687
[NesterovSolve] Iter:  610 overflow: 0.302 HPWL: 5657538
[NesterovSolve] Iter:  620 overflow: 0.278 HPWL: 5679598
[NesterovSolve] Iter:  630 overflow: 0.258 HPWL: 5706224
[NesterovSolve] Iter:  640 overflow: 0.233 HPWL: 5720087
[NesterovSolve] Iter:  650 overflow: 0.215 HPWL: 5754183
[INFO GPL-0075] Routability numCall: 2 inflationIterCnt: 2 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      12   13
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 156
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0
[INFO GPL-0065] OverflowTileCnt2: 0
[INFO GPL-0066] 0.5%RC: 1.0000
[INFO GPL-0067] 1.0%RC: 1.0000
[INFO GPL-0068] 2.0%RC: 0.9889
[INFO GPL-0069] 5.0%RC: 0.9386
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0000
[INFO GPL-0079] MinRC (1) violation occurred, total count: 1.
[INFO GPL-0045] InflatedAreaDelta:        0.000 um^2
[INFO GPL-0046] TargetDensity:            0.636
[INFO GPL-0049] WhiteSpaceArea:        4857.158 um^2
[INFO GPL-0050] NesterovInstsArea:     2665.056 um^2
[INFO GPL-0051] TotalFillerArea:        421.863 um^2
[INFO GPL-0052] TotalGCellsArea:       3086.919 um^2
[INFO GPL-0053] ExpectedGCellsArea:    3086.919 um^2
[INFO GPL-0054] NewTargetDensity:         0.636
[INFO GPL-0055] NewWhiteSpaceArea:     4857.158 um^2
[INFO GPL-0056] MovableArea:           3086.919 um^2
[INFO GPL-0057] NewNesterovInstArea:   2665.056 um^2
[INFO GPL-0058] NewTotalFillerArea:     421.863 um^2
[INFO GPL-0059] NewTotalGCellsArea:    3086.919 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter:  660 overflow: 0.535 HPWL: 5973975
[NesterovSolve] Iter:  670 overflow: 0.520 HPWL: 5853490
[NesterovSolve] Iter:  680 overflow: 0.516 HPWL: 5838952
[NesterovSolve] Iter:  690 overflow: 0.520 HPWL: 5838857
[NesterovSolve] Iter:  700 overflow: 0.518 HPWL: 5843701
[NesterovSolve] Iter:  710 overflow: 0.517 HPWL: 5842741
[NesterovSolve] Iter:  720 overflow: 0.518 HPWL: 5840770
[NesterovSolve] Iter:  730 overflow: 0.518 HPWL: 5840981
[NesterovSolve] Iter:  740 overflow: 0.517 HPWL: 5841943
[NesterovSolve] Iter:  750 overflow: 0.517 HPWL: 5841280
[NesterovSolve] Iter:  760 overflow: 0.517 HPWL: 5841217
[NesterovSolve] Iter:  770 overflow: 0.517 HPWL: 5841740
[NesterovSolve] Iter:  780 overflow: 0.517 HPWL: 5841573
[NesterovSolve] Iter:  790 overflow: 0.516 HPWL: 5840480
[NesterovSolve] Iter:  800 overflow: 0.516 HPWL: 5840297
[NesterovSolve] Iter:  810 overflow: 0.515 HPWL: 5840933
[NesterovSolve] Iter:  820 overflow: 0.514 HPWL: 5840916
[NesterovSolve] Iter:  830 overflow: 0.513 HPWL: 5840673
[NesterovSolve] Iter:  840 overflow: 0.511 HPWL: 5840888
[NesterovSolve] Iter:  850 overflow: 0.508 HPWL: 5841242
[NesterovSolve] Iter:  860 overflow: 0.503 HPWL: 5838654
[NesterovSolve] Iter:  870 overflow: 0.494 HPWL: 5829441
[NesterovSolve] Iter:  880 overflow: 0.486 HPWL: 5819330
[NesterovSolve] Iter:  890 overflow: 0.475 HPWL: 5807768
[NesterovSolve] Iter:  900 overflow: 0.464 HPWL: 5796692
[NesterovSolve] Iter:  910 overflow: 0.443 HPWL: 5768619
[NesterovSolve] Iter:  920 overflow: 0.414 HPWL: 5717789
[NesterovSolve] Iter:  930 overflow: 0.390 HPWL: 5672429
[NesterovSolve] Iter:  940 overflow: 0.371 HPWL: 5667287
[NesterovSolve] Iter:  950 overflow: 0.347 HPWL: 5656782
[NesterovSolve] Iter:  960 overflow: 0.321 HPWL: 5653017
[NesterovSolve] Iter:  970 overflow: 0.294 HPWL: 5660951
[NesterovSolve] Iter:  980 overflow: 0.273 HPWL: 5682496
[NesterovSolve] Iter:  990 overflow: 0.252 HPWL: 5710917
[NesterovSolve] Iter: 1000 overflow: 0.227 HPWL: 5724906
[NesterovSolve] Iter: 1010 overflow: 0.209 HPWL: 5763050
[INFO GPL-0075] Routability numCall: 3 inflationIterCnt: 3 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      12   13
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 156
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0
[INFO GPL-0065] OverflowTileCnt2: 0
[INFO GPL-0066] 0.5%RC: 1.0000
[INFO GPL-0067] 1.0%RC: 1.0000
[INFO GPL-0068] 2.0%RC: 0.9889
[INFO GPL-0069] 5.0%RC: 0.9386
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0000
[INFO GPL-0079] MinRC (1) violation occurred, total count: 2.
[INFO GPL-0045] InflatedAreaDelta:        0.000 um^2
[INFO GPL-0046] TargetDensity:            0.636
[INFO GPL-0049] WhiteSpaceArea:        4857.158 um^2
[INFO GPL-0050] NesterovInstsArea:     2665.056 um^2
```

```
[INFO GPL-0051] TotalFillerArea:        421.863 um^2
[INFO GPL-0052] TotalGCellsArea:       3086.919 um^2
[INFO GPL-0053] ExpectedGCellsArea:    3086.919 um^2
[INFO GPL-0054] NewTargetDensity:         0.636
[INFO GPL-0055] NewWhiteSpaceArea:     4857.158 um^2
[INFO GPL-0056] MovableArea:           3086.919 um^2
[INFO GPL-0057] NewNesterovInstArea:   2665.056 um^2
[INFO GPL-0058] NewTotalFillerArea:     421.863 um^2
[INFO GPL-0059] NewTotalGCellsArea:    3086.919 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter: 1020 overflow: 0.521 HPWL: 5925600
[NesterovSolve] Iter: 1030 overflow: 0.517 HPWL: 5854950
[NesterovSolve] Iter: 1040 overflow: 0.517 HPWL: 5839530
[NesterovSolve] Iter: 1050 overflow: 0.520 HPWL: 5843892
[NesterovSolve] Iter: 1060 overflow: 0.518 HPWL: 5845493
[NesterovSolve] Iter: 1070 overflow: 0.517 HPWL: 5842872
[NesterovSolve] Iter: 1080 overflow: 0.518 HPWL: 5841330
[NesterovSolve] Iter: 1090 overflow: 0.518 HPWL: 5841766
[NesterovSolve] Iter: 1100 overflow: 0.517 HPWL: 5842235
[NesterovSolve] Iter: 1110 overflow: 0.517 HPWL: 5841584
[NesterovSolve] Iter: 1120 overflow: 0.517 HPWL: 5841699
[NesterovSolve] Iter: 1130 overflow: 0.517 HPWL: 5842332
[NesterovSolve] Iter: 1140 overflow: 0.516 HPWL: 5841975
[NesterovSolve] Iter: 1150 overflow: 0.516 HPWL: 5841170
[NesterovSolve] Iter: 1160 overflow: 0.516 HPWL: 5841595
[NesterovSolve] Iter: 1170 overflow: 0.515 HPWL: 5842439
[NesterovSolve] Iter: 1180 overflow: 0.514 HPWL: 5842978
[NesterovSolve] Iter: 1190 overflow: 0.512 HPWL: 5843372
[NesterovSolve] Iter: 1200 overflow: 0.510 HPWL: 5844514
[NesterovSolve] Iter: 1210 overflow: 0.507 HPWL: 5844212
[NesterovSolve] Iter: 1220 overflow: 0.500 HPWL: 5839553
[NesterovSolve] Iter: 1230 overflow: 0.492 HPWL: 5829843
[NesterovSolve] Iter: 1240 overflow: 0.483 HPWL: 5819255
[NesterovSolve] Iter: 1250 overflow: 0.472 HPWL: 5805943
[NesterovSolve] Iter: 1260 overflow: 0.459 HPWL: 5796319
[NesterovSolve] Iter: 1270 overflow: 0.434 HPWL: 5758446
[NesterovSolve] Iter: 1280 overflow: 0.405 HPWL: 5701832
[NesterovSolve] Iter: 1290 overflow: 0.385 HPWL: 5667659
[NesterovSolve] Iter: 1300 overflow: 0.365 HPWL: 5664282
[NesterovSolve] Iter: 1310 overflow: 0.338 HPWL: 5654438
[NesterovSolve] Iter: 1320 overflow: 0.312 HPWL: 5655942
[NesterovSolve] Iter: 1330 overflow: 0.288 HPWL: 5669394
[NesterovSolve] Iter: 1340 overflow: 0.267 HPWL: 5692861
[NesterovSolve] Iter: 1350 overflow: 0.242 HPWL: 5716796
[NesterovSolve] Iter: 1360 overflow: 0.221 HPWL: 5739099
[NesterovSolve] Iter: 1370 overflow: 0.203 HPWL: 5773801
[INFO GPL-0075] Routability numCall: 4 inflationIterCnt: 4 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      12   13
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 156
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0
[INFO GPL-0065] OverflowTileCnt2: 0
[INFO GPL-0066] 0.5%RC: 1.0000
[INFO GPL-0067] 1.0%RC: 1.0000
[INFO GPL-0068] 2.0%RC: 0.9889
[INFO GPL-0069] 5.0%RC: 0.9364
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0000
[INFO GPL-0079] MinRC (1) violation occurred, total count: 3.
[INFO GPL-0045] InflatedAreaDelta:        0.000 um^2
[INFO GPL-0046] TargetDensity:            0.636
Revert Routability Procedure. Target density higher than max, or minRC max violations.
[INFO GPL-0080] minRcViolatedCnt: 3
[INFO GPL-0047] SavedMinRC: 1.0000
[INFO GPL-0048] SavedTargetDensity: 0.6355
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter: 1380 overflow: 0.521 HPWL: 5873273
[NesterovSolve] Iter: 1390 overflow: 0.515 HPWL: 5844760
[NesterovSolve] Iter: 1400 overflow: 0.518 HPWL: 5836387
[NesterovSolve] Iter: 1410 overflow: 0.519 HPWL: 5843121
[NesterovSolve] Iter: 1420 overflow: 0.517 HPWL: 5843366
[NesterovSolve] Iter: 1430 overflow: 0.517 HPWL: 5841554
[NesterovSolve] Iter: 1440 overflow: 0.518 HPWL: 5840667
[NesterovSolve] Iter: 1450 overflow: 0.518 HPWL: 5841802
[NesterovSolve] Iter: 1460 overflow: 0.517 HPWL: 5841620
[NesterovSolve] Iter: 1470 overflow: 0.517 HPWL: 5841148
[NesterovSolve] Iter: 1480 overflow: 0.517 HPWL: 5841469
[NesterovSolve] Iter: 1490 overflow: 0.517 HPWL: 5841774
[NesterovSolve] Iter: 1500 overflow: 0.516 HPWL: 5840955
[NesterovSolve] Iter: 1510 overflow: 0.516 HPWL: 5840204
[NesterovSolve] Iter: 1520 overflow: 0.516 HPWL: 5840662
[NesterovSolve] Iter: 1530 overflow: 0.514 HPWL: 5840981
[NesterovSolve] Iter: 1540 overflow: 0.513 HPWL: 5840821
[NesterovSolve] Iter: 1550 overflow: 0.512 HPWL: 5840679
[NesterovSolve] Iter: 1560 overflow: 0.509 HPWL: 5841205
[NesterovSolve] Iter: 1570 overflow: 0.505 HPWL: 5840322
[NesterovSolve] Iter: 1580 overflow: 0.498 HPWL: 5833822
[NesterovSolve] Iter: 1590 overflow: 0.489 HPWL: 5823627
[NesterovSolve] Iter: 1600 overflow: 0.480 HPWL: 5812783
[NesterovSolve] Iter: 1610 overflow: 0.468 HPWL: 5799940
[NesterovSolve] Iter: 1620 overflow: 0.452 HPWL: 5786200
[NesterovSolve] Iter: 1630 overflow: 0.425 HPWL: 5739269
[NesterovSolve] Iter: 1640 overflow: 0.399 HPWL: 5683577
[NesterovSolve] Iter: 1650 overflow: 0.381 HPWL: 5667059
[NesterovSolve] Iter: 1660 overflow: 0.358 HPWL: 5661713
[NesterovSolve] Iter: 1670 overflow: 0.331 HPWL: 5649790
[NesterovSolve] Iter: 1680 overflow: 0.304 HPWL: 5655514
[NesterovSolve] Iter: 1690 overflow: 0.281 HPWL: 5676007
[NesterovSolve] Iter: 1700 overflow: 0.261 HPWL: 5700535
[NesterovSolve] Iter: 1710 overflow: 0.236 HPWL: 5715523
[NesterovSolve] Iter: 1720 overflow: 0.216 HPWL: 5748367
[NesterovSolve] Iter: 1730 overflow: 0.196 HPWL: 5779845
[NesterovSolve] Iter: 1740 overflow: 0.174 HPWL: 5798781
[NesterovSolve] Iter: 1750 overflow: 0.155 HPWL: 5827150
```

```
display(gpl)
```

```
────────────────────────────────────────── Render Image (w/ KLayout) ──────────────────────────────────────────
[14:57:43] VERBOSE  Running 'KLayout.Render'…                                                          step.py:1088
[14:57:43] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_ptnn1x7v/klayout-render.log…     step.py:1268
```

Time Elapsed: 4.92s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Detailed Placement

This aligns the fuzzy placement from before with the grid, "legalizing" it.

```
DetailedPlacement = Step.factory.get("OpenROAD.DetailedPlacement")

dpl = DetailedPlacement(state_in=gpl.state_out)
dpl.start()
```

```
────────────────────────────────────────────────────────────── Detailed Placement ──────────────────────────────────────────────────────────────
[14:57:44] VERBOSE  Running 'OpenROAD.DetailedPlacement'…                                                                          step.py:1088
[14:57:44] VERBOSE  Logging subprocess to                                                                                           step.py:1268
                    openlane_run/24-openroad-detailedplacement/openroad-detailedplacement.log…
Reading OpenROAD database at '/content/openlane_run/23-openroad-globalplacement/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:57:45] WARNING  [STA-0366] port 'clk' not found.                                                                              openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:57:45] WARNING  [STA-0366] port 'clk' not found.                                                                              openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:57:45] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                            openroad.py:235
[INFO] Setting timing derate to: 5%
[14:57:45] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                           openroad.py:235
Placement Analysis
---------------------------------
total displacement        625.7 u
average displacement        1.5 u
max displacement            7.6 u
original HPWL            5934.9 u
legalized HPWL           6534.3 u
delta HPWL                   10 %

[INFO DPL-0020] Mirrored 84 instances
[INFO DPL-0021] HPWL before            6534.3 u
[INFO DPL-0022] HPWL after             6411.8 u
[INFO DPL-0023] HPWL delta               -1.9 %
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/24-openroad-detailedplacement/SISO.odb'…
Writing netlist to '/content/openlane_run/24-openroad-detailedplacement/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/24-openroad-detailedplacement/SISO.pnl.v'…
Writing layout to '/content/openlane_run/24-openroad-detailedplacement/SISO.def'…
Writing timing constraints to '/content/openlane_run/24-openroad-detailedplacement/SISO.sdc'…
```

Format	Path
nl	openlane_run/24-openroad-detailedplacement/SISO.nl.v
pnl	openlane_run/24-openroad-detailedplacement/SISO.pnl.v
def	openlane_run/24-openroad-detailedplacement/SISO.def
odb	openlane_run/24-openroad-detailedplacement/SISO.odb

```
display(dpl)
```

```
────────────────────────────────────────────────────────────── Render Image (w/ KLayout) ──────────────────────────────────────────────────────────────
[14:57:46] VERBOSE  Running 'KLayout.Render'…                                                                                       step.py:1088
[14:57:46] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_i8y1mdf1/klayout-render.log…                                 step.py:1268
```

Time Elapsed: 1.44s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Clock Tree Synthesis (CTS)

With the cells now having a final placement, we can go ahead and create what is known as the clock tree, i.e., the hierarchical set of buffers used for clock signal to minimize what is known as "clock skew"- variable delay of the clock cycle from register to register because of factors such as metal wire length, clock load (number of gates connected to the same clock buffer,) et cetera.

The CTS step creates the cells and places the between the gaps in the detailed placement above.

```
CTS = Step.factory.get("OpenROAD.CTS")

cts = CTS(state_in=dpl.state_out)
cts.start()
```

```
────────────────────────────────────────────── Clock Tree Synthesis ──────────────────────────────────────────────
[14:57:48] VERBOSE  Running 'OpenROAD.CTS'…                                                          step.py:1088
[14:57:48] VERBOSE  Logging subprocess to openlane_run/25-openroad-cts/openroad-cts.log…             step.py:1268
Reading timing models for corner nom_tt_025C_1v80…
Reading timing library for the 'nom_tt_025C_1v80' corner at
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading timing models for corner nom_ff_n40C_1v95…
Reading timing library for the 'nom_ff_n40C_1v95' corner at
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ff_n40C_1v95.lib'…
Reading timing models for corner nom_ss_100C_1v60…
Reading timing library for the 'nom_ss_100C_1v60' corner at
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ss_100C_1v60.lib'…
Reading OpenROAD database at '/content/openlane_run/24-openroad-detailedplacement/SISO.odb'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:57:53] WARNING  [STA-0366] port 'clk' not found.                                                  openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:57:53] WARNING  [STA-0366] port 'clk' not found.                                                  openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:57:53] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                openroad.py:235
[INFO] Setting timing derate to: 5%
[14:57:53] WARNING  [STA-0450] virtual clock clk can not be propagated.                               openroad.py:235
[INFO] Setting RC values…
[INFO] Configuring cts characterization…
[INFO] Performing clock tree synthesis…
[INFO] Looking for the following net(s): clk
[INFO] Running Clock Tree Synthesis…
[INFO CTS-0050] Root buffer is sky130_fd_sc_hd__clkbuf_16.
[INFO CTS-0051] Sink buffer is sky130_fd_sc_hd__clkbuf_8.
[INFO CTS-0052] The following clock buffers will be used for CTS:
sky130_fd_sc_hd__clkbuf_2
sky130_fd_sc_hd__clkbuf_4
sky130_fd_sc_hd__clkbuf_8
[INFO CTS-0049] Characterization buffer is sky130_fd_sc_hd__clkbuf_8.
[14:58:06] WARNING  [CTS-0083] No clock nets have been found.                                         openroad.py:235
[INFO CTS-0008] TritonCTS found 0 clock nets.
[14:58:06] WARNING  [CTS-0082] No valid clock nets in the design.                                     openroad.py:235
[14:58:06] WARNING  [STA-0450] virtual clock clk can not be propagated.                               openroad.py:235
[INFO] Repairing long wires on clock nets…
[INFO RSZ-0058] Using max wire length 6335um.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/25-openroad-cts/SISO.odb'…
Writing netlist to '/content/openlane_run/25-openroad-cts/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/25-openroad-cts/SISO.pnl.v'…
Writing layout to '/content/openlane_run/25-openroad-cts/SISO.def'…
Writing timing constraints to '/content/openlane_run/25-openroad-cts/SISO.sdc'…
[INFO] Legalizing…
Placement Analysis
---------------------------------
total displacement          0.0 u
average displacement        0.0 u
max displacement            0.0 u
original HPWL            6411.8 u
legalized HPWL           6534.3 u
delta HPWL                    2 %

[INFO DPL-0020] Mirrored 84 instances
[INFO DPL-0021] HPWL before            6534.3 u
[INFO DPL-0022] HPWL after             6411.8 u
[INFO DPL-0023] HPWL delta               -1.9 %
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/25-openroad-cts/SISO.odb'…
Writing netlist to '/content/openlane_run/25-openroad-cts/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/25-openroad-cts/SISO.pnl.v'…
Writing layout to '/content/openlane_run/25-openroad-cts/SISO.def'…
Writing timing constraints to '/content/openlane_run/25-openroad-cts/SISO.sdc'…
```

Format	Path
nl	openlane_run/25-openroad-cts/SISO.nl.v
pnl	openlane_run/25-openroad-cts/SISO.pnl.v

```
display(cts)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[14:58:07] VERBOSE  Running 'KLayout.Render'…                                                  step.py:1088
[14:58:07] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_4qf735c_/klayout-render.log…  step.py:1268
```

Time Elapsed: 18.97s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Global Routing

Global routing "plans" the routes the wires between two gates (or gates and I/O pins/the PDN) will take. The results of global routing (which are called "routing guides") are stored in internal data structures and have no effect on the actual design, so there is no `display()` statement.

```
GlobalRouting = Step.factory.get("OpenROAD.GlobalRouting")

grt = GlobalRouting(state_in=cts.state_out)
grt.start()
```

```
──────────────────────────────────────────────────────── Global Routing ────────────────────────────────────────────────────────
[14:58:07] VERBOSE  Running 'OpenROAD.GlobalRouting'…                                                          step.py:1088
[14:58:07] VERBOSE  Logging subprocess to                                                                      step.py:1268
                    openlane_run/26-openroad-globalrouting/openroad-globalrouting.log…
Reading OpenROAD database at '/content/openlane_run/25-openroad-cts/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:58:08] WARNING  [STA-0366] port 'clk' not found.                                                        openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:58:08] WARNING  [STA-0366] port 'clk' not found.                                                        openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:58:08] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                      openroad.py:235
[INFO] Setting timing derate to: 5%
[14:58:08] WARNING  [STA-0450] virtual clock clk can not be propagated.                                     openroad.py:235
[14:58:08] WARNING  [STA-0450] virtual clock clk can not be propagated.                                     openroad.py:235
[INFO] Setting signal min routing layer to: met1 and clock min routing layer to met1.
[INFO] Setting signal max routing layer to: met5 and clock max routing layer to met5.
-congestion_iterations 50 -verbose
[INFO GRT-0020] Min routing layer: met1
[INFO GRT-0021] Max routing layer: met5
[INFO GRT-0022] Global adjustment: 30%
[INFO GRT-0023] Grid origin: (0, 0)
[INFO GRT-0043] No OR_DEFAULT vias defined.
[INFO GRT-0088] Layer li1     Track-Pitch = 0.4600  line-2-Via Pitch: 0.3400
[INFO GRT-0088] Layer met1    Track-Pitch = 0.3400  line-2-Via Pitch: 0.3400
[INFO GRT-0088] Layer met2    Track-Pitch = 0.4600  line-2-Via Pitch: 0.3500
[INFO GRT-0088] Layer met3    Track-Pitch = 0.6800  line-2-Via Pitch: 0.6150
[INFO GRT-0088] Layer met4    Track-Pitch = 0.9200  line-2-Via Pitch: 1.0400
[INFO GRT-0088] Layer met5    Track-Pitch = 3.4000  line-2-Via Pitch: 3.1100
[INFO GRT-0019] Found 0 clock nets.
[INFO GRT-0001] Minimum degree: 2
[INFO GRT-0002] Maximum degree: 34
[INFO GRT-0003] Macros: 0
[INFO GRT-0043] No OR_DEFAULT vias defined.
[INFO GRT-0004] Blockages: 255

[INFO GRT-0053] Routing resources analysis:
Routing      Original      Derated      Resource
Layer     Direction    Resources     Resources    Reduction (%)
-------------------------------------------------------------
li1        Vertical            0             0          0.00%
met1       Horizontal       3280          1619          50.64%
met2       Vertical         2381          1430          39.94%
met3       Horizontal       1634           965          40.94%
met4       Vertical          968           498          48.55%
met5       Horizontal        322           132          59.01%
-------------------------------------------------------------

[INFO GRT-0197] Via related to pin nodes: 1652
[INFO GRT-0198] Via related Steiner nodes: 15
[INFO GRT-0199] Via filling finished.
[INFO GRT-0111] Final number of vias: 2033
[INFO GRT-0112] Final usage 3D: 7006

[INFO GRT-0096] Final congestion report:
Layer         Resource        Demand        Usage (%)    Max H / Max V / Total Overflow
---------------------------------------------------------------------------------------
li1                  0             0            0.00%             0 /  0 /  0
met1              1619           385           23.78%             0 /  0 /  0
met2              1430           422           29.51%             0 /  0 /  0
met3               965            88            9.12%             0 /  0 /  0
met4               498            12            2.41%             0 /  0 /  0
met5               132             0            0.00%             0 /  0 /  0
---------------------------------------------------------------------------------------
Total             4644           907           19.53%             0 /  0 /  0

[INFO GRT-0018] Total wirelength: 11681 um
[INFO GRT-0014] Routed nets: 325
[INFO] Setting RC values…
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/26-openroad-globalrouting/SISO.odb'…
Writing layout to '/content/openlane_run/26-openroad-globalrouting/SISO.def'…
```

Format	Path
nl	openlane_run/25-openroad-cts/SISO.nl.v
pnl	openlane_run/25-openroad-cts/SISO.pnl.v

Detailed Routing

Detailed routing uses the guides from Global Routing to actually create wires on the metal layers and connect the gates, making the connections finally physical.

This is typically the longest step in the flow.

```
DetailedRouting = Step.factory.get("OpenROAD.DetailedRouting")

drt = DetailedRouting(state_in=grt.state_out)
drt.start()
```

```
Detailed Routing
[14:58:09] VERBOSE  Running 'OpenROAD.DetailedRouting'…                                   step.py:1088
[14:58:09] INFO     Running TritonRoute with 2 threads…                                  openroad.py:1619
[14:58:09] VERBOSE  Logging subprocess to                                                 step.py:1268
                    openlane_run/27-openroad-detailedrouting/openroad-detailedrouting.log…
Reading OpenROAD database at '/content/openlane_run/26-openroad-globalrouting/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:58:10] WARNING  [STA-0366] port 'clk' not found.                                      openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:58:10] WARNING  [STA-0366] port 'clk' not found.                                      openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:58:10] WARNING  [STA-0419] transition time can not be specified for virtual clocks.    openroad.py:235
[INFO] Setting timing derate to: 5%
[14:58:10] WARNING  [STA-0450] virtual clock clk can not be propagated.                   openroad.py:235
[INFO ORD-0030] Using 2 thread(s).
[INFO DRT-0149] Reading tech and libs.
[14:58:10] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer mcon
[14:58:10] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer mcon
[14:58:10] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via
[14:58:10] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via
[14:58:10] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via2
[14:58:10] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via2
[14:58:10] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via3
[14:58:10] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via3
[14:58:10] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via4
[14:58:10] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via4

Units:                1000
Number of layers:     13
Number of macros:     441
Number of vias:       29
Number of viarulegen: 25

[INFO DRT-0150] Reading design.

Design:                   SISO
Die area:                 ( 0 0 ) ( 84045 94765 )
Number of track patterns: 12
Number of DEF vias:       0
Number of components:     415
Number of terminals:      98
Number of snets:          2
Number of nets:           325

[INFO DRT-0167] List of default vias:
Layer via
default via: M1M2_PR
Layer via2
default via: M2M3_PR
Layer via3
default via: M3M4_PR
Layer via4
default via: M4M5_PR
[INFO DRT-0162] Library cell analysis.
[INFO DRT-0163] Instance analysis.
[INFO DRT-0164] Number of unique instances = 110.
[INFO DRT-0168] Init region query.
[INFO DRT-0024]   Complete FR_MASTERSLICE.
[INFO DRT-0024]   Complete Fr_VIA.
[INFO DRT-0024]   Complete li1.
[INFO DRT-0024]   Complete mcon.
[INFO DRT-0024]   Complete met1.
[INFO DRT-0024]   Complete via.
[INFO DRT-0024]   Complete met2.
[INFO DRT-0024]   Complete via2.
[INFO DRT-0024]   Complete met3.
[INFO DRT-0024]   Complete via3.
[INFO DRT-0024]   Complete met4.
[INFO DRT-0024]   Complete via4.
[INFO DRT-0024]   Complete met5.
[INFO DRT-0033] FR_MASTERSLICE shape region query size = 0.
[INFO DRT-0033] FR_VIA shape region query size = 0.
[INFO DRT-0033] li1 shape region query size = 8401.
[INFO DRT-0033] mcon shape region query size = 0.
[INFO DRT-0033] met1 shape region query size = 1164.
[INFO DRT-0033] via shape region query size = 324.
[INFO DRT-0033] met2 shape region query size = 148.
[INFO DRT-0033] via2 shape region query size = 270.
[INFO DRT-0033] met3 shape region query size = 218.
[INFO DRT-0033] via3 shape region query size = 270.
[INFO DRT-0033] met4 shape region query size = 70.
[INFO DRT-0033] via4 shape region query size = 8.
[INFO DRT-0033] met5 shape region query size = 16.
[INFO DRT-0165] Start pin access.
[INFO DRT-0078]   Complete 407 pins.
[INFO DRT-0079]   Complete 100 unique inst patterns.
[INFO DRT-0081]   Complete 104 unique inst patterns.
[INFO DRT-0084]   Complete 200 groups.
#scanned instances     = 415
#unique  instances     = 110
#stdCellGenAp          = 2810
#stdCellValidPlanarAp  = 28
#stdCellValidViaAp     = 2224
#stdCellPinNoAp        = 0
#stdCellPinCnt         = 998
#instTermValidViaApCnt = 0
#macroGenAp            = 0
#macroValidPlanarAp    = 0
#macroValidViaAp       = 0
#macroNoAp             = 0
[INFO DRT-0166] Complete pin access.
[INFO DRT-0267] cpu time = 00:00:18, elapsed time = 00:00:11, memory = 115.90 (MB), peak = 287.45 (MB)

Number of guides:     2119

[INFO DRT-0169] Post process guides.
[INFO DRT-0176] GCELLGRID X 0 DO 12 STEP 6900 ;
[INFO DRT-0177] GCELLGRID Y 0 DO 13 STEP 6900 ;
[INFO DRT-0028]   Complete FR_MASTERSLICE.
[INFO DRT-0028]   Complete Fr_VIA.
[INFO DRT-0028]   Complete li1.
[INFO DRT-0028]   Complete mcon.
```

```
[INFO DRT-0028]   Complete met1.
[INFO DRT-0028]   Complete via.
[INFO DRT-0028]   Complete met2.
[INFO DRT-0028]   Complete via2.
[INFO DRT-0028]   Complete met3.
[INFO DRT-0028]   Complete via3.
[INFO DRT-0028]   Complete met4.
[INFO DRT-0028]   Complete via4.
[INFO DRT-0028]   Complete met5.
[INFO DRT-0178] Init guide query.
[INFO DRT-0035]   Complete FR_MASTERSLICE (guide).
[INFO DRT-0035]   Complete Fr_VIA (guide).
[INFO DRT-0035]   Complete li1 (guide).
[INFO DRT-0035]   Complete mcon (guide).
[INFO DRT-0035]   Complete met1 (guide).
[INFO DRT-0035]   Complete via (guide).
[INFO DRT-0035]   Complete met2 (guide).
[INFO DRT-0035]   Complete via2 (guide).
[INFO DRT-0035]   Complete met3 (guide).
[INFO DRT-0035]   Complete via3 (guide).
[INFO DRT-0035]   Complete met4 (guide).
[INFO DRT-0035]   Complete via4 (guide).
[INFO DRT-0035]   Complete met5 (guide).
[INFO DRT-0036] FR_MASTERSLICE guide region query size = 0.
[INFO DRT-0036] FR_VIA guide region query size = 0.
[INFO DRT-0036] li1 guide region query size = 726.
[INFO DRT-0036] mcon guide region query size = 0.
[INFO DRT-0036] met1 guide region query size = 554.
[INFO DRT-0036] via guide region query size = 0.
[INFO DRT-0036] met2 guide region query size = 318.
[INFO DRT-0036] via2 guide region query size = 0.
[INFO DRT-0036] met3 guide region query size = 60.
[INFO DRT-0036] via3 guide region query size = 0.
[INFO DRT-0036] met4 guide region query size = 2.
[INFO DRT-0036] via4 guide region query size = 0.
[INFO DRT-0036] met5 guide region query size = 0.
[INFO DRT-0179] Init gr pin query.
[INFO DRT-0245] skipped writing guide updates to database.
[INFO DRT-0185] Post process initialize RPin region query.
[INFO DRT-0181] Start track assignment.
[INFO DRT-0184] Done with 1046 vertical wires in 1 frboxes and 614 horizontal wires in 1 frboxes.
[INFO DRT-0186] Done with 94 vertical wires in 1 frboxes and 133 horizontal wires in 1 frboxes.
[INFO DRT-0182] Complete track assignment.
[INFO DRT-0267] cpu time = 00:00:00, elapsed time = 00:00:00, memory = 118.83 (MB), peak = 287.45 (MB)
[INFO DRT-0187] Start routing data preparation.
[INFO DRT-0267] cpu time = 00:00:00, elapsed time = 00:00:00, memory = 118.83 (MB), peak = 287.45 (MB)
[INFO DRT-0194] Start detail routing.
[INFO DRT-0195] Start 0th optimization iteration.
Completing 10% with 0 violations.
elapsed time = 00:00:01, memory = 128.57 (MB).
Completing 20% with 15 violations.
elapsed time = 00:00:02, memory = 143.90 (MB).
Completing 30% with 30 violations.
elapsed time = 00:00:04, memory = 150.46 (MB).
Completing 40% with 52 violations.
elapsed time = 00:00:05, memory = 150.46 (MB).
[INFO DRT-0199]   Number of violations = 83.
Viol/Layer         li1   met1   met2
Metal Spacing        2     23      1
Recheck              1      8      6
Short                0     28     14
[INFO DRT-0267] cpu time = 00:00:05, elapsed time = 00:00:05, memory = 497.53 (MB), peak = 497.53 (MB)
Total wire length = 6947 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 2752 um.
Total wire length on LAYER met2 = 3178 um.
Total wire length on LAYER met3 = 945 um.
Total wire length on LAYER met4 = 70 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 2024.
Up-via summary (total 2024):

-----------------------
FR_MASTERSLICE       0
li1     979
met1     980
met2      61
met3       4
met4       0
-----------------------
2024


[INFO DRT-0195] Start 1st optimization iteration.
Completing 10% with 83 violations.
elapsed time = 00:00:00, memory = 497.53 (MB).
Completing 20% with 83 violations.
elapsed time = 00:00:00, memory = 497.53 (MB).
Completing 30% with 83 violations.
elapsed time = 00:00:01, memory = 497.53 (MB).
Completing 40% with 76 violations.
elapsed time = 00:00:01, memory = 497.53 (MB).
Completing 50% with 76 violations.
elapsed time = 00:00:01, memory = 497.53 (MB).
Completing 60% with 50 violations.
elapsed time = 00:00:02, memory = 497.83 (MB).
[INFO DRT-0199]   Number of violations = 7.
Viol/Layer        met1   met2
Metal Spacing        4      1
Recheck              2      0
[INFO DRT-0267] cpu time = 00:00:03, elapsed time = 00:00:03, memory = 497.83 (MB), peak = 508.16 (MB)
Total wire length = 6858 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 2719 um.
Total wire length on LAYER met2 = 3127 um.
Total wire length on LAYER met3 = 941 um.
Total wire length on LAYER met4 = 70 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 1990.
Up-via summary (total 1990):

-----------------------
FR_MASTERSLICE       0
li1     978
met1     945
met2      63
met3       4
met4       0
-----------------------
1990


[INFO DRT-0195] Start 2nd optimization iteration.
Completing 10% with 7 violations.
elapsed time = 00:00:00, memory = 497.83 (MB).
Completing 20% with 7 violations.
elapsed time = 00:00:00, memory = 497.83 (MB).
Completing 30% with 7 violations.
```

```
elapsed time = 00:00:00, memory = 497.83 (MB).
Completing 40% with 7 violations.
elapsed time = 00:00:00, memory = 497.83 (MB).
Completing 50% with 7 violations.
elapsed time = 00:00:00, memory = 497.83 (MB).
Completing 60% with 7 violations.
elapsed time = 00:00:00, memory = 497.83 (MB).
Completing 70% with 7 violations.
elapsed time = 00:00:00, memory = 497.83 (MB).
Completing 80% with 7 violations.
elapsed time = 00:00:00, memory = 497.83 (MB).
Completing 90% with 2 violations.
elapsed time = 00:00:02, memory = 497.83 (MB).
Completing 100% with 2 violations.
elapsed time = 00:00:02, memory = 497.83 (MB).
[INFO DRT-0199]   Number of violations = 2.
Viol/Layer        met1   met2
Metal Spacing        1      1
[INFO DRT-0267] cpu time = 00:00:03, elapsed time = 00:00:02, memory = 497.83 (MB), peak = 508.16 (MB)
Total wire length = 6841 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 2705 um.
Total wire length on LAYER met2 = 3122 um.
Total wire length on LAYER met3 = 942 um.
Total wire length on LAYER met4 = 70 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 1987.
Up-via summary (total 1987):

-----------------------
FR_MASTERSLICE       0
li1     978
met1     942
met2      63
met3       4
met4       0
-----------------------
1987


[INFO DRT-0195] Start 3rd optimization iteration.
Completing 10% with 2 violations.
elapsed time = 00:00:00, memory = 503.75 (MB).
Completing 20% with 0 violations.
elapsed time = 00:00:00, memory = 503.75 (MB).
Completing 30% with 0 violations.
elapsed time = 00:00:00, memory = 503.75 (MB).
Completing 40% with 0 violations.
elapsed time = 00:00:00, memory = 503.75 (MB).
[INFO DRT-0199]   Number of violations = 0.
[INFO DRT-0267] cpu time = 00:00:00, elapsed time = 00:00:00, memory = 503.75 (MB), peak = 508.16 (MB)
Total wire length = 6835 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 2696 um.
Total wire length on LAYER met2 = 3125 um.
Total wire length on LAYER met3 = 942 um.
Total wire length on LAYER met4 = 70 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 1988.
Up-via summary (total 1988):

-----------------------
FR_MASTERSLICE       0
li1     978
met1     943
met2      63
met3       4
met4       0
-----------------------
1988


[INFO DRT-0198] Complete detail routing.
Total wire length = 6835 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 2696 um.
Total wire length on LAYER met2 = 3125 um.
Total wire length on LAYER met3 = 942 um.
Total wire length on LAYER met4 = 70 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 1988.
Up-via summary (total 1988):

-----------------------
FR_MASTERSLICE       0
li1     978
met1     943
met2      63
met3       4
met4       0
-----------------------
```

Start coding or generate with AI.

Double-click (or enter) to edit

```
display(drt)
```

```
────────────────────────────────────────── Render Image (w/ KLayout) ──────────────────────────────────────────
[14:58:35] VERBOSE  Running 'KLayout.Render'…                                                          step.py:1088
[14:58:35] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_jbwj118l/klayout-render.log…     step.py:1268
```

Time Elapsed: 26.32s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Fill Insertion

Finally, as we're done placing all the essential cells, the only thing left to do is fill in the gaps.

We prioritize the use of decap (decoupling capacitor) cells, which further supports the power distribution network, but when there aren't any small enough cells, we just use regular fill cells.

```
FillInsertion = Step.factory.get("OpenROAD.FillInsertion")
fill = FillInsertion(state_in=drt.state_out)
fill.start()
```

```
──────────────────────────────────────────────────────── Fill Insertion ────────────────────────────────────────────────────────
[14:58:36] VERBOSE  Running 'OpenROAD.FillInsertion'…                                                          step.py:1088
[14:58:36] VERBOSE  Logging subprocess to                                                                      step.py:1268
                    openlane_run/28-openroad-fillinsertion/openroad-fillinsertion.log…
Reading OpenROAD database at '/content/openlane_run/27-openroad-detailedrouting/SISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[14:58:37] WARNING  [STA-0366] port 'clk' not found.                                                           openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[14:58:37] WARNING  [STA-0366] port 'clk' not found.                                                           openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[14:58:37] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                         openroad.py:235
[INFO] Setting timing derate to: 5%
[14:58:37] WARNING  [STA-0450] virtual clock clk can not be propagated.                                        openroad.py:235
sky130_ef_sc_hd__decap_12 sky130_fd_sc_hd__decap_8 sky130_fd_sc_hd__decap_6 sky130_fd_sc_hd__decap_4
sky130_fd_sc_hd__decap_3 sky130_fd_sc_hd__fill*
[INFO DPL-0001] Placed 362 filler instances.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/28-openroad-fillinsertion/SISO.odb'…
Writing netlist to '/content/openlane_run/28-openroad-fillinsertion/SISO.nl.v'…
Writing powered netlist to '/content/openlane_run/28-openroad-fillinsertion/SISO.pnl.v'…
Writing layout to '/content/openlane_run/28-openroad-fillinsertion/SISO.def'…
Writing timing constraints to '/content/openlane_run/28-openroad-fillinsertion/SISO.sdc'…
```

Format	Path
nl	openlane_run/28-openroad-fillinsertion/SISO.nl.v
pnl	openlane_run/28-openroad-fillinsertion/SISO.pnl.v
def	openlane_run/28-openroad-fillinsertion/SISO.def
odb	openlane_run/28-openroad-fillinsertion/SISO.odb

```
display(fill)
```

```
──────────────────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────────────────
[14:58:37] VERBOSE  Running 'KLayout.Render'…                                                                  step.py:1088
[14:58:37] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_pm6_x4cx/klayout-render.log…            step.py:1268
```

Time Elapsed: 1.03s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Parasitics Extraction a.k.a. Resistance/Capacitance Extraction (RCX)

This step does not alter the design- rather, it computes the Parasitic elements of the circuit, which have an effect of timing, as we prepare to do the final timing analysis.

The parasitic elements are saved in the **Standard Parasitics Exchange Format**, or SPEF. OpenLane creates a SPEF file for each interconnect corner as described in the Corners and STA section of the documentation.

```
RCX = Step.factory.get("OpenROAD.RCX")

rcx = RCX(state_in=fill.state_out)
rcx.start()
```

```
─────────────────────────────── Parasitic Resistance/Capacitance Extraction ───────────────────────────────
[14:58:38] VERBOSE  Running 'OpenROAD.RCX'…                                                    step.py:1088
[14:58:39] INFO     Running RCX for corners matching min_*                                  openroad.py:1748
                    (/content/openlane_run/29-openroad-rcx/min/rcx.log)…
[14:58:39] VERBOSE  Logging subprocess to openlane_run/29-openroad-rcx/min/rcx.log…            step.py:1268
[14:58:39] INFO     Running RCX for corners matching nom_*                                  openroad.py:1748
                    (/content/openlane_run/29-openroad-rcx/nom/rcx.log)…
[14:58:39] VERBOSE  Logging subprocess to openlane_run/29-openroad-rcx/nom/rcx.log…            step.py:1268
[14:58:40] INFO     Finished RCX for corners matching min_*.                                openroad.py:1757
[14:58:40] INFO     Running RCX for corners matching max_*                                  openroad.py:1748
                    (/content/openlane_run/29-openroad-rcx/max/rcx.log)…
[14:58:40] VERBOSE  Logging subprocess to openlane_run/29-openroad-rcx/max/rcx.log…            step.py:1268
[14:58:40] INFO     Finished RCX for corners matching nom_*.                                openroad.py:1757
[14:58:41] INFO     Finished RCX for corners matching max_*.                                openroad.py:1757
```

Format	Path
nl	openlane_run/28-openroad-fillinsertion/SISO.nl.v
pnl	openlane_run/28-openroad-fillinsertion/SISO.pnl.v
def	openlane_run/28-openroad-fillinsertion/SISO.def
odb	openlane_run/28-openroad-fillinsertion/SISO.odb
sdc	openlane_run/28-openroad-fillinsertion/SISO.sdc
spef	nom_* openlane_run/29-openroad-rcx/nom/SISO.nom.spef min_* openlane_run/29-openroad-rcx/min/SISO.min.spef max_* openlane_run/29-openroad-rcx/max/SISO.max.spef

Static Timing Analysis (Post-PnR)

STA is a process that verifies that a chip meets certain constraints on clock and data timings to run at its rated clock speed. See Corners and STA in the documentation for more info.

This step generates two kinds of files:

- `.lib` : Liberty™-compatible Library files. Can be used to do static timing analysis when creating a design with this design as a sub-macro.
- `.sdf` : Standard Delay Format. Can be used with certain simulation software to do *dynamic* timing analysis.

Unfortunately, the `.lib` files coming out of OpenLane right now are not super reliable for timing purposes and are only provided for completeness. When using OpenLane-created macros withing other designs, it is best to use the macro's final netlist and extracted parasitics instead.

```
STAPostPNR = Step.factory.get("OpenROAD.STAPostPNR")

sta_post_pnr = STAPostPNR(state_in=rcx.state_out)
sta_post_pnr.start()
```

```
──────────────────────────────────────── Static Timing Analysis (Post-PnR) ────────────────────────────────────────
[14:58:41] VERBOSE  Running 'OpenROAD.STAPostPNR'…                                                   step.py:1088
[14:58:41] INFO     Starting STA for the nom_tt_025C_1v80 timing corner…                           openroad.py:561
[14:58:41] INFO     Starting STA for the nom_ss_100C_1v60 timing corner…                           openroad.py:561
[14:58:41] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/nom_tt_025C_1v80/sta.log…
[14:58:41] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/nom_ss_100C_1v60/sta.log…
[14:58:42] INFO     Finished STA for the nom_ss_100C_1v60 timing corner.                           openroad.py:576
[14:58:42] INFO     Finished STA for the nom_tt_025C_1v80 timing corner.                           openroad.py:576
[14:58:42] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/nom_tt_025C_1v80/filter_unannotated.log…
[14:58:42] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/nom_ss_100C_1v60/filter_unannotated.log…
[14:58:43] INFO     Starting STA for the nom_ff_n40C_1v95 timing corner…                           openroad.py:561
[14:58:43] INFO     Starting STA for the min_tt_025C_1v80 timing corner…                           openroad.py:561
[14:58:43] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/nom_ff_n40C_1v95/sta.log…
[14:58:43] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/min_tt_025C_1v80/sta.log…
[14:58:44] INFO     Finished STA for the min_tt_025C_1v80 timing corner.                           openroad.py:576
[14:58:44] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/min_tt_025C_1v80/filter_unannotated.log…
[14:58:46] INFO     Starting STA for the min_ss_100C_1v60 timing corner…                           openroad.py:561
[14:58:46] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/min_ss_100C_1v60/sta.log…
[14:58:46] INFO     Finished STA for the nom_ff_n40C_1v95 timing corner.                           openroad.py:576
[14:58:46] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/nom_ff_n40C_1v95/filter_unannotated.log…
[14:58:47] INFO     Finished STA for the min_ss_100C_1v60 timing corner.                           openroad.py:576
[14:58:47] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/min_ss_100C_1v60/filter_unannotated.log…
[14:58:47] INFO     Starting STA for the min_ff_n40C_1v95 timing corner…                           openroad.py:561
[14:58:47] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/min_ff_n40C_1v95/sta.log…
[14:58:48] INFO     Starting STA for the max_tt_025C_1v80 timing corner…                           openroad.py:561
[14:58:48] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/max_tt_025C_1v80/sta.log…
[14:58:50] INFO     Finished STA for the max_tt_025C_1v80 timing corner.                           openroad.py:576
[14:58:50] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/max_tt_025C_1v80/filter_unannotated.log…
[14:58:50] INFO     Finished STA for the min_ff_n40C_1v95 timing corner.                           openroad.py:576
[14:58:50] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/min_ff_n40C_1v95/filter_unannotated.log…
[14:58:51] INFO     Starting STA for the max_ss_100C_1v60 timing corner…                           openroad.py:561
[14:58:51] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/max_ss_100C_1v60/sta.log…
[14:58:51] INFO     Starting STA for the max_ff_n40C_1v95 timing corner…                           openroad.py:561
[14:58:51] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/max_ff_n40C_1v95/sta.log…
[14:58:53] INFO     Finished STA for the max_ss_100C_1v60 timing corner.                           openroad.py:576
[14:58:53] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/max_ss_100C_1v60/filter_unannotated.log…
[14:58:56] INFO     Finished STA for the max_ff_n40C_1v95 timing corner.                           openroad.py:576
[14:58:56] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/30-openroad-stapostpnr/max_ff_n40C_1v95/filter_unannotated.log…
```

Corner/Group	Hold Worst Slack	Reg to Reg Paths	Hold TNS	Hold Vio Count	of whi… reg to reg	Setup Worst Slack	Reg to Reg Pat…	Setup TNS	Set… Vio Cou…	of which reg to reg	Max Cap Vio…	Max Slew Viol…
Overall	4.02…	N/A	0.0…	0	0	-2.4…	N/A	-64.…	93	0	5	36
nom_tt_025C_1v80	4.18…	N/A	0.0…	0	0	1.72…	N/A	0.00…	0	0	0	36
nom_ss_100C_1v60	4.59…	N/A	0.0…	0	0	-2.3…	N/A	-62.…	31	0	5	36
nom_ff_n40C_1v95	4.02…	N/A	0.0…	0	0	3.26…	N/A	0.00…	0	0	0	4
min_tt_025C_1v80	4.17…	N/A	0.0…	0	0	1.76…	N/A	0.00…	0	0	0	36
min_ss_100C_1v60	4.58…	N/A	0.0…	0	0	-2.2…	N/A	-60.…	31	0	3	36
min_ff_n40C_1v95	4.02…	N/A	0.0…	0	0	3.29…	N/A	0.00…	0	0	0	2
max_tt_025C_1v80	4.18…	N/A	0.0…	0	0	1.68…	N/A	0.00…	0	0	0	36
max_ss_100C_1v60	4.60…	N/A	0.0…	0	0	-2.4…	N/A	-64.…	31	0	5	36
max_ff_n40C_1v95	4.03…	N/A	0.0…	0	0	3.23…	N/A	0.00…	0	0	0	4

Corner/Group	Hold Worst Slack	Reg to Reg Paths	Hold TNS	Hold Vio Count	of which reg to reg	Setup Worst Slack	Reg to Reg Paths	Setup TNS	Setup Vio Count	of which reg to reg	Max Cap Violatio…	Max Slew Violati…
Overall	4.0245	N/A	0.0000	0	0	-2.4145	N/A	-64.1156	93	0	5	36
nom_tt_025C_1v80	4.1817	N/A	0.0000	0	0	1.7292	N/A	0.0000	0	0	0	36
nom_ss_100C_1v60	4.5913	N/A	0.0000	0	0	-2.3454	N/A	-62.0659	31	0	5	36
nom_ff_n40C_1v95	4.0279	N/A	0.0000	0	0	3.2657	N/A	0.0000	0	0	0	4
min_tt_025C_1v80	4.1751	N/A	0.0000	0	0	1.7661	N/A	0.0000	0	0	0	36
min_ss_100C_1v60	4.5837	N/A	0.0000	0	0	-2.2977	N/A	-60.4811	31	0	3	36
min_ff_n40C_1v95	4.0245	N/A	0.0000	0	0	3.2913	N/A	0.0000	0	0	0	2
max_tt_025C_1v80	4.1888	N/A	0.0000	0	0	1.6889	N/A	0.0000	0	0	0	36
max_ss_100C_1v60	4.6011	N/A	0.0000	0	0	-2.4145	N/A	-64.1156	31	0	5	36
max_ff_n40C_1v95	4.0325	N/A	0.0000	0	0	3.2373	N/A	0.0000	0	0	0	4

Format	Path
nl	openlane_run/28-openroad-fillinsertion/SISO.nl.v
pnl	openlane_run/28-openroad-fillinsertion/SISO.pnl.v
def	openlane_run/28-openroad-fillinsertion/SISO.def
odb	openlane_run/28-openroad-fillinsertion/SISO.odb
sdc	openlane_run/28-openroad-fillinsertion/SISO.sdc
sdf	nom_tt_025C_1v80 openlane_run/30-openroad-stapostpnr/nom_tt_025C_1v80/SISO__nom_tt_025C_1v80.sdf
	nom_ss_100C_1v60 openlane_run/30-openroad-stapostpnr/nom_ss_100C_1v60/SISO__nom_ss_100C_1v60.sdf
	nom_ff_n40C_1v95 openlane_run/30-openroad-stapostpnr/nom_ff_n40C_1v95/SISO__nom_ff_n40C_1v95.sdf
	min_tt_025C_1v80 openlane_run/30-openroad-stapostpnr/min_tt_025C_1v80/SISO__min_tt_025C_1v80.sdf
	min_ss_100C_1v60 openlane_run/30-openroad-stapostpnr/min_ss_100C_1v60/SISO__min_ss_100C_1v60.sdf
	min_ff_n40C_1v95 openlane_run/30-openroad-stapostpnr/min_ff_n40C_1v95/SISO__min_ff_n40C_1v95.sdf
	max_tt_025C_1v80 openlane_run/30-openroad-stapostpnr/max_tt_025C_1v80/SISO__max_tt_025C_1v80.sdf
	max_ss_100C_1v60 openlane_run/30-openroad-stapostpnr/max_ss_100C_1v60/SISO__max_ss_100C_1v60.sdf
	max_ff_n40C_1v95 openlane_run/30-openroad-stapostpnr/max_ff_n40C_1v95/SISO__max_ff_n40C_1v95.sdf
spef	nom_* openlane_run/29-openroad-rcx/nom/SISO.nom.spef
	min_* openlane_run/29-openroad-rcx/min/SISO.min.spef
	max_* openlane_run/29-openroad-rcx/max/SISO.max.spef
lib	nom_tt_025C_1v80 openlane_run/30-openroad-stapostpnr/nom_tt_025C_1v80/SISO__nom_tt_025C_1v80.lib
	nom_ss_100C_1v60 openlane_run/30-openroad-stapostpnr/nom_ss_100C_1v60/SISO__nom_ss_100C_1v60.lib
	nom_ff_n40C_1v95 openlane_run/30-openroad-stapostpnr/nom_ff_n40C_1v95/SISO__nom_ff_n40C_1v95.lib
	min_tt_025C_1v80 openlane_run/30-openroad-stapostpnr/min_tt_025C_1v80/SISO__min_tt_025C_1v80.lib
	min_ss_100C_1v60 openlane_run/30-openroad-stapostpnr/min_ss_100C_1v60/SISO__min_ss_100C_1v60.lib

Stream-out

Stream-out is the process of converting the designs from the abstract formats using during floorplanning, placement and routing into a concrete format called GDSII (lit. Graphic Design System 2), which is the final file that is then sent for fabrication.

```
StreamOut = Step.factory.get("KLayout.StreamOut")

gds = StreamOut(state_in=sta_post_pnr.state_out)
gds.start()
```

```
──────────────────────────────────────── GDSII Stream Out (KLayout) ────────────────────────────────────────
[14:58:56] VERBOSE  Running 'KLayout.StreamOut'…                                                  step.py:1088
[14:58:57] VERBOSE  Logging subprocess to openlane_run/31-klayout-streamout/klayout-streamout.log…  step.py:1268
[INFO] Clearing cells…
[INFO] Merging GDS files…
[INFO] Copying top level cell 'SISO'…
[INFO] Checking for missing GDS…
[INFO] All LEF cells have matching GDS cells.
[INFO] Writing out GDS '/content/openlane_run/31-klayout-streamout/SISO.klayout.gds'…
[INFO] Done.
```

Format	Path
nl	openlane_run/28-openroad-fillinsertion/SISO.nl.v
pnl	openlane_run/28-openroad-fillinsertion/SISO.pnl.v
def	openlane_run/28-openroad-fillinsertion/SISO.def
odb	openlane_run/28-openroad-fillinsertion/SISO.odb
sdc	openlane_run/28-openroad-fillinsertion/SISO.sdc
sdf	nom_tt_025C_1v80 openlane_run/30-openroad-stapostpnr/nom_tt_025C_1v80/SISO__nom_tt_025C_1v80.sdf
	nom_ss_100C_1v60 openlane_run/30-openroad-stapostpnr/nom_ss_100C_1v60/SISO__nom_ss_100C_1v60.sdf
	nom_ff_n40C_1v95 openlane_run/30-openroad-stapostpnr/nom_ff_n40C_1v95/SISO__nom_ff_n40C_1v95.sdf
	min_tt_025C_1v80 openlane_run/30-openroad-stapostpnr/min_tt_025C_1v80/SISO__min_tt_025C_1v80.sdf
	min_ss_100C_1v60 openlane_run/30-openroad-stapostpnr/min_ss_100C_1v60/SISO__min_ss_100C_1v60.sdf
	min_ff_n40C_1v95 openlane_run/30-openroad-stapostpnr/min_ff_n40C_1v95/SISO__min_ff_n40C_1v95.sdf
	max_tt_025C_1v80 openlane_run/30-openroad-stapostpnr/max_tt_025C_1v80/SISO__max_tt_025C_1v80.sdf
	max_ss_100C_1v60 openlane_run/30-openroad-stapostpnr/max_ss_100C_1v60/SISO__max_ss_100C_1v60.sdf
	max_ff_n40C_1v95 openlane_run/30-openroad-stapostpnr/max_ff_n40C_1v95/SISO__max_ff_n40C_1v95.sdf
spef	nom_* openlane_run/29-openroad-rcx/nom/SISO.nom.spef
	min_* openlane_run/29-openroad-rcx/min/SISO.min.spef
	max_* openlane_run/29-openroad-rcx/max/SISO.max.spef
lib	nom_tt_025C_1v80 openlane_run/30-openroad-stapostpnr/nom_tt_025C_1v80/SISO__nom_tt_025C_1v80.lib
	nom_ss_100C_1v60 openlane_run/30-openroad-stapostpnr/nom_ss_100C_1v60/SISO__nom_ss_100C_1v60.lib
	nom_ff_n40C_1v95 openlane_run/30-openroad-stapostpnr/nom_ff_n40C_1v95/SISO__nom_ff_n40C_1v95.lib
	min_tt_025C_1v80 openlane_run/30-openroad-stapostpnr/min_tt_025C_1v80/SISO__min_tt_025C_1v80.lib
	min_ss_100C_1v60 openlane_run/30-openroad-stapostpnr/min_ss_100C_1v60/SISO__min_ss_100C_1v60.lib
	min_ff_n40C_1v95 openlane_run/30-openroad-stapostpnr/min_ff_n40C_1v95/SISO__min_ff_n40C_1v95.lib
	max_tt_025C_1v80 openlane_run/30-openroad-stapostpnr/max_tt_025C_1v80/SISO__max_tt_025C_1v80.lib
	max_ss_100C_1v60 openlane_run/30-openroad-stapostpnr/max_ss_100C_1v60/SISO__max_ss_100C_1v60.lib
	max_ff_n40C_1v95 openlane_run/30-openroad-stapostpnr/max_ff_n40C_1v95/SISO__max_ff_n40C_1v95.lib
gds	openlane_run/31-klayout-streamout/SISO.gds
klayout_gds	openlane_run/31-klayout-streamout/SISO.klayout.gds

```
display(gds)
```

```
──────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────
[14:58:57] VERBOSE  Running 'KLayout.Render'…                                    step.py:1088
[14:58:57] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_yefelusq/klayout-render.log…  step.py:1268
```

Time Elapsed: 0.63s

Views updated:

- GDSII Stream
- GDSII Stream (KLayout)

Preview:

Design Rule Checks (DRC)

DRC determines that the final layout does not violate any of the rules set by the foundry to ensure the design is actually manufacturable- for example, not enough space between two wires, *too much* space between tap cells, and so on.

A design not passing DRC will typically be rejected by the foundry, who also run DRC on their side.

```
DRC = Step.factory.get("Magic.DRC")

drc = DRC(state_in=gds.state_out)
drc.start()
```

```
──────────────────────────────────────────────────────── Design Rule Checks ────────────────────────────────────────────────────────
[14:58:58] VERBOSE  Running 'Magic.DRC'…                                                                                  step.py:1088
[14:58:58] VERBOSE  Logging subprocess to openlane_run/32-magic-drc/magic-drc.log…                                         step.py:1268

Magic 8.3 revision 483 - Compiled on Sun Jun  2 18:57:41 UTC 2024.
Starting magic under Tcl interpreter
Using the terminal as the console.
Using NULL graphics device.
Processing system .magicrc file
Sourcing design .magicrc for technology sky130A ...
2 Magic internal units = 1 Lambda
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
ubm
Scaled tech values by 2 / 1 to match internal grid scaling
Loading sky130A Device Generator Menu ...
Loading "/content/openlane_ipynb/openlane/scripts/magic/wrapper.tcl" from command line.
Warning: Calma reading is not undoable!  I hope that's OK.
Library written using GDS-II Release 6.0
Library name: LIB
Reading "VIA_M3M4_PR".
Reading "VIA_M2M3_PR".
Reading "VIA_M1M2_PR_MR".
Reading "VIA_M1M2_PR".
Reading "VIA_L1M1_PR_MR".
Reading "VIA_via2_3_2000_480_1_6_320_320".
Reading "VIA_via3_4_2000_480_1_5_400_400".
Reading "VIA_via4_5_2000_480_1_5_400_400".
Reading "VIA_via5_6_2000_2000_1_1_1600_1600".
Reading "sky130_fd_sc_hd__buf_2".
Reading "sky130_fd_sc_hd__conb_1".
Reading "sky130_fd_sc_hd__nor4b_2".
Reading "sky130_fd_sc_hd__a211o_2".
Reading "sky130_fd_sc_hd__nor4_2".
Reading "sky130_fd_sc_hd__and4b_2".
Reading "sky130_fd_sc_hd__o2111a_2".
Reading "sky130_fd_sc_hd__and3b_2".
Reading "sky130_fd_sc_hd__nor3_2".
Reading "sky130_fd_sc_hd__a31oi_2".
Reading "sky130_fd_sc_hd__o221a_2".
Reading "sky130_fd_sc_hd__o31a_2".
Reading "sky130_fd_sc_hd__or4_2".
Reading "sky130_fd_sc_hd__nand3_2".
Reading "sky130_fd_sc_hd__a22o_2".
Reading "sky130_fd_sc_hd__nand4_2".
Reading "sky130_fd_sc_hd__o211a_2".
Reading "sky130_fd_sc_hd__o22a_2".
Reading "sky130_fd_sc_hd__o21bai_2".
Reading "sky130_fd_sc_hd__o2bb2a_2".
Reading "sky130_fd_sc_hd__a2111o_2".
Reading "sky130_fd_sc_hd__a21bo_2".
Reading "sky130_fd_sc_hd__or3b_2".
Reading "sky130_fd_sc_hd__nand2b_2".
Reading "sky130_fd_sc_hd__a22oi_2".
Reading "sky130_fd_sc_hd__a21o_2".
Reading "sky130_fd_sc_hd__a21boi_2".
Reading "sky130_fd_sc_hd__o32a_2".
Reading "sky130_fd_sc_hd__or4b_2".
Reading "sky130_fd_sc_hd__a31o_2".
Reading "sky130_fd_sc_hd__and4bb_2".
Reading "sky130_fd_sc_hd__a221o_2".
Reading "sky130_fd_sc_hd__and4_2".
Reading "sky130_fd_sc_hd__o21a_2".
Reading "sky130_fd_sc_hd__and2b_2".
Reading "sky130_fd_sc_hd__o21ai_2".
Reading "sky130_fd_sc_hd__a32o_2".
Reading "sky130_fd_sc_hd__or3_2".
Reading "sky130_fd_sc_hd__nor2_2".
Reading "sky130_fd_sc_hd__xnor2_2".
Reading "sky130_fd_sc_hd__xor2_2".
Reading "sky130_fd_sc_hd__a21oi_2".
Reading "sky130_fd_sc_hd__and3_2".
Reading "sky130_fd_sc_hd__and2_2".
Reading "sky130_fd_sc_hd__or2_2".
Reading "sky130_fd_sc_hd__nand2_2".
Reading "sky130_fd_sc_hd__inv_2".
Reading "sky130_fd_sc_hd__tapvpwrvgnd_1".
Reading "sky130_fd_sc_hd__decap_3".
Reading "sky130_fd_sc_hd__decap_8".
Reading "sky130_fd_sc_hd__decap_4".
Reading "sky130_ef_sc_hd__decap_12".
Reading "sky130_fd_sc_hd__decap_6".
Reading "sky130_fd_sc_hd__fill_2".
Reading "sky130_fd_sc_hd__fill_1".
Reading "SISO".
[INFO] Loading SISO

DRC style is now "drc(full)"
Loading DRC CIF style.
No errors found.
[INFO] COUNT: 0
[INFO] Should be divided by 3 or 4
[INFO] DRC Checking DONE (/content/openlane_run/32-magic-drc/reports/drc_violations.magic.rpt)
[INFO] Saving mag view with DRC errors (/content/openlane_run/32-magic-drc/views/SISO.drc.mag)
[INFO] Saved
```

Format	Path	
nl	openlane_run/28-openroad-fillinsertion/SISO.nl.v	
pnl	openlane_run/28-openroad-fillinsertion/SISO.pnl.v	
def	openlane_run/28-openroad-fillinsertion/SISO.def	
odb	openlane_run/28-openroad-fillinsertion/SISO.odb	
sdc	openlane_run/28-openroad-fillinsertion/SISO.sdc	
sdf	nom_tt_025C_1v80	openlane_run/30-openroad-stapostpnr/nom_tt_025C_1v80/SISO__nom_tt_025C_1v80.sdf
	nom_ss_100C_1v60	openlane_run/30-openroad-stapostpnr/nom_ss_100C_1v60/SISO__nom_ss_100C_1v60.sdf
	nom_ff_n40C_1v95	openlane_run/30-openroad-stapostpnr/nom_ff_n40C_1v95/SISO__nom_ff_n40C_1v95.sdf
	min_tt_025C_1v80	openlane_run/30-openroad-stapostpnr/min_tt_025C_1v80/SISO__min_tt_025C_1v80.sdf
	min_ss_100C_1v60	openlane_run/30-openroad-stapostpnr/min_ss_100C_1v60/SISO__min_ss_100C_1v60.sdf
	min_ff_n40C_1v95	openlane_run/30-openroad-stapostpnr/min_ff_n40C_1v95/SISO__min_ff_n40C_1v95.sdf
	max_tt_025C_1v80	openlane_run/30-openroad-stapostpnr/max_tt_025C_1v80/SISO__max_tt_025C_1v80.sdf
	max_ss_100C_1v60	openlane_run/30-openroad-stapostpnr/max_ss_100C_1v60/SISO__max_ss_100C_1v60.sdf
	max_ff_n40C_1v95	openlane_run/30-openroad-stapostpnr/max_ff_n40C_1v95/SISO__max_ff_n40C_1v95.sdf
spef	nom_*	openlane_run/29-openroad-rcx/nom/SISO.nom.spef
	min_*	openlane_run/29-openroad-rcx/min/SISO.min.spef
	max_*	openlane_run/29-openroad-rcx/max/SISO.max.spef
lib	nom_tt_025C_1v80	openlane_run/30-openroad-stapostpnr/nom_tt_025C_1v80/SISO__nom_tt_025C_1v80.lib
	nom_ss_100C_1v60	openlane_run/30-openroad-stapostpnr/nom_ss_100C_1v60/SISO__nom_ss_100C_1v60.lib
	nom_ff_n40C_1v95	openlane_run/30-openroad-stapostpnr/nom_ff_n40C_1v95/SISO__nom_ff_n40C_1v95.lib
	min_tt_025C_1v80	openlane_run/30-openroad-stapostpnr/min_tt_025C_1v80/SISO__min_tt_025C_1v80.lib
	min_ss_100C_1v60	openlane_run/30-openroad-stapostpnr/min_ss_100C_1v60/SISO__min_ss_100C_1v60.lib
	min_ff_n40C_1v95	openlane_run/30-openroad-stapostpnr/min_ff_n40C_1v95/SISO__min_ff_n40C_1v95.lib
	max_tt_025C_1v80	openlane_run/30-openroad-stapostpnr/max_tt_025C_1v80/SISO__max_tt_025C_1v80.lib

SPICE Extraction for Layout vs. Schematic Check

This step tries to reconstruct a SPICE netlist from the GDSII file, so it can later be used for the **Layout vs. Schematic** (LVS) check.

```
SpiceExtraction = Step.factory.get("Magic.SpiceExtraction")

spx = SpiceExtraction(state_in=drc.state_out)
spx.start()
```

```
──────────────────────────────────────── SPICE Model Extraction ────────────────────────────────────────
[14:59:01] VERBOSE  Running 'Magic.SpiceExtraction'…                                          step.py:1088
[14:59:01] VERBOSE  Logging subprocess to                                                     step.py:1268
                    openlane_run/33-magic-spiceextraction/magic-spiceextraction.log…

Magic 8.3 revision 483 - Compiled on Sun Jun  2 18:57:41 UTC 2024.
Starting magic under Tcl interpreter
Using the terminal as the console.
Using NULL graphics device.
Processing system .magicrc file
Sourcing design .magicrc for technology sky130A ...
2 Magic internal units = 1 Lambda
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
ubm
Scaled tech values by 2 / 1 to match internal grid scaling
Loading sky130A Device Generator Menu ...
Loading "/content/openlane_ipynb/openlane/scripts/magic/wrapper.tcl" from command line.
> lef read /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef
Reading LEF data from file /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef.
This action cannot be undone.
LEF read, Line 78 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 79 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 112 (Message): Unknown keyword "MINENCLOSEDAREA" in LEF file; ignoring.
LEF read, Line 114 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 115 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 121 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 122 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 123 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 156 (Message): Unknown keyword "MINENCLOSEDAREA" in LEF file; ignoring.
LEF read, Line 164 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 165 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 167 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 168 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 169 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 206 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 207 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 209 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 210 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 211 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 248 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 249 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 251 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 252 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 253 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 290 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 291 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read: Processed 797 lines.
> lef read /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef
Reading LEF data from file /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef.
This action cannot be undone.
LEF read: Processed 278 lines.
> lef read /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef
Reading LEF data from file /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef.
This action cannot be undone.
LEF read: Processed 56535 lines.
> def read /content/openlane_run/28-openroad-fillinsertion/SISO.def -noblockage -labels
Reading DEF data from file /content/openlane_run/28-openroad-fillinsertion/SISO.def.
This action cannot be undone.
Processed 4 vias total.
Processed 777 subcell instances total.
Processed 98 pins total.
Processed 2 special nets total.
Processed 325 nets total.
DEF read: Processed 5643 lines.
Moving label "_018_" from metal1 to via1 in cell SISO.
Moving label "_029_" from metal1 to via1 in cell SISO.
Moving label "_043_" from metal2 to via1 in cell SISO.
Moving label "_064_" from metal1 to via1 in cell SISO.
Moving label "_193_" from metal2 to via2 in cell SISO.
Moving label "y[13]" from metal2 to via2 in cell SISO.
Moving label "y[21]" from metal2 to via2 in cell SISO.
Moving label "y[23]" from metal2 to via2 in cell SISO.
Processing SISO
Extracting sky130_ef_sc_hd__decap_12 into sky130_ef_sc_hd__decap_12.ext:
Extracting sky130_fd_sc_hd__decap_3 into sky130_fd_sc_hd__decap_3.ext:
Extracting sky130_fd_sc_hd__fill_1 into sky130_fd_sc_hd__fill_1.ext:
Extracting sky130_fd_sc_hd__decap_6 into sky130_fd_sc_hd__decap_6.ext:
Extracting sky130_fd_sc_hd__decap_4 into sky130_fd_sc_hd__decap_4.ext:
Extracting sky130_fd_sc_hd__tapvpwrvgnd_1 into sky130_fd_sc_hd__tapvpwrvgnd_1.ext:
Extracting sky130_fd_sc_hd__and3_2 into sky130_fd_sc_hd__and3_2.ext:
Extracting sky130_fd_sc_hd__buf_2 into sky130_fd_sc_hd__buf_2.ext:
Extracting sky130_fd_sc_hd__xor2_2 into sky130_fd_sc_hd__xor2_2.ext:
Extracting sky130_fd_sc_hd__decap_8 into sky130_fd_sc_hd__decap_8.ext:
Extracting sky130_fd_sc_hd__fill_2 into sky130_fd_sc_hd__fill_2.ext:
Extracting sky130_fd_sc_hd__nand2_2 into sky130_fd_sc_hd__nand2_2.ext:
Extracting sky130_fd_sc_hd__xnor2_2 into sky130_fd_sc_hd__xnor2_2.ext:
Extracting sky130_fd_sc_hd__or2_2 into sky130_fd_sc_hd__or2_2.ext:
Extracting sky130_fd_sc_hd__and2_2 into sky130_fd_sc_hd__and2_2.ext:
Extracting sky130_fd_sc_hd__and4bb_2 into sky130_fd_sc_hd__and4bb_2.ext:
Extracting sky130_fd_sc_hd__conb_1 into sky130_fd_sc_hd__conb_1.ext:
Extracting sky130_fd_sc_hd__a31o_2 into sky130_fd_sc_hd__a31o_2.ext:
Extracting sky130_fd_sc_hd__and3b_2 into sky130_fd_sc_hd__and3b_2.ext:
Extracting sky130_fd_sc_hd__o21a_2 into sky130_fd_sc_hd__o21a_2.ext:
Extracting sky130_fd_sc_hd__nor2_2 into sky130_fd_sc_hd__nor2_2.ext:
Extracting sky130_fd_sc_hd__nor4_2 into sky130_fd_sc_hd__nor4_2.ext:
Extracting sky130_fd_sc_hd__o32a_2 into sky130_fd_sc_hd__o32a_2.ext:
Extracting sky130_fd_sc_hd__o21ai_2 into sky130_fd_sc_hd__o21ai_2.ext:
Extracting sky130_fd_sc_hd__a21oi_2 into sky130_fd_sc_hd__a21oi_2.ext:
Extracting sky130_fd_sc_hd__nor3_2 into sky130_fd_sc_hd__nor3_2.ext:
Extracting sky130_fd_sc_hd__or3_2 into sky130_fd_sc_hd__or3_2.ext:
Extracting sky130_fd_sc_hd__and4_2 into sky130_fd_sc_hd__and4_2.ext:
Extracting sky130_fd_sc_hd__a221o_2 into sky130_fd_sc_hd__a221o_2.ext:
Extracting sky130_fd_sc_hd__inv_2 into sky130_fd_sc_hd__inv_2.ext:
Extracting sky130_fd_sc_hd__or4b_2 into sky130_fd_sc_hd__or4b_2.ext:
Extracting sky130_fd_sc_hd__a21bo_2 into sky130_fd_sc_hd__a21bo_2.ext:
Extracting sky130_fd_sc_hd__a31oi_2 into sky130_fd_sc_hd__a31oi_2.ext:
Extracting sky130_fd_sc_hd__a21o_2 into sky130_fd_sc_hd__a21o_2.ext:
Extracting sky130_fd_sc_hd__a21boi_2 into sky130_fd_sc_hd__a21boi_2.ext:
Extracting sky130_fd_sc_hd__nand2b_2 into sky130_fd_sc_hd__nand2b_2.ext:
Extracting sky130_fd_sc_hd__nand4_2 into sky130_fd_sc_hd__nand4_2.ext:
Extracting sky130_fd_sc_hd__a22o_2 into sky130_fd_sc_hd__a22o_2.ext:
Extracting sky130_fd_sc_hd__o221a_2 into sky130_fd_sc_hd__o221a_2.ext:
Extracting sky130_fd_sc_hd__and4b_2 into sky130_fd_sc_hd__and4b_2.ext:
Extracting sky130_fd_sc_hd__and2b_2 into sky130_fd_sc_hd__and2b_2.ext:
Extracting sky130_fd_sc_hd__nand3_2 into sky130_fd_sc_hd__nand3_2.ext:
Extracting sky130_fd_sc_hd__nor4b_2 into sky130_fd_sc_hd__nor4b_2.ext:
Extracting sky130_fd_sc_hd__o21bai_2 into sky130_fd_sc_hd__o21bai_2.ext:
Extracting sky130_fd_sc_hd__o2111a_2 into sky130_fd_sc_hd__o2111a_2.ext:
Extracting sky130_fd_sc_hd__o31a_2 into sky130_fd_sc_hd__o31a_2.ext:
Extracting sky130_fd_sc_hd__o211a_2 into sky130_fd_sc_hd__o211a_2.ext:
Extracting sky130_fd_sc_hd__or4_2 into sky130_fd_sc_hd__or4_2.ext:
Extracting sky130_fd_sc_hd__o22a_2 into sky130_fd_sc_hd__o22a_2.ext:
Extracting sky130_fd_sc_hd__or3b_2 into sky130_fd_sc_hd__or3b_2.ext:
Extracting sky130_fd_sc_hd__a2111o_2 into sky130_fd_sc_hd__a2111o_2.ext:
Extracting sky130_fd_sc_hd__a211o_2 into sky130_fd_sc_hd__a211o_2.ext:
Extracting sky130_fd_sc_hd__a22oi_2 into sky130_fd_sc_hd__a22oi_2.ext:
```

```
Extracting sky130_fd_sc_hd__o2bb2a_2 into sky130_fd_sc_hd__o2bb2a_2.ext:
Extracting sky130_fd_sc_hd__a32o_2 into sky130_fd_sc_hd__a32o_2.ext:
Extracting SISO into SISO.ext:
```

Open in Colab

Task : 3 - Multiple Input, Single Output (MISO)

Avinash Baraiya- 202201211

Malhar Vaghasiya - 202201183

Smeet Agrawal - 202101237

Priyesh Tandel - 202101222

Samarth Panchal- 202101456

OpenLane Colab

This Google Colab notebook will:

- Install OpenLane and its dependencies
- Run a simple design, namely a serial-parallel multiplier, through the flow and targeting the open source sky130 PDK by Google and Skywater.

Setup Nix

Nix is a package manager with an emphasis on reproducible builds, and it is the primary method for installing OpenLane 2.

This step installs the Nix package manager and enables the experimental "flakes" feature.

If you're not in a Colab, this just sets the environment variables. You will need to install Nix and enable flakes on your own following this guide.

Show code

Get OpenLane

Click the ▷ button to download and install OpenLane.

This will install OpenLane's tool dependencies using Nix, and OpenLane itself using PIP.

Note that `python3-tk` may need to be installed using your OS's package manager.

openlane_version: "version-2.1"

pdk_root: "~/.volare"

pdk: "sky130"

Show code

Downloading OpenLane…

```
  % Total    % Received % Xferd  Average Speed   Time    Time     Time  Current
                                 Dload  Upload   Total   Spent    Left  Speed
  0     0    0     0    0     0      0      0 --:--:-- --:--:-- --:--:--     0
100 9491k    0 9491k    0     0  7599k      0 --:--:--  0:00:01 --:--:-- 30.6M
```

Downloading OpenLane's dependencies…

Downloading Python dependencies using PIP…

Downloading PDK…

```
Version bdc9412b3e468c102d01b7cf6337be06ec6e9c9a enabled for the sky130 PDK.
```

Done.

```
import openlane

print(openlane.__version__)
```

```
2.1.11
```

Creating the design

Now that OpenLane is set up, we can write a Verilog file as follows:

```
%%writefile MISO.v

module MISO(
    input [31:0] x,
    input [31:0] y,
    input [31:0] z,
    output [63:0] out
);

    // Intermediate wires
    wire [63:0] o1, o2, o3;
    wire [63:0] out_temp1, out_temp2, out_temp3;
    wire [63:0] out_temp;

    // Weight declaration
    reg [3:0] w [2:0];

    // Initialize weights
    initial begin
        w[0] = 4'b0001;
        w[1] = 4'b0111;
        w[2] = 4'b0011;
    end

    // Instantiate neuron modules
    neuron n1 (.out_neuron(o1), .input_neuron(x), .weight_value(w[0]));
    neuron n2 (.out_neuron(o2), .input_neuron(y), .weight_value(w[1]));
```

```
    neuron n3 (.out_neuron(o3), .input_neuron(z), .weight_value(w[2]));

    // Instantiate ReLU modules
    ReLU r1 (.in(o1), .out(out_temp1));
    ReLU r2 (.in(o2), .out(out_temp2));
    ReLU r3 (.in(o3), .out(out_temp3));

    // Sum the outputs of the ReLU modules
    assign out_temp = out_temp1 + out_temp2 + out_temp3;

    // Final ReLU on the summed output
    ReLU r_final (.in(out_temp), .out(out));

endmodule

module neuron(
    output reg [63:0] out_neuron,
    input [31:0] input_neuron,
    input [3:0] weight_value
);

    // Bias constant
    wire [63:0] bias = 1;

    // Intermediate multiplication result
    reg [63:0] out_mul;

    // Compute neuron output
    always @(*) begin
        out_mul = weight_value * input_neuron;
        out_neuron = out_mul + bias;
    end

endmodule

module ReLU(
    input signed [63:0] in,
    output reg [63:0] out
);

    always @(*) begin
        if (in < 0) begin
            out = 0;
        end else begin
            out = in;
        end
    end

endmodule
```

```
Overwriting MISO.v
```

Setting up the configuration

OpenLane requries you to configure any Flow before using it. This is done using the `config` module.

For colaboratories, REPLs and other interactive environments where there is no concrete Flow object, the Configuration may be initialized using `Config.interactive`, which will automatically propagate the configuration to any future steps.

You can find the documentation for `Config.interactive` here.

```
from openlane.config import Config

Config.interactive(
    "MISO",
    PDK="sky130A",
    CLOCK_PORT="clk",
    CLOCK_NET="clk",
    CLOCK_PERIOD=10,
    PRIMARY_GDSII_STREAMOUT_TOOL="klayout",
)
```

Interactive Configuration

Initial Values

```
CELL_BB_VERILOG_MODELS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/sky130_fd_sc_hd__blackbox.v
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/sky130_fd_sc_hd__blackbox_pp.v
CELL_GDS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/gds/sky130_fd_sc_hd.gds
CELL_LEFS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef
CELL_PAD_EXCLUDE:
- sky130_fd_sc_hd__tap*
- sky130_fd_sc_hd__decap*
- sky130_ef_sc_hd__decap*
- sky130_fd_sc_hd__fill*
CELL_SPICE_MODELS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__decap_12.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_12.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_4.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_8.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_fd_sc_hd.spice
CELL_VERILOG_MODELS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/primitives.v
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/sky130_fd_sc_hd.v
CLOCK_NET: clk
CLOCK_PERIOD: 10
CLOCK_PORT: clk
CLOCK_TRANSITION_CONSTRAINT: 0.15
CLOCK_UNCERTAINTY_CONSTRAINT: 0.25
CLOCK_WIRE_RC_LAYERS: null
DECAP_CELL:
- sky130_ef_sc_hd__decap_12
- sky130_fd_sc_hd__decap_8
- sky130_fd_sc_hd__decap_6
- sky130_fd_sc_hd__decap_4
- sky130_fd_sc_hd__decap_3
DEFAULT_CORNER: nom_tt_025C_1v80
DEFAULT_MAX_TRAN: null
DESIGN_DIR: .
DESIGN_NAME: MISO
DIE_AREA: null
DIODE_CELL: sky130_fd_sc_hd__diode_2/DIODE
ENDCAP_CELL: sky130_fd_sc_hd__decap_3
EXTRA_EXCLUDED_CELLS: null
EXTRA_GDS_FILES: null
EXTRA_LEFS: null
EXTRA_LIBS: null
EXTRA_SPICE_MODELS: null
EXTRA_VERILOG_MODELS: null
FALLBACK_SDC_FILE: /content/openlane_ipynb/openlane/scripts/base.sdc
FILL_CELL:
- sky130_fd_sc_hd__fill*
FP_IO_HLAYER: met3
FP_IO_VLAYER: met2
FP_TAPCELL_DIST: 13
FP_TRACKS_INFO: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tracks.info
GND_NETS: null
GND_PIN: VGND
GPIO_PADS_LEF:
- /root/.volare/sky130A/libs.ref/sky130_fd_io/lef/sky130_fd_io.lef
- /root/.volare/sky130A/libs.ref/sky130_fd_io/lef/sky130_ef_io.lef
GPIO_PADS_LEF_CORE_SIDE:
- /root/.volare/sky130A/libs.tech/openlane/custom_cells/lef/sky130_fd_io_core.lef
- /root/.volare/sky130A/libs.tech/openlane/custom_cells/lef/sky130_ef_io_core.lef
GPIO_PADS_VERILOG:
- /root/.volare/sky130A/libs.ref/sky130_fd_io/verilog/sky130_ef_io.v
GPIO_PAD_CELLS:
- sky130_fd_io*
- sky130_ef_io*
IO_DELAY_CONSTRAINT: 20
LIB:
  '*_ff_n40C_1v95':
  - /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ff_n40C_1v95.lib
  '*_ss_100C_1v60':
  - /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ss_100C_1v60.lib
  '*_tt_025C_1v80':
  - /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
MACROS: null
MAX_CAPACITANCE_CONSTRAINT: 0.2
MAX_FANOUT_CONSTRAINT: 10
MAX_TRANSITION_CONSTRAINT: 0.75
OUTPUT_CAP_LOAD: 33.442
PDK: sky130A
PDK_ROOT: /root/.volare
PLACE_SITE: unithd
PNR_EXCLUDED_CELL_FILE: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/drc_exclude.cells
PRIMARY_GDSII_STREAMOUT_TOOL: klayout
RT_MAX_LAYER: met5
RT_MIN_LAYER: met1
SCL_GROUND_PINS:
- VGND
- VNB
SCL_POWER_PINS:
- VPWR
- VPB
SIGNAL_WIRE_RC_LAYERS: null
STA_CORNERS:
- nom_tt_025C_1v80
- nom_ss_100C_1v60
- nom_ff_n40C_1v95
- min_tt_025C_1v80
- min_ss_100C_1v60
- min_ff_n40C_1v95
- max_tt_025C_1v80
- max_ss_100C_1v60
- max_ff_n40C_1v95
STD_CELL_LIBRARY: sky130_fd_sc_hd
SYNTH_BUFFER_CELL: sky130_fd_sc_hd__buf_2/A/X
SYNTH_CLK_DRIVING_CELL: null
SYNTH_DRIVING_CELL: sky130_fd_sc_hd__inv_2/Y
SYNTH_EXCLUDED_CELL_FILE: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/no_synth.cells
SYNTH_TIEHI_CELL: sky130_fd_sc_hd__conb_1/HI
SYNTH_TIELO_CELL: sky130_fd_sc_hd__conb_1/LO
TECH_LEFS:
  max_*: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__max.tlef
  min_*: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__min.tlef
  nom_*: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef
TIME_DERATING_CONSTRAINT: 5
TRISTATE_CELLS:
- sky130_fd_sc_hd__ebuf*
VDD_NETS: null
```

```
  VDD_PIN: VPWR
  VDD_PIN_VOLTAGE: 1.8
  WELLTAP_CELL: sky130_fd_sc_hd__tapvpwrvgnd_1
  WIRE_LENGTH_THRESHOLD: null
  meta:
    flow: null
    openlane_version: 2.1.11
    step: null
    substituting_steps: null
    version: 1
```

Running implementation steps

There are two ways to obtain OpenLane's built-in implementation steps:

- via directly importing from the `steps` module using its category:
  - `from openlane.steps import Yosys` then `Synthesis = Yosys.Synthesis`
- by using the step's id from the registry:
  - `from openlane.steps import Step` then `Synthesis = Step.factory.get("Yosys.Synthesis")`

You can find a full list of included steps here: https://openlane2.readthedocs.io/en/latest/reference/step_config_vars.html

```
from openlane.steps import Step
```

- First, get the step (and display its help)...

```
Synthesis = Step.factory.get("Yosys.Synthesis")

Synthesis.display_help()
```

(step-yosys-synthesis)=

Synthesis

```
Performs synthesis and technology mapping on Verilog RTL files
using Yosys and ABC, emitting a netlist.

Some metrics will also be extracted and updated, namely:

* ``design__instance__count``
* ``design__instance_unmapped__count``
* ``design__instance__area``
```

Importing

```
from openlane.steps.yosys import Synthesis

# or

from openlane.steps import Step

Synthesis = Step.factory.get("Yosys.Synthesis")
```

Inputs and Outputs

Inputs	Outputs
	Verilog Netlist (.nl.v)

(yosys.synthesis-configuration-variables)=

Configuration Variables

Variable Name	Type	Description	Default	Units
SYNTH_LATCH_MAP{#var-yosys-synthesis-synth_latch_map}PDK	Path?	A path to a file containing the latch mapping for Yosys.	None	
SYNTH_TRISTATE_MAP{#var-yosys-synthesis-synth_tristate_map}PDK	Path?	A path to a file containing the tri-state buffer mapping for Yosys.	None	
SYNTH_CSA_MAP{#var-yosys-synthesis-synth_csa_map}PDK	Path?	A path to a file containing the carry-select adder mapping for Yosys.	None	
SYNTH_RCA_MAP{#var-yosys-synthesis-synth_rca_map}PDK	Path?	A path to a file containing the ripple-carry adder mapping for Yosys.	None	
SYNTH_FA_MAP{#var-yosys-synthesis-synth_fa_map}PDK	Path?	A path to a file containing the full adder mapping for Yosys.	None	
SYNTH_MUX_MAP{#var-yosys-synthesis-synth_mux_map}PDK	Path?	A path to a file containing the mux mapping for Yosys.	None	
SYNTH_MUX4_MAP{#var-yosys-synthesis-synth_mux4_map}PDK	Path?	A path to a file containing the mux4 mapping for Yosys.	None	
USE_LIGHTER{#var-yosys-synthesis-use_lighter}	bool	Activates Lighter, an experimental plugin that attempts to optimize clock-gated flip-flops.	False	
LIGHTER_DFF_MAP{#var-yosys-synthesis-lighter_dff_map}	Path?	An override to the custom DFF map file provided for the given SCL by Lighter.	None	
YOSYS_LOG_LEVEL{#var-yosys-synthesis-yosys_log_level}	'ALL' | 'WARNING' | 'ERROR'	Which log level for Yosys. At WARNING or higher, the initialization splash is also disabled.	ALL	
SYNTH_CHECKS_ALLOW_TRISTATE{#var-yosys-synthesis-synth_checks_allow_tristate}	bool	Ignore multiple-driver warnings if they are connected to tri-state buffers on a best-effort basis.	True	
SYNTH_AUTONAME{#var-yosys-synthesis-synth_autoname}	bool	Generates names for netlist instances. This results in instance names that can be extremely long, but are more human-readable.	False	
SYNTH_STRATEGY{#var-yosys-synthesis-synth_strategy}	'AREA 0' | 'AREA 1' | 'AREA 2' | 'AREA 3' | 'DELAY 0' | 'DELAY 1' | 'DELAY 2' | 'DELAY 3' | 'DELAY 4'	Strategies for abc logic synthesis and technology mapping. AREA strategies usually result in a more compact design, while DELAY strategies usually result in a design that runs at a higher frequency. Please note that there is no way to know which strategy is the best before trying them.	AREA 0	
SYNTH_ABC_BUFFERING{#var-yosys-synthesis-synth_abc_buffering}	bool	Enables `abc` cell buffering.	False	
SYNTH_ABC_LEGACY_REFACTOR{#var-yosys-synthesis-synth_abc_legacy_refactor}	bool	Replaces the ABC command `drf -l` with `refactor` which matches older versions of OpenLane but is more unstable.	False	
SYNTH_ABC_LEGACY_REWRITE{#var-yosys-synthesis-synth_abc_legacy_rewrite}	bool	Replaces the ABC command `drw -l` with `rewrite` which matches older versions of OpenLane but is more unstable.	False	
SYNTH_DIRECT_WIRE_BUFFERING{#var-yosys-synthesis-synth_direct_wire_buffering}	bool	Enables inserting buffer cells for directly connected wires.	True	
SYNTH_SPLITNETS{#var-yosys-synthesis-synth_splitnets}	bool	Splits multi-bit nets into single-bit nets. Easier to trace but may not be supported by all tools.	True	
SYNTH_SIZING{#var-yosys-synthesis-synth_sizing}	bool	Enables `abc` cell sizing (instead of buffering).	False	
SYNTH_NO_FLAT{#var-yosys-synthesis-synth_no_flat}	bool	A flag that disables flattening the hierarchy during synthesis, only flattening it after synthesis, mapping and optimizations.	False	
SYNTH_SHARE_RESOURCES{#var-yosys-synthesis-synth_share_resources}	bool	A flag that enables yosys to reduce the number of cells by determining shareable resources and merging them.	True	
SYNTH_ADDER_TYPE{#var-yosys-synthesis-synth_adder_type}	'YOSYS' | 'FA' | 'RCA' | 'CSA'	Adder type to which the $addand$sub operators are mapped to. Possible values are `YOSYS/FA/RCA/CSA`; where `YOSYS` refers to using Yosys internal adder definition, `FA` refers to full-adder structure, `RCA` refers to ripple carry adder structure, and `CSA` refers to carry select adder.	YOSYS	
SYNTH_EXTRA_MAPPING_FILE{#var-yosys-synthesis-synth_extra_mapping_file}	Path?	Points to an extra techmap file for yosys that runs right after yosys `synth` before generic techmap.	None	
SYNTH_PARAMETERS{#var-yosys-synthesis-synth_parameters}	List[str]?	Key-value pairs to be `chparam`ed in Yosys, in the format `key1=value1`.	None	
SYNTH_ELABORATE_ONLY{#var-yosys-synthesis-synth_elaborate_only}	bool	"Elaborate" the design only without attempting any logic mapping. Useful when dealing with structural Verilog netlists.	False	
SYNTH_ELABORATE_FLATTEN{#var-yosys-synthesis-synth_elaborate_flatten}	bool	If `SYNTH_ELABORATE_ONLY` is specified, this variable controls whether or not the top level should be flattened.	True	
VERILOG_FILES{#var-yosys-synthesis-verilog_files}	List[Path]	The paths of the design's Verilog files.	None	
VERILOG_DEFINES{#var-yosys-synthesis-verilog_defines}	List[str]?	Preprocessor defines for input Verilog files.	None	

VERILOG_POWER_DEFINE{#var-yosys-synthesis-verilog_power_define}	str	Specifies the name of the define used to guard power and ground connections in the input RTL.	USE_POWER_PINS
VERILOG_INCLUDE_DIRS{#var-yosys-synthesis-verilog_include_dirs}	List[str]?	Specifies the Verilog `include` directories.	None
USE_SYNLIG{#var-yosys-synthesis-use_synlig}	bool	Use the Synlig plugin to process files, which has better SystemVerilog parsing capabilities but may not be compatible with all Yosys commands and attributes.	False
SYNLIG_DEFER{#var-yosys-synthesis-synlig_defer}	bool	Uses -defer flag when reading files the Synlig plugin, which may improve performance by reading each file separately, but is experimental.	False

- Then run it. Note you can pass step-specific configs using Python keyword arguments.

Synthesis

We need to start by converting our high-level Verilog to one that just shows the connections between small silicon patterns called "standard cells" in process called Synthesis. We can do this by passing the Verilog files as a configuration variable to `Yosys.Synthesis` as follows, then running it.

As this is the first step, we need to create an empty state and pass it to it.

```
from openlane.state import State

synthesis = Synthesis(
    VERILOG_FILES=["./MISO.v"],
    state_in=State(),
)
synthesis.start()
```

```
────────────────────────────────────────────────────────── Synthesis ──────────────────────────────────────────────────────────
[15:35:22] VERBOSE  Running 'Yosys.Synthesis'…                                                                    step.py:1088
[15:35:22] VERBOSE  Logging subprocess to openlane_run/52-yosys-synthesis/yosys-synthesis.log…                     step.py:1268

/-------------------------------------------------------------------------\
|                                                                         |
|  yosys -- Yosys Open SYnthesis Suite                                    |
|                                                                         |
|  Copyright (C) 2012 - 2020  Claire Xenia Wolf <claire@yosyshq.com>      |
|                                                                         |
|  Permission to use, copy, modify, and/or distribute this software for any |
|  purpose with or without fee is hereby granted, provided that the above |
|  copyright notice and this permission notice appear in all copies.      |
|                                                                         |
|  THE SOFTWARE IS PROVIDED "AS IS" AND THE AUTHOR DISCLAIMS ALL WARRANTIES |
|  WITH REGARD TO THIS SOFTWARE INCLUDING ALL IMPLIED WARRANTIES OF       |
|  MERCHANTABILITY AND FITNESS. IN NO EVENT SHALL THE AUTHOR BE LIABLE FOR |
|  ANY SPECIAL, DIRECT, INDIRECT, OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES |
|  WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN  |
|  ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF |
|  OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.         |
|                                                                         |
\-------------------------------------------------------------------------/

Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)

Loaded SDC plugin
[TCL: yosys -import] Command name collision: found pre-existing command `cd' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `eval' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `exec' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `read' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `trace' -> skip.

1. Executing Liberty frontend: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
Imported 428 cell types from liberty file.

2. Executing Verilog-2005 frontend: ./MISO.v
Parsing SystemVerilog input from `./MISO.v' to AST representation.
Generating RTLIL representation for module `\MISO'.
Generating RTLIL representation for module `\neuron'.
Generating RTLIL representation for module `\ReLU'.
Successfully finished Verilog frontend.

3. Executing HIERARCHY pass (managing design hierarchy).

3.1. Analyzing design hierarchy..
Top module:  \MISO
Used module:     \ReLU
Used module:     \neuron
Reprocessing module MISO because instantiated module neuron has become available.
Generating RTLIL representation for module `\MISO'.

3.2. Analyzing design hierarchy..
Top module:  \MISO
Used module:     \ReLU
Used module:     \neuron

3.3. Analyzing design hierarchy..
Top module:  \MISO
Used module:     \ReLU
Used module:     \neuron
Removed 0 unused modules.
Renaming module MISO to MISO.

4. Generating Graphviz representation of design.
Writing dot description to `/content/openlane_run/52-yosys-synthesis/hierarchy.dot'.
Dumping module MISO to page 1.

5. Executing TRIBUF pass.

6. Executing HIERARCHY pass (managing design hierarchy).

6.1. Analyzing design hierarchy..
Top module:  \MISO
Used module:     \ReLU
Used module:     \neuron

6.2. Analyzing design hierarchy..
Top module:  \MISO
Used module:     \ReLU
Used module:     \neuron
Removed 0 unused modules.

7. Executing PROC_CLEAN pass (remove empty switches from decision trees).
Cleaned up 0 empty switches.

8. Executing PROC_RMDEAD pass (remove dead branches from decision trees).
Marked 1 switch rules as full_case in process $proc$./MISO.v:68$19 in module ReLU.
Removed a total of 0 dead cases.

9. Executing PROC_PRUNE pass (remove redundant assignments in processes).
Removed 0 redundant assignments.
Promoted 6 assignments to connections.

10. Executing PROC_INIT pass (extract init attributes).

11. Executing PROC_ARST pass (detect async resets in processes).

12. Executing PROC_ROM pass (convert switches to ROMs).
Converted 0 switches.
<suppressed ~1 debug messages>

13. Executing PROC_MUX pass (convert decision trees to multiplexers).
Creating decoders for process `\MISO.$proc$./MISO.v:0$35'.
Creating decoders for process `\neuron.$proc$./MISO.v:56$16'.
Creating decoders for process `\ReLU.$proc$./MISO.v:68$19'.
1/1: $1\out[63:0]

14. Executing PROC_DLATCH pass (convert process syncs to latches).
No latch inferred for signal `\MISO.$memwr$\w$./MISO.v:20$24_EN' from process `\MISO.$proc$./MISO.v:0$35'.
No latch inferred for signal `\MISO.$memwr$\w$./MISO.v:21$25_EN' from process `\MISO.$proc$./MISO.v:0$35'.
No latch inferred for signal `\MISO.$memwr$\w$./MISO.v:22$26_EN' from process `\MISO.$proc$./MISO.v:0$35'.
No latch inferred for signal `\neuron.\out_neuron' from process `\neuron.$proc$./MISO.v:56$16'.
No latch inferred for signal `\neuron.\out_mul' from process `\neuron.$proc$./MISO.v:56$16'.
No latch inferred for signal `\ReLU.\out' from process `\ReLU.$proc$./MISO.v:68$19'.

15. Executing PROC_DFF pass (convert process syncs to FFs).

16. Executing PROC_MEMWR pass (convert process memory writes to cells).

17. Executing PROC_CLEAN pass (remove empty switches from decision trees).
Removing empty process `MISO.$proc$./MISO.v:0$35'.
Removing empty process `neuron.$proc$./MISO.v:56$16'.
Found and cleaned up 1 empty switch in `\ReLU.$proc$./MISO.v:68$19'.
Removing empty process `ReLU.$proc$./MISO.v:68$19'.
Cleaned up 1 empty switch.
```

```
18. Executing CHECK pass (checking for obvious problems).
Checking module MISO...
Checking module neuron...
Checking module ReLU...
Found and reported 0 problems.

19. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.
Optimizing module neuron.
Optimizing module ReLU.

20. Executing FLATTEN pass (flatten design).
Deleting now unused module neuron.
Deleting now unused module ReLU.
<suppressed ~7 debug messages>

21. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

22. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..
Removed 0 unused cells and 41 unused wires.
<suppressed ~1 debug messages>

23. Executing OPT pass (performing simple optimizations).

23.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

23.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

23.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

23.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MISO.
Performed a total of 0 changes.

23.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

23.6. Executing OPT_DFF pass (perform DFF optimizations).

23.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..

23.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

23.9. Finished OPT passes. (There is nothing left to do.)

24. Executing FSM pass (extract and optimize FSM).

24.1. Executing FSM_DETECT pass (finding FSMs in design).

24.2. Executing FSM_EXTRACT pass (extracting FSM from design).

24.3. Executing FSM_OPT pass (simple optimizations of FSMs).

24.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..

24.5. Executing FSM_OPT pass (simple optimizations of FSMs).

24.6. Executing FSM_RECODE pass (re-assigning FSM state encoding).

24.7. Executing FSM_INFO pass (dumping all available information on FSM cells).

24.8. Executing FSM_MAP pass (mapping FSMs to basic logic).

25. Executing OPT pass (performing simple optimizations).

25.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

25.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

25.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

25.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MISO.
Performed a total of 0 changes.

25.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

25.6. Executing OPT_DFF pass (perform DFF optimizations).

25.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..

25.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

25.9. Finished OPT passes. (There is nothing left to do.)

26. Executing WREDUCE pass (reducing word size of cells).
Removed top 30 address bits (of 32) from memory init port MISO.$meminit$\w$./MISO.v:20$32 (w).
Removed top 30 address bits (of 32) from memory init port MISO.$meminit$\w$./MISO.v:21$33 (w).
Removed top 30 address bits (of 32) from memory init port MISO.$meminit$\w$./MISO.v:22$34 (w).
Removed top 30 address bits (of 32) from memory read port MISO.$memrd$\w$./MISO.v:26$29 (w).
Removed top 30 address bits (of 32) from memory read port MISO.$memrd$\w$./MISO.v:27$30 (w).
Removed top 30 address bits (of 32) from memory read port MISO.$memrd$\w$./MISO.v:28$31 (w).
Removed top 28 bits (of 64) from port Y of cell MISO.$flatten\n1.$mul$./MISO.v:57$17 ($mul).
Removed top 28 bits (of 64) from port A of cell MISO.$flatten\n1.$add$./MISO.v:58$18 ($add).
Removed top 63 bits (of 64) from port B of cell MISO.$flatten\n1.$add$./MISO.v:58$18 ($add).
Removed top 27 bits (of 64) from port Y of cell MISO.$flatten\n1.$add$./MISO.v:58$18 ($add).
Removed top 63 bits (of 64) from port B of cell MISO.$flatten\n2.$add$./MISO.v:58$18 ($add).
Removed top 28 bits (of 64) from port Y of cell MISO.$flatten\n2.$mul$./MISO.v:57$17 ($mul).
Removed top 63 bits (of 64) from port B of cell MISO.$flatten\n3.$add$./MISO.v:58$18 ($add).
Removed top 28 bits (of 64) from port Y of cell MISO.$flatten\n3.$mul$./MISO.v:57$17 ($mul).
```

```
Removed top 27 bits (of 64) from mux cell MISO.$flatten\r1.$procmux$40 ($mux).
Removed top 26 bits (of 64) from port A of cell MISO.$flatten\r1.$lt$./MISO.v:69$20 ($lt).
Removed top 31 bits (of 32) from port B of cell MISO.$flatten\r1.$lt$./MISO.v:69$20 ($lt).
Converting cell MISO.$flatten\r1.$lt$./MISO.v:69$20 ($lt) from signed to unsigned.
Removed top 1 bits (of 38) from port A of cell MISO.$flatten\r1.$lt$./MISO.v:69$20 ($lt).
Removed top 31 bits (of 32) from port B of cell MISO.$flatten\r2.$lt$./MISO.v:69$20 ($lt).
Removed top 31 bits (of 32) from port B of cell MISO.$flatten\r3.$lt$./MISO.v:69$20 ($lt).
Removed top 31 bits (of 32) from port B of cell MISO.$flatten\r_final.$lt$./MISO.v:69$20 ($lt).
Removed top 27 bits (of 64) from wire MISO.o1.
Removed top 27 bits (of 64) from wire MISO.out_temp1.

27. Executing PEEPOPT pass (run peephole optimizers).

28. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..
Removed 0 unused cells and 2 unused wires.
<suppressed ~1 debug messages>

29. Executing ALUMACC pass (create $alu and $macc cells).
Extracting $alu and $macc cells in module MISO:
creating $macc model for $add$./MISO.v:36$27 ($add).
creating $macc model for $add$./MISO.v:36$28 ($add).
creating $macc model for $flatten\n1.$add$./MISO.v:58$18 ($add).
creating $macc model for $flatten\n1.$mul$./MISO.v:57$17 ($mul).
creating $macc model for $flatten\n2.$add$./MISO.v:58$18 ($add).
creating $macc model for $flatten\n2.$mul$./MISO.v:57$17 ($mul).
creating $macc model for $flatten\n3.$add$./MISO.v:58$18 ($add).
creating $macc model for $flatten\n3.$mul$./MISO.v:57$17 ($mul).
merging $macc model for $flatten\n1.$mul$./MISO.v:57$17 into $flatten\n1.$add$./MISO.v:58$18.
merging $macc model for $add$./MISO.v:36$27 into $add$./MISO.v:36$28.
creating $alu model for $macc $flatten\n2.$add$./MISO.v:58$18.
creating $alu model for $macc $flatten\n3.$add$./MISO.v:58$18.
creating $macc cell for $flatten\n2.$mul$./MISO.v:57$17: $auto$alumacc.cc:365:replace_macc$44
creating $macc cell for $flatten\n1.$add$./MISO.v:58$18: $auto$alumacc.cc:365:replace_macc$45
creating $macc cell for $add$./MISO.v:36$28: $auto$alumacc.cc:365:replace_macc$46
creating $macc cell for $flatten\n3.$mul$./MISO.v:57$17: $auto$alumacc.cc:365:replace_macc$47
creating $alu model for $flatten\r1.$lt$./MISO.v:69$20 ($lt): new $alu
creating $alu model for $flatten\r2.$lt$./MISO.v:69$20 ($lt): new $alu
creating $alu model for $flatten\r3.$lt$./MISO.v:69$20 ($lt): new $alu
creating $alu model for $flatten\r_final.$lt$./MISO.v:69$20 ($lt): new $alu
creating $alu cell for $flatten\r_final.$lt$./MISO.v:69$20: $auto$alumacc.cc:485:replace_alu$52
creating $alu cell for $flatten\r3.$lt$./MISO.v:69$20: $auto$alumacc.cc:485:replace_alu$65
creating $alu cell for $flatten\r2.$lt$./MISO.v:69$20: $auto$alumacc.cc:485:replace_alu$78
creating $alu cell for $flatten\r1.$lt$./MISO.v:69$20: $auto$alumacc.cc:485:replace_alu$91
creating $alu cell for $flatten\n3.$add$./MISO.v:58$18: $auto$alumacc.cc:485:replace_alu$102
creating $alu cell for $flatten\n2.$add$./MISO.v:58$18: $auto$alumacc.cc:485:replace_alu$105
created 6 $alu and 4 $macc cells.

30. Executing SHARE pass (SAT-based resource sharing).

31. Executing OPT pass (performing simple optimizations).

31.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.
<suppressed ~4 debug messages>

31.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

31.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

31.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MISO.
Performed a total of 0 changes.

31.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

31.6. Executing OPT_DFF pass (perform DFF optimizations).

31.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..
Removed 6 unused cells and 9 unused wires.
<suppressed ~7 debug messages>

31.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

31.9. Rerunning OPT passes. (Maybe there is more to do..)

31.10. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

31.11. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MISO.
Performed a total of 0 changes.

31.12. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

31.13. Executing OPT_DFF pass (perform DFF optimizations).

31.14. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..

31.15. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

31.16. Finished OPT passes. (There is nothing left to do.)

32. Executing MEMORY pass.

32.1. Executing OPT_MEM pass (optimize memories).
MISO.w: removing const-1 lane 0
MISO.w: removing const-0 lane 3
Performed a total of 1 transformations.

32.2. Executing OPT_MEM_PRIORITY pass (removing unnecessary memory write priority relations).
Performed a total of 0 transformations.

32.3. Executing OPT_MEM_FEEDBACK pass (finding memory read-to-write feedback paths).

32.4. Executing MEMORY_BMUX2ROM pass (converting muxes to ROMs).
```

```
32.5. Executing MEMORY_DFF pass (merging $dff cells to $memrd).
Checking read port `\w'[0] in module `\MISO': no output FF found.
Checking read port `\w'[1] in module `\MISO': no output FF found.
Checking read port `\w'[2] in module `\MISO': no output FF found.
Checking read port address `\w'[0] in module `\MISO': no address FF found.
Checking read port address `\w'[1] in module `\MISO': no address FF found.
Checking read port address `\w'[2] in module `\MISO': no address FF found.

32.6. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..

32.7. Executing MEMORY_SHARE pass (consolidating $memrd/$memwr cells).
Consolidating read ports of memory MISO.w by address:
Merging ports 1, 2 (address 2'01).
Consolidating read ports of memory MISO.w by address:
Merging ports 0, 1 (address 2'10).

32.8. Executing OPT_MEM_WIDEN pass (optimize memories where all ports are wide).
Widening base width of memory w in module MISO by factor 4.
Performed a total of 1 transformations.

32.9. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..
Removed 0 unused cells and 1 unused wires.
<suppressed ~1 debug messages>

32.10. Executing MEMORY_COLLECT pass (generating $mem cells).

33. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..

34. Executing OPT pass (performing simple optimizations).

34.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.
<suppressed ~240 debug messages>

34.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

34.3. Executing OPT_DFF pass (perform DFF optimizations).

34.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..
Removed 0 unused cells and 54 unused wires.
<suppressed ~1 debug messages>

34.5. Finished fast OPT passes.

35. Executing MEMORY_MAP pass (converting memories to logic and flip-flops).
Mapping memory \w in module \MISO:
created 1 $dff cells and 0 static cells of width 8.
read interface: 0 $dff and 0 $mux cells.
write interface: 0 write mux blocks.

36. Executing OPT pass (performing simple optimizations).

36.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

36.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

36.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

36.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MISO.
Consolidated identical input bits for $mux cell $flatten\r2.$procmux$40:
Old ports: A=64'0000000000000000000000000000000000000000000000000000000000000000, B={
27'000000000000000000000000000 \r2.in [36:0] }, Y=\out_temp2
New ports: A=37'0000000000000000000000000000000000000, B=\r2.in [36:0], Y=\out_temp2 [36:0]
New connections: \out_temp2 [63:37] = 27'000000000000000000000000000
Consolidated identical input bits for $mux cell $flatten\r3.$procmux$40:
Old ports: A=64'0000000000000000000000000000000000000000000000000000000000000000, B={
27'000000000000000000000000000 \r3.in [36:0] }, Y=\out_temp3
New ports: A=37'0000000000000000000000000000000000000, B=\r3.in [36:0], Y=\out_temp3 [36:0]
New connections: \out_temp3 [63:37] = 27'000000000000000000000000000
Optimizing cells in module \MISO.
Performed a total of 2 changes.

36.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

36.6. Executing OPT_SHARE pass.

36.7. Executing OPT_DFF pass (perform DFF optimizations).

36.8. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..
Removed 0 unused cells and 1 unused wires.
<suppressed ~1 debug messages>

36.9. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

36.10. Rerunning OPT passes. (Maybe there is more to do..)

36.11. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MISO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

36.12. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MISO.
Performed a total of 0 changes.

36.13. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

36.14. Executing OPT_SHARE pass.

36.15. Executing OPT_DFF pass (perform DFF optimizations).

36.16. Executing OPT_CLEAN pass (remove unused cells and wires).
```

```
Finding unused cells or wires in module \MISO..

36.17. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

36.18. Finished OPT passes. (There is nothing left to do.)

37. Executing TECHMAP pass (map to technology primitives).

37.1. Executing Verilog-2005 frontend:
/nix/store/sx2v0i73mn1ih2z1nk61pm9n5gjgpidy-yosys/bin/../share/yosys/techmap.v
Parsing Verilog input from `/nix/store/sx2v0i73mn1ih2z1nk61pm9n5gjgpidy-yosys/bin/../share/yosys/techmap.v' to AST
representation.
Generating RTLIL representation for module `\_90_simplemap_bool_ops'.
Generating RTLIL representation for module `\_90_simplemap_reduce_ops'.
Generating RTLIL representation for module `\_90_simplemap_logic_ops'.
Generating RTLIL representation for module `\_90_simplemap_compare_ops'.
Generating RTLIL representation for module `\_90_simplemap_various'.
Generating RTLIL representation for module `\_90_simplemap_registers'.
Generating RTLIL representation for module `\_90_shift_ops_shr_shl_sshl_sshr'.
Generating RTLIL representation for module `\_90_shift_shiftx'.
Generating RTLIL representation for module `\_90_fa'.
Generating RTLIL representation for module `\_90_lcu'.
Generating RTLIL representation for module `\_90_alu'.
Generating RTLIL representation for module `\_90_macc'.
Generating RTLIL representation for module `\_90_alumacc'.
Generating RTLIL representation for module `\$__div_mod_u'.
Generating RTLIL representation for module `\$__div_mod_trunc'.
Generating RTLIL representation for module `\_90_div'.
Generating RTLIL representation for module `\_90_mod'.
Generating RTLIL representation for module `\$__div_mod_floor'.
Generating RTLIL representation for module `\_90_divfloor'.
Generating RTLIL representation for module `\_90_modfloor'.
Generating RTLIL representation for module `\_90_pow'.
Generating RTLIL representation for module `\_90_pmux'.
Generating RTLIL representation for module `\_90_demux'.
Generating RTLIL representation for module `\_90_lut'.
Successfully finished Verilog frontend.

37.2. Continuing TECHMAP pass.
Using extmapper simplemap for cells of type $reduce_and.
Using extmapper simplemap for cells of type $xor.
Using extmapper maccmap for cells of type $macc.
add \y * 4'0111 (32x4 bits, unsigned)
add \out_temp1 (37 bits, unsigned)
add { 27'000000000000000000000000000 \out_temp3 [36:0] } (64 bits, unsigned)
add { 27'000000000000000000000000000 \out_temp2 [36:0] } (64 bits, unsigned)
Using extmapper simplemap for cells of type $or.
Using extmapper simplemap for cells of type $not.
add \z * 4'0011 (32x4 bits, unsigned)
Using template $paramod$7fa6970f0c97644a990ba1d0dcc56c6042128be7\_90_alu for cells of type $alu.
add \x * 4'0001 (32x4 bits, unsigned)
add 37'0000000000000000000000000000000000001 (37 bits, unsigned)
packed 1 (1) bits / 1 words into adder tree
Using extmapper simplemap for cells of type $mux.
Using template $paramod$95d318accac8c1bf0af46dacce337e7889a498bd\_90_alu for cells of type $alu.
Using template $paramod$c66b509f0dbff04a70da2bd22d8e6a343f873dbd\_90_alu for cells of type $alu.
Using extmapper simplemap for cells of type $and.
Using template $paramod\_90_fa\WIDTH=32'00000000000000000000000000100100 for cells of type $fa.
Using template $paramod$9fb24bf0faa43f804d3c379242188667e42c235c\_90_alu for cells of type $alu.
Using template $paramod\_90_fa\WIDTH=32'00000000000000000000000000100101 for cells of type $fa.
Using template $paramod$039520c137afc9cd69dd56c3fb11a4e1fbe5f664\_90_alu for cells of type $alu.
Using template $paramod\_90_lcu\WIDTH=32'00000000000000000000000000100101 for cells of type $lcu.
Using extmapper simplemap for cells of type $pos.
Using template $paramod\_90_lcu\WIDTH=32'00000000000000000000000001000000 for cells of type $lcu.
Using template $paramod\_90_lcu\WIDTH=32'00000000000000000000000000100100 for cells of type $lcu.
No more expansions possible.
<suppressed ~2967 debug messages>

38. Executing OPT pass (performing simple optimizations).

38.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.
<suppressed ~4138 debug messages>

38.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
<suppressed ~717 debug messages>
Removed a total of 239 cells.

38.3. Executing OPT_DFF pass (perform DFF optimizations).

38.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..
Removed 428 unused cells and 1726 unused wires.
<suppressed ~429 debug messages>

38.5. Finished fast OPT passes.

39. Executing ABC pass (technology mapping using ABC).

39.1. Extracting gate netlist of module `\MISO' to `<abc-temp-dir>/input.blif'..
Extracted 1958 gates and 2055 wires to a netlist network with 96 inputs and 38 outputs.

39.1.1. Executing ABC.
Running ABC command: "/nix/store/wq2q0njg3sx8wvj2akz7x1qxwyrv9xlr-yosys-abc/bin/abc" -s -f
<abc-temp-dir>/abc.script 2>&1
ABC: ABC command line: "source <abc-temp-dir>/abc.script".
ABC:
ABC: + read_blif <abc-temp-dir>/input.blif
ABC: + read_library <abc-temp-dir>/stdcells.genlib
ABC: Entered genlib library with 13 gates from file "<abc-temp-dir>/stdcells.genlib".
ABC: + strash
ABC: + dretime
ABC: + map
ABC: + write_blif <abc-temp-dir>/output.blif

39.1.2. Re-integrating ABC results.
ABC RESULTS:              NAND cells:       48
ABC RESULTS:               NOT cells:       74
ABC RESULTS:              XNOR cells:      183
ABC RESULTS:             ORNOT cells:       84
ABC RESULTS:            ANDNOT cells:      444
ABC RESULTS:               XOR cells:      332
ABC RESULTS:               AND cells:       52
ABC RESULTS:               NOR cells:      106
ABC RESULTS:                OR cells:      267
ABC RESULTS:        internal signals:     1921
ABC RESULTS:           input signals:       96
ABC RESULTS:          output signals:       38
Removing temp directory.

40. Executing OPT pass (performing simple optimizations).

40.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

40.2. Executing OPT_MERGE pass (detect identical cells).
```

```
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

40.3. Executing OPT_DFF pass (perform DFF optimizations).

40.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..
Removed 0 unused cells and 619 unused wires.
<suppressed ~1 debug messages>

40.5. Finished fast OPT passes.

41. Executing HIERARCHY pass (managing design hierarchy).

41.1. Analyzing design hierarchy..
Top module:  \MISO

41.2. Analyzing design hierarchy..
Top module:  \MISO
Removed 0 unused modules.

42. Printing statistics.

=== MISO ===

   Number of wires:               1586
   Number of wire bits:           3302
   Number of public wires:          34
   Number of public wire bits:    1750
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:               1590
     $_ANDNOT_                     444
     $_AND_                         52
     $_NAND_                        48
     $_NOR_                        106
     $_NOT_                         74
     $_ORNOT_                       84
     $_OR_                         267
     $_XNOR_                       183
     $_XOR_                        332

43. Executing CHECK pass (checking for obvious problems).
Checking module MISO...
Found and reported 0 problems.

44. Generating Graphviz representation of design.
Writing dot description to `/content/openlane_run/52-yosys-synthesis/primitive_techmap.dot'.
Dumping module MISO to page 1.

45. Executing OPT pass (performing simple optimizations).

45.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

45.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

45.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MISO..
Creating internal representation of mux trees.
No muxes found in this module.
Removed 0 multiplexer ports.

45.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MISO.
Performed a total of 0 changes.

45.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MISO'.
Removed a total of 0 cells.

45.6. Executing OPT_DFF pass (perform DFF optimizations).

45.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..

45.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module MISO.

45.9. Finished OPT passes. (There is nothing left to do.)

46. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..
Removed 0 unused cells and 30 unused wires.
<suppressed ~30 debug messages>
{
"creator": "Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)",
"invocation": "stat -json -liberty /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib ",
"modules": {
"\\MISO": {
"num_wires":         1556,
"num_wire_bits":     1712,
"num_pub_wires":     4,
"num_pub_wire_bits": 160,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         1590,
"num_cells_by_type": {
"$_ANDNOT_": 444,
"$_AND_": 52,
"$_NAND_": 48,
"$_NOR_": 106,
"$_NOT_": 74,
"$_ORNOT_": 84,
"$_OR_": 267,
"$_XNOR_": 183,
"$_XOR_": 332
}
}
},
"design": {
"num_wires":         1556,
"num_wire_bits":     1712,
"num_pub_wires":     4,
"num_pub_wire_bits": 160,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         1590,
"num_cells_by_type": {
"$_ANDNOT_": 444,
"$_AND_": 52,
"$_NAND_": 48,
"$_NOR_": 106,
```

```
"$_NOR_": 106,
"$_NOT_": 74,
"$_ORNOT_": 84,
"$_OR_": 267,
"$_XNOR_": 183,
"$_XOR_": 332
}
}
}

47. Printing statistics.

=== MISO ===

Number of wires:               1556
Number of wire bits:           1712
Number of public wires:           4
Number of public wire bits:     160
Number of memories:               0
Number of memory bits:            0
Number of processes:              0
Number of cells:               1590
$_ANDNOT_                     444
$_AND_                         52
$_NAND_                        48
$_NOR_                        106
$_NOT_                         74
$_ORNOT_                       84
$_OR_                         267
$_XNOR_                       183
$_XOR_                        332

Area for cell type $_NOT_ is unknown!
Area for cell type $_AND_ is unknown!
Area for cell type $_NAND_ is unknown!
Area for cell type $_OR_ is unknown!
Area for cell type $_NOR_ is unknown!
Area for cell type $_XOR_ is unknown!
Area for cell type $_XNOR_ is unknown!
Area for cell type $_ANDNOT_ is unknown!
Area for cell type $_ORNOT_ is unknown!

mapping tbuf
[INFO] Applying tri-state buffer mapping from
'/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tribuff_map.v'...

48. Executing TECHMAP pass (map to technology primitives).

48.1. Executing Verilog-2005 frontend: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tribuff_map.v
Parsing Verilog input from `/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tribuff_map.v' to AST
representation.
Generating RTLIL representation for module `\$_TBUF_'.
Successfully finished Verilog frontend.

48.2. Continuing TECHMAP pass.
No more expansions possible.
<suppressed ~3 debug messages>

49. Executing SIMPLEMAP pass (map simple cells to gate primitives).
[INFO] Applying latch mapping from '/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/latch_map.v'...

50. Executing TECHMAP pass (map to technology primitives).

50.1. Executing Verilog-2005 frontend: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/latch_map.v
Parsing Verilog input from `/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/latch_map.v' to AST
representation.
Generating RTLIL representation for module `\$_DLATCH_P_'.
Generating RTLIL representation for module `\$_DLATCH_N_'.
Successfully finished Verilog frontend.

50.2. Continuing TECHMAP pass.
No more expansions possible.
<suppressed ~4 debug messages>

51. Executing SIMPLEMAP pass (map simple cells to gate primitives).

52. Executing DFFLIBMAP pass (mapping DFF cells to sequential cells from liberty file).
cell sky130_fd_sc_hd__dfxtp_2 (noninv, pins=3, area=21.27) is a direct match for cell type $_DFF_P_.
cell sky130_fd_sc_hd__dfrtp_2 (noninv, pins=4, area=26.28) is a direct match for cell type $_DFF_PN0_.
cell sky130_fd_sc_hd__dfstp_2 (noninv, pins=4, area=26.28) is a direct match for cell type $_DFF_PN1_.
cell sky130_fd_sc_hd__dfbbn_2 (noninv, pins=6, area=35.03) is a direct match for cell type $_DFFSR_NNN_.
final dff cell mappings:
unmapped dff cell: $_DFF_N_
\sky130_fd_sc_hd__dfxtp_2 _DFF_P_ (.CLK( C), .D( D), .Q( Q));
unmapped dff cell: $_DFF_NN0_
unmapped dff cell: $_DFF_NN1_
unmapped dff cell: $_DFF_NP0_
unmapped dff cell: $_DFF_NP1_
\sky130_fd_sc_hd__dfrtp_2 _DFF_PN0_ (.CLK( C), .D( D), .Q( Q), .RESET_B( R));
\sky130_fd_sc_hd__dfstp_2 _DFF_PN1_ (.CLK( C), .D( D), .Q( Q), .SET_B( R));
unmapped dff cell: $_DFF_PP0_
unmapped dff cell: $_DFF_PP1_
\sky130_fd_sc_hd__dfbbn_2 _DFFSR_NNN_ (.CLK_N( C), .D( D), .Q( Q), .Q_N(~Q), .RESET_B( R), .SET_B( S));
unmapped dff cell: $_DFFSR_NNP_
unmapped dff cell: $_DFFSR_NPN_
unmapped dff cell: $_DFFSR_NPP_
unmapped dff cell: $_DFFSR_PNN_
unmapped dff cell: $_DFFSR_PNP_
unmapped dff cell: $_DFFSR_PPN_
unmapped dff cell: $_DFFSR_PPP_

52.1. Executing DFFLEGALIZE pass (convert FFs to types supported by the target).
Mapping DFF cells in module `\MISO':
{
"creator": "Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)",
"invocation": "stat -json -liberty /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib ",
"modules": {
"\\MISO": {
"num_wires":         1556,
"num_wire_bits":     1712,
"num_pub_wires":     4,
"num_pub_wire_bits": 160,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         1590,
"num_cells_by_type": {
"$_ANDNOT_": 444,
"$_AND_": 52,
"$_NAND_": 48,
"$_NOR_": 106,
"$_NOT_": 74,
"$_ORNOT_": 84,
"$_OR_": 267,
"$_XNOR_": 183,
"$_XOR_": 332
}
}
```

```
},
"design": {
"num_wires":         1556,
"num_wire_bits":     1712,
"num_pub_wires":     4,
"num_pub_wire_bits": 160,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         1590,
"num_cells_by_type": {
"$_ANDNOT_": 444,
"$_AND_": 52,
"$_NAND_": 48,
"$_NOR_": 106,
"$_NOT_": 74,
"$_ORNOT_": 84,
"$_OR_": 267,
"$_XNOR_": 183,
"$_XOR_": 332
}
}
}

53. Printing statistics.

=== MISO ===

Number of wires:               1556
Number of wire bits:           1712
Number of public wires:           4
Number of public wire bits:     160
Number of memories:               0
Number of memory bits:            0
Number of processes:              0
Number of cells:               1590
$_ANDNOT_                     444
$_AND_                         52
$_NAND_                        48
$_NOR_                        106
$_NOT_                         74
$_ORNOT_                       84
$_OR_                         267
$_XNOR_                       183
$_XOR_                        332

Area for cell type $_NOT_ is unknown!
Area for cell type $_AND_ is unknown!
Area for cell type $_NAND_ is unknown!
Area for cell type $_OR_ is unknown!
Area for cell type $_NOR_ is unknown!
Area for cell type $_XOR_ is unknown!
Area for cell type $_XNOR_ is unknown!
Area for cell type $_ANDNOT_ is unknown!
Area for cell type $_ORNOT_ is unknown!

[INFO] Using strategy "AREA 0"...

54. Executing ABC pass (technology mapping using ABC).

54.1. Extracting gate netlist of module `\MISO' to `/tmp/yosys-abc-VWabOl/input.blif'..
Extracted 1590 gates and 1686 wires to a netlist network with 96 inputs and 38 outputs.

54.1.1. Executing ABC.
Running ABC command: "/nix/store/wq2q0njg3sx8wvj2akz7x1qxwyrv9xlr-yosys-abc/bin/abc" -s -f
/tmp/yosys-abc-VWabOl/abc.script 2>&1
ABC: ABC command line: "source /tmp/yosys-abc-VWabOl/abc.script".
ABC:
ABC: + read_blif /tmp/yosys-abc-VWabOl/input.blif
ABC: + read_lib -w /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib
ABC: Parsing finished successfully.  Parsing time =     0.17 sec
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfbbn_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfrbp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfrtp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfrtp_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfsbp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfstp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfstp_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfxbp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfxtp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfxtp_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtn_1".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtn_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtn_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtp_1".
ABC: Scl_LibertyReadGenlib() skipped three-state cell "sky130_fd_sc_hd__ebufn_2".
ABC: Scl_LibertyReadGenlib() skipped three-state cell "sky130_fd_sc_hd__ebufn_4".
ABC: Scl_LibertyReadGenlib() skipped three-state cell "sky130_fd_sc_hd__ebufn_8".
ABC: Library "sky130_fd_sc_hd__tt_025C_1v80" from "/content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib"
has 175 cells (17 skipped: 14 seq; 3 tri-state; 0 no func; 0 dont_use).  Time =     0.29 sec
ABC: Memory =    9.54 MB. Time =     0.29 sec
ABC: Warning: Detected 2 multi-output gates (for example, "sky130_fd_sc_hd__fa_1").
ABC: + read_constr -v /content/openlane_run/52-yosys-synthesis/synthesis.sdc
ABC: Setting driving cell to be "sky130_fd_sc_hd__inv_2/Y".
ABC: Setting output load to be 33.442001.
ABC: + read_constr /content/openlane_run/52-yosys-synthesis/synthesis.sdc
ABC: + fx
ABC: + mfs
ABC: + strash
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + retime -D -D 10000 -M 5
ABC: + scleanup
ABC: Error: The network is combinational.
ABC: + fraig_store
ABC: + balance
ABC: + fraig_store
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + fraig_store
ABC: + balance
```

```
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + fraig_store
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + fraig_store
ABC: + fraig_restore
ABC: + amap -m -Q 0.1 -F 20 -A 20 -C 5000
ABC: + retime -D -D 10000
ABC: + &get -n
ABC: + &st
ABC: + &dch
ABC: + &nf
ABC: + &put
ABC: +

ABC: + stime -p
ABC: Cannot find the default PI driving cell (sky130_fd_sc_hd__inv_2/Y) in the library.
ABC: WireLoad = "none"  Gates =   1183 (  2.5 %)   Cap = 10.1 ff (  1.8 %)   Area =    11672.45 ( 93.7 %)   Delay =
7951.31 ps  (  4.0 %)
ABC: Path  0 --      15 : 0    7 pi                        A =   0.00  Df =   0.0   -0.0 ps  S =   0.0 ps  Cin =
0.0 ff  Cout =  37.1 ff  Cmax =   0.0 ff  G =    0
ABC: Path  1 --     228 : 2    2 sky130_fd_sc_hd__xor2_2   A =  16.27  Df = 203.3  -28.8 ps  S = 210.0 ps  Cin =
8.6 ff  Cout =  13.5 ff  Cmax = 130.0 ff  G =  152
ABC: Path  2 --     229 : 2    2 sky130_fd_sc_hd__xnor2_2  A =  16.27  Df = 421.3  -35.9 ps  S = 225.2 ps  Cin =
8.5 ff  Cout =  13.7 ff  Cmax = 121.8 ff  G =  154
ABC: Path  3 --     232 : 2    2 sky130_fd_sc_hd__xnor2_2  A =  16.27  Df = 659.4  -41.4 ps  S = 220.7 ps  Cin =
8.5 ff  Cout =  13.2 ff  Cmax = 121.8 ff  G =  148
ABC: Path  4 --     234 : 2    3 sky130_fd_sc_hd__xor2_2   A =  16.27  Df = 919.1  -88.7 ps  S = 208.5 ps  Cin =
8.6 ff  Cout =  13.4 ff  Cmax = 130.0 ff  G =  149
ABC: Path  5 --     237 : 3    3 sky130_fd_sc_hd__or3b_2   A =   8.76  Df =1434.2 -364.4 ps  S = 112.4 ps  Cin =
1.5 ff  Cout =  13.1 ff  Cmax = 269.2 ff  G =  831
ABC: Path  6 --     302 : 3    3 sky130_fd_sc_hd__or3_2    A =   7.51  Df =1983.2 -750.1 ps  S = 116.2 ps  Cin =
1.5 ff  Cout =  15.4 ff  Cmax = 310.4 ff  G =  969
ABC: Path  7 --     352 : 2    5 sky130_fd_sc_hd__nor2_2   A =   6.26  Df =2200.7 -381.0 ps  S = 194.3 ps  Cin =
4.4 ff  Cout =  15.7 ff  Cmax = 141.9 ff  G =  340
ABC: Path  8 --     501 : 4    3 sky130_fd_sc_hd__or4b_2   A =  10.01  Df =2876.9 -769.2 ps  S = 147.7 ps  Cin =
1.5 ff  Cout =  15.8 ff  Cmax = 265.5 ff  G = 1025
ABC: Path  9 --     574 : 3    6 sky130_fd_sc_hd__or3_2    A =   7.51  Df =3473.3-1158.9 ps  S = 142.0 ps  Cin =
1.5 ff  Cout =  26.4 ff  Cmax = 310.4 ff  G = 1665
ABC: Path 10 --     693 : 4    4 sky130_fd_sc_hd__or4_2    A =   8.76  Df =4218.8-1726.0 ps  S = 139.9 ps  Cin =
1.5 ff  Cout =  13.4 ff  Cmax = 310.4 ff  G =  843
ABC: Path 11 --     929 : 5    7 sky130_fd_sc_hd__a2111o_2 A =  12.51  Df =4753.4-1739.9 ps  S = 116.8 ps  Cin =
2.4 ff  Cout =  21.6 ff  Cmax = 324.1 ff  G =  851
ABC: Path 12 --    1176 : 4    5 sky130_fd_sc_hd__or4_2    A =   8.76  Df =5513.0-2300.3 ps  S = 156.1 ps  Cin =
1.5 ff  Cout =  18.8 ff  Cmax = 310.4 ff  G = 1202
ABC: Path 13 --    1213 : 2    2 sky130_fd_sc_hd__nor2_2   A =   6.26  Df =5732.7-2102.6 ps  S = 178.7 ps  Cin =
4.4 ff  Cout =  14.0 ff  Cmax = 141.9 ff  G =  300
ABC: Path 14 --    1251 : 2    2 sky130_fd_sc_hd__xor2_2   A =  16.27  Df =6003.2-2183.2 ps  S = 208.2 ps  Cin =
8.6 ff  Cout =  13.2 ff  Cmax = 130.0 ff  G =  147
ABC: Path 15 --    1253 : 2    2 sky130_fd_sc_hd__xor2_2   A =  16.27  Df =6243.0-2255.3 ps  S = 190.9 ps  Cin =
8.6 ff  Cout =  11.5 ff  Cmax = 130.0 ff  G =  128
ABC: Path 16 --    1263 : 2    3 sky130_fd_sc_hd__xnor2_2  A =  16.27  Df =6463.2 -591.6 ps  S = 222.9 ps  Cin =
8.5 ff  Cout =  13.4 ff  Cmax = 121.8 ff  G =  153
ABC: Path 17 --    1264 : 2    3 sky130_fd_sc_hd__xnor2_2  A =  16.27  Df =6719.7 -314.3 ps  S = 281.1 ps  Cin =
8.5 ff  Cout =  18.5 ff  Cmax = 121.8 ff  G =  206
ABC: Path 18 --    1286 : 2    1 sky130_fd_sc_hd__nor2_2   A =   6.26  Df =6797.2  -32.5 ps  S =  67.0 ps  Cin =
4.4 ff  Cout =   2.5 ff  Cmax = 141.9 ff  G =   53
ABC: Path 19 --    1290 : 5    2 sky130_fd_sc_hd__a221o_2  A =  11.26  Df =7158.9 -102.2 ps  S =  65.0 ps  Cin =
2.3 ff  Cout =   7.0 ff  Cmax = 299.4 ff  G =  289
ABC: Path 20 --    1293 : 3    2 sky130_fd_sc_hd__o21a_2   A =   8.76  Df =7380.6 -164.9 ps  S =  51.8 ps  Cin =
2.4 ff  Cout =   6.6 ff  Cmax = 294.8 ff  G =  261
ABC: Path 21 --    1314 : 4    2 sky130_fd_sc_hd__a2bb2o_2 A =  11.26  Df =7635.6 -242.1 ps  S =  75.8 ps  Cin =
1.7 ff  Cout =  11.1 ff  Cmax = 300.3 ff  G =  617
ABC: Path 22 --    1316 : 5    1 sky130_fd_sc_hd__a32o_2   A =  11.26  Df =7951.3 -306.3 ps  S = 207.7 ps  Cin =
2.3 ff  Cout =  33.4 ff  Cmax = 264.6 ff  G = 1430
ABC: Start-point = pi14 (\y [4]).  End-point = po35 (\out [35]).
ABC: + print_stats -m
ABC: netlist                       : i/o =   96/   38  lat =    0  nd =  1183  edge =   2893  area =11675.51  delay
=23.00  lev = 23
ABC: + write_blif /tmp/yosys-abc-VWabOl/output.blif

54.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__nor3b_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o2111a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o22a_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__a31oi_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__o21ba_2 cells:        6
ABC RESULTS:   sky130_fd_sc_hd__and4bb_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__o2bb2a_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__o221a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a311o_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a211o_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__or4b_2 cells:        4
ABC RESULTS:   sky130_fd_sc_hd__nand4_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a311oi_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__and4_2 cells:        8
ABC RESULTS:   sky130_fd_sc_hd__a41o_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__o2111ai_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a2111oi_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a2111o_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__or3b_2 cells:        9
ABC RESULTS:   sky130_fd_sc_hd__a211oi_2 cells:        4
ABC RESULTS:   sky130_fd_sc_hd__o211ai_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o31a_2 cells:        6
ABC RESULTS:   sky130_fd_sc_hd__o22ai_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__o21bai_2 cells:        5
ABC RESULTS:   sky130_fd_sc_hd__nor4_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__and4b_2 cells:        7
ABC RESULTS:   sky130_fd_sc_hd__o311a_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__o41a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o41ai_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__or4bb_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__and3b_2 cells:        11
ABC RESULTS:   sky130_fd_sc_hd__a21bo_2 cells:        9
ABC RESULTS:   sky130_fd_sc_hd__nand3b_2 cells:        5
ABC RESULTS:   sky130_fd_sc_hd__or4_2 cells:        9
ABC RESULTS:   sky130_fd_sc_hd__a22oi_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__mux2_1 cells:        14
ABC RESULTS:   sky130_fd_sc_hd__a31o_2 cells:        10
ABC RESULTS:   sky130_fd_sc_hd__o31ai_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__o32a_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__and2b_2 cells:        33
```

```
ABC RESULTS:   sky130_fd_sc_hd__nand3_2 cells:       15
ABC RESULTS:   sky130_fd_sc_hd__o211a_2 cells:        5
ABC RESULTS:   sky130_fd_sc_hd__a21boi_2 cells:        9
ABC RESULTS:   sky130_fd_sc_hd__nand2b_2 cells:       29
ABC RESULTS:   sky130_fd_sc_hd__nor3_2 cells:       14
ABC RESULTS:   sky130_fd_sc_hd__a21o_2 cells:       46
ABC RESULTS:   sky130_fd_sc_hd__a221o_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__o21a_2 cells:       15
ABC RESULTS:   sky130_fd_sc_hd__inv_2 cells:       30
ABC RESULTS:   sky130_fd_sc_hd__and2_2 cells:       68
ABC RESULTS:   sky130_fd_sc_hd__or3_2 cells:       22
ABC RESULTS:   sky130_fd_sc_hd__a22o_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__or2_2 cells:       87
ABC RESULTS:   sky130_fd_sc_hd__nand2_2 cells:      128
ABC RESULTS:   sky130_fd_sc_hd__and3_2 cells:       34
ABC RESULTS:   sky130_fd_sc_hd__a21oi_2 cells:       79
ABC RESULTS:   sky130_fd_sc_hd__o21ai_2 cells:       24
ABC RESULTS:   sky130_fd_sc_hd__xnor2_2 cells:      181
ABC RESULTS:   sky130_fd_sc_hd__nor2_2 cells:      107
ABC RESULTS:   sky130_fd_sc_hd__a2bb2o_2 cells:        4
ABC RESULTS:   sky130_fd_sc_hd__xor2_2 cells:       92
ABC RESULTS:   sky130_fd_sc_hd__a32o_2 cells:        5
ABC RESULTS:          _const0_ cells:        2
ABC RESULTS:        internal signals:     1552
ABC RESULTS:           input signals:       96
ABC RESULTS:          output signals:       38
Removing temp directory.

55. Executing SETUNDEF pass (replace undef values with defined constants).

56. Executing HILOMAP pass (mapping to constant drivers).

57. Executing SPLITNETS pass (splitting up multi-bit signals).

58. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MISO..
Removed 0 unused cells and 1714 unused wires.
<suppressed ~1 debug messages>

59. Executing INSBUF pass (insert buffer cells for connected wires).

60. Executing CHECK pass (checking for obvious problems).
Checking module MISO...
Found and reported 0 problems.
{
"creator": "Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)",
"invocation": "stat -json -liberty /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib ",
"modules": {
"\\MISO": {
"num_wires":         1149,
"num_wire_bits":     1305,
"num_pub_wires":     4,
"num_pub_wire_bits": 160,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         1209,
"area":              11777.545600,
"num_cells_by_type": {
"sky130_fd_sc_hd__a2111o_2": 2,
"sky130_fd_sc_hd__a2111oi_2": 1,
"sky130_fd_sc_hd__a211o_2": 2,
"sky130_fd_sc_hd__a211oi_2": 4,
"sky130_fd_sc_hd__a21bo_2": 9,
"sky130_fd_sc_hd__a21boi_2": 9,
"sky130_fd_sc_hd__a21o_2": 46,
"sky130_fd_sc_hd__a21oi_2": 79,
"sky130_fd_sc_hd__a221o_2": 3,
"sky130_fd_sc_hd__a22o_2": 3,
"sky130_fd_sc_hd__a22oi_2": 1,
"sky130_fd_sc_hd__a2bb2o_2": 4,
"sky130_fd_sc_hd__a311o_2": 1,
"sky130_fd_sc_hd__a311oi_2": 1,
"sky130_fd_sc_hd__a31o_2": 10,
"sky130_fd_sc_hd__a31oi_2": 2,
"sky130_fd_sc_hd__a32o_2": 5,
"sky130_fd_sc_hd__a41o_2": 2,
"sky130_fd_sc_hd__and2_2": 68,
"sky130_fd_sc_hd__and2b_2": 33,
"sky130_fd_sc_hd__and3_2": 34,
"sky130_fd_sc_hd__and3b_2": 11,
"sky130_fd_sc_hd__and4_2": 8,
"sky130_fd_sc_hd__and4b_2": 7,
"sky130_fd_sc_hd__and4bb_2": 3,
"sky130_fd_sc_hd__conb_1": 28,
"sky130_fd_sc_hd__inv_2": 30,
"sky130_fd_sc_hd__mux2_1": 14,
"sky130_fd_sc_hd__nand2_2": 128,
"sky130_fd_sc_hd__nand2b_2": 29,
"sky130_fd_sc_hd__nand3_2": 15,
"sky130_fd_sc_hd__nand3b_2": 5,
"sky130_fd_sc_hd__nand4_2": 1,
"sky130_fd_sc_hd__nor2_2": 107,
"sky130_fd_sc_hd__nor3_2": 14,
"sky130_fd_sc_hd__nor3b_2": 1,
"sky130_fd_sc_hd__nor4_2": 2,
"sky130_fd_sc_hd__o2111a_2": 1,
"sky130_fd_sc_hd__o2111ai_2": 1,
"sky130_fd_sc_hd__o211a_2": 5,
"sky130_fd_sc_hd__o211ai_2": 1,
"sky130_fd_sc_hd__o21a_2": 15,
"sky130_fd_sc_hd__o21ai_2": 24,
"sky130_fd_sc_hd__o21ba_2": 6,
"sky130_fd_sc_hd__o21bai_2": 5,
"sky130_fd_sc_hd__o221a_2": 1,
"sky130_fd_sc_hd__o22a_2": 2,
"sky130_fd_sc_hd__o22ai_2": 2,
"sky130_fd_sc_hd__o2bb2a_2": 2,
"sky130_fd_sc_hd__o311a_2": 3,
"sky130_fd_sc_hd__o31a_2": 6,
"sky130_fd_sc_hd__o31ai_2": 2,
"sky130_fd_sc_hd__o32a_2": 3,
"sky130_fd_sc_hd__o41a_2": 1,
"sky130_fd_sc_hd__o41ai_2": 2,
"sky130_fd_sc_hd__or2_2": 87,
"sky130_fd_sc_hd__or3_2": 22,
"sky130_fd_sc_hd__or3b_2": 9,
"sky130_fd_sc_hd__or4_2": 9,
"sky130_fd_sc_hd__or4b_2": 4,
"sky130_fd_sc_hd__or4bb_2": 1,
"sky130_fd_sc_hd__xnor2_2": 181,
"sky130_fd_sc_hd__xor2_2": 92
}
}
},
"design": {
"num_wires":         1149,
"num_wire_bits":     1305,
```

```
    "num_pub_wires":     4,
    "num_pub_wire_bits": 160,
    "num_memories":      0,
    "num_memory_bits":   0,
    "num_processes":     0,
    "num_cells":         1209,
    "area":              11777.545600,
    "num_cells_by_type": {
    "sky130_fd_sc_hd__a2111o_2": 2,
    "sky130_fd_sc_hd__a2111oi_2": 1,
    "sky130_fd_sc_hd__a211o_2": 2,
    "sky130_fd_sc_hd__a211oi_2": 4,
    "sky130_fd_sc_hd__a21bo_2": 9,
    "sky130_fd_sc_hd__a21boi_2": 9,
    "sky130_fd_sc_hd__a21o_2": 46,
    "sky130_fd_sc_hd__a21oi_2": 79,
    "sky130_fd_sc_hd__a221o_2": 3,
    "sky130_fd_sc_hd__a22o_2": 3,
    "sky130_fd_sc_hd__a22oi_2": 1,
    "sky130_fd_sc_hd__a2bb2o_2": 4,
    "sky130_fd_sc_hd__a311o_2": 1,
    "sky130_fd_sc_hd__a311oi_2": 1,
    "sky130_fd_sc_hd__a31o_2": 10,
    "sky130_fd_sc_hd__a31oi_2": 2,
    "sky130_fd_sc_hd__a32o_2": 5,
    "sky130_fd_sc_hd__a41o_2": 2,
    "sky130_fd_sc_hd__and2_2": 68,
    "sky130_fd_sc_hd__and2b_2": 33,
    "sky130_fd_sc_hd__and3_2": 34,
    "sky130_fd_sc_hd__and3b_2": 11,
    "sky130_fd_sc_hd__and4_2": 8,
    "sky130_fd_sc_hd__and4b_2": 7,
    "sky130_fd_sc_hd__and4bb_2": 3,
    "sky130_fd_sc_hd__conb_1": 28,
    "sky130_fd_sc_hd__inv_2": 30,
    "sky130_fd_sc_hd__mux2_1": 14,
    "sky130_fd_sc_hd__nand2_2": 128,
    "sky130_fd_sc_hd__nand2b_2": 29,
    "sky130_fd_sc_hd__nand3_2": 15,
    "sky130_fd_sc_hd__nand3b_2": 5,
    "sky130_fd_sc_hd__nand4_2": 1,
    "sky130_fd_sc_hd__nor2_2": 107,
    "sky130_fd_sc_hd__nor3_2": 14,
    "sky130_fd_sc_hd__nor3b_2": 1,
    "sky130_fd_sc_hd__nor4_2": 2,
    "sky130_fd_sc_hd__o2111a_2": 1,
    "sky130_fd_sc_hd__o2111ai_2": 1,
    "sky130_fd_sc_hd__o211a_2": 5,
    "sky130_fd_sc_hd__o211ai_2": 1,
    "sky130_fd_sc_hd__o21a_2": 15,
    "sky130_fd_sc_hd__o21ai_2": 24,
    "sky130_fd_sc_hd__o21ba_2": 6,
    "sky130_fd_sc_hd__o21bai_2": 5,
    "sky130_fd_sc_hd__o221a_2": 1,
    "sky130_fd_sc_hd__o22a_2": 2,
    "sky130_fd_sc_hd__o22ai_2": 2,
    "sky130_fd_sc_hd__o2bb2a_2": 2,
    "sky130_fd_sc_hd__o311a_2": 3,
    "sky130_fd_sc_hd__o31a_2": 6,
    "sky130_fd_sc_hd__o31ai_2": 2,
    "sky130_fd_sc_hd__o32a_2": 3,
    "sky130_fd_sc_hd__o41a_2": 1,
    "sky130_fd_sc_hd__o41ai_2": 2,
    "sky130_fd_sc_hd__or2_2": 87,
    "sky130_fd_sc_hd__or3_2": 22,
    "sky130_fd_sc_hd__or3b_2": 9,
    "sky130_fd_sc_hd__or4_2": 9,
    "sky130_fd_sc_hd__or4b_2": 4,
    "sky130_fd_sc_hd__or4bb_2": 1,
    "sky130_fd_sc_hd__xnor2_2": 181,
    "sky130_fd_sc_hd__xor2_2": 92
    }
    }
    }
```


61. Printing statistics.

```
=== MISO ===

Number of wires:               1149
Number of wire bits:           1305
```

```
display(synthesis)
```

Time Elapsed: 12.92s

Views updated:

- Verilog Netlist

Floorplanning

Floorplanning does two things:

- Determines the dimensions of the final chip.
- Creates the "cell placement grid" which placed cells must be aligned to.
  - Each cell in the grid is called a "site." Cells can occupy multiple sites, with the overwhelming majority of cells occupying multiple sites by width, and some standard cell libraries supporting varying heights as well.

> Don't forget- you may call `display_help()` on any Step class to get a full list of configuration variables.

```
Floorplan = Step.factory.get("OpenROAD.Floorplan")

floorplan = Floorplan(state_in=synthesis.state_out)
floorplan.start()
```

```
─────────────────────────────────────── Floorplan Initialization ───────────────────────────────────────
[15:35:35] VERBOSE  Running 'OpenROAD.Floorplan'…                                          step.py:1088
[15:35:35] VERBOSE  Logging subprocess to openlane_run/53-openroad-floorplan/openroad-floorplan.log…  step.py:1268
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading technology LEF file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef'…
[INFO ODB-0227] LEF file: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef, created
13 layers, 25 vias
Reading cell LEF file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef'…
The NOWIREEXTENSIONATPIN statement will be ignored. See file
/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef at line 2.

[INFO ODB-0227] LEF file: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef, created 4 library
cells
Reading cell LEF file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef'…
The NOWIREEXTENSIONATPIN statement will be ignored. See file
/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef at line 2.

[INFO ODB-0227] LEF file: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef, created 437
library cells
Reading top-level netlist at '/content/openlane_run/52-yosys-synthesis/MISO.nl.v'…
Linking design 'MISO' from netlist…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[15:35:37] WARNING  [STA-0366] port 'clk' not found.                                        openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[15:35:37] WARNING  [STA-0366] port 'clk' not found.                                        openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[15:35:37] WARNING  [STA-0419] transition time can not be specified for virtual clocks.      openroad.py:235
[INFO] Setting timing derate to: 5%
[15:35:37] WARNING  [STA-0450] virtual clock clk can not be propagated.                     openroad.py:235
Using site height: 2.72 and site width: 0.46…
[INFO] Using relative sizing for the floorplan.
[INFO IFP-0001] Added 56 rows of 333 site unithd.
[INFO IFP-0030] Inserted 0 tiecells using sky130_fd_sc_hd__conb_1/LO.
[INFO IFP-0030] Inserted 0 tiecells using sky130_fd_sc_hd__conb_1/HI.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 164.515 175.235 (µm).
[INFO] Floorplanned on a core area of 5.52 10.88 158.7 163.2 (µm).
Writing metric design__die__bbox: 0.0 0.0 164.515 175.235
Writing metric design__core__bbox: 5.52 10.88 158.7 163.2
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/53-openroad-floorplan/MISO.odb'…
Writing netlist to '/content/openlane_run/53-openroad-floorplan/MISO.nl.v'…
Writing powered netlist to '/content/openlane_run/53-openroad-floorplan/MISO.pnl.v'…
Writing layout to '/content/openlane_run/53-openroad-floorplan/MISO.def'…
Writing timing constraints to '/content/openlane_run/53-openroad-floorplan/MISO.sdc'…
```

Format	Path
nl	openlane_run/53-openroad-floorplan/MISO.nl.v
pnl	openlane_run/53-openroad-floorplan/MISO.pnl.v
def	openlane_run/53-openroad-floorplan/MISO.def

```
display(floorplan)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[15:35:37] VERBOSE  Running 'KLayout.Render'…                                                    step.py:1088
[15:35:37] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_ymqpleb5/klayout-render.log…  step.py:1268
```

Time Elapsed: 2.05s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Tap/Endcap Cell Insertion

This places two kinds of cells on the floorplan:

- End cap/boundary cells: Added at the beginning and end of each row. True to their name, they "cap off" the core area of a design.
- Tap cells: Placed in a polka dot-ish fashion across the rows. Tap cells connect VDD to the nwell and the psubstrate to VSS, which the majority of cells do not do themselves to save area- but if you go long enough without one such connection you end up with the cell "latching-up"; i.e.; refusing to switch back to LO from HI.

  There is a maximum distance between tap cells enforced as part of every foundry process.

```
TapEndcapInsertion = Step.factory.get("OpenROAD.TapEndcapInsertion")

tdi = TapEndcapInsertion(state_in=floorplan.state_out)
tdi.start()
```

```
──────────────────────────────────────────── Tap/Decap Insertion ────────────────────────────────────────────
[15:35:39] VERBOSE  Running 'OpenROAD.TapEndcapInsertion'…                                   step.py:1088
[15:35:39] VERBOSE  Logging subprocess to                                                     step.py:1268
                    openlane_run/54-openroad-tapendcapinsertion/openroad-tapendcapinsertion.log…
Reading OpenROAD database at '/content/openlane_run/53-openroad-floorplan/MISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[15:35:39] WARNING  [STA-0366] port 'clk' not found.                                          openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[15:35:39] WARNING  [STA-0366] port 'clk' not found.                                          openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[15:35:40] WARNING  [STA-0419] transition time can not be specified for virtual clocks.        openroad.py:235
[INFO] Setting timing derate to: 5%
[15:35:40] WARNING  [STA-0450] virtual clock clk can not be propagated.                       openroad.py:235
[INFO TAP-0004] Inserted 112 endcaps.
[INFO TAP-0005] Inserted 319 tapcells.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/54-openroad-tapendcapinsertion/MISO.odb'…
Writing netlist to '/content/openlane_run/54-openroad-tapendcapinsertion/MISO.nl.v'…
Writing powered netlist to '/content/openlane_run/54-openroad-tapendcapinsertion/MISO.pnl.v'…
Writing layout to '/content/openlane_run/54-openroad-tapendcapinsertion/MISO.def'…
Writing timing constraints to '/content/openlane_run/54-openroad-tapendcapinsertion/MISO.sdc'…
```

Format	Path
nl	openlane_run/54-openroad-tapendcapinsertion/MISO.nl.v
pnl	openlane_run/54-openroad-tapendcapinsertion/MISO.pnl.v
def	openlane_run/54-openroad-tapendcapinsertion/MISO.def
odb	openlane_run/54-openroad-tapendcapinsertion/MISO.odb

```
display(tdi)
```

```
──────────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────────
[15:35:40] VERBOSE  Running 'KLayout.Render'…                                                 step.py:1088
[15:35:40] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_vih9br23/klayout-render.log…  step.py:1268
```

Time Elapsed: 1.34s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

I/O Placement

This places metal pins at the edges of the design corresponding to the top level inputs and outputs for your design. These pins act as the interface with other designs when you integrate it with other designs.

```
IOPlacement = Step.factory.get("OpenROAD.IOPlacement")

ioplace = IOPlacement(state_in=tdi.state_out)
ioplace.start()
```

```
I/O Placement
[15:35:41] VERBOSE  Running 'OpenROAD.IOPlacement'…                                   step.py:1088
[15:35:41] VERBOSE  Logging subprocess to                                             step.py:1268
                    openlane_run/55-openroad-ioplacement/openroad-ioplacement.log…
Reading OpenROAD database at '/content/openlane_run/54-openroad-tapendcapinsertion/MISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[15:35:42] WARNING  [STA-0366] port 'clk' not found.                                  openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[15:35:42] WARNING  [STA-0366] port 'clk' not found.                                  openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[15:35:42] WARNING  [STA-0419] transition time can not be specified for virtual clocks.  openroad.py:235
[INFO] Setting timing derate to: 5%
[15:35:42] WARNING  [STA-0450] virtual clock clk can not be propagated.                openroad.py:235
[INFO] place_pins args: -min_distance 3
Found 0 macro blocks.
[INFO PPL-0010] Tentative 0 to set up sections.
[INFO PPL-0001] Number of slots          206
[INFO PPL-0002] Number of I/O            160
[INFO PPL-0003] Number of I/O w/sink     160
[INFO PPL-0004] Number of I/O w/o sink   0
[INFO PPL-0005] Slots per section        200
[INFO PPL-0006] Slots increase factor    0.01
[INFO PPL-0008] Successfully assigned pins to sections.
[INFO PPL-0012] I/O nets HPWL: 20173.51 um.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/55-openroad-ioplacement/MISO.odb'…
Writing netlist to '/content/openlane_run/55-openroad-ioplacement/MISO.nl.v'…
Writing powered netlist to '/content/openlane_run/55-openroad-ioplacement/MISO.pnl.v'…
Writing layout to '/content/openlane_run/55-openroad-ioplacement/MISO.def'…
Writing timing constraints to '/content/openlane_run/55-openroad-ioplacement/MISO.sdc'…
```

Format	Path
nl	openlane_run/55-openroad-ioplacement/MISO.nl.v
pnl	openlane_run/55-openroad-ioplacement/MISO.pnl.v
def	openlane_run/55-openroad-ioplacement/MISO.def
odb	openlane_run/55-openroad-ioplacement/MISO.odb

```
display(ioplace)
```

```
Render Image (w/ KLayout)
[15:35:42] VERBOSE  Running 'KLayout.Render'…                                         step.py:1088
[15:35:42] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_ky7tgub9/klayout-render.log…  step.py:1268
```

Time Elapsed: 1.44s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Generating the Power Distribution Network (PDN)

This creates the power distribution network for your design, which is essentially a plaid pattern of horizontal and vertical "straps" across the design that is then connected to the rails' VDD and VSS (via the tap cells.)

You can find an explanation of how the power distribution network works at this link:
https://openlane2.readthedocs.io/en/latest/usage/hardening_macros.html#pdn-generation

While we typically don't need to mess with the PDN too much, the SPM is a small design, so we're going to need to make the plaid pattern formed by the PDN a bit smaller.

```
GeneratePDN = Step.factory.get("OpenROAD.GeneratePDN")

pdn = GeneratePDN(
    state_in=ioplace.state_out,
    FP_PDN_VWIDTH=2,
    FP_PDN_HWIDTH=2,
    FP_PDN_VPITCH=30,
    FP_PDN_HPITCH=30,
)
pdn.start()
```

```
─────────────────────────────────── Power Distribution Network Generation ───────────────────────────────────
[15:35:43] VERBOSE  Running 'OpenROAD.GeneratePDN'…                                                  step.py:1088
[15:35:43] INFO     'FP_PDN_CFG' not explicitly set, setting it to                                openroad.py:1174
                    /content/openlane_ipynb/openlane/scripts/openroad/common/pdn_cfg.tcl…
[15:35:44] VERBOSE  Logging subprocess to                                                            step.py:1268
                    openlane_run/56-openroad-generatepdn/openroad-generatepdn.log…
Reading OpenROAD database at '/content/openlane_run/55-openroad-ioplacement/MISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[15:35:44] WARNING  [STA-0366] port 'clk' not found.                                              openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[15:35:44] WARNING  [STA-0366] port 'clk' not found.                                              openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.1499999999999999944488848768742172978818416595458984375
[15:35:44] WARNING  [STA-0419] transition time can not be specified for virtual clocks.            openroad.py:235
[INFO] Setting timing derate to: 5%
[15:35:44] WARNING  [STA-0450] virtual clock clk can not be propagated.                           openroad.py:235
[INFO] Setting global connections...
[INFO PDN-0001] Inserting grid: stdcell_grid
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/56-openroad-generatepdn/MISO.odb'…
Writing netlist to '/content/openlane_run/56-openroad-generatepdn/MISO.nl.v'…
Writing powered netlist to '/content/openlane_run/56-openroad-generatepdn/MISO.pnl.v'…
Writing layout to '/content/openlane_run/56-openroad-generatepdn/MISO.def'…
Writing timing constraints to '/content/openlane_run/56-openroad-generatepdn/MISO.sdc'…
[INFO PSM-0040] All shapes on net VPWR are connected.
[INFO PSM-0040] All shapes on net VGND are connected.
```

Format	Path
nl	openlane_run/56-openroad-generatepdn/MISO.nl.v
pnl	openlane_run/56-openroad-generatepdn/MISO.pnl.v
def	openlane_run/56-openroad-generatepdn/MISO.def
odb	openlane_run/56-openroad-generatepdn/MISO.odb

```
display(pdn)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[15:35:45] VERBOSE  Running 'KLayout.Render'…                                                  step.py:1088
[15:35:45] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_uib0u1qf/klayout-render.log…  step.py:1268
```

Time Elapsed: 1.44s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Global Placement

Global Placement is deciding on a fuzzy, non-final location for each of the cells, with the aim of minimizing the distance between cells that are connected together (more specifically, the total length of the not-yet-created wires that will connect them).

As you will see in the `.display()` in the second cell below, the placement is considered "illegal", i.e., not properly aligned with the cell placement grid. This is addressed by "Detailed Placement", also referred to as "placement legalization", which is the next step.

```
GlobalPlacement = Step.factory.get("OpenROAD.GlobalPlacement")

gpl = GlobalPlacement(state_in=pdn.state_out)
gpl.start()
```

```
──────────────────────────────────────────────────────────── Global Placement ────────────────────────────────────────────────────────────
[15:35:46] VERBOSE  Running 'OpenROAD.GlobalPlacement'…                                                                          step.py:1088
[15:35:46] INFO     'PL_TARGET_DENSITY_PCT' not explicitly set, using dynamically calculated                                  openroad.py:1260
                    target density: 62.187900…
[15:35:46] VERBOSE  Logging subprocess to                                                                                        step.py:1268
                    openlane_run/57-openroad-globalplacement/openroad-globalplacement.log…
Reading OpenROAD database at '/content/openlane_run/56-openroad-generatepdn/MISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[15:35:47] WARNING  [STA-0366] port 'clk' not found.                                                                              openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[15:35:47] WARNING  [STA-0366] port 'clk' not found.                                                                              openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[15:35:47] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                           openroad.py:235
[INFO] Setting timing derate to: 5%
[15:35:47] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                          openroad.py:235
[INFO] Setting RC values…
[INFO] Setting signal min routing layer to: met1 and clock min routing layer to met1.
[INFO] Setting signal max routing layer to: met5 and clock max routing layer to met5.
[INFO GPL-0002] DBU: 1000
[INFO GPL-0003] SiteSize: (  0.460  2.720 ) um
[INFO GPL-0004] CoreBBox: (  5.520 10.880 ) ( 158.700 163.200 ) um
[INFO GPL-0006] NumInstances:              1640
[INFO GPL-0007] NumPlaceInstances:         1209
[INFO GPL-0008] NumFixedInstances:          431
[INFO GPL-0009] NumDummyInstances:            0
[INFO GPL-0010] NumNets:                   1305
[INFO GPL-0011] NumPins:                   4262
[INFO GPL-0012] DieBBox:  (  0.000  0.000 ) ( 164.515 175.235 ) um
[INFO GPL-0013] CoreBBox: (  5.520 10.880 ) ( 158.700 163.200 ) um
[INFO GPL-0016] CoreArea:             23332.378 um^2
[INFO GPL-0017] NonPlaceInstsArea:      819.536 um^2
[INFO GPL-0018] PlaceInstsArea:       11777.546 um^2
[INFO GPL-0019] Util:                    52.315 %
[INFO GPL-0020] StdInstsArea:         11777.546 um^2
[INFO GPL-0021] MacroInstsArea:           0.000 um^2
[InitialPlace]  Iter: 1 CG residual: 0.00000447 HPWL: 31952055
[InitialPlace]  Iter: 2 CG residual: 0.00000012 HPWL: 26208269
[InitialPlace]  Iter: 3 CG residual: 0.00000012 HPWL: 26243464
[InitialPlace]  Iter: 4 CG residual: 0.00000009 HPWL: 26265816
[InitialPlace]  Iter: 5 CG residual: 0.00000011 HPWL: 26250892
[INFO GPL-0031] FillerInit:NumGCells:      1438
[INFO GPL-0032] FillerInit:NumGNets:       1305
[INFO GPL-0033] FillerInit:NumGPins:       4262
[INFO GPL-0023] TargetDensity:            0.622
[INFO GPL-0024] AvrgPlaceInstArea:        9.742 um^2
[INFO GPL-0025] IdealBinArea:            15.665 um^2
[INFO GPL-0026] IdealBinCnt:               1489
[INFO GPL-0027] TotalBinArea:         23332.378 um^2
[INFO GPL-0028] BinCnt:        32     32
[INFO GPL-0029] BinSize: (  4.787  4.760 )
[INFO GPL-0030] NumBins: 1024
[NesterovSolve] Iter:    1 overflow: 0.911 HPWL: 20599978
[INFO GPL-0100] worst slack -1.8e-09
[INFO GPL-0103] Weighted 127 nets.
[NesterovSolve] Iter:   10 overflow: 0.682 HPWL: 25605735
[INFO GPL-0100] worst slack -1.88e-09
[INFO GPL-0103] Weighted 126 nets.
[NesterovSolve] Iter:   20 overflow: 0.606 HPWL: 26390336
[NesterovSolve] Snapshot saved at iter = 22
[NesterovSolve] Iter:   30 overflow: 0.589 HPWL: 26209866
[NesterovSolve] Iter:   40 overflow: 0.596 HPWL: 25988508
[NesterovSolve] Iter:   50 overflow: 0.599 HPWL: 25930282
[NesterovSolve] Iter:   60 overflow: 0.600 HPWL: 25957783
[NesterovSolve] Iter:   70 overflow: 0.601 HPWL: 25999869
[NesterovSolve] Iter:   80 overflow: 0.602 HPWL: 26004750
[NesterovSolve] Iter:   90 overflow: 0.601 HPWL: 25997408
[NesterovSolve] Iter:  100 overflow: 0.599 HPWL: 26002480
[NesterovSolve] Iter:  110 overflow: 0.598 HPWL: 25997064
[NesterovSolve] Iter:  120 overflow: 0.599 HPWL: 25980945
[NesterovSolve] Iter:  130 overflow: 0.600 HPWL: 25978347
[NesterovSolve] Iter:  140 overflow: 0.600 HPWL: 25994191
[NesterovSolve] Iter:  150 overflow: 0.597 HPWL: 26005257
[NesterovSolve] Iter:  160 overflow: 0.596 HPWL: 26014190
[NesterovSolve] Iter:  170 overflow: 0.594 HPWL: 26037412
[NesterovSolve] Iter:  180 overflow: 0.590 HPWL: 26062938
[NesterovSolve] Iter:  190 overflow: 0.585 HPWL: 26099287
[NesterovSolve] Iter:  200 overflow: 0.576 HPWL: 26138837
[NesterovSolve] Iter:  210 overflow: 0.564 HPWL: 26132880
[NesterovSolve] Iter:  220 overflow: 0.547 HPWL: 26131200
[NesterovSolve] Iter:  230 overflow: 0.525 HPWL: 26099782
[NesterovSolve] Iter:  240 overflow: 0.493 HPWL: 26011996
[INFO GPL-0100] worst slack -1.81e-09
[INFO GPL-0103] Weighted 127 nets.
[NesterovSolve] Iter:  250 overflow: 0.454 HPWL: 25766704
[NesterovSolve] Iter:  260 overflow: 0.420 HPWL: 25372229
[NesterovSolve] Iter:  270 overflow: 0.389 HPWL: 25109223
[NesterovSolve] Iter:  280 overflow: 0.359 HPWL: 25044816
[NesterovSolve] Iter:  290 overflow: 0.331 HPWL: 24987794
[NesterovSolve] Iter:  300 overflow: 0.305 HPWL: 24805957
[NesterovSolve] Iter:  310 overflow: 0.284 HPWL: 24800268
[INFO GPL-0100] worst slack -1.77e-09
[INFO GPL-0103] Weighted 127 nets.
[NesterovSolve] Iter:  320 overflow: 0.259 HPWL: 24800788
[NesterovSolve] Iter:  330 overflow: 0.240 HPWL: 24815285
[NesterovSolve] Iter:  340 overflow: 0.220 HPWL: 24858933
[INFO GPL-0100] worst slack -1.76e-09
[INFO GPL-0103] Weighted 127 nets.
[NesterovSolve] Iter:  350 overflow: 0.202 HPWL: 24964317
[INFO GPL-0075] Routability numCall: 1 inflationIterCnt: 1 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      23   25
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 575
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0.06666672229766846
[INFO GPL-0065] OverflowTileCnt2: 1
[INFO GPL-0066] 0.5%RC: 1.0111
[INFO GPL-0067] 1.0%RC: 1.0061
[INFO GPL-0068] 2.0%RC: 0.9875
[INFO GPL-0069] 5.0%RC: 0.9392
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0086
[INFO GPL-0078] FinalRC lower than minRC (1e+30), min RC updated.
[INFO GPL-0045] InflatedAreaDelta:        7.217 um^2
[INFO GPL-0046] TargetDensity:            0.622
[INFO GPL-0049] WhiteSpaceArea:       22512.842 um^2
[INFO GPL-0050] NesterovInstsArea:    11777.546 um^2
[INFO GPL-0051] TotalFillerArea:       2222.717 um^2
[INFO GPL-0052] TotalGCellsArea:      14000.262 um^2
```

```
[INFO GPL-0053] ExpectedGCellsArea:   14007.479 um^2
[INFO GPL-0054] NewTargetDensity:         0.622
[INFO GPL-0055] NewWhiteSpaceArea:    22512.842 um^2
[INFO GPL-0056] MovableArea:          14007.479 um^2
[INFO GPL-0057] NewNesterovInstArea:  11784.762 um^2
[INFO GPL-0058] NewTotalFillerArea:    2222.717 um^2
[INFO GPL-0059] NewTotalGCellsArea:   14007.479 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter:  360 overflow: 0.588 HPWL: 26199924
[NesterovSolve] Iter:  370 overflow: 0.594 HPWL: 26007348
[NesterovSolve] Iter:  380 overflow: 0.597 HPWL: 25949730
[NesterovSolve] Iter:  390 overflow: 0.599 HPWL: 25978800
[NesterovSolve] Iter:  400 overflow: 0.600 HPWL: 26017888
[NesterovSolve] Iter:  410 overflow: 0.601 HPWL: 26030317
[NesterovSolve] Iter:  420 overflow: 0.599 HPWL: 26023967
[NesterovSolve] Iter:  430 overflow: 0.596 HPWL: 26020292
[NesterovSolve] Iter:  440 overflow: 0.596 HPWL: 26010935
[NesterovSolve] Iter:  450 overflow: 0.598 HPWL: 25997258
[NesterovSolve] Iter:  460 overflow: 0.600 HPWL: 25999614
[NesterovSolve] Iter:  470 overflow: 0.599 HPWL: 26015465
[NesterovSolve] Iter:  480 overflow: 0.598 HPWL: 26023161
[NesterovSolve] Iter:  490 overflow: 0.597 HPWL: 26023206
[NesterovSolve] Iter:  500 overflow: 0.596 HPWL: 26023481
[NesterovSolve] Iter:  510 overflow: 0.595 HPWL: 26023907
[NesterovSolve] Iter:  520 overflow: 0.595 HPWL: 26024309
[NesterovSolve] Iter:  530 overflow: 0.594 HPWL: 26031914
[NesterovSolve] Iter:  540 overflow: 0.592 HPWL: 26049318
[NesterovSolve] Iter:  550 overflow: 0.588 HPWL: 26074296
[NesterovSolve] Iter:  560 overflow: 0.585 HPWL: 26099731
[NesterovSolve] Iter:  570 overflow: 0.580 HPWL: 26126788
[NesterovSolve] Iter:  580 overflow: 0.568 HPWL: 26119115
[NesterovSolve] Iter:  590 overflow: 0.559 HPWL: 26092535
[NesterovSolve] Iter:  600 overflow: 0.545 HPWL: 26074294
[NesterovSolve] Iter:  610 overflow: 0.530 HPWL: 26052757
[NesterovSolve] Iter:  620 overflow: 0.506 HPWL: 25992823
[NesterovSolve] Iter:  630 overflow: 0.479 HPWL: 25824894
[NesterovSolve] Iter:  640 overflow: 0.448 HPWL: 25580566
[NesterovSolve] Iter:  650 overflow: 0.418 HPWL: 25233550
[NesterovSolve] Iter:  660 overflow: 0.394 HPWL: 25099024
[NesterovSolve] Iter:  670 overflow: 0.364 HPWL: 25005036
[NesterovSolve] Iter:  680 overflow: 0.343 HPWL: 24966186
[NesterovSolve] Iter:  690 overflow: 0.319 HPWL: 24839451
[NesterovSolve] Iter:  700 overflow: 0.301 HPWL: 24805821
[NesterovSolve] Iter:  710 overflow: 0.274 HPWL: 24812853
[NesterovSolve] Iter:  720 overflow: 0.254 HPWL: 24820075
[NesterovSolve] Iter:  730 overflow: 0.236 HPWL: 24901624
[NesterovSolve] Iter:  740 overflow: 0.214 HPWL: 24938805
[INFO GPL-0075] Routability numCall: 2 inflationIterCnt: 2 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      23   25
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 575
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0.13333332538604736
[INFO GPL-0065] OverflowTileCnt2: 1
[INFO GPL-0066] 0.5%RC: 1.0222
[INFO GPL-0067] 1.0%RC: 1.0121
[INFO GPL-0068] 2.0%RC: 0.9922
[INFO GPL-0069] 5.0%RC: 0.9405
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0172
[INFO GPL-0079] MinRC (1.0085858) violation occurred, total count: 1.
[INFO GPL-0045] InflatedAreaDelta:       32.590 um^2
[INFO GPL-0046] TargetDensity:            0.622
[INFO GPL-0049] WhiteSpaceArea:       22512.842 um^2
[INFO GPL-0050] NesterovInstsArea:    11784.762 um^2
[INFO GPL-0051] TotalFillerArea:       2222.717 um^2
[INFO GPL-0052] TotalGCellsArea:      14007.479 um^2
[INFO GPL-0053] ExpectedGCellsArea:   14040.069 um^2
[INFO GPL-0054] NewTargetDensity:         0.624
[INFO GPL-0055] NewWhiteSpaceArea:    22512.842 um^2
[INFO GPL-0056] MovableArea:          14040.069 um^2
[INFO GPL-0057] NewNesterovInstArea:  11817.352 um^2
[INFO GPL-0058] NewTotalFillerArea:    2222.717 um^2
[INFO GPL-0059] NewTotalGCellsArea:   14040.069 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter:  750 overflow: 0.591 HPWL: 26341663
[NesterovSolve] Iter:  760 overflow: 0.591 HPWL: 26090634
[NesterovSolve] Iter:  770 overflow: 0.596 HPWL: 25964895
[NesterovSolve] Iter:  780 overflow: 0.598 HPWL: 25958599
[NesterovSolve] Iter:  790 overflow: 0.600 HPWL: 26001205
[NesterovSolve] Iter:  800 overflow: 0.601 HPWL: 26030056
[NesterovSolve] Iter:  810 overflow: 0.600 HPWL: 26029645
[NesterovSolve] Iter:  820 overflow: 0.598 HPWL: 26023461
[NesterovSolve] Iter:  830 overflow: 0.596 HPWL: 26018804
[NesterovSolve] Iter:  840 overflow: 0.597 HPWL: 26005455
[NesterovSolve] Iter:  850 overflow: 0.599 HPWL: 25997044
[NesterovSolve] Iter:  860 overflow: 0.600 HPWL: 26009123
[NesterovSolve] Iter:  870 overflow: 0.599 HPWL: 26022040
[NesterovSolve] Iter:  880 overflow: 0.598 HPWL: 26025081
[NesterovSolve] Iter:  890 overflow: 0.597 HPWL: 26024947
[NesterovSolve] Iter:  900 overflow: 0.596 HPWL: 26025347
[NesterovSolve] Iter:  910 overflow: 0.595 HPWL: 26024051
[NesterovSolve] Iter:  920 overflow: 0.595 HPWL: 26027500
[NesterovSolve] Iter:  930 overflow: 0.593 HPWL: 26038844
[NesterovSolve] Iter:  940 overflow: 0.591 HPWL: 26058210
[NesterovSolve] Iter:  950 overflow: 0.587 HPWL: 26079826
[NesterovSolve] Iter:  960 overflow: 0.583 HPWL: 26104410
[NesterovSolve] Iter:  970 overflow: 0.575 HPWL: 26126727
[NesterovSolve] Iter:  980 overflow: 0.564 HPWL: 26100056
[NesterovSolve] Iter:  990 overflow: 0.552 HPWL: 26074926
[NesterovSolve] Iter: 1000 overflow: 0.538 HPWL: 26050737
[NesterovSolve] Iter: 1010 overflow: 0.519 HPWL: 26020169
[NesterovSolve] Iter: 1020 overflow: 0.493 HPWL: 25896304
[NesterovSolve] Iter: 1030 overflow: 0.462 HPWL: 25703052
[NesterovSolve] Iter: 1040 overflow: 0.431 HPWL: 25406097
[NesterovSolve] Iter: 1050 overflow: 0.409 HPWL: 25127912
[NesterovSolve] Iter: 1060 overflow: 0.378 HPWL: 25029326
[NesterovSolve] Iter: 1070 overflow: 0.353 HPWL: 24953757
[NesterovSolve] Iter: 1080 overflow: 0.329 HPWL: 24928987
[NesterovSolve] Iter: 1090 overflow: 0.309 HPWL: 24793709
[NesterovSolve] Iter: 1100 overflow: 0.289 HPWL: 24825903
[NesterovSolve] Iter: 1110 overflow: 0.264 HPWL: 24790187
[NesterovSolve] Iter: 1120 overflow: 0.247 HPWL: 24865100
[NesterovSolve] Iter: 1130 overflow: 0.225 HPWL: 24919241
[NesterovSolve] Iter: 1140 overflow: 0.204 HPWL: 24984151
[INFO GPL-0075] Routability numCall: 3 inflationIterCnt: 3 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      23   25
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 575
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0.13333332538604736
[INFO GPL-0065] OverflowTileCnt2: 1
[INFO GPL-0066] 0.5%RC: 1.0222
```

```
[INFO GPL-0067] 1.0%RC: 1.0061
[INFO GPL-0068] 2.0%RC: 0.9859
[INFO GPL-0069] 5.0%RC: 0.9329
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0141
[INFO GPL-0079] MinRC (1.0085858) violation occurred, total count: 2.
[INFO GPL-0045] InflatedAreaDelta:       32.015 um^2
[INFO GPL-0046] TargetDensity:            0.624
[INFO GPL-0049] WhiteSpaceArea:       22512.842 um^2
[INFO GPL-0050] NesterovInstsArea:    11817.352 um^2
[INFO GPL-0051] TotalFillerArea:       2222.717 um^2
[INFO GPL-0052] TotalGCellsArea:      14040.069 um^2
[INFO GPL-0053] ExpectedGCellsArea:   14072.084 um^2
[INFO GPL-0054] NewTargetDensity:         0.625
[INFO GPL-0055] NewWhiteSpaceArea:    22512.842 um^2
[INFO GPL-0056] MovableArea:          14072.084 um^2
[INFO GPL-0057] NewNesterovInstArea:  11849.368 um^2
[INFO GPL-0058] NewTotalFillerArea:    2222.717 um^2
[INFO GPL-0059] NewTotalGCellsArea:   14072.084 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter: 1150 overflow: 0.589 HPWL: 26204708
[NesterovSolve] Iter: 1160 overflow: 0.595 HPWL: 26013647
[NesterovSolve] Iter: 1170 overflow: 0.598 HPWL: 25955409
[NesterovSolve] Iter: 1180 overflow: 0.599 HPWL: 25984968
[NesterovSolve] Iter: 1190 overflow: 0.601 HPWL: 26023934
[NesterovSolve] Iter: 1200 overflow: 0.601 HPWL: 26036135
[NesterovSolve] Iter: 1210 overflow: 0.599 HPWL: 26028817
[NesterovSolve] Iter: 1220 overflow: 0.597 HPWL: 26025867
[NesterovSolve] Iter: 1230 overflow: 0.597 HPWL: 26016936
[NesterovSolve] Iter: 1240 overflow: 0.598 HPWL: 26002660
[NesterovSolve] Iter: 1250 overflow: 0.600 HPWL: 26004568
[NesterovSolve] Iter: 1260 overflow: 0.600 HPWL: 26020423
[NesterovSolve] Iter: 1270 overflow: 0.599 HPWL: 26028598
[NesterovSolve] Iter: 1280 overflow: 0.598 HPWL: 26029337
[NesterovSolve] Iter: 1290 overflow: 0.597 HPWL: 26029609
[NesterovSolve] Iter: 1300 overflow: 0.596 HPWL: 26029697
[NesterovSolve] Iter: 1310 overflow: 0.595 HPWL: 26029778
[NesterovSolve] Iter: 1320 overflow: 0.594 HPWL: 26036970
[NesterovSolve] Iter: 1330 overflow: 0.592 HPWL: 26054637
[NesterovSolve] Iter: 1340 overflow: 0.589 HPWL: 26079792
[NesterovSolve] Iter: 1350 overflow: 0.585 HPWL: 26106188
[NesterovSolve] Iter: 1360 overflow: 0.581 HPWL: 26136514
[NesterovSolve] Iter: 1370 overflow: 0.569 HPWL: 26131246
[NesterovSolve] Iter: 1380 overflow: 0.559 HPWL: 26102114
[NesterovSolve] Iter: 1390 overflow: 0.546 HPWL: 26086750
[NesterovSolve] Iter: 1400 overflow: 0.530 HPWL: 26060877
[NesterovSolve] Iter: 1410 overflow: 0.506 HPWL: 26001321
[NesterovSolve] Iter: 1420 overflow: 0.477 HPWL: 25831987
[NesterovSolve] Iter: 1430 overflow: 0.448 HPWL: 25591261
[NesterovSolve] Iter: 1440 overflow: 0.418 HPWL: 25247957
[NesterovSolve] Iter: 1450 overflow: 0.393 HPWL: 25119895
[NesterovSolve] Iter: 1460 overflow: 0.364 HPWL: 24993108
[NesterovSolve] Iter: 1470 overflow: 0.344 HPWL: 24948757
[NesterovSolve] Iter: 1480 overflow: 0.321 HPWL: 24858024
[NesterovSolve] Iter: 1490 overflow: 0.303 HPWL: 24798947
[NesterovSolve] Iter: 1500 overflow: 0.274 HPWL: 24824637
[NesterovSolve] Iter: 1510 overflow: 0.256 HPWL: 24824505
[NesterovSolve] Iter: 1520 overflow: 0.236 HPWL: 24904695
[NesterovSolve] Iter: 1530 overflow: 0.212 HPWL: 24944247
[INFO GPL-0075] Routability numCall: 4 inflationIterCnt: 4 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      23   25
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 575
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0
[INFO GPL-0065] OverflowTileCnt2: 0
[INFO GPL-0066] 0.5%RC: 1.0000
[INFO GPL-0067] 1.0%RC: 1.0000
[INFO GPL-0068] 2.0%RC: 0.9844
[INFO GPL-0069] 5.0%RC: 0.9392
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0000
[INFO GPL-0078] FinalRC lower than minRC (1.0085858), min RC updated.
[INFO GPL-0045] InflatedAreaDelta:        0.000 um^2
[INFO GPL-0046] TargetDensity:            0.625
[INFO GPL-0049] WhiteSpaceArea:       22512.842 um^2
[INFO GPL-0050] NesterovInstsArea:    11849.368 um^2
[INFO GPL-0051] TotalFillerArea:       2222.717 um^2
[INFO GPL-0052] TotalGCellsArea:      14072.084 um^2
[INFO GPL-0053] ExpectedGCellsArea:   14072.084 um^2
[INFO GPL-0054] NewTargetDensity:         0.625
[INFO GPL-0055] NewWhiteSpaceArea:    22512.842 um^2
[INFO GPL-0056] MovableArea:          14072.084 um^2
[INFO GPL-0057] NewNesterovInstArea:  11849.368 um^2
[INFO GPL-0058] NewTotalFillerArea:    2222.717 um^2
[INFO GPL-0059] NewTotalGCellsArea:   14072.084 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter: 1540 overflow: 0.591 HPWL: 26342261
[NesterovSolve] Iter: 1550 overflow: 0.591 HPWL: 26093955
[NesterovSolve] Iter: 1560 overflow: 0.596 HPWL: 25967210
[NesterovSolve] Iter: 1570 overflow: 0.599 HPWL: 25962107
[NesterovSolve] Iter: 1580 overflow: 0.600 HPWL: 26004186
[NesterovSolve] Iter: 1590 overflow: 0.601 HPWL: 26032504
[NesterovSolve] Iter: 1600 overflow: 0.600 HPWL: 26031872
[NesterovSolve] Iter: 1610 overflow: 0.598 HPWL: 26025636
[NesterovSolve] Iter: 1620 overflow: 0.596 HPWL: 26021413
[NesterovSolve] Iter: 1630 overflow: 0.597 HPWL: 26007833
[NesterovSolve] Iter: 1640 overflow: 0.599 HPWL: 25999193
[NesterovSolve] Iter: 1650 overflow: 0.600 HPWL: 26011285
[NesterovSolve] Iter: 1660 overflow: 0.599 HPWL: 26024228
[NesterovSolve] Iter: 1670 overflow: 0.598 HPWL: 26027683
[NesterovSolve] Iter: 1680 overflow: 0.597 HPWL: 26027686
[NesterovSolve] Iter: 1690 overflow: 0.596 HPWL: 26027836
[NesterovSolve] Iter: 1700 overflow: 0.595 HPWL: 26026445
[NesterovSolve] Iter: 1710 overflow: 0.595 HPWL: 26029607
[NesterovSolve] Iter: 1720 overflow: 0.593 HPWL: 26040913
[NesterovSolve] Iter: 1730 overflow: 0.591 HPWL: 26060661
[NesterovSolve] Iter: 1740 overflow: 0.587 HPWL: 26082890
[NesterovSolve] Iter: 1750 overflow: 0.583 HPWL: 26108772
[NesterovSolve] Iter: 1760 overflow: 0.575 HPWL: 26132705
[NesterovSolve] Iter: 1770 overflow: 0.564 HPWL: 26105345
[NesterovSolve] Iter: 1780 overflow: 0.552 HPWL: 26080844
[NesterovSolve] Iter: 1790 overflow: 0.537 HPWL: 26056756
[NesterovSolve] Iter: 1800 overflow: 0.519 HPWL: 26022588
[NesterovSolve] Iter: 1810 overflow: 0.492 HPWL: 25901146
[NesterovSolve] Iter: 1820 overflow: 0.462 HPWL: 25696165
[NesterovSolve] Iter: 1830 overflow: 0.430 HPWL: 25412366
[NesterovSolve] Iter: 1840 overflow: 0.410 HPWL: 25145815
[NesterovSolve] Iter: 1850 overflow: 0.377 HPWL: 25021959
[NesterovSolve] Iter: 1860 overflow: 0.351 HPWL: 24941952
[NesterovSolve] Iter: 1870 overflow: 0.330 HPWL: 24926368
```

```
[NesterovSolve] Iter: 1870 overflow: 0.330 HPWL: 24926368
[NesterovSolve] Iter: 1880 overflow: 0.308 HPWL: 24809943
[NesterovSolve] Iter: 1890 overflow: 0.290 HPWL: 24845138
[NesterovSolve] Iter: 1900 overflow: 0.265 HPWL: 24799536
[NesterovSolve] Iter: 1910 overflow: 0.246 HPWL: 24866310
[NesterovSolve] Iter: 1920 overflow: 0.225 HPWL: 24919938
[NesterovSolve] Iter: 1930 overflow: 0.204 HPWL: 24983783
[INFO GPL-0075] Routability numCall: 5 inflationIterCnt: 0 bloatIterCnt: 1
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      23   25
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 575
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0.20000004768371582
[INFO GPL-0065] OverflowTileCnt2: 1
[INFO GPL-0066] 0.5%RC: 1.0333
[INFO GPL-0067] 1.0%RC: 1.0121
[INFO GPL-0068] 2.0%RC: 0.9922
[INFO GPL-0069] 5.0%RC: 0.9462
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0227
[INFO GPL-0079] MinRC (1) violation occurred, total count: 1.
[INFO GPL-0045] InflatedAreaDelta:       41.834 um^2
[INFO GPL-0046] TargetDensity:            0.625
[INFO GPL-0049] WhiteSpaceArea:       22512.842 um^2
[INFO GPL-0050] NesterovInstsArea:    11849.368 um^2
[INFO GPL-0051] TotalFillerArea:       2222.717 um^2
[INFO GPL-0052] TotalGCellsArea:      14072.084 um^2
[INFO GPL-0053] ExpectedGCellsArea:   14113.918 um^2
[INFO GPL-0054] NewTargetDensity:         0.627
[INFO GPL-0055] NewWhiteSpaceArea:    22512.842 um^2
[INFO GPL-0056] MovableArea:          14113.918 um^2
[INFO GPL-0057] NewNesterovInstArea:  11891.201 um^2
[INFO GPL-0058] NewTotalFillerArea:    2222.717 um^2
[INFO GPL-0059] NewTotalGCellsArea:   14113.918 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter: 1940 overflow: 0.589 HPWL: 26207999
[NesterovSolve] Iter: 1950 overflow: 0.595 HPWL: 26018583
[NesterovSolve] Iter: 1960 overflow: 0.598 HPWL: 25960502
[NesterovSolve] Iter: 1970 overflow: 0.600 HPWL: 25990379
[NesterovSolve] Iter: 1980 overflow: 0.602 HPWL: 26029678
[NesterovSolve] Iter: 1990 overflow: 0.602 HPWL: 26041080
[NesterovSolve] Iter: 2000 overflow: 0.600 HPWL: 26032967
[NesterovSolve] Iter: 2010 overflow: 0.598 HPWL: 26030649
[NesterovSolve] Iter: 2020 overflow: 0.597 HPWL: 26022002
[NesterovSolve] Iter: 2030 overflow: 0.599 HPWL: 26007697
[NesterovSolve] Iter: 2040 overflow: 0.601 HPWL: 26009758
[NesterovSolve] Iter: 2050 overflow: 0.600 HPWL: 26025315
[NesterovSolve] Iter: 2060 overflow: 0.599 HPWL: 26033518
[NesterovSolve] Iter: 2070 overflow: 0.598 HPWL: 26034455
[NesterovSolve] Iter: 2080 overflow: 0.597 HPWL: 26034703
[NesterovSolve] Iter: 2090 overflow: 0.596 HPWL: 26034851
[NesterovSolve] Iter: 2100 overflow: 0.596 HPWL: 26035225
[NesterovSolve] Iter: 2110 overflow: 0.595 HPWL: 26042671
[NesterovSolve] Iter: 2120 overflow: 0.593 HPWL: 26060972
[NesterovSolve] Iter: 2130 overflow: 0.589 HPWL: 26086365
[NesterovSolve] Iter: 2140 overflow: 0.586 HPWL: 26113235
[NesterovSolve] Iter: 2150 overflow: 0.581 HPWL: 26144557
[NesterovSolve] Iter: 2160 overflow: 0.569 HPWL: 26138701
[NesterovSolve] Iter: 2170 overflow: 0.559 HPWL: 26110919
[NesterovSolve] Iter: 2180 overflow: 0.546 HPWL: 26094146
[NesterovSolve] Iter: 2190 overflow: 0.530 HPWL: 26065303
[NesterovSolve] Iter: 2200 overflow: 0.506 HPWL: 26009162
[NesterovSolve] Iter: 2210 overflow: 0.477 HPWL: 25832152
[NesterovSolve] Iter: 2220 overflow: 0.447 HPWL: 25594924
[NesterovSolve] Iter: 2230 overflow: 0.418 HPWL: 25263791
[NesterovSolve] Iter: 2240 overflow: 0.393 HPWL: 25143443
[NesterovSolve] Iter: 2250 overflow: 0.363 HPWL: 24988325
[NesterovSolve] Iter: 2260 overflow: 0.346 HPWL: 24975257
[NesterovSolve] Iter: 2270 overflow: 0.322 HPWL: 24890242
[NesterovSolve] Iter: 2280 overflow: 0.303 HPWL: 24794232
[NesterovSolve] Iter: 2290 overflow: 0.274 HPWL: 24810436
[NesterovSolve] Iter: 2300 overflow: 0.256 HPWL: 24844616
[NesterovSolve] Iter: 2310 overflow: 0.233 HPWL: 24909740
[NesterovSolve] Iter: 2320 overflow: 0.215 HPWL: 24976838
[INFO GPL-0075] Routability numCall: 6 inflationIterCnt: 1 bloatIterCnt: 1
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      23   25
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 575
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0.06666672229766846
[INFO GPL-0065] OverflowTileCnt2: 1
[INFO GPL-0066] 0.5%RC: 1.0111
[INFO GPL-0067] 1.0%RC: 1.0000
[INFO GPL-0068] 2.0%RC: 0.9844
[INFO GPL-0069] 5.0%RC: 0.9361
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0056
[INFO GPL-0079] MinRC (1) violation occurred, total count: 2.
[INFO GPL-0045] InflatedAreaDelta:       16.774 um^2
[INFO GPL-0046] TargetDensity:            0.627
[INFO GPL-0049] WhiteSpaceArea:       22512.842 um^2
[INFO GPL-0050] NesterovInstsArea:    11891.201 um^2
[INFO GPL-0051] TotalFillerArea:       2222.717 um^2
[INFO GPL-0052] TotalGCellsArea:      14113.918 um^2
[INFO GPL-0053] ExpectedGCellsArea:   14130.692 um^2
[INFO GPL-0054] NewTargetDensity:         0.628
[INFO GPL-0055] NewWhiteSpaceArea:    22512.842 um^2
[INFO GPL-0056] MovableArea:          14130.692 um^2
[INFO GPL-0057] NewNesterovInstArea:  11907.975 um^2
[INFO GPL-0058] NewTotalFillerArea:    2222.717 um^2
[INFO GPL-0059] NewTotalGCellsArea:   14130.692 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter: 2330 overflow: 0.592 HPWL: 26343384
[NesterovSolve] Iter: 2340 overflow: 0.592 HPWL: 26100013
[NesterovSolve] Iter: 2350 overflow: 0.597 HPWL: 25974388
[NesterovSolve] Iter: 2360 overflow: 0.599 HPWL: 25969750
[NesterovSolve] Iter: 2370 overflow: 0.601 HPWL: 26012414
[NesterovSolve] Iter: 2380 overflow: 0.602 HPWL: 26039834
[NesterovSolve] Iter: 2390 overflow: 0.601 HPWL: 26037824
[NesterovSolve] Iter: 2400 overflow: 0.599 HPWL: 26031957
[NesterovSolve] Iter: 2410 overflow: 0.597 HPWL: 26028589
[NesterovSolve] Iter: 2420 overflow: 0.598 HPWL: 26014951
[NesterovSolve] Iter: 2430 overflow: 0.600 HPWL: 26006463
[NesterovSolve] Iter: 2440 overflow: 0.601 HPWL: 26018412
[NesterovSolve] Iter: 2450 overflow: 0.600 HPWL: 26031085
[NesterovSolve] Iter: 2460 overflow: 0.599 HPWL: 26034826
[NesterovSolve] Iter: 2470 overflow: 0.598 HPWL: 26034740
[NesterovSolve] Iter: 2480 overflow: 0.597 HPWL: 26034878
[NesterovSolve] Iter: 2490 overflow: 0.596 HPWL: 26033949
[NesterovSolve] Iter: 2500 overflow: 0.595 HPWL: 26037438
```

```
[NesterovSolve] Iter: 2510 overflow: 0.594 HPWL: 26049267
[NesterovSolve] Iter: 2520 overflow: 0.591 HPWL: 26069822
[NesterovSolve] Iter: 2530 overflow: 0.588 HPWL: 26092587
[NesterovSolve] Iter: 2540 overflow: 0.584 HPWL: 26119466
[NesterovSolve] Iter: 2550 overflow: 0.575 HPWL: 26142386
[NesterovSolve] Iter: 2560 overflow: 0.564 HPWL: 26115534
[NesterovSolve] Iter: 2570 overflow: 0.552 HPWL: 26090775
[NesterovSolve] Iter: 2580 overflow: 0.537 HPWL: 26065303
[NesterovSolve] Iter: 2590 overflow: 0.520 HPWL: 26028808
[NesterovSolve] Iter: 2600 overflow: 0.491 HPWL: 25904376
[NesterovSolve] Iter: 2610 overflow: 0.462 HPWL: 25692546
[NesterovSolve] Iter: 2620 overflow: 0.430 HPWL: 25405227
[NesterovSolve] Iter: 2630 overflow: 0.410 HPWL: 25163943
[NesterovSolve] Iter: 2640 overflow: 0.376 HPWL: 25025602
[NesterovSolve] Iter: 2650 overflow: 0.352 HPWL: 24935837
[NesterovSolve] Iter: 2660 overflow: 0.333 HPWL: 24958086
[NesterovSolve] Iter: 2670 overflow: 0.309 HPWL: 24864808
[NesterovSolve] Iter: 2680 overflow: 0.289 HPWL: 24841503
[NesterovSolve] Iter: 2690 overflow: 0.264 HPWL: 24831306
[NesterovSolve] Iter: 2700 overflow: 0.248 HPWL: 24872134
[NesterovSolve] Iter: 2710 overflow: 0.225 HPWL: 24931686
[NesterovSolve] Iter: 2720 overflow: 0.203 HPWL: 25000851
[INFO GPL-0075] Routability numCall: 7 inflationIterCnt: 2 bloatIterCnt: 1
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:      23   25
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 575
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0.13333332538604736
[INFO GPL-0065] OverflowTileCnt2: 1
[INFO GPL-0066] 0.5%RC: 1.0222
[INFO GPL-0067] 1.0%RC: 1.0121
[INFO GPL-0068] 2.0%RC: 0.9812
[INFO GPL-0069] 5.0%RC: 0.9316
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0172
[INFO GPL-0079] MinRC (1) violation occurred, total count: 3.
[INFO GPL-0045] InflatedAreaDelta:       41.323 um^2
[INFO GPL-0046] TargetDensity:            0.628
Revert Routability Procedure. Target density higher than max, or minRC max violations.
[INFO GPL-0080] minRcViolatedCnt: 3
[INFO GPL-0047] SavedMinRC: 1.0000
[INFO GPL-0048] SavedTargetDensity: 0.6251
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter: 2730 overflow: 0.587 HPWL: 26167915
[NesterovSolve] Iter: 2740 overflow: 0.593 HPWL: 25977761
[NesterovSolve] Iter: 2750 overflow: 0.595 HPWL: 25927829
[NesterovSolve] Iter: 2760 overflow: 0.596 HPWL: 25959015
[NesterovSolve] Iter: 2770 overflow: 0.599 HPWL: 25996149
[NesterovSolve] Iter: 2780 overflow: 0.599 HPWL: 26009668
[NesterovSolve] Iter: 2790 overflow: 0.597 HPWL: 26006389
[NesterovSolve] Iter: 2800 overflow: 0.594 HPWL: 26001698
[NesterovSolve] Iter: 2810 overflow: 0.594 HPWL: 25990725
[NesterovSolve] Iter: 2820 overflow: 0.596 HPWL: 25976047
[NesterovSolve] Iter: 2830 overflow: 0.597 HPWL: 25977903
[NesterovSolve] Iter: 2840 overflow: 0.597 HPWL: 25994389
[NesterovSolve] Iter: 2850 overflow: 0.596 HPWL: 26002671
[NesterovSolve] Iter: 2860 overflow: 0.595 HPWL: 26003657
[NesterovSolve] Iter: 2870 overflow: 0.594 HPWL: 26004468
[NesterovSolve] Iter: 2880 overflow: 0.593 HPWL: 26002838
[NesterovSolve] Iter: 2890 overflow: 0.593 HPWL: 26001887
[NesterovSolve] Iter: 2900 overflow: 0.591 HPWL: 26007237
[NesterovSolve] Iter: 2910 overflow: 0.589 HPWL: 26021137
[NesterovSolve] Iter: 2920 overflow: 0.586 HPWL: 26043915
[NesterovSolve] Iter: 2930 overflow: 0.582 HPWL: 26067104
[NesterovSolve] Iter: 2940 overflow: 0.577 HPWL: 26093888
[NesterovSolve] Iter: 2950 overflow: 0.566 HPWL: 26078181
[NesterovSolve] Iter: 2960 overflow: 0.556 HPWL: 26050086
[NesterovSolve] Iter: 2970 overflow: 0.541 HPWL: 26036596
[NesterovSolve] Iter: 2980 overflow: 0.526 HPWL: 26012018
[NesterovSolve] Iter: 2990 overflow: 0.501 HPWL: 25931287
```

```
display(gpl)
```

```
────────────────────────────────────────── Render Image (w/ KLayout) ──────────────────────────────────────────
[15:36:00] VERBOSE  Running 'KLayout.Render'…                                                          step.py:1088
[15:36:00] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_609iq6zk/klayout-render.log…     step.py:1268
```

Time Elapsed: 14.31s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Detailed Placement

This aligns the fuzzy placement from before with the grid, "legalizing" it.

```
DetailedPlacement = Step.factory.get("OpenROAD.DetailedPlacement")

dpl = DetailedPlacement(state_in=gpl.state_out)
dpl.start()
```

```
────────────────────────────────────────────────────────── Detailed Placement ──────────────────────────────────────────────────────────
[15:36:02] VERBOSE  Running 'OpenROAD.DetailedPlacement'…                                                                    step.py:1088
[15:36:02] VERBOSE  Logging subprocess to                                                                                     step.py:1268
                    openlane_run/58-openroad-detailedplacement/openroad-detailedplacement.log…
Reading OpenROAD database at '/content/openlane_run/57-openroad-globalplacement/MISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[15:36:03] WARNING  [STA-0366] port 'clk' not found.                                                                        openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[15:36:03] WARNING  [STA-0366] port 'clk' not found.                                                                        openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[15:36:03] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                      openroad.py:235
[INFO] Setting timing derate to: 5%
[15:36:03] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                     openroad.py:235
Placement Analysis
---------------------------------
total displacement       2803.9 u
average displacement        1.7 u
max displacement            8.8 u
original HPWL           25412.7 u
legalized HPWL          28426.9 u
delta HPWL                   12 %

[INFO DPL-0020] Mirrored 478 instances
[INFO DPL-0021] HPWL before           28426.9 u
[INFO DPL-0022] HPWL after            27510.3 u
[INFO DPL-0023] HPWL delta               -3.2 %
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/58-openroad-detailedplacement/MISO.odb'…
Writing netlist to '/content/openlane_run/58-openroad-detailedplacement/MISO.nl.v'…
Writing powered netlist to '/content/openlane_run/58-openroad-detailedplacement/MISO.pnl.v'…
Writing layout to '/content/openlane_run/58-openroad-detailedplacement/MISO.def'…
Writing timing constraints to '/content/openlane_run/58-openroad-detailedplacement/MISO.sdc'…
```

Format	Path
nl	openlane_run/58-openroad-detailedplacement/MISO.nl.v
pnl	openlane_run/58-openroad-detailedplacement/MISO.pnl.v
def	openlane_run/58-openroad-detailedplacement/MISO.def
odb	openlane_run/58-openroad-detailedplacement/MISO.odb

```
display(dpl)
```

```
────────────────────────────────────────────────────────── Render Image (w/ KLayout) ──────────────────────────────────────────────────────────
[15:36:04] VERBOSE  Running 'KLayout.Render'…                                                                                 step.py:1088
[15:36:04] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_xiwjmvxr/klayout-render.log…                           step.py:1268
```

Time Elapsed: 1.43s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Clock Tree Synthesis (CTS)

With the cells now having a final placement, we can go ahead and create what is known as the clock tree, i.e., the hierarchical set of buffers used for clock signal to minimize what is known as "clock skew"- variable delay of the clock cycle from register to register because of factors such as metal wire length, clock load (number of gates connected to the same clock buffer,) et cetera.

The CTS step creates the cells and places the between the gaps in the detailed placement above.

```
CTS = Step.factory.get("OpenROAD.CTS")

cts = CTS(state_in=dpl.state_out)
cts.start()
```

```
─────────────────────────────────────────── Clock Tree Synthesis ───────────────────────────────────────────
[15:36:05] VERBOSE  Running 'OpenROAD.CTS'…                                                    step.py:1088
[15:36:05] VERBOSE  Logging subprocess to openlane_run/59-openroad-cts/openroad-cts.log…        step.py:1268
Reading timing models for corner nom_tt_025C_1v80…
Reading timing library for the 'nom_tt_025C_1v80' corner at
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading timing models for corner nom_ff_n40C_1v95…
Reading timing library for the 'nom_ff_n40C_1v95' corner at
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ff_n40C_1v95.lib'…
Reading timing models for corner nom_ss_100C_1v60…
Reading timing library for the 'nom_ss_100C_1v60' corner at
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ss_100C_1v60.lib'…
Reading OpenROAD database at '/content/openlane_run/58-openroad-detailedplacement/MISO.odb'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[15:36:09] WARNING  [STA-0366] port 'clk' not found.                                            openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[15:36:09] WARNING  [STA-0366] port 'clk' not found.                                            openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[15:36:09] WARNING  [STA-0419] transition time can not be specified for virtual clocks.          openroad.py:235
[INFO] Setting timing derate to: 5%
[15:36:09] WARNING  [STA-0450] virtual clock clk can not be propagated.                         openroad.py:235
[INFO] Setting RC values…
[INFO] Configuring cts characterization…
[INFO] Performing clock tree synthesis…
[INFO] Looking for the following net(s): clk
[INFO] Running Clock Tree Synthesis…
[INFO CTS-0050] Root buffer is sky130_fd_sc_hd__clkbuf_16.
[INFO CTS-0051] Sink buffer is sky130_fd_sc_hd__clkbuf_8.
[INFO CTS-0052] The following clock buffers will be used for CTS:
sky130_fd_sc_hd__clkbuf_2
sky130_fd_sc_hd__clkbuf_4
sky130_fd_sc_hd__clkbuf_8
[INFO CTS-0049] Characterization buffer is sky130_fd_sc_hd__clkbuf_8.
[15:36:17] WARNING  [CTS-0083] No clock nets have been found.                                   openroad.py:235
[INFO CTS-0008] TritonCTS found 0 clock nets.
[15:36:17] WARNING  [CTS-0082] No valid clock nets in the design.                               openroad.py:235
[15:36:17] WARNING  [STA-0450] virtual clock clk can not be propagated.                         openroad.py:235
[INFO] Repairing long wires on clock nets…
[INFO RSZ-0058] Using max wire length 6335um.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/59-openroad-cts/MISO.odb'…
Writing netlist to '/content/openlane_run/59-openroad-cts/MISO.nl.v'…
Writing powered netlist to '/content/openlane_run/59-openroad-cts/MISO.pnl.v'…
Writing layout to '/content/openlane_run/59-openroad-cts/MISO.def'…
Writing timing constraints to '/content/openlane_run/59-openroad-cts/MISO.sdc'…
[INFO] Legalizing…
Placement Analysis
---------------------------------
total displacement          0.0 u
average displacement        0.0 u
max displacement            0.0 u
original HPWL           27510.3 u
legalized HPWL          28426.9 u
delta HPWL                    3 %

[INFO DPL-0020] Mirrored 478 instances
[INFO DPL-0021] HPWL before           28426.9 u
[INFO DPL-0022] HPWL after            27510.3 u
[INFO DPL-0023] HPWL delta               -3.2 %
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/59-openroad-cts/MISO.odb'…
Writing netlist to '/content/openlane_run/59-openroad-cts/MISO.nl.v'…
Writing powered netlist to '/content/openlane_run/59-openroad-cts/MISO.pnl.v'…
Writing layout to '/content/openlane_run/59-openroad-cts/MISO.def'…
Writing timing constraints to '/content/openlane_run/59-openroad-cts/MISO.sdc'…
```

Format	Path
nl	openlane_run/59-openroad-cts/MISO.nl.v
pnl	openlane_run/59-openroad-cts/MISO.pnl.v

```
display(cts)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[15:36:19] VERBOSE  Running 'KLayout.Render'…                                                  step.py:1088
[15:36:19] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_0a9oir04/klayout-render.log…  step.py:1268
```

Time Elapsed: 13.45s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Global Routing

Global routing "plans" the routes the wires between two gates (or gates and I/O pins/the PDN) will take. The results of global routing (which are called "routing guides") are stored in internal data structures and have no effect on the actual design, so there is no `display()` statement.

```
GlobalRouting = Step.factory.get("OpenROAD.GlobalRouting")

grt = GlobalRouting(state_in=cts.state_out)
grt.start()
```

```
──────────────────────────────────────────────────────── Global Routing ────────────────────────────────────────────────────────
[15:36:20] VERBOSE  Running 'OpenROAD.GlobalRouting'…                                                          step.py:1088
[15:36:20] VERBOSE  Logging subprocess to                                                                      step.py:1268
                    openlane_run/60-openroad-globalrouting/openroad-globalrouting.log…
Reading OpenROAD database at '/content/openlane_run/59-openroad-cts/MISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[15:36:20] WARNING  [STA-0366] port 'clk' not found.                                                        openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[15:36:20] WARNING  [STA-0366] port 'clk' not found.                                                        openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.1499999999999999944488848768742172978818416595458984375
[15:36:20] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                      openroad.py:235
[INFO] Setting timing derate to: 5%
[15:36:20] WARNING  [STA-0450] virtual clock clk can not be propagated.                                     openroad.py:235
[15:36:20] WARNING  [STA-0450] virtual clock clk can not be propagated.                                     openroad.py:235
[INFO] Setting signal min routing layer to: met1 and clock min routing layer to met1.
[INFO] Setting signal max routing layer to: met5 and clock max routing layer to met5.
-congestion_iterations 50 -verbose
[INFO GRT-0020] Min routing layer: met1
[INFO GRT-0021] Max routing layer: met5
[INFO GRT-0022] Global adjustment: 30%
[INFO GRT-0023] Grid origin: (0, 0)
[INFO GRT-0043] No OR_DEFAULT vias defined.
[INFO GRT-0088] Layer li1     Track-Pitch = 0.4600  line-2-Via Pitch: 0.3400
[INFO GRT-0088] Layer met1    Track-Pitch = 0.3400  line-2-Via Pitch: 0.3400
[INFO GRT-0088] Layer met2    Track-Pitch = 0.4600  line-2-Via Pitch: 0.3500
[INFO GRT-0088] Layer met3    Track-Pitch = 0.6800  line-2-Via Pitch: 0.6150
[INFO GRT-0088] Layer met4    Track-Pitch = 0.9200  line-2-Via Pitch: 1.0400
[INFO GRT-0088] Layer met5    Track-Pitch = 3.4000  line-2-Via Pitch: 3.1100
[INFO GRT-0019] Found 0 clock nets.
[INFO GRT-0001] Minimum degree: 2
[INFO GRT-0002] Maximum degree: 12
[INFO GRT-0003] Macros: 0
[INFO GRT-0043] No OR_DEFAULT vias defined.
[INFO GRT-0004] Blockages: 1365

[INFO GRT-0053] Routing resources analysis:
Routing      Original      Derated      Resource
Layer     Direction    Resources     Resources    Reduction (%)
-------------------------------------------------------------
li1        Vertical            0             0          0.00%
met1       Horizontal      11644          5723          50.85%
met2       Vertical         8955          5581          37.68%
met3       Horizontal       5822          3635          37.56%
met4       Vertical         3637          1822          49.90%
met5       Horizontal       1146           462          59.69%
-------------------------------------------------------------

[INFO GRT-0101] Running extra iterations to remove overflow.
[INFO GRT-0197] Via related to pin nodes: 6277
[INFO GRT-0198] Via related Steiner nodes: 33
[INFO GRT-0199] Via filling finished.
[INFO GRT-0111] Final number of vias: 7719
[INFO GRT-0112] Final usage 3D: 27041

[INFO GRT-0096] Final congestion report:
Layer         Resource        Demand        Usage (%)    Max H / Max V / Total Overflow
---------------------------------------------------------------------------------------
li1                  0             0            0.00%             0 /  0 /  0
met1              5723          1693           29.58%             0 /  0 /  0
met2              5581          1925           34.49%             0 /  0 /  0
met3              3635           235            6.46%             0 /  0 /  0
met4              1822            31            1.70%             0 /  0 /  0
met5               462             0            0.00%             0 /  0 /  0
---------------------------------------------------------------------------------------
Total            17223          3884           22.55%             0 /  0 /  0

[INFO GRT-0018] Total wirelength: 45781 um
[INFO GRT-0014] Routed nets: 1305
[INFO] Setting RC values…
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/60-openroad-globalrouting/MISO.odb'…
Writing layout to '/content/openlane_run/60-openroad-globalrouting/MISO.def'…
```

Format	Path
nl	openlane_run/59-openroad-cts/MISO.nl.v
pnl	openlane_run/59-openroad-cts/MISO.pnl.v

Detailed Routing

Detailed routing uses the guides from Global Routing to actually create wires on the metal layers and connect the gates, making the connections finally physical.

This is typically the longest step in the flow.

```
DetailedRouting = Step.factory.get("OpenROAD.DetailedRouting")

drt = DetailedRouting(state_in=grt.state_out)
drt.start()
```

```
Detailed Routing
[15:36:21] VERBOSE  Running 'OpenROAD.DetailedRouting'…                                   step.py:1088
[15:36:21] INFO     Running TritonRoute with 2 threads…                                  openroad.py:1619
[15:36:21] VERBOSE  Logging subprocess to                                                 step.py:1268
                    openlane_run/61-openroad-detailedrouting/openroad-detailedrouting.log…
Reading OpenROAD database at '/content/openlane_run/60-openroad-globalrouting/MISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[15:36:22] WARNING  [STA-0366] port 'clk' not found.                                      openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[15:36:22] WARNING  [STA-0366] port 'clk' not found.                                      openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[15:36:22] WARNING  [STA-0419] transition time can not be specified for virtual clocks.    openroad.py:235
[INFO] Setting timing derate to: 5%
[15:36:22] WARNING  [STA-0450] virtual clock clk can not be propagated.                   openroad.py:235
[INFO ORD-0030] Using 2 thread(s).
[INFO DRT-0149] Reading tech and libs.
[15:36:22] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer mcon
[15:36:22] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer mcon
[15:36:22] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via
[15:36:22] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via
[15:36:22] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via2
[15:36:22] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via2
[15:36:22] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via3
[15:36:22] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via3
[15:36:22] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via4
[15:36:22] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via4

Units:                1000
Number of layers:     13
Number of macros:     441
Number of vias:       29
Number of viarulegen: 25

[INFO DRT-0150] Reading design.

Design:                   MISO
Die area:                 ( 0 0 ) ( 164515 175235 )
Number of track patterns: 12
Number of DEF vias:       0
Number of components:     1640
Number of terminals:      162
Number of snets:          2
Number of nets:           1305

[INFO DRT-0167] List of default vias:
Layer via
default via: M1M2_PR
Layer via2
default via: M2M3_PR
Layer via3
default via: M3M4_PR
Layer via4
default via: M4M5_PR
[INFO DRT-0162] Library cell analysis.
[INFO DRT-0163] Instance analysis.
[INFO DRT-0164] Number of unique instances = 172.
[INFO DRT-0168] Init region query.
[INFO DRT-0024]   Complete FR_MASTERSLICE.
[INFO DRT-0024]   Complete Fr_VIA.
[INFO DRT-0024]   Complete li1.
[INFO DRT-0024]   Complete mcon.
[INFO DRT-0024]   Complete met1.
[INFO DRT-0024]   Complete via.
[INFO DRT-0024]   Complete met2.
[INFO DRT-0024]   Complete via2.
[INFO DRT-0024]   Complete met3.
[INFO DRT-0024]   Complete via3.
[INFO DRT-0024]   Complete met4.
[INFO DRT-0024]   Complete via4.
[INFO DRT-0024]   Complete met5.
[INFO DRT-0033] FR_MASTERSLICE shape region query size = 0.
[INFO DRT-0033] FR_VIA shape region query size = 0.
[INFO DRT-0033] li1 shape region query size = 36154.
[INFO DRT-0033] mcon shape region query size = 0.
[INFO DRT-0033] met1 shape region query size = 4901.
[INFO DRT-0033] via shape region query size = 1710.
[INFO DRT-0033] met2 shape region query size = 626.
[INFO DRT-0033] via2 shape region query size = 1425.
[INFO DRT-0033] met3 shape region query size = 959.
[INFO DRT-0033] via3 shape region query size = 1425.
[INFO DRT-0033] met4 shape region query size = 355.
[INFO DRT-0033] via4 shape region query size = 50.
[INFO DRT-0033] met5 shape region query size = 70.
[INFO DRT-0165] Start pin access.
[INFO DRT-0078]   Complete 700 pins.
[INFO DRT-0079]   Complete 100 unique inst patterns.
[INFO DRT-0081]   Complete 166 unique inst patterns.
[INFO DRT-0084]   Complete 785 groups.
#scanned instances     = 1640
#unique  instances     = 172
#stdCellGenAp          = 4692
#stdCellValidPlanarAp  = 28
#stdCellValidViaAp     = 3777
#stdCellPinNoAp        = 0
#stdCellPinCnt         = 4102
#instTermValidViaApCnt = 0
#macroGenAp            = 0
#macroValidPlanarAp    = 0
#macroValidViaAp       = 0
#macroNoAp             = 0
[INFO DRT-0166] Complete pin access.
[INFO DRT-0267] cpu time = 00:00:42, elapsed time = 00:00:25, memory = 122.78 (MB), peak = 291.43 (MB)

Number of guides:     8049

[INFO DRT-0169] Post process guides.
[INFO DRT-0176] GCELLGRID X 0 DO 23 STEP 6900 ;
[INFO DRT-0177] GCELLGRID Y 0 DO 25 STEP 6900 ;
[INFO DRT-0028]   Complete FR_MASTERSLICE.
[INFO DRT-0028]   Complete Fr_VIA.
[INFO DRT-0028]   Complete li1.
[INFO DRT-0028]   Complete mcon.
```

```
[INFO DRT-0028]   Complete met1.
[INFO DRT-0028]   Complete via.
[INFO DRT-0028]   Complete met2.
[INFO DRT-0028]   Complete via2.
[INFO DRT-0028]   Complete met3.
[INFO DRT-0028]   Complete via3.
[INFO DRT-0028]   Complete met4.
[INFO DRT-0028]   Complete via4.
[INFO DRT-0028]   Complete met5.
[INFO DRT-0178] Init guide query.
[INFO DRT-0035]   Complete FR_MASTERSLICE (guide).
[INFO DRT-0035]   Complete Fr_VIA (guide).
[INFO DRT-0035]   Complete li1 (guide).
[INFO DRT-0035]   Complete mcon (guide).
[INFO DRT-0035]   Complete met1 (guide).
[INFO DRT-0035]   Complete via (guide).
[INFO DRT-0035]   Complete met2 (guide).
[INFO DRT-0035]   Complete via2 (guide).
[INFO DRT-0035]   Complete met3 (guide).
[INFO DRT-0035]   Complete via3 (guide).
[INFO DRT-0035]   Complete met4 (guide).
[INFO DRT-0035]   Complete via4 (guide).
[INFO DRT-0035]   Complete met5 (guide).
[INFO DRT-0036] FR_MASTERSLICE guide region query size = 0.
[INFO DRT-0036] FR_VIA guide region query size = 0.
[INFO DRT-0036] li1 guide region query size = 2830.
[INFO DRT-0036] mcon guide region query size = 0.
[INFO DRT-0036] met1 guide region query size = 2123.
[INFO DRT-0036] via guide region query size = 0.
[INFO DRT-0036] met2 guide region query size = 1134.
[INFO DRT-0036] via2 guide region query size = 0.
[INFO DRT-0036] met3 guide region query size = 110.
[INFO DRT-0036] via3 guide region query size = 0.
[INFO DRT-0036] met4 guide region query size = 4.
[INFO DRT-0036] via4 guide region query size = 0.
[INFO DRT-0036] met5 guide region query size = 0.
[INFO DRT-0179] Init gr pin query.
[INFO DRT-0245] skipped writing guide updates to database.
[INFO DRT-0185] Post process initialize RPin region query.
[INFO DRT-0181] Start track assignment.
[INFO DRT-0184] Done with 3968 vertical wires in 1 frboxes and 2233 horizontal wires in 1 frboxes.
[INFO DRT-0186] Done with 390 vertical wires in 1 frboxes and 541 horizontal wires in 1 frboxes.
[INFO DRT-0182] Complete track assignment.
[INFO DRT-0267] cpu time = 00:00:01, elapsed time = 00:00:00, memory = 135.05 (MB), peak = 291.43 (MB)
[INFO DRT-0187] Start routing data preparation.
[INFO DRT-0267] cpu time = 00:00:00, elapsed time = 00:00:00, memory = 135.05 (MB), peak = 291.43 (MB)
[INFO DRT-0194] Start detail routing.
[INFO DRT-0195] Start 0th optimization iteration.
Completing 10% with 0 violations.
elapsed time = 00:00:01, memory = 161.36 (MB).
Completing 20% with 0 violations.
elapsed time = 00:00:03, memory = 163.96 (MB).
Completing 30% with 49 violations.
elapsed time = 00:00:06, memory = 179.13 (MB).
Completing 40% with 49 violations.
elapsed time = 00:00:06, memory = 181.45 (MB).
Completing 50% with 49 violations.
elapsed time = 00:00:07, memory = 167.40 (MB).
Completing 60% with 125 violations.
elapsed time = 00:00:08, memory = 176.68 (MB).
Completing 70% with 125 violations.
elapsed time = 00:00:11, memory = 188.28 (MB).
Completing 80% with 203 violations.
elapsed time = 00:00:12, memory = 203.75 (MB).
Completing 90% with 203 violations.
elapsed time = 00:00:12, memory = 203.75 (MB).
Completing 100% with 283 violations.
elapsed time = 00:00:14, memory = 188.39 (MB).
[INFO DRT-0199]   Number of violations = 372.
Viol/Layer          li1   mcon   met1    via   met2   met3
Cut Spacing           0      1      0      0      0      0
Metal Spacing        27      0     82      0     11     10
Recheck               0      0     46      0     40      3
Short                 0      0    131      1     20      0
[INFO DRT-0267] cpu time = 00:00:22, elapsed time = 00:00:14, memory = 528.25 (MB), peak = 528.25 (MB)
Total wire length = 29020 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 12327 um.
Total wire length on LAYER met2 = 13793 um.
Total wire length on LAYER met3 = 2690 um.
Total wire length on LAYER met4 = 209 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 8057.
Up-via summary (total 8057):

-----------------------
FR_MASTERSLICE       0
li1    4017
met1    3921
met2     111
met3       8
met4       0
-----------------------
8057


[INFO DRT-0195] Start 1st optimization iteration.
Completing 10% with 372 violations.
elapsed time = 00:00:01, memory = 528.25 (MB).
Completing 20% with 372 violations.
elapsed time = 00:00:04, memory = 528.25 (MB).
Completing 30% with 332 violations.
elapsed time = 00:00:05, memory = 543.77 (MB).
Completing 40% with 332 violations.
elapsed time = 00:00:06, memory = 543.77 (MB).
Completing 50% with 332 violations.
elapsed time = 00:00:07, memory = 528.38 (MB).
Completing 60% with 271 violations.
elapsed time = 00:00:09, memory = 528.38 (MB).
Completing 70% with 271 violations.
elapsed time = 00:00:10, memory = 528.38 (MB).
Completing 80% with 174 violations.
elapsed time = 00:00:12, memory = 528.38 (MB).
Completing 90% with 174 violations.
elapsed time = 00:00:12, memory = 528.38 (MB).
Completing 100% with 73 violations.
elapsed time = 00:00:12, memory = 528.38 (MB).
[INFO DRT-0199]   Number of violations = 73.
Viol/Layer        met1   met2
Metal Spacing       17      5
Short               48      3
[INFO DRT-0267] cpu time = 00:00:19, elapsed time = 00:00:13, memory = 528.38 (MB), peak = 543.77 (MB)
Total wire length = 28810 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 12253 um.
Total wire length on LAYER met2 = 13708 um.
Total wire length on LAYER met3 = 2644 um.
Total wire length on LAYER met4 = 204 um.
```

```
Total wire length on LAYER met5 = 0 um.
Total number of vias = 7982.
Up-via summary (total 7982):

-----------------------
FR_MASTERSLICE       0
li1    4010
met1    3851
met2     113
met3       8
met4       0
-----------------------
7982


[INFO DRT-0195] Start 2nd optimization iteration.
Completing 10% with 73 violations.
elapsed time = 00:00:00, memory = 528.38 (MB).
Completing 20% with 73 violations.
elapsed time = 00:00:00, memory = 528.38 (MB).
Completing 30% with 73 violations.
elapsed time = 00:00:01, memory = 528.38 (MB).
Completing 40% with 73 violations.
elapsed time = 00:00:01, memory = 528.38 (MB).
Completing 50% with 73 violations.
elapsed time = 00:00:05, memory = 528.38 (MB).
Completing 60% with 77 violations.
elapsed time = 00:00:06, memory = 528.38 (MB).
Completing 70% with 77 violations.
elapsed time = 00:00:08, memory = 530.43 (MB).
Completing 80% with 77 violations.
elapsed time = 00:00:09, memory = 531.46 (MB).
Completing 90% with 76 violations.
elapsed time = 00:00:12, memory = 531.46 (MB).
Completing 100% with 82 violations.
elapsed time = 00:00:13, memory = 531.46 (MB).
[INFO DRT-0199]   Number of violations = 82.
Viol/Layer        met1   met2
Metal Spacing       19      5
Short               54      4
[INFO DRT-0267] cpu time = 00:00:20, elapsed time = 00:00:14, memory = 531.82 (MB), peak = 544.10 (MB)
Total wire length = 28762 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 12247 um.
Total wire length on LAYER met2 = 13662 um.
Total wire length on LAYER met3 = 2649 um.
Total wire length on LAYER met4 = 204 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 7974.
Up-via summary (total 7974):

-----------------------
FR_MASTERSLICE       0
li1    4010
met1    3839
met2     117
met3       8
met4       0
-----------------------
7974


[INFO DRT-0195] Start 3rd optimization iteration.
Completing 10% with 82 violations.
elapsed time = 00:00:01, memory = 531.82 (MB).
Completing 20% with 82 violations.
elapsed time = 00:00:02, memory = 535.95 (MB).
Completing 30% with 52 violations.
elapsed time = 00:00:03, memory = 535.95 (MB).
Completing 40% with 52 violations.
elapsed time = 00:00:03, memory = 535.95 (MB).
Completing 50% with 52 violations.
elapsed time = 00:00:03, memory = 535.95 (MB).
Completing 60% with 31 violations.
elapsed time = 00:00:04, memory = 535.95 (MB).
Completing 70% with 31 violations.
elapsed time = 00:00:06, memory = 535.95 (MB).
Completing 80% with 7 violations.
elapsed time = 00:00:06, memory = 535.95 (MB).
Completing 90% with 7 violations.
elapsed time = 00:00:06, memory = 535.95 (MB).
Completing 100% with 0 violations.
elapsed time = 00:00:07, memory = 535.95 (MB).
[INFO DRT-0199]   Number of violations = 0.
[INFO DRT-0267] cpu time = 00:00:11, elapsed time = 00:00:08, memory = 535.95 (MB), peak = 544.10 (MB)
Total wire length = 28752 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 12011 um.
Total wire length on LAYER met2 = 13680 um.
Total wire length on LAYER met3 = 2846 um.
Total wire length on LAYER met4 = 214 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 8051.
Up-via summary (total 8051):

-----------------------
FR_MASTERSLICE       0
li1    4010
met1    3880
met2     151
met3      10
met4       0
-----------------------
8051


[INFO DRT-0198] Complete detail routing.
Total wire length = 28752 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 12011 um.
Total wire length on LAYER met2 = 13680 um.
Total wire length on LAYER met3 = 2846 um.
Total wire length on LAYER met4 = 214 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 8051.
Up-via summary (total 8051):

-----------------------
FR_MASTERSLICE       0
li1    4010
met1    3880
met2     151
met3      10
```

Start coding or generate with AI.

Double-click (or enter) to edit

```
display(drt)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[15:37:40] VERBOSE  Running 'KLayout.Render'…                                                    step.py:1088
[15:37:40] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_i5ro_9_4/klayout-render.log…  step.py:1268
```

Time Elapsed: 78.62s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Fill Insertion

Finally, as we're done placing all the essential cells, the only thing left to do is fill in the gaps.

We prioritize the use of decap (decoupling capacitor) cells, which further supports the power distribution network, but when there aren't any small enough cells, we just use regular fill cells.

```
FillInsertion = Step.factory.get("OpenROAD.FillInsertion")

fill = FillInsertion(state_in=drt.state_out)
fill.start()
```

```
────────────────────────────────────────────────────────────── Fill Insertion ──────────────────────────────────────────────────────────────
[15:37:41] VERBOSE  Running 'OpenROAD.FillInsertion'…                                                                          step.py:1088
[15:37:41] VERBOSE  Logging subprocess to                                                                                      step.py:1268
                    openlane_run/62-openroad-fillinsertion/openroad-fillinsertion.log…
Reading OpenROAD database at '/content/openlane_run/61-openroad-detailedrouting/MISO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[15:37:42] WARNING  [STA-0366] port 'clk' not found.                                                                           openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[15:37:42] WARNING  [STA-0366] port 'clk' not found.                                                                           openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[15:37:42] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                         openroad.py:235
[INFO] Setting timing derate to: 5%
[15:37:42] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                        openroad.py:235
sky130_ef_sc_hd__decap_12 sky130_fd_sc_hd__decap_8 sky130_fd_sc_hd__decap_6 sky130_fd_sc_hd__decap_4
sky130_fd_sc_hd__decap_3 sky130_fd_sc_hd__fill*
[INFO DPL-0001] Placed 1552 filler instances.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/62-openroad-fillinsertion/MISO.odb'…
Writing netlist to '/content/openlane_run/62-openroad-fillinsertion/MISO.nl.v'…
Writing powered netlist to '/content/openlane_run/62-openroad-fillinsertion/MISO.pnl.v'…
Writing layout to '/content/openlane_run/62-openroad-fillinsertion/MISO.def'…
Writing timing constraints to '/content/openlane_run/62-openroad-fillinsertion/MISO.sdc'…
```

Format	Path
nl	openlane_run/62-openroad-fillinsertion/MISO.nl.v
pnl	openlane_run/62-openroad-fillinsertion/MISO.pnl.v
def	openlane_run/62-openroad-fillinsertion/MISO.def
odb	openlane_run/62-openroad-fillinsertion/MISO.odb

```
display(fill)
```

```
──────────────────────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────────────────────
[15:37:42] VERBOSE  Running 'KLayout.Render'…                                                                                  step.py:1088
[15:37:42] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_em6uu1ya/klayout-render.log…                            step.py:1268
```

Time Elapsed: 1.04s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Parasitics Extraction a.k.a. Resistance/Capacitance Extraction (RCX)

This step does not alter the design- rather, it computes the Parasitic elements of the circuit, which have an effect of timing, as we prepare to do the final timing analysis.

The parasitic elements are saved in the **Standard Parasitics Exchange Format**, or SPEF. OpenLane creates a SPEF file for each interconnect corner as described in the Corners and STA section of the documentation.

```
RCX = Step.factory.get("OpenROAD.RCX")

rcx = RCX(state_in=fill.state_out)
rcx.start()
```

```
─────────────────────────────── Parasitic Resistance/Capacitance Extraction ───────────────────────────────
[15:37:43] VERBOSE  Running 'OpenROAD.RCX'…                                                    step.py:1088
[15:37:43] INFO     Running RCX for corners matching nom_*                                  openroad.py:1748
                    (/content/openlane_run/63-openroad-rcx/nom/rcx.log)…
[15:37:43] VERBOSE  Logging subprocess to openlane_run/63-openroad-rcx/nom/rcx.log…            step.py:1268
[15:37:43] INFO     Running RCX for corners matching min_*                                  openroad.py:1748
                    (/content/openlane_run/63-openroad-rcx/min/rcx.log)…
[15:37:43] VERBOSE  Logging subprocess to openlane_run/63-openroad-rcx/min/rcx.log…            step.py:1268
[15:37:45] INFO     Finished RCX for corners matching min_*.                                openroad.py:1757
[15:37:45] INFO     Running RCX for corners matching max_*                                  openroad.py:1748
                    (/content/openlane_run/63-openroad-rcx/max/rcx.log)…
[15:37:45] VERBOSE  Logging subprocess to openlane_run/63-openroad-rcx/max/rcx.log…            step.py:1268
[15:37:45] INFO     Finished RCX for corners matching nom_*.                                openroad.py:1757
[15:37:46] INFO     Finished RCX for corners matching max_*.                                openroad.py:1757
```

Format	Path
nl	openlane_run/62-openroad-fillinsertion/MISO.nl.v
pnl	openlane_run/62-openroad-fillinsertion/MISO.pnl.v
def	openlane_run/62-openroad-fillinsertion/MISO.def
odb	openlane_run/62-openroad-fillinsertion/MISO.odb
sdc	openlane_run/62-openroad-fillinsertion/MISO.sdc
spef	nom_* openlane_run/63-openroad-rcx/nom/MISO.nom.spef min_* openlane_run/63-openroad-rcx/min/MISO.min.spef max_* openlane_run/63-openroad-rcx/max/MISO.max.spef

Static Timing Analysis (Post-PnR)

STA is a process that verifies that a chip meets certain constraints on clock and data timings to run at its rated clock speed. See Corners and STA in the documentation for more info.

This step generates two kinds of files:

- `.lib` : Liberty™-compatible Library files. Can be used to do static timing analysis when creating a design with this design as a sub-macro.
- `.sdf` : Standard Delay Format. Can be used with certain simulation software to do *dynamic* timing analysis.

Unfortunately, the `.lib` files coming out of OpenLane right now are not super reliable for timing purposes and are only provided for completeness. When using OpenLane-created macros withing other designs, it is best to use the macro's final netlist and extracted parasitics instead.

```
STAPostPNR = Step.factory.get("OpenROAD.STAPostPNR")

sta_post_pnr = STAPostPNR(state_in=rcx.state_out)
sta_post_pnr.start()
```

```
──────────────────────────────────────── Static Timing Analysis (Post-PnR) ────────────────────────────────────────
[15:37:46] VERBOSE  Running 'OpenROAD.STAPostPNR'…                                                   step.py:1088
[15:37:46] INFO     Starting STA for the nom_tt_025C_1v80 timing corner…                            openroad.py:561
[15:37:46] INFO     Starting STA for the nom_ss_100C_1v60 timing corner…                            openroad.py:561
[15:37:46] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/nom_tt_025C_1v80/sta.log…
[15:37:46] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/nom_ss_100C_1v60/sta.log…
[15:37:50] INFO     Finished STA for the nom_tt_025C_1v80 timing corner.                            openroad.py:576
[15:37:50] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/nom_tt_025C_1v80/filter_unannotated.log…
[15:37:50] INFO     Finished STA for the nom_ss_100C_1v60 timing corner.                            openroad.py:576
[15:37:50] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/nom_ss_100C_1v60/filter_unannotated.log…
[15:37:51] INFO     Starting STA for the nom_ff_n40C_1v95 timing corner…                            openroad.py:561
[15:37:51] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/nom_ff_n40C_1v95/sta.log…
[15:37:52] INFO     Starting STA for the min_tt_025C_1v80 timing corner…                            openroad.py:561
[15:37:52] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/min_tt_025C_1v80/sta.log…
[15:37:56] INFO     Finished STA for the min_tt_025C_1v80 timing corner.                            openroad.py:576
[15:37:56] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/min_tt_025C_1v80/filter_unannotated.log…
[15:37:56] INFO     Finished STA for the nom_ff_n40C_1v95 timing corner.                            openroad.py:576
[15:37:56] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/nom_ff_n40C_1v95/filter_unannotated.log…
[15:37:57] INFO     Starting STA for the min_ss_100C_1v60 timing corner…                            openroad.py:561
[15:37:57] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/min_ss_100C_1v60/sta.log…
[15:37:57] INFO     Starting STA for the min_ff_n40C_1v95 timing corner…                            openroad.py:561
[15:37:57] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/min_ff_n40C_1v95/sta.log…
[15:38:01] INFO     Finished STA for the min_ss_100C_1v60 timing corner.                            openroad.py:576
[15:38:01] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/min_ss_100C_1v60/filter_unannotated.log…
[15:38:02] INFO     Starting STA for the max_tt_025C_1v80 timing corner…                            openroad.py:561
[15:38:02] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/max_tt_025C_1v80/sta.log…
[15:38:02] INFO     Finished STA for the min_ff_n40C_1v95 timing corner.                            openroad.py:576
[15:38:02] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/min_ff_n40C_1v95/filter_unannotated.log…
[15:38:04] INFO     Starting STA for the max_ss_100C_1v60 timing corner…                            openroad.py:561
[15:38:04] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/max_ss_100C_1v60/sta.log…
[15:38:08] INFO     Finished STA for the max_tt_025C_1v80 timing corner.                            openroad.py:576
[15:38:08] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/max_tt_025C_1v80/filter_unannotated.log…
[15:38:09] INFO     Starting STA for the max_ff_n40C_1v95 timing corner…                            openroad.py:561
[15:38:09] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/max_ff_n40C_1v95/sta.log…
[15:38:09] INFO     Finished STA for the max_ss_100C_1v60 timing corner.                            openroad.py:576
[15:38:09] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/max_ss_100C_1v60/filter_unannotated.log…
[15:38:12] INFO     Finished STA for the max_ff_n40C_1v95 timing corner.                            openroad.py:576
[15:38:12] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/64-openroad-stapostpnr/max_ff_n40C_1v95/filter_unannotated.log…
```

Corner/Group	Hold Worst Slack	Reg to Reg Paths	Hold TNS	Hold Vio Count	of whi… reg to reg	Setup Worst Slack	Reg to Reg Pat…	Setup TNS	Set… Vio Cou…	of which reg to reg	Max Cap Vio…	Max Slew Viol…
Overall	3.99…	N/A	0.0…	0	0	-12.…	N/A	-243…	147	0	0	66
nom_tt_025C_1v80	4.13…	N/A	0.0…	0	0	-2.7…	N/A	-35.…	19	0	0	10
nom_ss_100C_1v60	4.50…	N/A	0.0…	0	0	-12.…	N/A	-241…	30	0	0	64
nom_ff_n40C_1v95	4.00…	N/A	0.0…	0	0	0.65…	N/A	0.00…	0	0	0	0
min_tt_025C_1v80	4.12…	N/A	0.0…	0	0	-2.7…	N/A	-34.…	19	0	0	6
min_ss_100C_1v60	4.48…	N/A	0.0…	0	0	-12.…	N/A	-238…	30	0	0	66
min_ff_n40C_1v95	3.99…	N/A	0.0…	0	0	0.68…	N/A	0.00…	0	0	0	0
max_tt_025C_1v80	4.14…	N/A	0.0…	0	0	-2.8…	N/A	-36.…	19	0	0	12
max_ss_100C_1v60	4.53…	N/A	0.0…	0	0	-12.…	N/A	-243…	30	0	0	64
max_ff_n40C_1v95	4.01…	N/A	0.0…	0	0	0.61…	N/A	0.00…	0	0	0	0

Corner/Group	Hold Worst Slack	Reg to Reg Paths	Hold TNS	Hold Vio Count	of which reg to reg	Setup Worst Slack	Reg to Reg Paths	Setup TNS	Setup Vio Count	of which reg to reg	Max Cap Violatio…	Max Slew Violati…
Overall	3.9969	N/A	0.0000	0	0	-12.9366	N/A	-243.99…	147	0	0	66
nom_tt_025C_1v80	4.1344	N/A	0.0000	0	0	-2.7548	N/A	-35.7568	19	0	0	10
nom_ss_100C_1v60	4.5048	N/A	0.0000	0	0	-12.8264	N/A	-241.16…	30	0	0	64
nom_ff_n40C_1v95	4.0052	N/A	0.0000	0	0	0.6531	N/A	0.0000	0	0	0	0
min_tt_025C_1v80	4.1226	N/A	0.0000	0	0	-2.7001	N/A	-34.7285	19	0	0	6
min_ss_100C_1v60	4.4815	N/A	0.0000	0	0	-12.7378	N/A	-238.84…	30	0	0	66
min_ff_n40C_1v95	3.9969	N/A	0.0000	0	0	0.6895	N/A	0.0000	0	0	0	0
max_tt_025C_1v80	4.1488	N/A	0.0000	0	0	-2.8171	N/A	-36.9254	19	0	0	12
max_ss_100C_1v60	4.5319	N/A	0.0000	0	0	-12.9366	N/A	-243.99…	30	0	0	64
max_ff_n40C_1v95	4.0153	N/A	0.0000	0	0	0.6122	N/A	0.0000	0	0	0	0

Format	Path
nl	openlane_run/62-openroad-fillinsertion/MISO.nl.v
pnl	openlane_run/62-openroad-fillinsertion/MISO.pnl.v
def	openlane_run/62-openroad-fillinsertion/MISO.def
odb	openlane_run/62-openroad-fillinsertion/MISO.odb
sdc	openlane_run/62-openroad-fillinsertion/MISO.sdc
sdf	nom_tt_025C_1v80 openlane_run/64-openroad-stapostpnr/nom_tt_025C_1v80/MISO__nom_tt_025C_1v80.sdf
	nom_ss_100C_1v60 openlane_run/64-openroad-stapostpnr/nom_ss_100C_1v60/MISO__nom_ss_100C_1v60.sdf
	nom_ff_n40C_1v95 openlane_run/64-openroad-stapostpnr/nom_ff_n40C_1v95/MISO__nom_ff_n40C_1v95.sdf
	min_tt_025C_1v80 openlane_run/64-openroad-stapostpnr/min_tt_025C_1v80/MISO__min_tt_025C_1v80.sdf
	min_ss_100C_1v60 openlane_run/64-openroad-stapostpnr/min_ss_100C_1v60/MISO__min_ss_100C_1v60.sdf
	min_ff_n40C_1v95 openlane_run/64-openroad-stapostpnr/min_ff_n40C_1v95/MISO__min_ff_n40C_1v95.sdf
	max_tt_025C_1v80 openlane_run/64-openroad-stapostpnr/max_tt_025C_1v80/MISO__max_tt_025C_1v80.sdf
	max_ss_100C_1v60 openlane_run/64-openroad-stapostpnr/max_ss_100C_1v60/MISO__max_ss_100C_1v60.sdf
	max_ff_n40C_1v95 openlane_run/64-openroad-stapostpnr/max_ff_n40C_1v95/MISO__max_ff_n40C_1v95.sdf
spef	nom_* openlane_run/63-openroad-rcx/nom/MISO.nom.spef
	min_* openlane_run/63-openroad-rcx/min/MISO.min.spef
	max_* openlane_run/63-openroad-rcx/max/MISO.max.spef
lib	nom_tt_025C_1v80 openlane_run/64-openroad-stapostpnr/nom_tt_025C_1v80/MISO__nom_tt_025C_1v80.lib
	nom_ss_100C_1v60 openlane_run/64-openroad-stapostpnr/nom_ss_100C_1v60/MISO__nom_ss_100C_1v60.lib
	nom_ff_n40C_1v95 openlane_run/64-openroad-stapostpnr/nom_ff_n40C_1v95/MISO__nom_ff_n40C_1v95.lib
	min_tt_025C_1v80 openlane_run/64-openroad-stapostpnr/min_tt_025C_1v80/MISO__min_tt_025C_1v80.lib
	min_ss_100C_1v60 openlane_run/64-openroad-stapostpnr/min_ss_100C_1v60/MISO__min_ss_100C_1v60.lib

Stream-out

Stream-out is the process of converting the designs from the abstract formats using during floorplanning, placement and routing into a concrete format called GDSII (lit. Graphic Design System 2), which is the final file that is then sent for fabrication.

```
StreamOut = Step.factory.get("KLayout.StreamOut")

gds = StreamOut(state_in=sta_post_pnr.state_out)
gds.start()
```

```
──────────────────────────────────────── GDSII Stream Out (KLayout) ────────────────────────────────────────
[15:38:13] VERBOSE  Running 'KLayout.StreamOut'…                                                  step.py:1088
[15:38:13] VERBOSE  Logging subprocess to openlane_run/65-klayout-streamout/klayout-streamout.log…  step.py:1268
[INFO] Clearing cells…
[INFO] Merging GDS files…
[INFO] Copying top level cell 'MISO'…
[INFO] Checking for missing GDS…
[INFO] All LEF cells have matching GDS cells.
[INFO] Writing out GDS '/content/openlane_run/65-klayout-streamout/MISO.klayout.gds'…
[INFO] Done.
```

Format	Path	
nl	openlane_run/62-openroad-fillinsertion/MISO.nl.v	
pnl	openlane_run/62-openroad-fillinsertion/MISO.pnl.v	
def	openlane_run/62-openroad-fillinsertion/MISO.def	
odb	openlane_run/62-openroad-fillinsertion/MISO.odb	
sdc	openlane_run/62-openroad-fillinsertion/MISO.sdc	
sdf	nom_tt_025C_1v80	openlane_run/64-openroad-stapostpnr/nom_tt_025C_1v80/MISO__nom_tt_025C_1v80.sdf
	nom_ss_100C_1v60	openlane_run/64-openroad-stapostpnr/nom_ss_100C_1v60/MISO__nom_ss_100C_1v60.sdf
	nom_ff_n40C_1v95	openlane_run/64-openroad-stapostpnr/nom_ff_n40C_1v95/MISO__nom_ff_n40C_1v95.sdf
	min_tt_025C_1v80	openlane_run/64-openroad-stapostpnr/min_tt_025C_1v80/MISO__min_tt_025C_1v80.sdf
	min_ss_100C_1v60	openlane_run/64-openroad-stapostpnr/min_ss_100C_1v60/MISO__min_ss_100C_1v60.sdf
	min_ff_n40C_1v95	openlane_run/64-openroad-stapostpnr/min_ff_n40C_1v95/MISO__min_ff_n40C_1v95.sdf
	max_tt_025C_1v80	openlane_run/64-openroad-stapostpnr/max_tt_025C_1v80/MISO__max_tt_025C_1v80.sdf
	max_ss_100C_1v60	openlane_run/64-openroad-stapostpnr/max_ss_100C_1v60/MISO__max_ss_100C_1v60.sdf
	max_ff_n40C_1v95	openlane_run/64-openroad-stapostpnr/max_ff_n40C_1v95/MISO__max_ff_n40C_1v95.sdf
spef	nom_*	openlane_run/63-openroad-rcx/nom/MISO.nom.spef
	min_*	openlane_run/63-openroad-rcx/min/MISO.min.spef
	max_*	openlane_run/63-openroad-rcx/max/MISO.max.spef
lib	nom_tt_025C_1v80	openlane_run/64-openroad-stapostpnr/nom_tt_025C_1v80/MISO__nom_tt_025C_1v80.lib
	nom_ss_100C_1v60	openlane_run/64-openroad-stapostpnr/nom_ss_100C_1v60/MISO__nom_ss_100C_1v60.lib
	nom_ff_n40C_1v95	openlane_run/64-openroad-stapostpnr/nom_ff_n40C_1v95/MISO__nom_ff_n40C_1v95.lib
	min_tt_025C_1v80	openlane_run/64-openroad-stapostpnr/min_tt_025C_1v80/MISO__min_tt_025C_1v80.lib
	min_ss_100C_1v60	openlane_run/64-openroad-stapostpnr/min_ss_100C_1v60/MISO__min_ss_100C_1v60.lib
	min_ff_n40C_1v95	openlane_run/64-openroad-stapostpnr/min_ff_n40C_1v95/MISO__min_ff_n40C_1v95.lib
	max_tt_025C_1v80	openlane_run/64-openroad-stapostpnr/max_tt_025C_1v80/MISO__max_tt_025C_1v80.lib
	max_ss_100C_1v60	openlane_run/64-openroad-stapostpnr/max_ss_100C_1v60/MISO__max_ss_100C_1v60.lib
	max_ff_n40C_1v95	openlane_run/64-openroad-stapostpnr/max_ff_n40C_1v95/MISO__max_ff_n40C_1v95.lib
gds	openlane_run/65-klayout-streamout/MISO.gds	
klayout.gds	openlane_run/65-klayout-streamout/MISO.klayout.gds	

```
display(gds)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[15:38:14] VERBOSE  Running 'KLayout.Render'…                                                    step.py:1088
[15:38:14] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_sde05cf2/klayout-render.log…  step.py:1268
```

Time Elapsed: 0.72s

Views updated:

- GDSII Stream
- GDSII Stream (KLayout)

Preview:

Design Rule Checks (DRC)

DRC determines that the final layout does not violate any of the rules set by the foundry to ensure the design is actually manufacturable- for example, not enough space between two wires, *too much* space between tap cells, and so on.

A design not passing DRC will typically be rejected by the foundry, who also run DRC on their side.

```
DRC = Step.factory.get("Magic.DRC")

drc = DRC(state_in=gds.state_out)
drc.start()
```

```
──────────────────────────────────────────────────────── Design Rule Checks ────────────────────────────────────────────────────────
[15:38:15] VERBOSE  Running 'Magic.DRC'…                                                                                  step.py:1088
[15:38:15] VERBOSE  Logging subprocess to openlane_run/66-magic-drc/magic-drc.log…                                         step.py:1268

Magic 8.3 revision 483 - Compiled on Sun Jun  2 18:57:41 UTC 2024.
Starting magic under Tcl interpreter
Using the terminal as the console.
Using NULL graphics device.
Processing system .magicrc file
Sourcing design .magicrc for technology sky130A ...
2 Magic internal units = 1 Lambda
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
ubm
Scaled tech values by 2 / 1 to match internal grid scaling
Loading sky130A Device Generator Menu ...
Loading "/content/openlane_ipynb/openlane/scripts/magic/wrapper.tcl" from command line.
Warning: Calma reading is not undoable!  I hope that's OK.
Library written using GDS-II Release 6.0
Library name: LIB
Reading "VIA_M1M2_PR_MR".
Reading "VIA_M2M3_PR".
Reading "VIA_M3M4_PR".
Reading "VIA_M1M2_PR".
Reading "VIA_L1M1_PR_MR".
Reading "VIA_via2_3_2000_480_1_6_320_320".
Reading "VIA_via3_4_2000_480_1_5_400_400".
Reading "VIA_via4_5_2000_480_1_5_400_400".
Reading "VIA_via5_6_2000_2000_1_1_1600_1600".
Reading "sky130_fd_sc_hd__conb_1".
Reading "sky130_fd_sc_hd__o2111a_2".
Reading "sky130_fd_sc_hd__o22a_2".
Reading "sky130_fd_sc_hd__o21ba_2".
Reading "sky130_fd_sc_hd__a31oi_2".
Reading "sky130_fd_sc_hd__nor3b_2".
Reading "sky130_fd_sc_hd__a221o_2".
Reading "sky130_fd_sc_hd__a22oi_2".
Reading "sky130_fd_sc_hd__or4bb_2".
Reading "sky130_fd_sc_hd__o41a_2".
Reading "sky130_fd_sc_hd__o32a_2".
Reading "sky130_fd_sc_hd__o22ai_2".
Reading "sky130_fd_sc_hd__o211ai_2".
Reading "sky130_fd_sc_hd__a2111o_2".
Reading "sky130_fd_sc_hd__a2111oi_2".
Reading "sky130_fd_sc_hd__o2111ai_2".
Reading "sky130_fd_sc_hd__o41ai_2".
Reading "sky130_fd_sc_hd__a311oi_2".
Reading "sky130_fd_sc_hd__nand4_2".
Reading "sky130_fd_sc_hd__o311a_2".
Reading "sky130_fd_sc_hd__or4b_2".
Reading "sky130_fd_sc_hd__a211o_2".
Reading "sky130_fd_sc_hd__or4_2".
Reading "sky130_fd_sc_hd__nor4_2".
Reading "sky130_fd_sc_hd__a21bo_2".
Reading "sky130_fd_sc_hd__a32o_2".
Reading "sky130_fd_sc_hd__a2bb2o_2".
Reading "sky130_fd_sc_hd__a22o_2".
Reading "sky130_fd_sc_hd__o21bai_2".
Reading "sky130_fd_sc_hd__a311o_2".
Reading "sky130_fd_sc_hd__mux2_1".
Reading "sky130_fd_sc_hd__a31o_2".
Reading "sky130_fd_sc_hd__a211oi_2".
Reading "sky130_fd_sc_hd__o221a_2".
Reading "sky130_fd_sc_hd__a41o_2".
Reading "sky130_fd_sc_hd__or3b_2".
Reading "sky130_fd_sc_hd__nand3_2".
Reading "sky130_fd_sc_hd__and4_2".
Reading "sky130_fd_sc_hd__o31a_2".
Reading "sky130_fd_sc_hd__o211a_2".
Reading "sky130_fd_sc_hd__o21ai_2".
Reading "sky130_fd_sc_hd__or3_2".
Reading "sky130_fd_sc_hd__o2bb2a_2".
Reading "sky130_fd_sc_hd__inv_2".
Reading "sky130_fd_sc_hd__nor3_2".
Reading "sky130_fd_sc_hd__nand3b_2".
Reading "sky130_fd_sc_hd__and4b_2".
Reading "sky130_fd_sc_hd__nand2b_2".
Reading "sky130_fd_sc_hd__a21boi_2".
Reading "sky130_fd_sc_hd__a21oi_2".
Reading "sky130_fd_sc_hd__o21a_2".
Reading "sky130_fd_sc_hd__xnor2_2".
Reading "sky130_fd_sc_hd__and3b_2".
Reading "sky130_fd_sc_hd__nor2_2".
Reading "sky130_fd_sc_hd__and3_2".
Reading "sky130_fd_sc_hd__and2b_2".
Reading "sky130_fd_sc_hd__a21o_2".
Reading "sky130_fd_sc_hd__and4bb_2".
Reading "sky130_fd_sc_hd__xor2_2".
Reading "sky130_fd_sc_hd__o31ai_2".
Reading "sky130_fd_sc_hd__and2_2".
Reading "sky130_fd_sc_hd__nand2_2".
Reading "sky130_fd_sc_hd__or2_2".
Reading "sky130_fd_sc_hd__tapvpwrvgnd_1".
Reading "sky130_fd_sc_hd__decap_4".
Reading "sky130_fd_sc_hd__decap_6".
Reading "sky130_fd_sc_hd__decap_8".
Reading "sky130_fd_sc_hd__fill_2".
Reading "sky130_ef_sc_hd__decap_12".
Reading "sky130_fd_sc_hd__decap_3".
Reading "sky130_fd_sc_hd__fill_1".
Reading "MISO".
5000 uses
10000 uses
[INFO] Loading MISO

DRC style is now "drc(full)"
Loading DRC CIF style.
No errors found.
[INFO] COUNT: 0
[INFO] Should be divided by 3 or 4
[INFO] DRC Checking DONE (/content/openlane_run/66-magic-drc/reports/drc_violations.magic.rpt)
[INFO] Saving mag view with DRC errors (/content/openlane_run/66-magic-drc/views/MISO.drc.mag)
[INFO] Saved
```

Format	Path	
nl	openlane_run/62-openroad-fillinsertion/MISO.nl.v	
pnl	openlane_run/62-openroad-fillinsertion/MISO.pnl.v	
def	openlane_run/62-openroad-fillinsertion/MISO.def	
odb	openlane_run/62-openroad-fillinsertion/MISO.odb	
sdc	openlane_run/62-openroad-fillinsertion/MISO.sdc	
	nom_tt_025C_1v80	openlane_run/64-openroad-stapostpnr/nom_tt_025C_1v80/MISO__nom_tt_025C_1v80.sdf
	nom_ss_100C_1v60	openlane_run/64-openroad-stapostpnr/nom_ss_100C_1v60/MISO__nom_ss_100C_1v60.sdf
	nom_ff_n40C_1v95	openlane_run/64-openroad-stapostpnr/nom_ff_n40C_1v95/MISO__nom_ff_n40C_1v95.sdf
	min_tt_025C_1v80	openlane_run/64-openroad-stapostpnr/min_tt_025C_1v80/MISO__min_tt_025C_1v80.sdf
sdf	min_ss_100C_1v60	openlane_run/64-openroad-stapostpnr/min_ss_100C_1v60/MISO__min_ss_100C_1v60.sdf

```
                min_ff_n40C_1v95   openlane_run/64-openroad-stapostpnr/min_ff_n40C_1v95/MISO__min_ff_n40C_1v95.sdf
                max_tt_025C_1v80   openlane_run/64-openroad-stapostpnr/max_tt_025C_1v80/MISO__max_tt_025C_1v80.sdf
                max_ss_100C_1v60 openlane_run/64-openroad-stapostpnr/max_ss_100C_1v60/MISO__max_ss_100C_1v60.sdf
                max_ff_n40C_1v95   openlane_run/64-openroad-stapostpnr/max_ff_n40C_1v95/MISO__max_ff_n40C_1v95.sdf
                nom_* openlane_run/63-openroad-rcx/nom/MISO.nom.spef
spef            min_*  openlane_run/63-openroad-rcx/min/MISO.min.spef
                max_* openlane_run/63-openroad-rcx/max/MISO.max.spef
                nom_tt_025C_1v80   openlane_run/64-openroad-stapostpnr/nom_tt_025C_1v80/MISO__nom_tt_025C_1v80.lib
                nom_ss_100C_1v60 openlane_run/64-openroad-stapostpnr/nom_ss_100C_1v60/MISO__nom_ss_100C_1v60.lib
                nom_ff_n40C_1v95   openlane_run/64-openroad-stapostpnr/nom_ff_n40C_1v95/MISO__nom_ff_n40C_1v95.lib
                min_tt_025C_1v80   openlane_run/64-openroad-stapostpnr/min_tt_025C_1v80/MISO__min_tt_025C_1v80.lib
lib             min_ss_100C_1v60   openlane_run/64-openroad-stapostpnr/min_ss_100C_1v60/MISO__min_ss_100C_1v60.lib
                min_ff_n40C_1v95   openlane_run/64-openroad-stapostpnr/min_ff_n40C_1v95/MISO__min_ff_n40C_1v95.lib
```

SPICE Extraction for Layout vs. Schematic Check

This step tries to reconstruct a SPICE netlist from the GDSII file, so it can later be used for the **Layout vs. Schematic** (LVS) check.

```
SpiceExtraction = Step.factory.get("Magic.SpiceExtraction")

spx = SpiceExtraction(state_in=drc.state_out)
spx.start()
```

```
──────────────────────────────────────── SPICE Model Extraction ────────────────────────────────────────
[15:38:23] VERBOSE  Running 'Magic.SpiceExtraction'…                                          step.py:1088
[15:38:23] VERBOSE  Logging subprocess to                                                     step.py:1268
                    openlane_run/67-magic-spiceextraction/magic-spiceextraction.log…

Magic 8.3 revision 483 - Compiled on Sun Jun  2 18:57:41 UTC 2024.
Starting magic under Tcl interpreter
Using the terminal as the console.
Using NULL graphics device.
Processing system .magicrc file
Sourcing design .magicrc for technology sky130A ...
2 Magic internal units = 1 Lambda
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
ubm
Scaled tech values by 2 / 1 to match internal grid scaling
Loading sky130A Device Generator Menu ...
Loading "/content/openlane_ipynb/openlane/scripts/magic/wrapper.tcl" from command line.
> lef read /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef
Reading LEF data from file /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef.
This action cannot be undone.
LEF read, Line 78 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 79 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 112 (Message): Unknown keyword "MINENCLOSEDAREA" in LEF file; ignoring.
LEF read, Line 114 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 115 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 121 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 122 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 123 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 156 (Message): Unknown keyword "MINENCLOSEDAREA" in LEF file; ignoring.
LEF read, Line 164 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 165 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 167 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 168 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 169 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 206 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 207 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 209 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 210 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 211 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 248 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 249 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read, Line 251 (Message): Unknown keyword "MAXIMUMDENSITY" in LEF file; ignoring.
LEF read, Line 252 (Message): Unknown keyword "DENSITYCHECKWINDOW" in LEF file; ignoring.
LEF read, Line 253 (Message): Unknown keyword "DENSITYCHECKSTEP" in LEF file; ignoring.
LEF read, Line 290 (Message): Unknown keyword "ANTENNAMODEL" in LEF file; ignoring.
LEF read, Line 291 (Message): Unknown keyword "ANTENNADIFFSIDEAREARATIO" in LEF file; ignoring.
LEF read: Processed 797 lines.
> lef read /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef
Reading LEF data from file /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef.
This action cannot be undone.
LEF read: Processed 278 lines.
> lef read /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef
Reading LEF data from file /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef.
This action cannot be undone.
LEF read: Processed 56535 lines.
> def read /content/openlane_run/62-openroad-fillinsertion/MISO.def -noblockage -labels
Reading DEF data from file /content/openlane_run/62-openroad-fillinsertion/MISO.def.
This action cannot be undone.
Processed 4 vias total.
Processed 3192 subcell instances total.
Processed 162 pins total.
Processed 2 special nets total.
Processed 1305 nets total.
DEF read: Processed 22022 lines.
Moving label "VPWR" from metal1 to via1 in cell MISO.
Moving label "_0041_" from metal2 to via1 in cell MISO.
Moving label "_0183_" from metal2 to via2 in cell MISO.
Moving label "_0349_" from metal1 to via1 in cell MISO.
Moving label "_0376_" from metal1 to via1 in cell MISO.
Moving label "_0422_" from metal2 to via1 in cell MISO.
Moving label "_0461_" from metal1 to via1 in cell MISO.
Moving label "_0515_" from metal2 to via2 in cell MISO.
Moving label "_0578_" from metal1 to via1 in cell MISO.
Moving label "_0599_" from metal1 to via1 in cell MISO.
Moving label "_0613_" from metal1 to via1 in cell MISO.
Moving label "_0718_" from metal1 to via1 in cell MISO.
Moving label "_0747_" from metal1 to viali in cell MISO.
Moving label "_0821_" from metal1 to via1 in cell MISO.
Moving label "_0978_" from metal1 to via1 in cell MISO.
Moving label "_1021_" from metal1 to via1 in cell MISO.
Moving label "_1062_" from metal2 to via2 in cell MISO.
Moving label "out[18]" from metal2 to via2 in cell MISO.
Moving label "out[19]" from metal2 to via2 in cell MISO.
Moving label "out[50]" from metal2 to via2 in cell MISO.
Moving label "out[61]" from metal2 to via2 in cell MISO.
Moving label "out[62]" from metal2 to via2 in cell MISO.
Moving label "out[63]" from metal2 to via2 in cell MISO.
Moving label "x[3]" from metal2 to via2 in cell MISO.
Processing MISO
Extracting sky130_ef_sc_hd__decap_12 into sky130_ef_sc_hd__decap_12.ext:
Extracting sky130_fd_sc_hd__decap_3 into sky130_fd_sc_hd__decap_3.ext:
Extracting sky130_fd_sc_hd__conb_1 into sky130_fd_sc_hd__conb_1.ext:
Extracting sky130_fd_sc_hd__fill_1 into sky130_fd_sc_hd__fill_1.ext:
Extracting sky130_fd_sc_hd__decap_8 into sky130_fd_sc_hd__decap_8.ext:
Extracting sky130_fd_sc_hd__decap_4 into sky130_fd_sc_hd__decap_4.ext:
Extracting sky130_fd_sc_hd__tapvpwrvgnd_1 into sky130_fd_sc_hd__tapvpwrvgnd_1.ext:
Extracting sky130_fd_sc_hd__nand2_2 into sky130_fd_sc_hd__nand2_2.ext:
Extracting sky130_fd_sc_hd__xor2_2 into sky130_fd_sc_hd__xor2_2.ext:
Extracting sky130_fd_sc_hd__a21boi_2 into sky130_fd_sc_hd__a21boi_2.ext:
Extracting sky130_fd_sc_hd__or2_2 into sky130_fd_sc_hd__or2_2.ext:
Extracting sky130_fd_sc_hd__fill_2 into sky130_fd_sc_hd__fill_2.ext:
Extracting sky130_fd_sc_hd__nor2_2 into sky130_fd_sc_hd__nor2_2.ext:
Extracting sky130_fd_sc_hd__a21oi_2 into sky130_fd_sc_hd__a21oi_2.ext:
Extracting sky130_fd_sc_hd__and2_2 into sky130_fd_sc_hd__and2_2.ext:
Extracting sky130_fd_sc_hd__and2b_2 into sky130_fd_sc_hd__and2b_2.ext:
Extracting sky130_fd_sc_hd__xnor2_2 into sky130_fd_sc_hd__xnor2_2.ext:
Extracting sky130_fd_sc_hd__a21o_2 into sky130_fd_sc_hd__a21o_2.ext:
Extracting sky130_fd_sc_hd__and3_2 into sky130_fd_sc_hd__and3_2.ext:
Extracting sky130_fd_sc_hd__or3b_2 into sky130_fd_sc_hd__or3b_2.ext:
Extracting sky130_fd_sc_hd__mux2_1 into sky130_fd_sc_hd__mux2_1.ext:
Extracting sky130_fd_sc_hd__decap_6 into sky130_fd_sc_hd__decap_6.ext:
Extracting sky130_fd_sc_hd__and3b_2 into sky130_fd_sc_hd__and3b_2.ext:
Extracting sky130_fd_sc_hd__a22oi_2 into sky130_fd_sc_hd__a22oi_2.ext:
Extracting sky130_fd_sc_hd__o32a_2 into sky130_fd_sc_hd__o32a_2.ext:
Extracting sky130_fd_sc_hd__o21a_2 into sky130_fd_sc_hd__o21a_2.ext:
Extracting sky130_fd_sc_hd__a22o_2 into sky130_fd_sc_hd__a22o_2.ext:
Extracting sky130_fd_sc_hd__inv_2 into sky130_fd_sc_hd__inv_2.ext:
Extracting sky130_fd_sc_hd__and4b_2 into sky130_fd_sc_hd__and4b_2.ext:
Extracting sky130_fd_sc_hd__a32o_2 into sky130_fd_sc_hd__a32o_2.ext:
Extracting sky130_fd_sc_hd__or3_2 into sky130_fd_sc_hd__or3_2.ext:
Extracting sky130_fd_sc_hd__o21ai_2 into sky130_fd_sc_hd__o21ai_2.ext:
Extracting sky130_fd_sc_hd__a31o_2 into sky130_fd_sc_hd__a31o_2.ext:
Extracting sky130_fd_sc_hd__nand2b_2 into sky130_fd_sc_hd__nand2b_2.ext:
Extracting sky130_fd_sc_hd__o2111a_2 into sky130_fd_sc_hd__o2111a_2.ext:
Extracting sky130_fd_sc_hd__nand3_2 into sky130_fd_sc_hd__nand3_2.ext:
Extracting sky130_fd_sc_hd__o21ba_2 into sky130_fd_sc_hd__o21ba_2.ext:
```

```
Extracting sky130_fd_sc_hd__nor3_2 into sky130_fd_sc_hd__nor3_2.ext:
Extracting sky130_fd_sc_hd__o2bb2a_2 into sky130_fd_sc_hd__o2bb2a_2.ext:
Extracting sky130_fd_sc_hd__o21bai_2 into sky130_fd_sc_hd__o21bai_2.ext:
Extracting sky130_fd_sc_hd__o22a_2 into sky130_fd_sc_hd__o22a_2.ext:
Extracting sky130_fd_sc_hd__o311a_2 into sky130_fd_sc_hd__o311a_2.ext:
Extracting sky130_fd_sc_hd__a21bo_2 into sky130_fd_sc_hd__a21bo_2.ext:
Extracting sky130_fd_sc_hd__o41a_2 into sky130_fd_sc_hd__o41a_2.ext:
Extracting sky130_fd_sc_hd__or4_2 into sky130_fd_sc_hd__or4_2.ext:
Extracting sky130_fd_sc_hd__a31oi_2 into sky130_fd_sc_hd__a31oi_2.ext:
Extracting sky130_fd_sc_hd__a2111o_2 into sky130_fd_sc_hd__a2111o_2.ext:
Extracting sky130_fd_sc_hd__o211a_2 into sky130_fd_sc_hd__o211a_2.ext:
Extracting sky130_fd_sc_hd__and4bb_2 into sky130_fd_sc_hd__and4bb_2.ext:
Extracting sky130_fd_sc_hd__or4b_2 into sky130_fd_sc_hd__or4b_2.ext:
Extracting sky130_fd_sc_hd__o31a_2 into sky130_fd_sc_hd__o31a_2.ext:
Extracting sky130_fd_sc_hd__nand3b_2 into sky130_fd_sc_hd__nand3b_2.ext:
Extracting sky130_fd_sc_hd__o22ai_2 into sky130_fd_sc_hd__o22ai_2.ext:
Extracting sky130_fd_sc_hd__a221o_2 into sky130_fd_sc_hd__a221o_2.ext:
Extracting sky130_fd_sc_hd__o41ai_2 into sky130_fd_sc_hd__o41ai_2.ext:
Extracting sky130_fd_sc_hd__nor3b_2 into sky130_fd_sc_hd__nor3b_2.ext:
Extracting sky130_fd_sc_hd__o31ai_2 into sky130_fd_sc_hd__o31ai_2.ext:
Extracting sky130_fd_sc_hd__or4bb_2 into sky130_fd_sc_hd__or4bb_2.ext:
Extracting sky130_fd_sc_hd__a211o_2 into sky130_fd_sc_hd__a211o_2.ext:
Extracting sky130_fd_sc_hd__and4_2 into sky130_fd_sc_hd__and4_2.ext:
Extracting sky130_fd_sc_hd__o221a_2 into sky130_fd_sc_hd__o221a_2.ext:
Extracting sky130_fd_sc_hd__a2bb2o_2 into sky130_fd_sc_hd__a2bb2o_2.ext:
Extracting sky130_fd_sc_hd__a211oi_2 into sky130_fd_sc_hd__a211oi_2.ext:
Extracting sky130_fd_sc_hd__a311o_2 into sky130_fd_sc_hd__a311o_2.ext:
Extracting sky130_fd_sc_hd__a41o_2 into sky130_fd_sc_hd__a41o_2.ext:
Extracting sky130_fd_sc_hd__nor4_2 into sky130_fd_sc_hd__nor4_2.ext:
Extracting sky130_fd_sc_hd__a2111oi_2 into sky130_fd_sc_hd__a2111oi_2.ext:
Extracting sky130_fd_sc_hd__o2111ai_2 into sky130_fd_sc_hd__o2111ai_2.ext:
Extracting sky130_fd_sc_hd__nand4_2 into sky130_fd_sc_hd__nand4_2.ext:
Extracting sky130_fd_sc_hd__o211ai_2 into sky130_fd_sc_hd__o211ai_2.ext:
Extracting sky130_fd_sc_hd__a311oi_2 into sky130_fd_sc_hd__a311oi_2.ext:
Extracting MISO into MISO.ext:
exttospice finished.
Using technology "sky130A", version 1.0.466-0-gbdc9412
```

Format	Path
nl	openlane_run/62-openroad-fillinsertion/MISO.nl.v
pnl	openlane_run/62-openroad-fillinsertion/MISO.pnl.v
def	openlane_run/62-openroad-fillinsertion/MISO.def
odb	openlane_run/62-openroad-fillinsertion/MISO.odb
sdc	openlane_run/62-openroad-fillinsertion/MISO.sdc
sdf	nom_tt_025C_1v80 openlane_run/64-openroad-stapostpnr/nom_tt_025C_1v80/MISO__nom_tt_025C_1v80.sdf
	nom_ss_100C_1v60 openlane_run/64-openroad-stapostpnr/nom_ss_100C_1v60/MISO__nom_ss_100C_1v60.sdf
	nom_ff_n40C_1v95 openlane_run/64-openroad-stapostpnr/nom_ff_n40C_1v95/MISO__nom_ff_n40C_1v95.sdf
	min_tt_025C_1v80 openlane_run/64-openroad-stapostpnr/min_tt_025C_1v80/MISO__min_tt_025C_1v80.sdf
	min_ss_100C_1v60 openlane_run/64-openroad-stapostpnr/min_ss_100C_1v60/MISO__min_ss_100C_1v60.sdf
	min_ff_n40C_1v95 openlane_run/64-openroad-stapostpnr/min_ff_n40C_1v95/MISO__min_ff_n40C_1v95.sdf
	max_tt_025C_1v80 openlane_run/64-openroad-stapostpnr/max_tt_025C_1v80/MISO__max_tt_025C_1v80.sdf
	max_ss_100C_1v60 openlane_run/64-openroad-stapostpnr/max_ss_100C_1v60/MISO__max_ss_100C_1v60.sdf
	max_ff_n40C_1v95 openlane_run/64-openroad-stapostpnr/max_ff_n40C_1v95/MISO__max_ff_n40C_1v95.sdf
spef	nom_* openlane_run/63-openroad-rcx/nom/MISO.nom.spef
	min_* openlane_run/63-openroad-rcx/min/MISO.min.spef
	max_* openlane_run/63-openroad-rcx/max/MISO.max.spef
	nom_tt_025C_1v80 openlane_run/64-openroad-stapostpnr/nom_tt_025C_1v80/MISO__nom_tt_025C_1v80.lib
	nom_ss_100C_1v60 openlane_run/64-openroad-stapostpnr/nom_ss_100C_1v60/MISO__nom_ss_100C_1v60.lib
	nom_ff_n40C_1v95 openlane_run/64-openroad-stapostpnr/nom_ff_n40C_1v95/MISO__nom_ff_n40C_1v95.lib
	min_tt_025C_1v80 openlane_run/64-openroad-stapostpnr/min_tt_025C_1v80/MISO__min_tt_025C_1v80.lib

Layout vs. Schematic (LVS)

A comparison between the final Verilog netlist (from PnR) and the final SPICE netlist (extracted.)

This check effectively compares the physically implemented circuit to the final Verilog netlist output by OpenROAD.

The idea is, if there are any disconnects, shorts or other mismatches in the physical implementation that do not exist in the logical view of the design, they would be caught at this step.

Common issues that result in LVS violations include:

- Lack of fill cells or tap cells in the design
- Two unrelated signals to be shorted, or a wire to be disconnected (most commonly seen with misconfigured PDN)

Chips with LVS errors are typically dead on arrival.

```
LVS = Step.factory.get("Netgen.LVS")

lvs = LVS(state_in=spx.state_out)
lvs.start()
```

```
──────────────────────────────────────────────────────────── Netgen LVS ────────────────────────────────────────────────────────────
[15:38:26] VERBOSE  Running 'Netgen.LVS'…                                                                                  step.py:1088
[15:38:26] VERBOSE  Logging subprocess to openlane_run/68-netgen-lvs/netgen-lvs.log…                                       step.py:1268
Netgen 1.5.270 compiled on Sun Jun  2 19:00:27 UTC 2024
Warning: netgen command 'format' use fully-qualified name '::netgen::format'
Warning: netgen command 'global' use fully-qualified name '::netgen::global'
Warning:  A case-insensitive file has been read and so the      verilog file must be treated case-insensitive to
match.
Reading SPICE netlist file
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__decap_12.spice'...
Call to undefined subcircuit sky130_fd_pr__pfet_01v8_hvt
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_pr__nfet_01v8
Creating placeholder cell definition.
Reading SPICE netlist file '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_12.spice'...
Reading SPICE netlist file '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_4.spice'...
Reading SPICE netlist file '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_8.spice'...
Reading SPICE netlist file '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_fd_sc_hd.spice'...
Call to undefined subcircuit sky130_fd_sc_hd__nand2_2
Creating placeholder cell definition.
Call to undefined subcircuit sky130_fd_sc_hd__nor2_2
Creating placeholder cell definition.
Warning:  A case-insensitive file has been read and so the      verilog file must be treated case-insensitive to
match.
Note:  Implicit pin HI in instance _2326_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2327_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2328_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2329_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2330_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2331_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2332_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2333_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2334_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2335_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2336_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2337_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2338_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2339_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2340_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2341_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2342_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2343_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2344_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2345_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2346_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2347_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2348_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2349_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2350_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2351_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2352_ of sky130_fd_sc_hd__conb_1 in cell MISO
Note:  Implicit pin HI in instance _2353_ of sky130_fd_sc_hd__conb_1 in cell MISO
Treating empty subcircuits as black-box cells
Generating JSON file result
```

Open in Colab

Task : 4 - Multiple Input, Multiple Output (MIMO)

Avinash Baraiya- 202201211

Malhar Vaghasiya - 202201183

Smeet Agrawal - 202101237

Priyesh Tandel - 202101222

Samarth Panchal- 202101456

OpenLane Colab

This Google Colab notebook will:

- Install OpenLane and its dependencies
- Run a simple design, namely a serial-parallel multiplier, through the flow and targeting the open source sky130 PDK by Google and Skywater.

Setup Nix

Nix is a package manager with an emphasis on reproducible builds, and it is the primary method for installing OpenLane 2.

This step installs the Nix package manager and enables the experimental "flakes" feature.

If you're not in a Colab, this just sets the environment variables. You will need to install Nix and enable flakes on your own following this guide.

Show code

Get OpenLane

Click the ▷ button to download and install OpenLane.

This will install OpenLane's tool dependencies using Nix, and OpenLane itself using PIP.

Note that `python3-tk` may need to be installed using your OS's package manager.

openlane_version: "version-2.1"

pdk_root: "~/.volare"

pdk: "sky130"

Show code

Downloading OpenLane…

```
  % Total    % Received % Xferd  Average Speed   Time    Time     Time  Current
                                 Dload  Upload   Total   Spent    Left  Speed
  0     0    0     0    0     0      0      0 --:--:-- --:--:-- --:--:--     0
100 9491k    0 9491k    0     0  4640k      0 --:--:--  0:00:02 --:--:-- 12.9M
```

Downloading OpenLane's dependencies…

Downloading Python dependencies using PIP…

Downloading PDK…

```
Version bdc9412b3e468c102d01b7cf6337be06ec6e9c9a enabled for the sky130 PDK.
```

Done.

```
import openlane

print(openlane.__version__)
```

```
2.1.11
```

Creating the design

Now that OpenLane is set up, we can write a Verilog file as follows:

```
%%writefile MIMO.v

module MIMO(in1,in2,in3,in4,out_main1,out_main2);

input [3:0] in1,in2,in3,in4;
output [15:0] out_main1,out_main2;

wire [3:0] i1 = 4'b0000;
wire [3:0] i2 = 4'b0001;
wire [3:0] i3 = 4'b0010;
wire [3:0] i4 = 4'b0011;
wire [3:0] i5 = 4'b0100;
wire [3:0] i6 = 4'b0101;
wire [3:0] i7 = 4'b0110;
wire [3:0] i8 = 4'b0111;
wire [3:0] i9 = 4'b1000;

wire [3:0] w_val1,w_val2,w_val3,w_val4,w_val5,w_val6,w_val7,w_val8,w_val9;
wire [7:0] out_n1,out_n2,out_n3,out_n4;
wire [7:0] out_1,out_2,out_3,out_4;
wire [7:0] out_temp1,out_temp2,out_temp3;
wire [15:0] out_mem1,out_mem2;

mem m1(i1,w_val1);
neuron  n1(out_n1,in1,w_val1);
//normalization norm1(out_1,out_n1);
```

```
mem m2(i2,w_val2);
neuron  n2(out_n2,in2,w_val2);

mem m3(i3,w_val3);
neuron  n3(out_n3,in3,w_val3);

mem m4(i4,w_val4);
neuron  n4(out_n4,in4,w_val4);

relu R1(out_1,out_2,out_n1,out_n2,out_n3,out_n4);
//relu R3(out_3,out_n7,out_n8,out_n9);


assign  out_main1 = out_1;
assign  out_main2 = out_2;

endmodule

//mem

module mem(index,weight_value);
input [3:0] index;
output reg [3:0] weight_value;

always @(*)
begin
case(index)

4'b0000 : weight_value = 4'b0101;
4'b0001 : weight_value = 4'b1011;
4'b0010 : weight_value = 4'b1010;
4'b0011 : weight_value = 4'b0110;
4'b0100 : weight_value = 4'b0100;
4'b0101 : weight_value = 4'b1100;
4'b0110 : weight_value = 4'b1101;
4'b0111 : weight_value = 4'b1110;
4'b1000 : weight_value = 4'b1000;

endcase
end

endmodule

//relu
module relu(data_out1,data_out2,data_in1,data_in2,data_in3,data_in4);
input signed [7:0] data_in1,data_in2,data_in3,data_in4;
output reg signed [7:0] data_out1,data_out2;

reg  signed [7:0] data_temp1,data_temp2;
wire signed [3:0] inputs[7:0];

integer i;

assign inputs[0]= data_in1;
assign inputs[1]= data_in2;
assign inputs[2]= data_in3;
assign inputs[3]= data_in4;
//assign inputs[4]= data_in5;
//assign inputs[5]= data_in6;
//assign inputs[6]= data_in7;
//assign inputs[7]= data_in8;

always@(*)
begin
  data_temp1 = (inputs[0] > inputs[1]) ? inputs[0] : inputs[1];
  data_temp2 = (inputs[0] > inputs[1]) ? inputs[1] : inputs[0];

  for (i = 2; i < 3; i = i + 1) begin
    if (inputs[i] > data_temp1) begin
      data_temp2 = data_temp1;
      data_temp1 = inputs[i];
    end
    else if (inputs[i] > data_temp2) begin
      data_temp2 = inputs[i];
    end
  end

  data_out1 = data_temp1;
  data_out2 = data_temp2;
end

endmodule

//neuron
module neuron(out_neuron,input_neuron,weight_value);
input [3:0] weight_value;
input [3:0] input_neuron;
output [7:0] out_neuron;

wire [7:0] bias= 8'b00000001 ;
wire [7:0] out_mul;

smul s1 (out_mul,weight_value,input_neuron);
sadder s2(out_neuron,out_mul,bias);

endmodule

//add
module sadder(
  output signed [7:0] sum,
  input signed [7:0] a,
  input signed [7:0] b);

  assign sum = a + b;
endmodule

//mul
module smul(p,a,b);

input [3:0] a,b;
output [7:0] p;
supply1 one;
```

```
wire w1,w2,w3,w4,w5,w6,w7,w8,w9,w10,w11,w12,w13,w14,w15,w16,w17,w18,w19,w20,w21,w22,w23;

assign p[0]=a[0]&b[0];

half_adder HA1(a[1]&b[0],a[0]&b[1],p[1],w1);
half_adder HA2(a[2]&b[0],a[1]&b[1],w2,w3);
half_adder HA3(~(a[3]&b[0]),a[2]&b[1],w4,w5);

full_adder FA1(w2,w1,a[0]&b[2],p[2],w6);
full_adder FA2(w4,w3,a[1]&b[2],w7,w8);
full_adder FA3(w5,a[2]&b[2],~(a[3]&b[1]),w9,w10);

full_adder FA4(w6,w7,~(a[0]&b[3]),p[3],w11);
full_adder FA5(w8,w9,~(a[1]&b[3]),w12,w13);
full_adder FA6(w10,~(a[2]&b[3]),~(a[3]&b[2]),w14,w15);

full_adder FA7(one,w11,w12,p[4],w16);
half_adder HA4(w13,w14,w17,w18);
half_adder HA5(a[3]&b[3],w15,w19,w20);

half_adder HA6(w16,w17,p[5],w21);
half_adder HA7(w18,w19,w22,w23);

half_adder HA8(w21,w22,p[7],p[6]);

endmodule

module half_adder(x,y,s,cout);
input x,y;
output s,cout;
assign s=x^y;
assign cout=(x&y);
endmodule

module full_adder(x,y,cin,s,cout);
input x,y,cin;
output s,cout;
assign s=x^y^cin;
assign cout = (x&y)|(y&cin)|(x&cin);
endmodule
```

```
Overwriting MIMO.v
```

Setting up the configuration

OpenLane requries you to configure any Flow before using it. This is done using the `config` module.

For colaboratories, REPLs and other interactive environments where there is no concrete Flow object, the Configuration may be initialized using `Config.interactive`, which will automatically propagate the configuration to any future steps.

You can find the documentation for `Config.interactive` here.

```
from openlane.config import Config

Config.interactive(
    "MIMO",
    PDK="sky130A",
    CLOCK_PORT="clk",
    CLOCK_NET="clk",
    CLOCK_PERIOD=10,
    PRIMARY_GDSII_STREAMOUT_TOOL="klayout",
)
```

Interactive Configuration

Initial Values

```
CELL_BB_VERILOG_MODELS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/sky130_fd_sc_hd__blackbox.v
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/sky130_fd_sc_hd__blackbox_pp.v
CELL_GDS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/gds/sky130_fd_sc_hd.gds
CELL_LEFS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef
CELL_PAD_EXCLUDE:
- sky130_fd_sc_hd__tap*
- sky130_fd_sc_hd__decap*
- sky130_ef_sc_hd__decap*
- sky130_fd_sc_hd__fill*
CELL_SPICE_MODELS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__decap_12.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_12.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_4.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_ef_sc_hd__fill_8.spice
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/spice/sky130_fd_sc_hd.spice
CELL_VERILOG_MODELS:
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/primitives.v
- /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/verilog/sky130_fd_sc_hd.v
CLOCK_NET: clk
CLOCK_PERIOD: 10
CLOCK_PORT: clk
CLOCK_TRANSITION_CONSTRAINT: 0.15
CLOCK_UNCERTAINTY_CONSTRAINT: 0.25
CLOCK_WIRE_RC_LAYERS: null
DECAP_CELL:
- sky130_ef_sc_hd__decap_12
- sky130_fd_sc_hd__decap_8
- sky130_fd_sc_hd__decap_6
- sky130_fd_sc_hd__decap_4
- sky130_fd_sc_hd__decap_3
DEFAULT_CORNER: nom_tt_025C_1v80
DEFAULT_MAX_TRAN: null
DESIGN_DIR: .
DESIGN_NAME: MIMO
DIE_AREA: null
DIODE_CELL: sky130_fd_sc_hd__diode_2/DIODE
ENDCAP_CELL: sky130_fd_sc_hd__decap_3
EXTRA_EXCLUDED_CELLS: null
EXTRA_GDS_FILES: null
EXTRA_LEFS: null
EXTRA_LIBS: null
EXTRA_SPICE_MODELS: null
EXTRA_VERILOG_MODELS: null
FALLBACK_SDC_FILE: /content/openlane_ipynb/openlane/scripts/base.sdc
FILL_CELL:
- sky130_fd_sc_hd__fill*
FP_IO_HLAYER: met3
FP_IO_VLAYER: met2
FP_TAPCELL_DIST: 13
FP_TRACKS_INFO: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tracks.info
GND_NETS: null
GND_PIN: VGND
GPIO_PADS_LEF:
- /root/.volare/sky130A/libs.ref/sky130_fd_io/lef/sky130_fd_io.lef
- /root/.volare/sky130A/libs.ref/sky130_fd_io/lef/sky130_ef_io.lef
GPIO_PADS_LEF_CORE_SIDE:
- /root/.volare/sky130A/libs.tech/openlane/custom_cells/lef/sky130_fd_io_core.lef
- /root/.volare/sky130A/libs.tech/openlane/custom_cells/lef/sky130_ef_io_core.lef
GPIO_PADS_VERILOG:
- /root/.volare/sky130A/libs.ref/sky130_fd_io/verilog/sky130_ef_io.v
GPIO_PAD_CELLS:
- sky130_fd_io*
- sky130_ef_io*
IO_DELAY_CONSTRAINT: 20
LIB:
  '*_ff_n40C_1v95':
  - /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ff_n40C_1v95.lib
  '*_ss_100C_1v60':
  - /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ss_100C_1v60.lib
  '*_tt_025C_1v80':
  - /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
MACROS: null
MAX_CAPACITANCE_CONSTRAINT: 0.2
MAX_FANOUT_CONSTRAINT: 10
MAX_TRANSITION_CONSTRAINT: 0.75
OUTPUT_CAP_LOAD: 33.442
PDK: sky130A
PDK_ROOT: /root/.volare
PLACE_SITE: unithd
PNR_EXCLUDED_CELL_FILE: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/drc_exclude.cells
PRIMARY_GDSII_STREAMOUT_TOOL: klayout
RT_MAX_LAYER: met5
RT_MIN_LAYER: met1
SCL_GROUND_PINS:
- VGND
- VNB
SCL_POWER_PINS:
- VPWR
- VPB
SIGNAL_WIRE_RC_LAYERS: null
STA_CORNERS:
- nom_tt_025C_1v80
- nom_ss_100C_1v60
- nom_ff_n40C_1v95
- min_tt_025C_1v80
- min_ss_100C_1v60
- min_ff_n40C_1v95
- max_tt_025C_1v80
- max_ss_100C_1v60
- max_ff_n40C_1v95
STD_CELL_LIBRARY: sky130_fd_sc_hd
SYNTH_BUFFER_CELL: sky130_fd_sc_hd__buf_2/A/X
SYNTH_CLK_DRIVING_CELL: null
SYNTH_DRIVING_CELL: sky130_fd_sc_hd__inv_2/Y
SYNTH_EXCLUDED_CELL_FILE: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/no_synth.cells
SYNTH_TIEHI_CELL: sky130_fd_sc_hd__conb_1/HI
SYNTH_TIELO_CELL: sky130_fd_sc_hd__conb_1/LO
TECH_LEFS:
  max_*: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__max.tlef
  min_*: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__min.tlef
  nom_*: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef
TIME_DERATING_CONSTRAINT: 5
TRISTATE_CELLS:
- sky130_fd_sc_hd__ebuf*
VDD_NETS: null
```

```
  VDD_PIN: VPWR
  VDD_PIN_VOLTAGE: 1.8
  WELLTAP_CELL: sky130_fd_sc_hd__tapvpwrvgnd_1
  WIRE_LENGTH_THRESHOLD: null
  meta:
    flow: null
    openlane_version: 2.1.11
    step: null
    substituting_steps: null
    version: 1
```

Running implementation steps

There are two ways to obtain OpenLane's built-in implementation steps:

- via directly importing from the `steps` module using its category:
  - `from openlane.steps import Yosys` then `Synthesis = Yosys.Synthesis`
- by using the step's id from the registry:
  - `from openlane.steps import Step` then `Synthesis = Step.factory.get("Yosys.Synthesis")`

You can find a full list of included steps here: https://openlane2.readthedocs.io/en/latest/reference/step_config_vars.html

```
from openlane.steps import Step
```

- First, get the step (and display its help)...

```
Synthesis = Step.factory.get("Yosys.Synthesis")

Synthesis.display_help()
```

(step-yosys-synthesis)=

Synthesis

```
Performs synthesis and technology mapping on Verilog RTL files
using Yosys and ABC, emitting a netlist.

Some metrics will also be extracted and updated, namely:

* ``design__instance__count``
* ``design__instance_unmapped__count``
* ``design__instance__area``
```

Importing

```
from openlane.steps.yosys import Synthesis

# or

from openlane.steps import Step

Synthesis = Step.factory.get("Yosys.Synthesis")
```

Inputs and Outputs

Inputs	Outputs
	Verilog Netlist (.nl.v)

(yosys.synthesis-configuration-variables)=

Configuration Variables

Variable Name	Type	Description	Default	Units
SYNTH_LATCH_MAP{#var-yosys-synthesis-synth_latch_map}PDK	Path?	A path to a file containing the latch mapping for Yosys.	None	
SYNTH_TRISTATE_MAP{#var-yosys-synthesis-synth_tristate_map}PDK	Path?	A path to a file containing the tri-state buffer mapping for Yosys.	None	
SYNTH_CSA_MAP{#var-yosys-synthesis-synth_csa_map}PDK	Path?	A path to a file containing the carry-select adder mapping for Yosys.	None	
SYNTH_RCA_MAP{#var-yosys-synthesis-synth_rca_map}PDK	Path?	A path to a file containing the ripple-carry adder mapping for Yosys.	None	
SYNTH_FA_MAP{#var-yosys-synthesis-synth_fa_map}PDK	Path?	A path to a file containing the full adder mapping for Yosys.	None	
SYNTH_MUX_MAP{#var-yosys-synthesis-synth_mux_map}PDK	Path?	A path to a file containing the mux mapping for Yosys.	None	
SYNTH_MUX4_MAP{#var-yosys-synthesis-synth_mux4_map}PDK	Path?	A path to a file containing the mux4 mapping for Yosys.	None	
USE_LIGHTER{#var-yosys-synthesis-use_lighter}	bool	Activates Lighter, an experimental plugin that attempts to optimize clock-gated flip-flops.	False	
LIGHTER_DFF_MAP{#var-yosys-synthesis-lighter_dff_map}	Path?	An override to the custom DFF map file provided for the given SCL by Lighter.	None	
YOSYS_LOG_LEVEL{#var-yosys-synthesis-yosys_log_level}	'ALL' | 'WARNING' | 'ERROR'	Which log level for Yosys. At WARNING or higher, the initialization splash is also disabled.	ALL	
SYNTH_CHECKS_ALLOW_TRISTATE{#var-yosys-synthesis-synth_checks_allow_tristate}	bool	Ignore multiple-driver warnings if they are connected to tri-state buffers on a best-effort basis.	True	
SYNTH_AUTONAME{#var-yosys-synthesis-synth_autoname}	bool	Generates names for netlist instances. This results in instance names that can be extremely long, but are more human-readable.	False	
SYNTH_STRATEGY{#var-yosys-synthesis-synth_strategy}	'AREA 0' | 'AREA 1' | 'AREA 2' | 'AREA 3' | 'DELAY 0' | 'DELAY 1' | 'DELAY 2' | 'DELAY 3' | 'DELAY 4'	Strategies for abc logic synthesis and technology mapping. AREA strategies usually result in a more compact design, while DELAY strategies usually result in a design that runs at a higher frequency. Please note that there is no way to know which strategy is the best before trying them.	AREA 0	
SYNTH_ABC_BUFFERING{#var-yosys-synthesis-synth_abc_buffering}	bool	Enables `abc` cell buffering.	False	
SYNTH_ABC_LEGACY_REFACTOR{#var-yosys-synthesis-synth_abc_legacy_refactor}	bool	Replaces the ABC command `drf -l` with `refactor` which matches older versions of OpenLane but is more unstable.	False	
SYNTH_ABC_LEGACY_REWRITE{#var-yosys-synthesis-synth_abc_legacy_rewrite}	bool	Replaces the ABC command `drw -l` with `rewrite` which matches older versions of OpenLane but is more unstable.	False	
SYNTH_DIRECT_WIRE_BUFFERING{#var-yosys-synthesis-synth_direct_wire_buffering}	bool	Enables inserting buffer cells for directly connected wires.	True	
SYNTH_SPLITNETS{#var-yosys-synthesis-synth_splitnets}	bool	Splits multi-bit nets into single-bit nets. Easier to trace but may not be supported by all tools.	True	
SYNTH_SIZING{#var-yosys-synthesis-synth_sizing}	bool	Enables `abc` cell sizing (instead of buffering).	False	
SYNTH_NO_FLAT{#var-yosys-synthesis-synth_no_flat}	bool	A flag that disables flattening the hierarchy during synthesis, only flattening it after synthesis, mapping and optimizations.	False	
SYNTH_SHARE_RESOURCES{#var-yosys-synthesis-synth_share_resources}	bool	A flag that enables yosys to reduce the number of cells by determining shareable resources and merging them.	True	
SYNTH_ADDER_TYPE{#var-yosys-synthesis-synth_adder_type}	'YOSYS' | 'FA' | 'RCA' | 'CSA'	Adder type to which the $addand$sub operators are mapped to. Possible values are `YOSYS/FA/RCA/CSA`; where `YOSYS` refers to using Yosys internal adder definition, `FA` refers to full-adder structure, `RCA` refers to ripple carry adder structure, and `CSA` refers to carry select adder.	YOSYS	
SYNTH_EXTRA_MAPPING_FILE{#var-yosys-synthesis-synth_extra_mapping_file}	Path?	Points to an extra techmap file for yosys that runs right after yosys `synth` before generic techmap.	None	
SYNTH_PARAMETERS{#var-yosys-synthesis-synth_parameters}	List[str]?	Key-value pairs to be `chparam`ed in Yosys, in the format `key1=value1`.	None	
SYNTH_ELABORATE_ONLY{#var-yosys-synthesis-synth_elaborate_only}	bool	"Elaborate" the design only without attempting any logic mapping. Useful when dealing with structural Verilog netlists.	False	
SYNTH_ELABORATE_FLATTEN{#var-yosys-synthesis-synth_elaborate_flatten}	bool	If `SYNTH_ELABORATE_ONLY` is specified, this variable controls whether or not the top level should be flattened.	True	
VERILOG_FILES{#var-yosys-synthesis-verilog_files}	List[Path]	The paths of the design's Verilog files.	None	
VERILOG_DEFINES{#var-yosys-synthesis-verilog_defines}	List[str]?	Preprocessor defines for input Verilog files.	None	

VERILOG_POWER_DEFINE{#var-yosys-synthesis-verilog_power_define}	str	Specifies the name of the define used to guard power and ground connections in the input RTL.	USE_POWER_PINS
VERILOG_INCLUDE_DIRS{#var-yosys-synthesis-verilog_include_dirs}	List[str]?	Specifies the Verilog `include` directories.	None
USE_SYNLIG{#var-yosys-synthesis-use_synlig}	bool	Use the Synlig plugin to process files, which has better SystemVerilog parsing capabilities but may not be compatible with all Yosys commands and attributes.	False
SYNLIG_DEFER{#var-yosys-synthesis-synlig_defer}	bool	Uses -defer flag when reading files the Synlig plugin, which may improve performance by reading each file separately, but is experimental.	False

- Then run it. Note you can pass step-specific configs using Python keyword arguments.

Synthesis

We need to start by converting our high-level Verilog to one that just shows the connections between small silicon patterns called "standard cells" in process called Synthesis. We can do this by passing the Verilog files as a configuration variable to `Yosys.Synthesis` as follows, then running it.

As this is the first step, we need to create an empty state and pass it to it.

```
from openlane.state import State

synthesis = Synthesis(
    VERILOG_FILES=["./MIMO.v"],
    state_in=State(),
)
synthesis.start()
```

```
──────────────────────────────────────────────────────── Synthesis ────────────────────────────────────────────────────────
[16:11:58] VERBOSE  Running 'Yosys.Synthesis'…                                                          step.py:1088
[16:11:58] VERBOSE  Logging subprocess to openlane_run/90-yosys-synthesis/yosys-synthesis.log…          step.py:1268

/-----------------------------------------------------------------------------\
|                                                                             |
|  yosys -- Yosys Open SYnthesis Suite                                        |
|                                                                             |
|  Copyright (C) 2012 - 2020  Claire Xenia Wolf <claire@yosyshq.com>          |
|                                                                             |
|  Permission to use, copy, modify, and/or distribute this software for any  |
|  purpose with or without fee is hereby granted, provided that the above    |
|  copyright notice and this permission notice appear in all copies.          |
|                                                                             |
|  THE SOFTWARE IS PROVIDED "AS IS" AND THE AUTHOR DISCLAIMS ALL WARRANTIES  |
|  WITH REGARD TO THIS SOFTWARE INCLUDING ALL IMPLIED WARRANTIES OF           |
|  MERCHANTABILITY AND FITNESS. IN NO EVENT SHALL THE AUTHOR BE LIABLE FOR    |
|  ANY SPECIAL, DIRECT, INDIRECT, OR CONSEQUENTIAL DAMAGES OR ANY DAMAGES     |
|  WHATSOEVER RESULTING FROM LOSS OF USE, DATA OR PROFITS, WHETHER IN AN      |
|  ACTION OF CONTRACT, NEGLIGENCE OR OTHER TORTIOUS ACTION, ARISING OUT OF    |
|  OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THIS SOFTWARE.             |
|                                                                             |
\-----------------------------------------------------------------------------/

Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)

Loaded SDC plugin
[TCL: yosys -import] Command name collision: found pre-existing command `cd' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `eval' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `exec' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `read' -> skip.
[TCL: yosys -import] Command name collision: found pre-existing command `trace' -> skip.

1. Executing Liberty frontend: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib
Imported 428 cell types from liberty file.

2. Executing Verilog-2005 frontend: ./MIMO.v
Parsing SystemVerilog input from `./MIMO.v' to AST representation.
Generating RTLIL representation for module `\MIMO'.
Generating RTLIL representation for module `\mem'.
Generating RTLIL representation for module `\relu'.
Generating RTLIL representation for module `\neuron'.
Generating RTLIL representation for module `\sadder'.
Generating RTLIL representation for module `\smul'.
Generating RTLIL representation for module `\half_adder'.
Generating RTLIL representation for module `\full_adder'.
Successfully finished Verilog frontend.

3. Executing HIERARCHY pass (managing design hierarchy).

3.1. Analyzing design hierarchy..
Top module:  \MIMO
Used module:     \relu
Used module:     \neuron
Used module:         \sadder
Used module:         \smul
Used module:             \half_adder
Used module:             \full_adder
Used module:     \mem

3.2. Analyzing design hierarchy..
Top module:  \MIMO
Used module:     \relu
Used module:     \neuron
Used module:         \sadder
Used module:         \smul
Used module:             \half_adder
Used module:             \full_adder
Used module:     \mem
Removed 0 unused modules.
Mapping positional arguments of cell smul.HA8 (half_adder).
Mapping positional arguments of cell smul.HA7 (half_adder).
Mapping positional arguments of cell smul.HA6 (half_adder).
Mapping positional arguments of cell smul.HA5 (half_adder).
Mapping positional arguments of cell smul.HA4 (half_adder).
Mapping positional arguments of cell smul.FA7 (full_adder).
Mapping positional arguments of cell smul.FA6 (full_adder).
Mapping positional arguments of cell smul.FA5 (full_adder).
Mapping positional arguments of cell smul.FA4 (full_adder).
Mapping positional arguments of cell smul.FA3 (full_adder).
Mapping positional arguments of cell smul.FA2 (full_adder).
Mapping positional arguments of cell smul.FA1 (full_adder).
Mapping positional arguments of cell smul.HA3 (half_adder).
Mapping positional arguments of cell smul.HA2 (half_adder).
Mapping positional arguments of cell smul.HA1 (half_adder).
Mapping positional arguments of cell neuron.s2 (sadder).
Mapping positional arguments of cell neuron.s1 (smul).
Mapping positional arguments of cell MIMO.R1 (relu).
Mapping positional arguments of cell MIMO.n4 (neuron).
Mapping positional arguments of cell MIMO.m4 (mem).
Mapping positional arguments of cell MIMO.n3 (neuron).
Mapping positional arguments of cell MIMO.m3 (mem).
Mapping positional arguments of cell MIMO.n2 (neuron).
Mapping positional arguments of cell MIMO.m2 (mem).
Mapping positional arguments of cell MIMO.n1 (neuron).
Mapping positional arguments of cell MIMO.m1 (mem).
Renaming module MIMO to MIMO.

4. Generating Graphviz representation of design.
Writing dot description to `/content/openlane_run/90-yosys-synthesis/hierarchy.dot'.
Dumping module MIMO to page 1.

5. Executing TRIBUF pass.

6. Executing HIERARCHY pass (managing design hierarchy).

6.1. Analyzing design hierarchy..
Top module:  \MIMO
Used module:     \relu
Used module:     \neuron
Used module:         \sadder
Used module:         \smul
Used module:             \half_adder
Used module:             \full_adder
Used module:     \mem

6.2. Analyzing design hierarchy..
Top module:  \MIMO
Used module:     \relu
Used module:     \neuron
Used module:         \sadder
Used module:         \smul
Used module:             \half_adder
Used module:             \full_adder
Used module:     \mem
Removed 0 unused modules.
```

```
7. Executing PROC_CLEAN pass (remove empty switches from decision trees).
Cleaned up 0 empty switches.

8. Executing PROC_RMDEAD pass (remove dead branches from decision trees).
Marked 2 switch rules as full_case in process $proc$./MIMO.v:91$3 in module relu.
Marked 1 switch rules as full_case in process $proc$./MIMO.v:53$2 in module mem.
Removed a total of 0 dead cases.

9. Executing PROC_PRUNE pass (remove redundant assignments in processes).
Removed 0 redundant assignments.
Promoted 10 assignments to connections.

10. Executing PROC_INIT pass (extract init attributes).

11. Executing PROC_ARST pass (detect async resets in processes).

12. Executing PROC_ROM pass (convert switches to ROMs).
Converted 0 switches.
<suppressed ~3 debug messages>

13. Executing PROC_MUX pass (convert decision trees to multiplexers).
Creating decoders for process `\relu.$proc$./MIMO.v:0$10'.
Creating decoders for process `\relu.$proc$./MIMO.v:91$3'.
1/3: $2\data_temp2[7:0]
2/3: $1\data_temp1[7:0]
3/3: $1\data_temp2[7:0]
Creating decoders for process `\mem.$proc$./MIMO.v:53$2'.
1/1: $1\weight_value[3:0]

14. Executing PROC_DLATCH pass (convert process syncs to latches).
No latch inferred for signal `\relu.\inputs[0]' from process `\relu.$proc$./MIMO.v:0$10'.
No latch inferred for signal `\relu.\inputs[1]' from process `\relu.$proc$./MIMO.v:0$10'.
No latch inferred for signal `\relu.\inputs[2]' from process `\relu.$proc$./MIMO.v:0$10'.
No latch inferred for signal `\relu.\inputs[3]' from process `\relu.$proc$./MIMO.v:0$10'.
No latch inferred for signal `\relu.\data_out1' from process `\relu.$proc$./MIMO.v:91$3'.
No latch inferred for signal `\relu.\data_out2' from process `\relu.$proc$./MIMO.v:91$3'.
No latch inferred for signal `\relu.\data_temp1' from process `\relu.$proc$./MIMO.v:91$3'.
No latch inferred for signal `\relu.\data_temp2' from process `\relu.$proc$./MIMO.v:91$3'.
No latch inferred for signal `\relu.\i' from process `\relu.$proc$./MIMO.v:91$3'.
Latch inferred for signal `\mem.\weight_value' from process `\mem.$proc$./MIMO.v:53$2':
$auto$proc_dlatch.cc:427:proc_dlatch$66

15. Executing PROC_DFF pass (convert process syncs to FFs).

16. Executing PROC_MEMWR pass (convert process memory writes to cells).

17. Executing PROC_CLEAN pass (remove empty switches from decision trees).
Removing empty process `relu.$proc$./MIMO.v:0$10'.
Found and cleaned up 2 empty switches in `\relu.$proc$./MIMO.v:91$3'.
Removing empty process `relu.$proc$./MIMO.v:91$3'.
Found and cleaned up 1 empty switch in `\mem.$proc$./MIMO.v:53$2'.
Removing empty process `mem.$proc$./MIMO.v:53$2'.
Cleaned up 3 empty switches.

18. Executing CHECK pass (checking for obvious problems).
Checking module MIMO...
Checking module half_adder...
Checking module smul...
Checking module sadder...
Checking module neuron...
Checking module relu...
Checking module mem...
Checking module full_adder...
Found and reported 0 problems.

19. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.
Optimizing module half_adder.
Optimizing module smul.
Optimizing module sadder.
Optimizing module neuron.
Optimizing module relu.
Optimizing module mem.
<suppressed ~13 debug messages>
Optimizing module full_adder.

20. Executing FLATTEN pass (flatten design).
Deleting now unused module half_adder.
Deleting now unused module smul.
Deleting now unused module sadder.
Deleting now unused module neuron.
Deleting now unused module relu.
Deleting now unused module mem.
Deleting now unused module full_adder.
<suppressed ~26 debug messages>

21. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.
<suppressed ~132 debug messages>

22. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..
Removed 93 unused cells and 523 unused wires.
<suppressed ~196 debug messages>

23. Executing OPT pass (performing simple optimizations).

23.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

23.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
<suppressed ~3 debug messages>
Removed a total of 1 cells.

23.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MIMO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
dead port 1/2 on $mux $flatten\R1.$procmux$47.
Removed 1 multiplexer ports.
<suppressed ~4 debug messages>

23.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MIMO.
Performed a total of 0 changes.

23.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

23.6. Executing OPT_DFF pass (perform DFF optimizations).
Handling always-active ARST on $flatten\m3.$auto$proc_dlatch.cc:427:proc_dlatch$66 ($dlatch) from module MIMO
(changing to const driver).
Handling always-active ARST on $flatten\m2.$auto$proc_dlatch.cc:427:proc_dlatch$66 ($dlatch) from module MIMO
(changing to const driver).
Handling always-active ARST on $flatten\m1.$auto$proc_dlatch.cc:427:proc_dlatch$66 ($dlatch) from module MIMO
```

```
(changing to const driver).

23.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..
Removed 0 unused cells and 29 unused wires.
<suppressed ~28 debug messages>

23.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.
<suppressed ~152 debug messages>

23.9. Rerunning OPT passes. (Maybe there is more to do..)

23.10. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MIMO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

23.11. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MIMO.
Performed a total of 0 changes.

23.12. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
<suppressed ~9 debug messages>
Removed a total of 3 cells.

23.13. Executing OPT_DFF pass (perform DFF optimizations).

23.14. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..
Removed 0 unused cells and 86 unused wires.
<suppressed ~1 debug messages>

23.15. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

23.16. Rerunning OPT passes. (Maybe there is more to do..)

23.17. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MIMO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

23.18. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MIMO.
Performed a total of 0 changes.

23.19. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

23.20. Executing OPT_DFF pass (perform DFF optimizations).

23.21. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..

23.22. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

23.23. Finished OPT passes. (There is nothing left to do.)

24. Executing FSM pass (extract and optimize FSM).

24.1. Executing FSM_DETECT pass (finding FSMs in design).

24.2. Executing FSM_EXTRACT pass (extracting FSM from design).

24.3. Executing FSM_OPT pass (simple optimizations of FSMs).

24.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..

24.5. Executing FSM_OPT pass (simple optimizations of FSMs).

24.6. Executing FSM_RECODE pass (re-assigning FSM state encoding).

24.7. Executing FSM_INFO pass (dumping all available information on FSM cells).

24.8. Executing FSM_MAP pass (mapping FSMs to basic logic).

25. Executing OPT pass (performing simple optimizations).

25.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

25.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

25.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MIMO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

25.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MIMO.
Performed a total of 0 changes.

25.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

25.6. Executing OPT_DFF pass (perform DFF optimizations).

25.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..

25.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

25.9. Finished OPT passes. (There is nothing left to do.)

26. Executing WREDUCE pass (reducing word size of cells).
Removed top 6 bits (of 8) from port B of cell MIMO.$flatten\n1.\s2.$add$./MIMO.v:132$11 ($add).
Removed top 4 bits (of 8) from port Y of cell MIMO.$flatten\n1.\s2.$add$./MIMO.v:132$11 ($add).
Removed top 4 bits (of 8) from port A of cell MIMO.$flatten\n1.\s2.$add$./MIMO.v:132$11 ($add).
Removed top 6 bits (of 8) from port B of cell MIMO.$flatten\n2.\s2.$add$./MIMO.v:132$11 ($add).
Removed top 4 bits (of 8) from port Y of cell MIMO.$flatten\n2.\s2.$add$./MIMO.v:132$11 ($add).
```

```
Removed top 4 bits (of 8) from port Y of cell MIMO.$flatten\n2.\s2.$add$./MIMO.v:132$11 ($add).
Removed top 4 bits (of 8) from port A of cell MIMO.$flatten\n2.\s2.$add$./MIMO.v:132$11 ($add).
Removed top 6 bits (of 8) from port B of cell MIMO.$flatten\n3.\s2.$add$./MIMO.v:132$11 ($add).
Removed top 4 bits (of 8) from port Y of cell MIMO.$flatten\n3.\s2.$add$./MIMO.v:132$11 ($add).
Removed top 4 bits (of 8) from port A of cell MIMO.$flatten\n3.\s2.$add$./MIMO.v:132$11 ($add).
Removed top 4 bits (of 8) from port B of cell MIMO.$flatten\R1.$gt$./MIMO.v:101$9 ($gt).
Removed top 4 bits (of 8) from port B of cell MIMO.$flatten\R1.$gt$./MIMO.v:97$8 ($gt).
Removed cell MIMO.$flatten\n1.\s1.\HA6.$xor$./MIMO.v:172$34 ($xor).
Removed cell MIMO.$flatten\n1.\s1.\HA8.$xor$./MIMO.v:172$34 ($xor).
Removed cell MIMO.$flatten\n1.\s1.\FA7.$xor$./MIMO.v:179$37 ($xor).
Removed cell MIMO.$flatten\n1.\s1.\HA8.$and$./MIMO.v:173$35 ($and).
Removed cell MIMO.$flatten\n2.\s1.\HA6.$xor$./MIMO.v:172$34 ($xor).
Removed cell MIMO.$flatten\n2.\s1.\HA8.$xor$./MIMO.v:172$34 ($xor).
Removed cell MIMO.$flatten\n2.\s1.\FA7.$xor$./MIMO.v:179$37 ($xor).
Removed cell MIMO.$flatten\n2.\s1.\HA8.$and$./MIMO.v:173$35 ($and).
Removed cell MIMO.$flatten\n3.\s1.\HA6.$xor$./MIMO.v:172$34 ($xor).
Removed cell MIMO.$flatten\n3.\s1.\HA8.$xor$./MIMO.v:172$34 ($xor).
Removed cell MIMO.$flatten\n3.\s1.\FA7.$xor$./MIMO.v:179$37 ($xor).
Removed cell MIMO.$flatten\n3.\s1.\HA8.$and$./MIMO.v:173$35 ($and).

27. Executing PEEPOPT pass (run peephole optimizers).

28. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..
Removed 66 unused cells and 144 unused wires.
<suppressed ~180 debug messages>

29. Executing ALUMACC pass (create $alu and $macc cells).
Extracting $alu and $macc cells in module MIMO:
creating $macc model for $flatten\n1.\s2.$add$./MIMO.v:132$11 ($add).
creating $macc model for $flatten\n2.\s2.$add$./MIMO.v:132$11 ($add).
creating $macc model for $flatten\n3.\s2.$add$./MIMO.v:132$11 ($add).
creating $alu model for $macc $flatten\n3.\s2.$add$./MIMO.v:132$11.
creating $alu model for $macc $flatten\n2.\s2.$add$./MIMO.v:132$11.
creating $alu model for $macc $flatten\n1.\s2.$add$./MIMO.v:132$11.
creating $alu model for $flatten\R1.$gt$./MIMO.v:101$9 ($gt): new $alu
creating $alu model for $flatten\R1.$gt$./MIMO.v:93$4 ($gt): new $alu
creating $alu model for $flatten\R1.$gt$./MIMO.v:97$8 ($gt): new $alu
creating $alu cell for $flatten\R1.$gt$./MIMO.v:97$8: $auto$alumacc.cc:485:replace_alu$150
creating $alu cell for $flatten\R1.$gt$./MIMO.v:93$4: $auto$alumacc.cc:485:replace_alu$157
creating $alu cell for $flatten\R1.$gt$./MIMO.v:101$9: $auto$alumacc.cc:485:replace_alu$170
creating $alu cell for $flatten\n1.\s2.$add$./MIMO.v:132$11: $auto$alumacc.cc:485:replace_alu$177
creating $alu cell for $flatten\n2.\s2.$add$./MIMO.v:132$11: $auto$alumacc.cc:485:replace_alu$180
creating $alu cell for $flatten\n3.\s2.$add$./MIMO.v:132$11: $auto$alumacc.cc:485:replace_alu$183
created 6 $alu and 0 $macc cells.

30. Executing SHARE pass (SAT-based resource sharing).

31. Executing OPT pass (performing simple optimizations).

31.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.
<suppressed ~2 debug messages>

31.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

31.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MIMO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

31.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MIMO.
Performed a total of 0 changes.

31.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

31.6. Executing OPT_DFF pass (perform DFF optimizations).

31.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..
Removed 1 unused cells and 4 unused wires.
<suppressed ~2 debug messages>

31.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

31.9. Rerunning OPT passes. (Maybe there is more to do..)

31.10. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MIMO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

31.11. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MIMO.
Performed a total of 0 changes.

31.12. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

31.13. Executing OPT_DFF pass (perform DFF optimizations).

31.14. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..

31.15. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

31.16. Finished OPT passes. (There is nothing left to do.)

32. Executing MEMORY pass.

32.1. Executing OPT_MEM pass (optimize memories).
Performed a total of 0 transformations.

32.2. Executing OPT_MEM_PRIORITY pass (removing unnecessary memory write priority relations).
Performed a total of 0 transformations.

32.3. Executing OPT_MEM_FEEDBACK pass (finding memory read-to-write feedback paths).

32.4. Executing MEMORY_BMUX2ROM pass (converting muxes to ROMs).

32.5. Executing MEMORY_DFF pass (merging $dff cells to $memrd).

32.6. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..
```

```
32.7. Executing MEMORY_SHARE pass (consolidating $memrd/$memwr cells).

32.8. Executing OPT_MEM_WIDEN pass (optimize memories where all ports are wide).
Performed a total of 0 transformations.

32.9. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..

32.10. Executing MEMORY_COLLECT pass (generating $mem cells).

33. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..

34. Executing OPT pass (performing simple optimizations).

34.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.
<suppressed ~24 debug messages>

34.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

34.3. Executing OPT_DFF pass (perform DFF optimizations).

34.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..
Removed 0 unused cells and 2 unused wires.
<suppressed ~2 debug messages>

34.5. Finished fast OPT passes.

35. Executing MEMORY_MAP pass (converting memories to logic and flip-flops).

36. Executing OPT pass (performing simple optimizations).

36.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

36.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

36.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MIMO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

36.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MIMO.
Consolidated identical input bits for $mux cell $flatten\R1.$procmux$44:
Old ports: A={ $flatten\R1.$ternary$./MIMO.v:94$7_Y [3] $flatten\R1.$ternary$./MIMO.v:94$7_Y [3]
$flatten\R1.$ternary$./MIMO.v:94$7_Y [3] $flatten\R1.$ternary$./MIMO.v:94$7_Y [3]
$flatten\R1.$ternary$./MIMO.v:94$7_Y }, B={ \n3.s1.FA4.s \n3.s1.FA4.s \n3.s1.FA4.s \n3.s1.FA4.s \n3.s1.FA4.s \in3
[1:0] 1'1 }, Y=$flatten\R1.$2\data_temp2[7:0]
New ports: A=$flatten\R1.$ternary$./MIMO.v:94$7_Y, B={ \n3.s1.FA4.s \in3 [1:0] 1'1 },
Y=$flatten\R1.$2\data_temp2[7:0] [3:0]
New connections: $flatten\R1.$2\data_temp2[7:0] [7:4] = { $flatten\R1.$2\data_temp2[7:0] [3]
$flatten\R1.$2\data_temp2[7:0] [3] $flatten\R1.$2\data_temp2[7:0] [3] $flatten\R1.$2\data_temp2[7:0] [3] }
Consolidated identical input bits for $mux cell $flatten\R1.$procmux$50:
Old ports: A={ $flatten\R1.$ternary$./MIMO.v:93$5_Y [3] $flatten\R1.$ternary$./MIMO.v:93$5_Y [3]
$flatten\R1.$ternary$./MIMO.v:93$5_Y [3] $flatten\R1.$ternary$./MIMO.v:93$5_Y [3]
$flatten\R1.$ternary$./MIMO.v:93$5_Y }, B={ \n3.s1.FA4.s \n3.s1.FA4.s \n3.s1.FA4.s \n3.s1.FA4.s \n3.s1.FA4.s \in3
[1:0] 1'1 }, Y=\R1.data_out1
New ports: A=$flatten\R1.$ternary$./MIMO.v:93$5_Y, B={ \n3.s1.FA4.s \in3 [1:0] 1'1 }, Y=\R1.data_out1 [3:0]
New connections: \R1.data_out1 [7:4] = { \R1.data_out1 [3] \R1.data_out1 [3] \R1.data_out1 [3] \R1.data_out1 [3] }
Optimizing cells in module \MIMO.
Consolidated identical input bits for $mux cell $flatten\R1.$procmux$53:
Old ports: A=$flatten\R1.$2\data_temp2[7:0], B={ $flatten\R1.$ternary$./MIMO.v:93$5_Y [3]
$flatten\R1.$ternary$./MIMO.v:93$5_Y [3] $flatten\R1.$ternary$./MIMO.v:93$5_Y [3]
$flatten\R1.$ternary$./MIMO.v:93$5_Y [3] $flatten\R1.$ternary$./MIMO.v:93$5_Y }, Y=\R1.data_out2
New ports: A=$flatten\R1.$2\data_temp2[7:0] [3:0], B=$flatten\R1.$ternary$./MIMO.v:93$5_Y, Y=\R1.data_out2 [3:0]
New connections: \R1.data_out2 [7:4] = { \R1.data_out2 [3] \R1.data_out2 [3] \R1.data_out2 [3] \R1.data_out2 [3] }
Optimizing cells in module \MIMO.
Performed a total of 3 changes.

36.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

36.6. Executing OPT_SHARE pass.

36.7. Executing OPT_DFF pass (perform DFF optimizations).

36.8. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..

36.9. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

36.10. Rerunning OPT passes. (Maybe there is more to do..)

36.11. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MIMO..
Creating internal representation of mux trees.
Evaluating internal representation of mux trees.
Analyzing evaluation results.
Removed 0 multiplexer ports.
<suppressed ~4 debug messages>

36.12. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MIMO.
Performed a total of 0 changes.

36.13. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

36.14. Executing OPT_SHARE pass.

36.15. Executing OPT_DFF pass (perform DFF optimizations).

36.16. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..

36.17. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

36.18. Finished OPT passes. (There is nothing left to do.)

37. Executing TECHMAP pass (map to technology primitives).

37.1. Executing Verilog-2005 frontend:
/nix/store/sx2v0i73mn1ih2z1nk61pm9n5gigpidy-yosys/bin/../share/yosys/techmap.v
```

```
Parsing Verilog input from `/nix/store/sx2v0i73mn1ih2z1nk61pm9n5gjgpidy-yosys/bin/../share/yosys/techmap.v' to AST
representation.
Generating RTLIL representation for module `\_90_simplemap_bool_ops'.
Generating RTLIL representation for module `\_90_simplemap_reduce_ops'.
Generating RTLIL representation for module `\_90_simplemap_logic_ops'.
Generating RTLIL representation for module `\_90_simplemap_compare_ops'.
Generating RTLIL representation for module `\_90_simplemap_various'.
Generating RTLIL representation for module `\_90_simplemap_registers'.
Generating RTLIL representation for module `\_90_shift_ops_shr_shl_sshl_sshr'.
Generating RTLIL representation for module `\_90_shift_shiftx'.
Generating RTLIL representation for module `\_90_fa'.
Generating RTLIL representation for module `\_90_lcu'.
Generating RTLIL representation for module `\_90_alu'.
Generating RTLIL representation for module `\_90_macc'.
Generating RTLIL representation for module `\_90_alumacc'.
Generating RTLIL representation for module `\$__div_mod_u'.
Generating RTLIL representation for module `\$__div_mod_trunc'.
Generating RTLIL representation for module `\_90_div'.
Generating RTLIL representation for module `\_90_mod'.
Generating RTLIL representation for module `\$__div_mod_floor'.
Generating RTLIL representation for module `\_90_divfloor'.
Generating RTLIL representation for module `\_90_modfloor'.
Generating RTLIL representation for module `\_90_pow'.
Generating RTLIL representation for module `\_90_pmux'.
Generating RTLIL representation for module `\_90_demux'.
Generating RTLIL representation for module `\_90_lut'.
Successfully finished Verilog frontend.

37.2. Continuing TECHMAP pass.
Using extmapper simplemap for cells of type $reduce_and.
Using extmapper simplemap for cells of type $or.
Using extmapper simplemap for cells of type $xor.
Using template $paramod$82dbbf18339f9c177cf323a2d12653b430c46f4d\_90_alu for cells of type $alu.
Using extmapper simplemap for cells of type $not.
Using extmapper simplemap for cells of type $and.
Using template $paramod$b68c83d65b53df4a22df31900ec7ed06cdd69e29\_90_alu for cells of type $alu.
Using extmapper simplemap for cells of type $mux.
Using template $paramod\_90_lcu\WIDTH=32'00000000000000000000000000000100 for cells of type $lcu.
Using extmapper simplemap for cells of type $pos.
No more expansions possible.
<suppressed ~356 debug messages>

38. Executing OPT pass (performing simple optimizations).

38.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.
<suppressed ~74 debug messages>

38.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
<suppressed ~24 debug messages>
Removed a total of 8 cells.

38.3. Executing OPT_DFF pass (perform DFF optimizations).

38.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..
Removed 18 unused cells and 146 unused wires.
<suppressed ~19 debug messages>

38.5. Finished fast OPT passes.

39. Executing ABC pass (technology mapping using ABC).

39.1. Extracting gate netlist of module `\MIMO' to `<abc-temp-dir>/input.blif'..
Extracted 118 gates and 130 wires to a netlist network with 11 inputs and 8 outputs.

39.1.1. Executing ABC.
Running ABC command: "/nix/store/wq2q0njg3sx8wvj2akz7x1qxwyrv9xlr-yosys-abc/bin/abc" -s -f
<abc-temp-dir>/abc.script 2>&1
ABC: ABC command line: "source <abc-temp-dir>/abc.script".
ABC:
ABC: + read_blif <abc-temp-dir>/input.blif
ABC: + read_library <abc-temp-dir>/stdcells.genlib
ABC: Entered genlib library with 13 gates from file "<abc-temp-dir>/stdcells.genlib".
ABC: + strash
ABC: + dretime
ABC: + map
ABC: + write_blif <abc-temp-dir>/output.blif

39.1.2. Re-integrating ABC results.
ABC RESULTS:               AND cells:        4
ABC RESULTS:              NAND cells:        2
ABC RESULTS:             ORNOT cells:        4
ABC RESULTS:               XOR cells:       20
ABC RESULTS:              XNOR cells:        8
ABC RESULTS:               NOT cells:       11
ABC RESULTS:            ANDNOT cells:       27
ABC RESULTS:                OR cells:       10
ABC RESULTS:               MUX cells:       17
ABC RESULTS:        internal signals:      111
ABC RESULTS:           input signals:       11
ABC RESULTS:          output signals:        8
Removing temp directory.

40. Executing OPT pass (performing simple optimizations).

40.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

40.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

40.3. Executing OPT_DFF pass (perform DFF optimizations).

40.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..
Removed 0 unused cells and 103 unused wires.
<suppressed ~33 debug messages>

40.5. Finished fast OPT passes.

41. Executing HIERARCHY pass (managing design hierarchy).

41.1. Analyzing design hierarchy..
Top module:  \MIMO

41.2. Analyzing design hierarchy..
Top module:  \MIMO
Removed 0 unused modules.

42. Printing statistics.

=== MIMO ===

Number of wires:                 291
Number of wire bits:             717
```

```
   Number of wire bits:          717
   Number of public wires:       196
   Number of public wire bits:   622
   Number of memories:             0
   Number of memory bits:          0
   Number of processes:            0
   Number of cells:              103
   $_ANDNOT_                      27
   $_AND_                          4
   $_MUX_                         17
   $_NAND_                         2
   $_NOT_                         11
   $_ORNOT_                        4
   $_OR_                          10
   $_XNOR_                         8
   $_XOR_                         20

43. Executing CHECK pass (checking for obvious problems).
Checking module MIMO...
Found and reported 0 problems.

44. Generating Graphviz representation of design.
Writing dot description to `/content/openlane_run/90-yosys-synthesis/primitive_techmap.dot'.
Dumping module MIMO to page 1.

45. Executing OPT pass (performing simple optimizations).

45.1. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

45.2. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

45.3. Executing OPT_MUXTREE pass (detect dead branches in mux trees).
Running muxtree optimizer on module \MIMO..
Creating internal representation of mux trees.
No muxes found in this module.
Removed 0 multiplexer ports.

45.4. Executing OPT_REDUCE pass (consolidate $*mux and $reduce_* inputs).
Optimizing cells in module \MIMO.
Performed a total of 0 changes.

45.5. Executing OPT_MERGE pass (detect identical cells).
Finding identical cells in module `\MIMO'.
Removed a total of 0 cells.

45.6. Executing OPT_DFF pass (perform DFF optimizations).

45.7. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..

45.8. Executing OPT_EXPR pass (perform const folding).
Optimizing module MIMO.

45.9. Finished OPT passes. (There is nothing left to do.)

46. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..
Removed 0 unused cells and 190 unused wires.
<suppressed ~190 debug messages>
{
"creator": "Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)",
"invocation": "stat -json -liberty /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib ",
"modules": {
"\\MIMO": {
"num_wires":         101,
"num_wire_bits":     143,
"num_pub_wires":     6,
"num_pub_wire_bits": 48,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         103,
"num_cells_by_type": {
"$_ANDNOT_": 27,
"$_AND_": 4,
"$_MUX_": 17,
"$_NAND_": 2,
"$_NOT_": 11,
"$_ORNOT_": 4,
"$_OR_": 10,
"$_XNOR_": 8,
"$_XOR_": 20
}
}
},
"design": {
"num_wires":         101,
"num_wire_bits":     143,
"num_pub_wires":     6,
"num_pub_wire_bits": 48,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         103,
"num_cells_by_type": {
"$_ANDNOT_": 27,
"$_AND_": 4,
"$_MUX_": 17,
"$_NAND_": 2,
"$_NOT_": 11,
"$_ORNOT_": 4,
"$_OR_": 10,
"$_XNOR_": 8,
"$_XOR_": 20
}
}
}

47. Printing statistics.

=== MIMO ===

   Number of wires:               101
   Number of wire bits:           143
   Number of public wires:          6
   Number of public wire bits:     48
   Number of memories:              0
   Number of memory bits:           0
   Number of processes:             0
   Number of cells:               103
   $_ANDNOT_                      27
   $_AND_                          4
   $_MUX_                         17
   $_NAND_                         2
   $_NOT_                         11
```

```
$_ORNOT_                          4
$_OR_                            10
$_XNOR_                           8
$_XOR_                           20

Area for cell type $_NOT_ is unknown!
Area for cell type $_AND_ is unknown!
Area for cell type $_NAND_ is unknown!
Area for cell type $_OR_ is unknown!
Area for cell type $_XOR_ is unknown!
Area for cell type $_XNOR_ is unknown!
Area for cell type $_ANDNOT_ is unknown!
Area for cell type $_ORNOT_ is unknown!
Area for cell type $_MUX_ is unknown!

mapping tbuf
[INFO] Applying tri-state buffer mapping from
'/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tribuff_map.v'...

48. Executing TECHMAP pass (map to technology primitives).

48.1. Executing Verilog-2005 frontend: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tribuff_map.v
Parsing Verilog input from `/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/tribuff_map.v' to AST
representation.
Generating RTLIL representation for module `\$_TBUF_'.
Successfully finished Verilog frontend.

48.2. Continuing TECHMAP pass.
No more expansions possible.
<suppressed ~3 debug messages>

49. Executing SIMPLEMAP pass (map simple cells to gate primitives).
[INFO] Applying latch mapping from '/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/latch_map.v'...

50. Executing TECHMAP pass (map to technology primitives).

50.1. Executing Verilog-2005 frontend: /root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/latch_map.v
Parsing Verilog input from `/root/.volare/sky130A/libs.tech/openlane/sky130_fd_sc_hd/latch_map.v' to AST
representation.
Generating RTLIL representation for module `\$_DLATCH_P_'.
Generating RTLIL representation for module `\$_DLATCH_N_'.
Successfully finished Verilog frontend.

50.2. Continuing TECHMAP pass.
No more expansions possible.
<suppressed ~4 debug messages>

51. Executing SIMPLEMAP pass (map simple cells to gate primitives).

52. Executing DFFLIBMAP pass (mapping DFF cells to sequential cells from liberty file).
cell sky130_fd_sc_hd__dfxtp_2 (noninv, pins=3, area=21.27) is a direct match for cell type $_DFF_P_.
cell sky130_fd_sc_hd__dfrtp_2 (noninv, pins=4, area=26.28) is a direct match for cell type $_DFF_PN0_.
cell sky130_fd_sc_hd__dfstp_2 (noninv, pins=4, area=26.28) is a direct match for cell type $_DFF_PN1_.
cell sky130_fd_sc_hd__dfbbn_2 (noninv, pins=6, area=35.03) is a direct match for cell type $_DFFSR_NNN_.
final dff cell mappings:
unmapped dff cell: $_DFF_N_
\sky130_fd_sc_hd__dfxtp_2 _DFF_P_ (.CLK( C), .D( D), .Q( Q));
unmapped dff cell: $_DFF_NN0_
unmapped dff cell: $_DFF_NN1_
unmapped dff cell: $_DFF_NP0_
unmapped dff cell: $_DFF_NP1_
\sky130_fd_sc_hd__dfrtp_2 _DFF_PN0_ (.CLK( C), .D( D), .Q( Q), .RESET_B( R));
\sky130_fd_sc_hd__dfstp_2 _DFF_PN1_ (.CLK( C), .D( D), .Q( Q), .SET_B( R));
unmapped dff cell: $_DFF_PP0_
unmapped dff cell: $_DFF_PP1_
\sky130_fd_sc_hd__dfbbn_2 _DFFSR_NNN_ (.CLK_N( C), .D( D), .Q( Q), .Q_N(~Q), .RESET_B( R), .SET_B( S));
unmapped dff cell: $_DFFSR_NNP_
unmapped dff cell: $_DFFSR_NPN_
unmapped dff cell: $_DFFSR_NPP_
unmapped dff cell: $_DFFSR_PNN_
unmapped dff cell: $_DFFSR_PNP_
unmapped dff cell: $_DFFSR_PPN_
unmapped dff cell: $_DFFSR_PPP_

52.1. Executing DFFLEGALIZE pass (convert FFs to types supported by the target).
Mapping DFF cells in module `\MIMO':
{
"creator": "Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)",
"invocation": "stat -json -liberty /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib ",
"modules": {
"\\MIMO": {
"num_wires":         101,
"num_wire_bits":     143,
"num_pub_wires":     6,
"num_pub_wire_bits": 48,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         103,
"num_cells_by_type": {
"$_ANDNOT_": 27,
"$_AND_": 4,
"$_MUX_": 17,
"$_NAND_": 2,
"$_NOT_": 11,
"$_ORNOT_": 4,
"$_OR_": 10,
"$_XNOR_": 8,
"$_XOR_": 20
}
}
},
"design": {
"num_wires":         101,
"num_wire_bits":     143,
"num_pub_wires":     6,
"num_pub_wire_bits": 48,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         103,
"num_cells_by_type": {
"$_ANDNOT_": 27,
"$_AND_": 4,
"$_MUX_": 17,
"$_NAND_": 2,
"$_NOT_": 11,
"$_ORNOT_": 4,
"$_OR_": 10,
"$_XNOR_": 8,
"$_XOR_": 20
}
}
}

53. Printing statistics.

=== MIMO ===
```

```
Number of wires:                 101
Number of wire bits:             143
Number of public wires:            6
Number of public wire bits:       48
Number of memories:                0
Number of memory bits:             0
Number of processes:               0
Number of cells:                 103
$_ANDNOT_                       27
$_AND_                           4
$_MUX_                          17
$_NAND_                          2
$_NOT_                          11
$_ORNOT_                         4
$_OR_                           10
$_XNOR_                          8
$_XOR_                          20

Area for cell type $_NOT_ is unknown!
Area for cell type $_AND_ is unknown!
Area for cell type $_NAND_ is unknown!
Area for cell type $_OR_ is unknown!
Area for cell type $_XOR_ is unknown!
Area for cell type $_XNOR_ is unknown!
Area for cell type $_ANDNOT_ is unknown!
Area for cell type $_ORNOT_ is unknown!
Area for cell type $_MUX_ is unknown!

[INFO] Using strategy "AREA 0"...

54. Executing ABC pass (technology mapping using ABC).

54.1. Extracting gate netlist of module `\MIMO' to `/tmp/yosys-abc-vHOnJt/input.blif'..
Extracted 103 gates and 114 wires to a netlist network with 11 inputs and 8 outputs.

54.1.1. Executing ABC.
Running ABC command: "/nix/store/wq2q0njg3sx8wvj2akz7x1qxwyrv9xlr-yosys-abc/bin/abc" -s -f
/tmp/yosys-abc-vHOnJt/abc.script 2>&1
ABC: ABC command line: "source /tmp/yosys-abc-vHOnJt/abc.script".
ABC:
ABC: + read_blif /tmp/yosys-abc-vHOnJt/input.blif
ABC: + read_lib -w /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib
ABC: Parsing finished successfully.  Parsing time =     0.25 sec
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfbbn_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfrbp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfrtp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfrtp_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfsbp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfstp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfstp_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfxbp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfxtp_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dfxtp_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtn_1".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtn_2".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtn_4".
ABC: Scl_LibertyReadGenlib() skipped sequential cell "sky130_fd_sc_hd__dlxtp_1".
ABC: Scl_LibertyReadGenlib() skipped three-state cell "sky130_fd_sc_hd__ebufn_2".
ABC: Scl_LibertyReadGenlib() skipped three-state cell "sky130_fd_sc_hd__ebufn_4".
ABC: Scl_LibertyReadGenlib() skipped three-state cell "sky130_fd_sc_hd__ebufn_8".
ABC: Library "sky130_fd_sc_hd__tt_025C_1v80" from "/content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib"
has 175 cells (17 skipped: 14 seq; 3 tri-state; 0 no func; 0 dont_use).  Time =     0.36 sec
ABC: Memory =    9.54 MB. Time =     0.36 sec
ABC: Warning: Detected 2 multi-output gates (for example, "sky130_fd_sc_hd__fa_1").
ABC: + read_constr -v /content/openlane_run/90-yosys-synthesis/synthesis.sdc
ABC: Setting driving cell to be "sky130_fd_sc_hd__inv_2/Y".
ABC: Setting output load to be 33.442001.
ABC: + read_constr /content/openlane_run/90-yosys-synthesis/synthesis.sdc
ABC: + fx
ABC: + mfs
ABC: + strash
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + retime -D -D 10000 -M 5
ABC: + scleanup
ABC: Error: The network is combinational.
ABC: + fraig_store
ABC: + balance
ABC: + fraig_store
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + fraig_store
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + fraig_store
ABC: + balance
ABC: + drw -l
ABC: + drf -l
ABC: + balance
ABC: + drw -l
ABC: + drw -l -z
ABC: + balance
ABC: + drf -l -z
ABC: + drw -l -z
ABC: + balance
ABC: + fraig_store
ABC: + fraig_restore
ABC: + amap -m -Q 0.1 -F 20 -A 20 -C 5000
ABC: + retime -D -D 10000
ABC: + &get -n
ABC: + &st
ABC: + &dch
```

```
ABC: + &dch
ABC: + &nf
ABC: + &put
ABC: +
ABC: + stime -p
ABC: Cannot find the default PI driving cell (sky130_fd_sc_hd__inv_2/Y) in the library.
ABC: WireLoad = "none"  Gates =     71 (  8.5 %)   Cap = 11.5 ff (  3.2 %)   Area =      669.39 ( 85.9 %)   Delay =
2548.77 ps  ( 46.5 %)
ABC: Path  0 --       3 : 0    6 pi                        A =   0.00  Df =   0.0   -0.0 ps  S =   0.0 ps  Cin =
0.0 ff  Cout =  25.6 ff  Cmax =   0.0 ff  G =    0
ABC: Path  1 --      22 : 2    2 sky130_fd_sc_hd__and2b_2  A =   8.76  Df = 190.7   -2.6 ps  S =  42.7 ps  Cin =
1.6 ff  Cout =   4.3 ff  Cmax = 310.4 ff  G =  256
ABC: Path  2 --      23 : 3    1 sky130_fd_sc_hd__o21a_2   A =   8.76  Df = 393.9  -79.6 ps  S =  59.5 ps  Cin =
2.4 ff  Cout =   8.4 ff  Cmax = 294.8 ff  G =  346
ABC: Path  3 --      24 : 2    4 sky130_fd_sc_hd__xnor2_2  A =  16.27  Df = 614.0 -134.7 ps  S = 252.1 ps  Cin =
8.5 ff  Cout =  16.0 ff  Cmax = 121.8 ff  G =  180
ABC: Path  4 --      37 : 5   12 sky130_fd_sc_hd__o221ai_2 A =  15.01  Df = 955.7  -65.6 ps  S = 549.6 ps  Cin =
4.5 ff  Cout =  40.3 ff  Cmax = 128.2 ff  G =  857
ABC: Path  5 --      68 : 3    3 sky130_fd_sc_hd__and3b_2  A =  10.01  Df =1234.8  -37.6 ps  S =  66.8 ps  Cin =
1.5 ff  Cout =   6.5 ff  Cmax = 309.5 ff  G =  413
ABC: Path  6 --      71 : 5    1 sky130_fd_sc_hd__o32a_2   A =  11.26  Df =1519.6 -145.1 ps  S =  58.7 ps  Cin =
2.3 ff  Cout =   4.7 ff  Cmax = 300.3 ff  G =  189
ABC: Path  7 --      75 : 5    3 sky130_fd_sc_hd__o311ai_2 A =  16.27  Df =1871.1 -371.2 ps  S = 346.2 ps  Cin =
4.4 ff  Cout =  11.6 ff  Cmax =  82.4 ff  G =  252
ABC: Path  8 --      76 : 2    6 sky130_fd_sc_hd__and2_2   A =   7.51  Df =2137.6 -376.3 ps  S = 115.8 ps  Cin =
1.5 ff  Cout =  19.1 ff  Cmax = 303.0 ff  G = 1255
ABC: Path  9 --      88 : 3    1 sky130_fd_sc_hd__mux2_1   A =  11.26  Df =2548.8 -322.3 ps  S = 300.1 ps  Cin =
2.3 ff  Cout =  33.4 ff  Cmax = 173.0 ff  G = 1465
ABC: Start-point = pi2 (\in2 [1]).  End-point = po5 (\out_main1 [1]).
ABC: + print_stats -m
ABC: netlist                       : i/o =   11/    8  lat =    0  nd =    71  edge =    194  area =669.48  delay =
9.00  lev = 9
ABC: + write_blif /tmp/yosys-abc-vHOnJt/output.blif

54.1.2. Re-integrating ABC results.
ABC RESULTS:   sky130_fd_sc_hd__xor2_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o21ai_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a22oi_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a2bb2o_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o221ai_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__nand2b_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__xnor2_2 cells:        6
ABC RESULTS:   sky130_fd_sc_hd__o41a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a21bo_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o22a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__nor2_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a31oi_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o31ai_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o211a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__a21boi_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__and2b_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__and3_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__and3b_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__inv_2 cells:        6
ABC RESULTS:   sky130_fd_sc_hd__o32a_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o21a_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__or2_2 cells:        4
ABC RESULTS:   sky130_fd_sc_hd__or3_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o311ai_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o21ba_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__o211ai_2 cells:        1
ABC RESULTS:   sky130_fd_sc_hd__nand3_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__a21oi_2 cells:        7
ABC RESULTS:   sky130_fd_sc_hd__a31o_2 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__a21o_2 cells:        3
ABC RESULTS:   sky130_fd_sc_hd__nand2_2 cells:        5
ABC RESULTS:   sky130_fd_sc_hd__mux2_1 cells:        2
ABC RESULTS:   sky130_fd_sc_hd__and2_2 cells:        2
ABC RESULTS:        internal signals:       95
ABC RESULTS:           input signals:       11
ABC RESULTS:          output signals:        8
Removing temp directory.

55. Executing SETUNDEF pass (replace undef values with defined constants).

56. Executing HILOMAP pass (mapping to constant drivers).

57. Executing SPLITNETS pass (splitting up multi-bit signals).

58. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \MIMO..
Removed 0 unused cells and 130 unused wires.
<suppressed ~1 debug messages>

59. Executing INSBUF pass (insert buffer cells for connected wires).
Add MIMO/$auto$insbuf.cc:97:execute$722: \out_main1 [7] -> \out_main1 [3]
Add MIMO/$auto$insbuf.cc:97:execute$723: \out_main1 [7] -> \out_main1 [4]
Add MIMO/$auto$insbuf.cc:97:execute$724: \out_main1 [7] -> \out_main1 [5]
Add MIMO/$auto$insbuf.cc:97:execute$725: \out_main1 [7] -> \out_main1 [6]
Add MIMO/$auto$insbuf.cc:97:execute$726: \out_main2 [7] -> \out_main2 [3]
Add MIMO/$auto$insbuf.cc:97:execute$727: \out_main2 [7] -> \out_main2 [4]
Add MIMO/$auto$insbuf.cc:97:execute$728: \out_main2 [7] -> \out_main2 [5]
Add MIMO/$auto$insbuf.cc:97:execute$729: \out_main2 [7] -> \out_main2 [6]

60. Executing CHECK pass (checking for obvious problems).
Checking module MIMO...
Found and reported 0 problems.
```


```
{
"creator": "Yosys 0.38 (git sha1 543faed9c8c, clang++ 17.0.6 -fPIC -Os)",
"invocation": "stat -json -liberty /content/openlane_run/tmp/374e7733592e45a48af6f42380ab5c7c.lib ",
"modules": {
"\\MIMO": {
"num_wires":         69,
"num_wire_bits":     111,
"num_pub_wires":     6,
"num_pub_wire_bits": 48,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         95,
"area":              769.488000,
"num_cells_by_type": {
"sky130_fd_sc_hd__a21bo_2": 1,
"sky130_fd_sc_hd__a21boi_2": 2,
"sky130_fd_sc_hd__a21o_2": 3,
"sky130_fd_sc_hd__a21oi_2": 7,
"sky130_fd_sc_hd__a22oi_2": 1,
"sky130_fd_sc_hd__a2bb2o_2": 1,
"sky130_fd_sc_hd__a31o_2": 2,
"sky130_fd_sc_hd__a31oi_2": 1,
"sky130_fd_sc_hd__and2_2": 2,
"sky130_fd_sc_hd__and2b_2": 3,
"sky130_fd_sc_hd__and3_2": 3,
"sky130_fd_sc_hd__and3b_2": 2,
"sky130_fd_sc_hd__buf_2": 8,
"sky130_fd_sc_hd__conb_1": 16,
"sky130_fd_sc_hd__inv_2": 6,
"sky130_fd_sc_hd__mux2_1": 2,
```

```
"sky130_fd_sc_hd__nand2_2": 5,
"sky130_fd_sc_hd__nand2b_2": 2,
"sky130_fd_sc_hd__nand3_2": 2,
"sky130_fd_sc_hd__nor2_2": 1,
"sky130_fd_sc_hd__o211a_2": 1,
"sky130_fd_sc_hd__o211ai_2": 1,
"sky130_fd_sc_hd__o21a_2": 3,
"sky130_fd_sc_hd__o21ai_2": 1,
"sky130_fd_sc_hd__o21ba_2": 1,
"sky130_fd_sc_hd__o221ai_2": 1,
"sky130_fd_sc_hd__o22a_2": 1,
"sky130_fd_sc_hd__o311ai_2": 1,
"sky130_fd_sc_hd__o31ai_2": 1,
"sky130_fd_sc_hd__o32a_2": 1,
"sky130_fd_sc_hd__o41a_2": 1,
"sky130_fd_sc_hd__or2_2": 4,
"sky130_fd_sc_hd__or3_2": 1,
"sky130_fd_sc_hd__xnor2_2": 6,
"sky130_fd_sc_hd__xor2_2": 1
}
}
},
"design": {
"num_wires":         69,
"num_wire_bits":     111,
"num_pub_wires":     6,
"num_pub_wire_bits": 48,
"num_memories":      0,
"num_memory_bits":   0,
"num_processes":     0,
"num_cells":         95,
"area":              769.488000,
"num_cells_by_type": {
"sky130_fd_sc_hd__a21bo_2": 1,
"sky130_fd_sc_hd__a21boi_2": 2,
"sky130_fd_sc_hd__a21o_2": 3,
"sky130_fd_sc_hd__a21oi_2": 7,
"sky130_fd_sc_hd__a22oi_2": 1,
"sky130_fd_sc_hd__a2bb2o_2": 1,
"sky130_fd_sc_hd__a31o_2": 2,
"sky130_fd_sc_hd__a31oi_2": 1,
"sky130_fd_sc_hd__and2_2": 2,
"sky130_fd_sc_hd__and2b_2": 3,
"sky130_fd_sc_hd__and3_2": 3,
"sky130_fd_sc_hd__and3b_2": 2,
"sky130_fd_sc_hd__buf_2": 8,
"sky130_fd_sc_hd__conb_1": 16,
"sky130_fd_sc_hd__inv_2": 6,
"sky130_fd_sc_hd__mux2_1": 2,
"sky130_fd_sc_hd__nand2_2": 5,
"sky130_fd_sc_hd__nand2b_2": 2,
```

```
display(synthesis)
```

Time Elapsed: 14.69s

Views updated:

- Verilog Netlist

Floorplanning

Floorplanning does two things:

- Determines the dimensions of the final chip.
- Creates the "cell placement grid" which placed cells must be aligned to.
  - Each cell in the grid is called a "site." Cells can occupy multiple sites, with the overwhelming majority of cells occupying multiple sites by width, and some standard cell libraries supporting varying heights as well.

> Don't forget- you may call `display_help()` on any Step class to get a full list of configuration variables.

```
Floorplan = Step.factory.get("OpenROAD.Floorplan")

floorplan = Floorplan(state_in=synthesis.state_out)
floorplan.start()
```

```
─────────────────────────────────────── Floorplan Initialization ───────────────────────────────────────
[16:12:13] VERBOSE  Running 'OpenROAD.Floorplan'…                                          step.py:1088
[16:12:13] VERBOSE  Logging subprocess to openlane_run/91-openroad-floorplan/openroad-floorplan.log…  step.py:1268
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading technology LEF file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef'…
[INFO ODB-0227] LEF file: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef, created
13 layers, 25 vias
Reading cell LEF file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef'…
The NOWIREEXTENSIONATPIN statement will be ignored. See file
/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef at line 2.

[INFO ODB-0227] LEF file: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_ef_sc_hd.lef, created 4 library
cells
Reading cell LEF file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef'…
The NOWIREEXTENSIONATPIN statement will be ignored. See file
/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef at line 2.

[INFO ODB-0227] LEF file: /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lef/sky130_fd_sc_hd.lef, created 437
library cells
Reading top-level netlist at '/content/openlane_run/90-yosys-synthesis/MIMO.nl.v'…
Linking design 'MIMO' from netlist…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[16:12:16] WARNING  [STA-0366] port 'clk' not found.                                        openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[16:12:16] WARNING  [STA-0366] port 'clk' not found.                                        openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[16:12:16] WARNING  [STA-0419] transition time can not be specified for virtual clocks.      openroad.py:235
[INFO] Setting timing derate to: 5%
[16:12:16] WARNING  [STA-0450] virtual clock clk can not be propagated.                     openroad.py:235
Using site height: 2.72 and site width: 0.46…
[INFO] Using relative sizing for the floorplan.
[INFO IFP-0001] Added 14 rows of 85 site unithd.
[INFO IFP-0030] Inserted 0 tiecells using sky130_fd_sc_hd__conb_1/LO.
[INFO IFP-0030] Inserted 0 tiecells using sky130_fd_sc_hd__conb_1/HI.
[INFO] Extracting DIE_AREA and CORE_AREA from the floorplan
[INFO] Floorplanned on a die area of 0.0 0.0 50.27 60.99 (µm).
[INFO] Floorplanned on a core area of 5.52 10.88 44.62 48.96 (µm).
Writing metric design__die__bbox: 0.0 0.0 50.27 60.99
Writing metric design__core__bbox: 5.52 10.88 44.62 48.96
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/91-openroad-floorplan/MIMO.odb'…
Writing netlist to '/content/openlane_run/91-openroad-floorplan/MIMO.nl.v'…
Writing powered netlist to '/content/openlane_run/91-openroad-floorplan/MIMO.pnl.v'…
Writing layout to '/content/openlane_run/91-openroad-floorplan/MIMO.def'…
Writing timing constraints to '/content/openlane_run/91-openroad-floorplan/MIMO.sdc'…
```

Format	Path
nl	openlane_run/91-openroad-floorplan/MIMO.nl.v
pnl	openlane_run/91-openroad-floorplan/MIMO.pnl.v
def	openlane_run/91-openroad-floorplan/MIMO.def

```
display(floorplan)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[16:12:16] VERBOSE  Running 'KLayout.Render'…                                                  step.py:1088
[16:12:16] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_zxcek4qw/klayout-render.log…  step.py:1268
```

Time Elapsed: 3.33s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Tap/Endcap Cell Insertion

This places two kinds of cells on the floorplan:

- End cap/boundary cells: Added at the beginning and end of each row. True to their name, they "cap off" the core area of a design.
- Tap cells: Placed in a polka dot-ish fashion across the rows. Tap cells connect VDD to the nwell and the psubstrate to VSS, which the majority of cells do not do themselves to save area- but if you go long enough without one such connection you end up with the cell "latching-up"; i.e.; refusing to switch back to LO from HI.

  There is a maximum distance between tap cells enforced as part of every foundry process.

```
TapEndcapInsertion = Step.factory.get("OpenROAD.TapEndcapInsertion")

tdi = TapEndcapInsertion(state_in=floorplan.state_out)
tdi.start()
```

```
──────────────────────────────────────────────────── Tap/Decap Insertion ────────────────────────────────────────────────────
[16:12:19] VERBOSE  Running 'OpenROAD.TapEndcapInsertion'…                                                          step.py:1088
[16:12:19] VERBOSE  Logging subprocess to                                                                            step.py:1268
                    openlane_run/92-openroad-tapendcapinsertion/openroad-tapendcapinsertion.log…
Reading OpenROAD database at '/content/openlane_run/91-openroad-floorplan/MIMO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[16:12:20] WARNING  [STA-0366] port 'clk' not found.                                                              openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[16:12:20] WARNING  [STA-0366] port 'clk' not found.                                                              openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[16:12:20] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                            openroad.py:235
[INFO] Setting timing derate to: 5%
[16:12:20] WARNING  [STA-0450] virtual clock clk can not be propagated.                                           openroad.py:235
[INFO TAP-0004] Inserted 28 endcaps.
[INFO TAP-0005] Inserted 16 tapcells.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/92-openroad-tapendcapinsertion/MIMO.odb'…
Writing netlist to '/content/openlane_run/92-openroad-tapendcapinsertion/MIMO.nl.v'…
Writing powered netlist to '/content/openlane_run/92-openroad-tapendcapinsertion/MIMO.pnl.v'…
Writing layout to '/content/openlane_run/92-openroad-tapendcapinsertion/MIMO.def'…
Writing timing constraints to '/content/openlane_run/92-openroad-tapendcapinsertion/MIMO.sdc'…
```

Format	Path
nl	openlane_run/92-openroad-tapendcapinsertion/MIMO.nl.v
pnl	openlane_run/92-openroad-tapendcapinsertion/MIMO.pnl.v
def	openlane_run/92-openroad-tapendcapinsertion/MIMO.def
odb	openlane_run/92-openroad-tapendcapinsertion/MIMO.odb

```
display(tdi)
```

```
──────────────────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────────────────
[16:12:21] VERBOSE  Running 'KLayout.Render'…                                                                        step.py:1088
[16:12:21] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_c9wf6vo5/klayout-render.log…                  step.py:1268
```

Time Elapsed: 1.69s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

I/O Placement

This places metal pins at the edges of the design corresponding to the top level inputs and outputs for your design. These pins act as the interface with other designs when you integrate it with other designs.

```
IOPlacement = Step.factory.get("OpenROAD.IOPlacement")

ioplace = IOPlacement(state_in=tdi.state_out)
ioplace.start()
```

```
I/O Placement
[16:12:21] VERBOSE  Running 'OpenROAD.IOPlacement'…                                   step.py:1088
[16:12:21] VERBOSE  Logging subprocess to                                             step.py:1268
                    openlane_run/93-openroad-ioplacement/openroad-ioplacement.log…
Reading OpenROAD database at '/content/openlane_run/92-openroad-tapendcapinsertion/MIMO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[16:12:23] WARNING  [STA-0366] port 'clk' not found.                                  openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[16:12:23] WARNING  [STA-0366] port 'clk' not found.                                  openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[16:12:23] WARNING  [STA-0419] transition time can not be specified for virtual clocks.  openroad.py:235
[INFO] Setting timing derate to: 5%
[16:12:23] WARNING  [STA-0450] virtual clock clk can not be propagated.                openroad.py:235
[INFO] place_pins args: -min_distance 3
Found 0 macro blocks.
[INFO PPL-0010] Tentative 0 to set up sections.
[INFO PPL-0001] Number of slots          68
[INFO PPL-0002] Number of I/O            48
[INFO PPL-0003] Number of I/O w/sink     43
[INFO PPL-0004] Number of I/O w/o sink   5
[INFO PPL-0005] Slots per section        200
[INFO PPL-0006] Slots increase factor    0.01
[INFO PPL-0008] Successfully assigned pins to sections.
[INFO PPL-0012] I/O nets HPWL: 1708.62 um.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/93-openroad-ioplacement/MIMO.odb'…
Writing netlist to '/content/openlane_run/93-openroad-ioplacement/MIMO.nl.v'…
Writing powered netlist to '/content/openlane_run/93-openroad-ioplacement/MIMO.pnl.v'…
Writing layout to '/content/openlane_run/93-openroad-ioplacement/MIMO.def'…
Writing timing constraints to '/content/openlane_run/93-openroad-ioplacement/MIMO.sdc'…
```

Format	Path
nl	openlane_run/93-openroad-ioplacement/MIMO.nl.v
pnl	openlane_run/93-openroad-ioplacement/MIMO.pnl.v
def	openlane_run/93-openroad-ioplacement/MIMO.def
odb	openlane_run/93-openroad-ioplacement/MIMO.odb

```
display(ioplace)
```

```
Render Image (w/ KLayout)
[16:12:23] VERBOSE  Running 'KLayout.Render'…                                         step.py:1088
[16:12:23] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_vrzaguif/klayout-render.log…  step.py:1268
```

Time Elapsed: 1.33s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Generating the Power Distribution Network (PDN)

This creates the power distribution network for your design, which is essentially a plaid pattern of horizontal and vertical "straps" across the design that is then connected to the rails' VDD and VSS (via the tap cells.)

You can find an explanation of how the power distribution network works at this link: https://openlane2.readthedocs.io/en/latest/usage/hardening_macros.html#pdn-generation

While we typically don't need to mess with the PDN too much, the SPM is a small design, so we're going to need to make the plaid pattern formed by the PDN a bit smaller.

```
GeneratePDN = Step.factory.get("OpenROAD.GeneratePDN")

pdn = GeneratePDN(
    state_in=ioplace.state_out,
    FP_PDN_VWIDTH=2,
    FP_PDN_HWIDTH=2,
    FP_PDN_VPITCH=30,
    FP_PDN_HPITCH=30,
)
pdn.start()
```

```
─────────────────────────────────── Power Distribution Network Generation ───────────────────────────────────
[16:12:24] VERBOSE  Running 'OpenROAD.GeneratePDN'…                                                  step.py:1088
[16:12:24] INFO     'FP_PDN_CFG' not explicitly set, setting it to                                openroad.py:1174
                    /content/openlane_ipynb/openlane/scripts/openroad/common/pdn_cfg.tcl…
[16:12:24] VERBOSE  Logging subprocess to                                                            step.py:1268
                    openlane_run/94-openroad-generatepdn/openroad-generatepdn.log…
Reading OpenROAD database at '/content/openlane_run/93-openroad-ioplacement/MIMO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[16:12:25] WARNING  [STA-0366] port 'clk' not found.                                                 openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[16:12:25] WARNING  [STA-0366] port 'clk' not found.                                                 openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[16:12:25] WARNING  [STA-0419] transition time can not be specified for virtual clocks.               openroad.py:235
[INFO] Setting timing derate to: 5%
[16:12:25] WARNING  [STA-0450] virtual clock clk can not be propagated.                              openroad.py:235
[INFO] Setting global connections...
[INFO PDN-0001] Inserting grid: stdcell_grid
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/94-openroad-generatepdn/MIMO.odb'…
Writing netlist to '/content/openlane_run/94-openroad-generatepdn/MIMO.nl.v'…
Writing powered netlist to '/content/openlane_run/94-openroad-generatepdn/MIMO.pnl.v'…
Writing layout to '/content/openlane_run/94-openroad-generatepdn/MIMO.def'…
Writing timing constraints to '/content/openlane_run/94-openroad-generatepdn/MIMO.sdc'…
[INFO PSM-0040] All shapes on net VPWR are connected.
[INFO PSM-0040] All shapes on net VGND are connected.
```

Format	Path
nl	openlane_run/94-openroad-generatepdn/MIMO.nl.v
pnl	openlane_run/94-openroad-generatepdn/MIMO.pnl.v
def	openlane_run/94-openroad-generatepdn/MIMO.def
odb	openlane_run/94-openroad-generatepdn/MIMO.odb

```
display(pdn)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[16:12:25] VERBOSE  Running 'KLayout.Render'…                                                   step.py:1088
[16:12:25] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_f56u9639/klayout-render.log…  step.py:1268
```

Time Elapsed: 1.45s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Global Placement

Global Placement is deciding on a fuzzy, non-final location for each of the cells, with the aim of minimizing the distance between cells that are connected together (more specifically, the total length of the not-yet-created wires that will connect them).

As you will see in the `.display()` in the second cell below, the placement is considered "illegal", i.e., not properly aligned with the cell placement grid. This is addressed by "Detailed Placement", also referred to as "placement legalization", which is the next step.

```
GlobalPlacement = Step.factory.get("OpenROAD.GlobalPlacement")

gpl = GlobalPlacement(state_in=pdn.state_out)
gpl.start()
```

```
──────────────────────────────────────────────────────────────────────────────── Global Placement ────────────────────────────────────────────────────────────────────────────────
[16:12:26] VERBOSE  Running 'OpenROAD.GlobalPlacement'…                                                                                                          step.py:1088
[16:12:26] INFO     'PL_TARGET_DENSITY_PCT' not explicitly set, using dynamically calculated                                                                  openroad.py:1260
                    target density: 63.025200…
[16:12:27] VERBOSE  Logging subprocess to                                                                                                                        step.py:1268
                    openlane_run/95-openroad-globalplacement/openroad-globalplacement.log…
Reading OpenROAD database at '/content/openlane_run/94-openroad-generatepdn/MIMO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[16:12:28] WARNING  [STA-0366] port 'clk' not found.                                                                                                             openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[16:12:28] WARNING  [STA-0366] port 'clk' not found.                                                                                                             openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[16:12:28] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                                                           openroad.py:235
[INFO] Setting timing derate to: 5%
[16:12:28] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                                                          openroad.py:235
[INFO] Setting RC values…
[INFO] Setting signal min routing layer to: met1 and clock min routing layer to met1.
[INFO] Setting signal max routing layer to: met5 and clock max routing layer to met5.
[INFO GPL-0002] DBU: 1000
[INFO GPL-0003] SiteSize: (  0.460  2.720 ) um
[INFO GPL-0004] CoreBBox: (  5.520 10.880 ) ( 44.620 48.960 ) um
[INFO GPL-0006] NumInstances:               139
[INFO GPL-0007] NumPlaceInstances:           95
[INFO GPL-0008] NumFixedInstances:           44
[INFO GPL-0009] NumDummyInstances:            0
[INFO GPL-0010] NumNets:                    111
[INFO GPL-0011] NumPins:                    345
[INFO GPL-0012] DieBBox:  (  0.000  0.000 ) ( 50.270 60.990 ) um
[INFO GPL-0013] CoreBBox: (  5.520 10.880 ) ( 44.620 48.960 ) um
[INFO GPL-0016] CoreArea:              1488.928 um^2
[INFO GPL-0017] NonPlaceInstsArea:      125.120 um^2
[INFO GPL-0018] PlaceInstsArea:         769.488 um^2
[INFO GPL-0019] Util:                    56.422 %
[INFO GPL-0020] StdInstsArea:           769.488 um^2
[INFO GPL-0021] MacroInstsArea:           0.000 um^2
[InitialPlace]  Iter: 1 CG residual: 0.00000006 HPWL: 3151740
[InitialPlace]  Iter: 2 CG residual: 0.00000003 HPWL: 1593929
[InitialPlace]  Iter: 3 CG residual: 0.00000005 HPWL: 1490340
[InitialPlace]  Iter: 4 CG residual: 0.00000005 HPWL: 1452059
[InitialPlace]  Iter: 5 CG residual: 0.00000010 HPWL: 1433140
[INFO GPL-0031] FillerInit:NumGCells:       106
[INFO GPL-0032] FillerInit:NumGNets:        111
[INFO GPL-0033] FillerInit:NumGPins:        345
[INFO GPL-0023] TargetDensity:            0.630
[INFO GPL-0024] AvrgPlaceInstArea:        8.100 um^2
[INFO GPL-0025] IdealBinArea:            12.852 um^2
[INFO GPL-0026] IdealBinCnt:                115
[INFO GPL-0027] TotalBinArea:          1488.928 um^2
[INFO GPL-0028] BinCnt:         8      8
[INFO GPL-0029] BinSize: (  4.888  4.760 )
[INFO GPL-0030] NumBins: 64
[NesterovSolve] Iter:    1 overflow: 0.690 HPWL: 1129679
[INFO GPL-0100] worst slack 3.26e-09
[INFO GPL-0103] Weighted 7 nets.
[INFO GPL-0100] worst slack 3.25e-09
[INFO GPL-0103] Weighted 9 nets.
[NesterovSolve] Snapshot saved at iter = 4
[NesterovSolve] Iter:   10 overflow: 0.527 HPWL: 1220040
[NesterovSolve] Iter:   20 overflow: 0.499 HPWL: 1220094
[NesterovSolve] Iter:   30 overflow: 0.513 HPWL: 1214256
[NesterovSolve] Iter:   40 overflow: 0.517 HPWL: 1213783
[NesterovSolve] Iter:   50 overflow: 0.510 HPWL: 1215712
[NesterovSolve] Iter:   60 overflow: 0.512 HPWL: 1214388
[NesterovSolve] Iter:   70 overflow: 0.514 HPWL: 1214067
[NesterovSolve] Iter:   80 overflow: 0.512 HPWL: 1215043
[NesterovSolve] Iter:   90 overflow: 0.512 HPWL: 1214779
[NesterovSolve] Iter:  100 overflow: 0.513 HPWL: 1214726
[NesterovSolve] Iter:  110 overflow: 0.513 HPWL: 1215400
[NesterovSolve] Iter:  120 overflow: 0.513 HPWL: 1215895
[NesterovSolve] Iter:  130 overflow: 0.513 HPWL: 1216525
[NesterovSolve] Iter:  140 overflow: 0.513 HPWL: 1217945
[NesterovSolve] Iter:  150 overflow: 0.513 HPWL: 1219776
[NesterovSolve] Iter:  160 overflow: 0.513 HPWL: 1223065
[NesterovSolve] Iter:  170 overflow: 0.510 HPWL: 1225477
[NesterovSolve] Iter:  180 overflow: 0.504 HPWL: 1230924
[NesterovSolve] Iter:  190 overflow: 0.489 HPWL: 1235555
[INFO GPL-0100] worst slack 3.29e-09
[INFO GPL-0103] Weighted 9 nets.
[NesterovSolve] Iter:  200 overflow: 0.469 HPWL: 1244798
[NesterovSolve] Iter:  210 overflow: 0.457 HPWL: 1253794
[NesterovSolve] Iter:  220 overflow: 0.442 HPWL: 1267212
[NesterovSolve] Iter:  230 overflow: 0.416 HPWL: 1285345
[NesterovSolve] Iter:  240 overflow: 0.384 HPWL: 1305378
[NesterovSolve] Iter:  250 overflow: 0.351 HPWL: 1326681
[NesterovSolve] Iter:  260 overflow: 0.323 HPWL: 1348467
[NesterovSolve] Iter:  270 overflow: 0.292 HPWL: 1368918
[INFO GPL-0100] worst slack 3.28e-09
[INFO GPL-0103] Weighted 8 nets.
[NesterovSolve] Iter:  280 overflow: 0.257 HPWL: 1392414
[NesterovSolve] Iter:  290 overflow: 0.233 HPWL: 1407622
[INFO GPL-0100] worst slack 3.26e-09
[INFO GPL-0103] Weighted 9 nets.
[INFO GPL-0075] Routability numCall: 1 inflationIterCnt: 1 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:       7    8
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 56
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0
[INFO GPL-0065] OverflowTileCnt2: 0
[INFO GPL-0066] 0.5%RC: 1.0000
[INFO GPL-0067] 1.0%RC: 1.0000
[INFO GPL-0068] 2.0%RC: 0.9750
[INFO GPL-0069] 5.0%RC: 0.9167
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 1.0000
[INFO GPL-0078] FinalRC lower than minRC (1e+30), min RC updated.
[INFO GPL-0045] InflatedAreaDelta:        0.000 um^2
[INFO GPL-0046] TargetDensity:            0.630
[INFO GPL-0049] WhiteSpaceArea:        1363.808 um^2
[INFO GPL-0050] NesterovInstsArea:      769.488 um^2
[INFO GPL-0051] TotalFillerArea:         90.055 um^2
[INFO GPL-0052] TotalGCellsArea:        859.543 um^2
[INFO GPL-0053] ExpectedGCellsArea:     859.543 um^2
[INFO GPL-0054] NewTargetDensity:         0.630
[INFO GPL-0055] NewWhiteSpaceArea:     1363.808 um^2
[INFO GPL-0056] MovableArea:            859.543 um^2
[INFO GPL-0057] NewNesterovInstArea:    769.488 um^2
[INFO GPL-0058] NewTotalFillerArea:      90.055 um^2
```

```
[INFO GPL-0059] NewTotalGCellsArea:     859.543 um^2
[NesterovSolve] Revert back to snapshot coordi
[NesterovSolve] Iter:  300 overflow: 0.579 HPWL: 1212143
[NesterovSolve] Iter:  310 overflow: 0.514 HPWL: 1226181
[NesterovSolve] Iter:  320 overflow: 0.510 HPWL: 1225905
[NesterovSolve] Iter:  330 overflow: 0.522 HPWL: 1220828
[NesterovSolve] Iter:  340 overflow: 0.516 HPWL: 1223637
[NesterovSolve] Iter:  350 overflow: 0.516 HPWL: 1223620
[NesterovSolve] Iter:  360 overflow: 0.520 HPWL: 1222270
[NesterovSolve] Iter:  370 overflow: 0.517 HPWL: 1223334
[NesterovSolve] Iter:  380 overflow: 0.517 HPWL: 1223551
[NesterovSolve] Iter:  390 overflow: 0.518 HPWL: 1222874
[NesterovSolve] Iter:  400 overflow: 0.518 HPWL: 1223162
[NesterovSolve] Iter:  410 overflow: 0.517 HPWL: 1223402
[NesterovSolve] Iter:  420 overflow: 0.518 HPWL: 1223166
[NesterovSolve] Iter:  430 overflow: 0.517 HPWL: 1223411
[NesterovSolve] Iter:  440 overflow: 0.517 HPWL: 1223879
[NesterovSolve] Iter:  450 overflow: 0.516 HPWL: 1224282
[NesterovSolve] Iter:  460 overflow: 0.516 HPWL: 1224963
[NesterovSolve] Iter:  470 overflow: 0.515 HPWL: 1225660
[NesterovSolve] Iter:  480 overflow: 0.513 HPWL: 1226405
[NesterovSolve] Iter:  490 overflow: 0.511 HPWL: 1228723
[NesterovSolve] Iter:  500 overflow: 0.508 HPWL: 1231109
[NesterovSolve] Iter:  510 overflow: 0.502 HPWL: 1231589
[NesterovSolve] Iter:  520 overflow: 0.494 HPWL: 1235068
[NesterovSolve] Iter:  530 overflow: 0.483 HPWL: 1238301
[NesterovSolve] Iter:  540 overflow: 0.472 HPWL: 1242044
[NesterovSolve] Iter:  550 overflow: 0.460 HPWL: 1248161
[NesterovSolve] Iter:  560 overflow: 0.452 HPWL: 1257984
[NesterovSolve] Iter:  570 overflow: 0.441 HPWL: 1272452
[NesterovSolve] Iter:  580 overflow: 0.415 HPWL: 1287049
[NesterovSolve] Iter:  590 overflow: 0.388 HPWL: 1300285
[NesterovSolve] Iter:  600 overflow: 0.363 HPWL: 1312956
[NesterovSolve] Iter:  610 overflow: 0.343 HPWL: 1337744
[NesterovSolve] Iter:  620 overflow: 0.318 HPWL: 1362072
[NesterovSolve] Iter:  630 overflow: 0.289 HPWL: 1384213
[NesterovSolve] Iter:  640 overflow: 0.252 HPWL: 1397172
[NesterovSolve] Iter:  650 overflow: 0.223 HPWL: 1415620
[NesterovSolve] Iter:  660 overflow: 0.201 HPWL: 1434610
[INFO GPL-0075] Routability numCall: 2 inflationIterCnt: 2 bloatIterCnt: 0
[INFO GPL-0036] TileBBox: (    0    0 ) ( 6900 6900 ) DBU
[INFO GPL-0038] TileCnt:       7    8
[INFO GPL-0039] numRoutingLayers: 6
[INFO GPL-0040] NumTiles: 56
[INFO GPL-0063] TotalRouteOverflowH2: 0
[INFO GPL-0064] TotalRouteOverflowV2: 0
[INFO GPL-0065] OverflowTileCnt2: 0
[INFO GPL-0066] 0.5%RC: 1.0000
[INFO GPL-0067] 1.0%RC: 0.9500
[INFO GPL-0068] 2.0%RC: 0.9000
[INFO GPL-0069] 5.0%RC: 0.8056
[INFO GPL-0070] 0.5rcK: 1
[INFO GPL-0071] 1.0rcK: 1
[INFO GPL-0072] 2.0rcK: 0
[INFO GPL-0073] 5.0rcK: 0
[INFO GPL-0074] FinalRC: 0.9750
[INFO GPL-0077] FinalRC lower than targetRC(1), routability not needed.
[NesterovSolve] Iter:  670 overflow: 0.171 HPWL: 1452098
[NesterovSolve] Iter:  680 overflow: 0.145 HPWL: 1463241
[INFO GPL-0100] worst slack 3.26e-09
[INFO GPL-0103] Weighted 5 nets.
[NesterovSolve] Iter:  690 overflow: 0.136 HPWL: 1490299
[NesterovSolve] Finished with Overflow: 0.099488
[INFO] Setting RC values…
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/95-openroad-globalplacement/MIMO.odb'…
Writing netlist to '/content/openlane_run/95-openroad-globalplacement/MIMO.nl.v'
```

```
display(gpl)
```

```
────────────────────────────────────────── Render Image (w/ KLayout) ──────────────────────────────────────────
[16:12:29] VERBOSE  Running 'KLayout.Render'…                                                          step.py:1088
[16:12:29] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_o5assgcw/klayout-render.log…     step.py:1268
```

Time Elapsed: 2.50s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Detailed Placement

This aligns the fuzzy placement from before with the grid, "legalizing" it.

```
DetailedPlacement = Step.factory.get("OpenROAD.DetailedPlacement")

dpl = DetailedPlacement(state_in=gpl.state_out)
dpl.start()
```

```
────────────────────────────────────────────────────────── Detailed Placement ──────────────────────────────────────────────────────────
[16:12:30] VERBOSE  Running 'OpenROAD.DetailedPlacement'…                                                                    step.py:1088
[16:12:30] VERBOSE  Logging subprocess to                                                                                     step.py:1268
                    openlane_run/96-openroad-detailedplacement/openroad-detailedplacement.log…
Reading OpenROAD database at '/content/openlane_run/95-openroad-globalplacement/MIMO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[16:12:31] WARNING  [STA-0366] port 'clk' not found.                                                                          openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[16:12:31] WARNING  [STA-0366] port 'clk' not found.                                                                          openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[16:12:31] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                       openroad.py:235
[INFO] Setting timing derate to: 5%
[16:12:31] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                       openroad.py:235
Placement Analysis
---------------------------------
total displacement        200.9 u
average displacement        1.4 u
max displacement            6.4 u
original HPWL            1484.8 u
legalized HPWL           1653.5 u
delta HPWL                   11 %

[INFO DPL-0020] Mirrored 27 instances
[INFO DPL-0021] HPWL before            1653.5 u
[INFO DPL-0022] HPWL after             1613.7 u
[INFO DPL-0023] HPWL delta               -2.4 %
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/96-openroad-detailedplacement/MIMO.odb'…
Writing netlist to '/content/openlane_run/96-openroad-detailedplacement/MIMO.nl.v'…
Writing powered netlist to '/content/openlane_run/96-openroad-detailedplacement/MIMO.pnl.v'…
Writing layout to '/content/openlane_run/96-openroad-detailedplacement/MIMO.def'…
Writing timing constraints to '/content/openlane_run/96-openroad-detailedplacement/MIMO.sdc'…
```

Format	Path
nl	openlane_run/96-openroad-detailedplacement/MIMO.nl.v
pnl	openlane_run/96-openroad-detailedplacement/MIMO.pnl.v
def	openlane_run/96-openroad-detailedplacement/MIMO.def
odb	openlane_run/96-openroad-detailedplacement/MIMO.odb

```
display(dpl)
```

```
────────────────────────────────────────────────────────── Render Image (w/ KLayout) ──────────────────────────────────────────────────────────
[16:12:31] VERBOSE  Running 'KLayout.Render'…                                                                                 step.py:1088
[16:12:31] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_opu3c6a_/klayout-render.log…                            step.py:1268
```

Time Elapsed: 1.23s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Clock Tree Synthesis (CTS)

With the cells now having a final placement, we can go ahead and create what is known as the clock tree, i.e., the hierarchical set of buffers used for clock signal to minimize what is known as "clock skew"- variable delay of the clock cycle from register to register because of factors such as metal wire length, clock load (number of gates connected to the same clock buffer,) et cetera.

The CTS step creates the cells and places the between the gaps in the detailed placement above.

```
CTS = Step.factory.get("OpenROAD.CTS")

cts = CTS(state_in=dpl.state_out)
cts.start()
```

```
────────────────────────────────────────────────────────── Clock Tree Synthesis ──────────────────────────────────────────────────────────
[16:12:32] VERBOSE  Running 'OpenROAD.CTS'…                                                                                    step.py:1088
[16:12:32] VERBOSE  Logging subprocess to openlane_run/97-openroad-cts/openroad-cts.log…                                       step.py:1268
Reading timing models for corner nom_tt_025C_1v80…
Reading timing library for the 'nom_tt_025C_1v80' corner at
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading timing models for corner nom_ff_n40C_1v95…
Reading timing library for the 'nom_ff_n40C_1v95' corner at
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ff_n40C_1v95.lib'…
Reading timing models for corner nom_ss_100C_1v60…
Reading timing library for the 'nom_ss_100C_1v60' corner at
'/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__ss_100C_1v60.lib'…
Reading OpenROAD database at '/content/openlane_run/96-openroad-detailedplacement/MIMO.odb'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[16:12:36] WARNING  [STA-0366] port 'clk' not found.                                                                            openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[16:12:36] WARNING  [STA-0366] port 'clk' not found.                                                                            openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[16:12:36] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                          openroad.py:235
[INFO] Setting timing derate to: 5%
[16:12:36] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                         openroad.py:235
[INFO] Setting RC values…
[INFO] Configuring cts characterization…
[INFO] Performing clock tree synthesis…
[INFO] Looking for the following net(s): clk
[INFO] Running Clock Tree Synthesis…
[INFO CTS-0050] Root buffer is sky130_fd_sc_hd__clkbuf_16.
[INFO CTS-0051] Sink buffer is sky130_fd_sc_hd__clkbuf_4.
[INFO CTS-0052] The following clock buffers will be used for CTS:
sky130_fd_sc_hd__clkbuf_2
sky130_fd_sc_hd__clkbuf_4
sky130_fd_sc_hd__clkbuf_8
[INFO CTS-0049] Characterization buffer is sky130_fd_sc_hd__clkbuf_8.
[16:12:53] WARNING  [CTS-0083] No clock nets have been found.                                                                   openroad.py:235
[INFO CTS-0008] TritonCTS found 0 clock nets.
[16:12:53] WARNING  [CTS-0082] No valid clock nets in the design.                                                               openroad.py:235
[16:12:53] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                         openroad.py:235
[INFO] Repairing long wires on clock nets…
[INFO RSZ-0058] Using max wire length 6335um.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/97-openroad-cts/MIMO.odb'…
Writing netlist to '/content/openlane_run/97-openroad-cts/MIMO.nl.v'…
Writing powered netlist to '/content/openlane_run/97-openroad-cts/MIMO.pnl.v'…
Writing layout to '/content/openlane_run/97-openroad-cts/MIMO.def'…
Writing timing constraints to '/content/openlane_run/97-openroad-cts/MIMO.sdc'…
[INFO] Legalizing…
Placement Analysis
---------------------------------
total displacement          0.0 u
average displacement        0.0 u
max displacement            0.0 u
original HPWL            1613.7 u
legalized HPWL           1653.5 u
delta HPWL                    2 %

[INFO DPL-0020] Mirrored 27 instances
[INFO DPL-0021] HPWL before            1653.5 u
[INFO DPL-0022] HPWL after             1613.7 u
[INFO DPL-0023] HPWL delta               -2.4 %
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/97-openroad-cts/MIMO.odb'…
Writing netlist to '/content/openlane_run/97-openroad-cts/MIMO.nl.v'…
Writing powered netlist to '/content/openlane_run/97-openroad-cts/MIMO.pnl.v'…
Writing layout to '/content/openlane_run/97-openroad-cts/MIMO.def'…
Writing timing constraints to '/content/openlane_run/97-openroad-cts/MIMO.sdc'…
```

Format	Path
nl	openlane_run/97-openroad-cts/MIMO.nl.v
pnl	openlane_run/97-openroad-cts/MIMO.pnl.v

```
display(cts)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[16:12:54] VERBOSE  Running 'KLayout.Render'…                                                   step.py:1088
[16:12:54] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_0hnz0nsx/klayout-render.log…  step.py:1268
```

Time Elapsed: 21.08s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Global Routing

Global routing "plans" the routes the wires between two gates (or gates and I/O pins/the PDN) will take. The results of global routing (which are called "routing guides") are stored in internal data structures and have no effect on the actual design, so there is no `display()` statement.

```
GlobalRouting = Step.factory.get("OpenROAD.GlobalRouting")

grt = GlobalRouting(state_in=cts.state_out)
grt.start()
```

```
──────────────────────────────────────────────────────── Global Routing ────────────────────────────────────────────────────────
[16:12:55] VERBOSE  Running 'OpenROAD.GlobalRouting'…                                                                  step.py:1088
[16:12:55] VERBOSE  Logging subprocess to                                                                              step.py:1268
                    openlane_run/98-openroad-globalrouting/openroad-globalrouting.log…
Reading OpenROAD database at '/content/openlane_run/97-openroad-cts/MIMO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[16:12:56] WARNING  [STA-0366] port 'clk' not found.                                                                  openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[16:12:56] WARNING  [STA-0366] port 'clk' not found.                                                                  openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[16:12:56] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                 openroad.py:235
[INFO] Setting timing derate to: 5%
[16:12:56] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                openroad.py:235
[16:12:56] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                openroad.py:235
[INFO] Setting signal min routing layer to: met1 and clock min routing layer to met1.
[INFO] Setting signal max routing layer to: met5 and clock max routing layer to met5.
-congestion_iterations 50 -verbose
[INFO GRT-0020] Min routing layer: met1
[INFO GRT-0021] Max routing layer: met5
[INFO GRT-0022] Global adjustment: 30%
[INFO GRT-0023] Grid origin: (0, 0)
[INFO GRT-0043] No OR_DEFAULT vias defined.
[INFO GRT-0088] Layer li1     Track-Pitch = 0.4600  line-2-Via Pitch: 0.3400
[INFO GRT-0088] Layer met1    Track-Pitch = 0.3400  line-2-Via Pitch: 0.3400
[INFO GRT-0088] Layer met2    Track-Pitch = 0.4600  line-2-Via Pitch: 0.3500
[INFO GRT-0088] Layer met3    Track-Pitch = 0.6800  line-2-Via Pitch: 0.6150
[INFO GRT-0088] Layer met4    Track-Pitch = 0.9200  line-2-Via Pitch: 1.0400
[INFO GRT-0088] Layer met5    Track-Pitch = 3.4000  line-2-Via Pitch: 3.1100
[INFO GRT-0019] Found 0 clock nets.
[INFO GRT-0001] Minimum degree: 2
[INFO GRT-0002] Maximum degree: 13
[INFO GRT-0003] Macros: 0
[INFO GRT-0043] No OR_DEFAULT vias defined.
[INFO GRT-0004] Blockages: 35

[INFO GRT-0053] Routing resources analysis:
Routing      Original      Derated      Resource
Layer     Direction    Resources     Resources    Reduction (%)
-------------------------------------------------------------
li1        Vertical            0             0          0.00%
met1       Horizontal       1219           593          51.35%
met2       Vertical          887           509          42.62%
met3       Horizontal        606           328          45.87%
met4       Vertical          366           186          49.18%
met5       Horizontal        117            54          53.85%
-------------------------------------------------------------

[INFO GRT-0197] Via related to pin nodes: 464
[INFO GRT-0198] Via related Steiner nodes: 3
[INFO GRT-0199] Via filling finished.
[INFO GRT-0111] Final number of vias: 570
[INFO GRT-0112] Final usage 3D: 1932

[INFO GRT-0096] Final congestion report:
Layer         Resource        Demand        Usage (%)    Max H / Max V / Total Overflow
---------------------------------------------------------------------------------------
li1                  0             0            0.00%             0 /  0 /  0
met1               593            93           15.68%             0 /  0 /  0
met2               509           103           20.24%             0 /  0 /  0
met3               328            26            7.93%             0 /  0 /  0
met4               186             0            0.00%             0 /  0 /  0
met5                54             0            0.00%             0 /  0 /  0
---------------------------------------------------------------------------------------
Total             1670           222           13.29%             0 /  0 /  0

[INFO GRT-0018] Total wirelength: 3215 um
[INFO GRT-0014] Routed nets: 106
[INFO] Setting RC values…
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/98-openroad-globalrouting/MIMO.odb'…
Writing layout to '/content/openlane_run/98-openroad-globalrouting/MIMO.def'…
```

Format	Path
nl	openlane_run/97-openroad-cts/MIMO.nl.v
pnl	openlane_run/97-openroad-cts/MIMO.pnl.v

Detailed Routing

Detailed routing uses the guides from Global Routing to actually create wires on the metal layers and connect the gates, making the connections finally physical.

This is typically the longest step in the flow.

```
DetailedRouting = Step.factory.get("OpenROAD.DetailedRouting")

drt = DetailedRouting(state_in=grt.state_out)
drt.start()
```

```
Detailed Routing
[16:12:56] VERBOSE  Running 'OpenROAD.DetailedRouting'…                                   step.py:1088
[16:12:56] INFO     Running TritonRoute with 2 threads…                                  openroad.py:1619
[16:12:56] VERBOSE  Logging subprocess to                                                 step.py:1268
                    openlane_run/99-openroad-detailedrouting/openroad-detailedrouting.log…
Reading OpenROAD database at '/content/openlane_run/98-openroad-globalrouting/MIMO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[16:12:57] WARNING  [STA-0366] port 'clk' not found.                                      openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[16:12:57] WARNING  [STA-0366] port 'clk' not found.                                      openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[16:12:57] WARNING  [STA-0419] transition time can not be specified for virtual clocks.    openroad.py:235
[INFO] Setting timing derate to: 5%
[16:12:57] WARNING  [STA-0450] virtual clock clk can not be propagated.                   openroad.py:235
[INFO ORD-0030] Using 2 thread(s).
[INFO DRT-0149] Reading tech and libs.
[16:12:57] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer mcon
[16:12:57] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer mcon
[16:12:57] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via
[16:12:57] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via
[16:12:57] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via2
[16:12:57] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via2
[16:12:57] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via3
[16:12:57] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via3
[16:12:57] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via4
[16:12:57] WARNING  [DRT-0349] LEF58_ENCLOSURE with no CUTCLASS is not supported. Skipping for   openroad.py:235
                    layer via4

Units:                1000
Number of layers:     13
Number of macros:     441
Number of vias:       28
Number of viarulegen: 25

[INFO DRT-0150] Reading design.

Design:                   MIMO
Die area:                 ( 0 0 ) ( 50270 60990 )
Number of track patterns: 12
Number of DEF vias:       0
Number of components:     139
Number of terminals:      50
Number of snets:          2
Number of nets:           111

[INFO DRT-0167] List of default vias:
Layer via
default via: M1M2_PR
Layer via2
default via: M2M3_PR
Layer via3
default via: M3M4_PR
Layer via4
default via: M4M5_PR
[INFO DRT-0162] Library cell analysis.
[INFO DRT-0163] Instance analysis.
[INFO DRT-0164] Number of unique instances = 61.
[INFO DRT-0168] Init region query.
[INFO DRT-0024]   Complete FR_MASTERSLICE.
[INFO DRT-0024]   Complete Fr_VIA.
[INFO DRT-0024]   Complete li1.
[INFO DRT-0024]   Complete mcon.
[INFO DRT-0024]   Complete met1.
[INFO DRT-0024]   Complete via.
[INFO DRT-0024]   Complete met2.
[INFO DRT-0024]   Complete via2.
[INFO DRT-0024]   Complete met3.
[INFO DRT-0024]   Complete via3.
[INFO DRT-0024]   Complete met4.
[INFO DRT-0024]   Complete via4.
[INFO DRT-0024]   Complete met5.
[INFO DRT-0033] FR_MASTERSLICE shape region query size = 0.
[INFO DRT-0033] FR_VIA shape region query size = 0.
[INFO DRT-0033] li1 shape region query size = 2319.
[INFO DRT-0033] mcon shape region query size = 0.
[INFO DRT-0033] met1 shape region query size = 334.
[INFO DRT-0033] via shape region query size = 90.
[INFO DRT-0033] met2 shape region query size = 42.
[INFO DRT-0033] via2 shape region query size = 75.
[INFO DRT-0033] met3 shape region query size = 81.
[INFO DRT-0033] via3 shape region query size = 75.
[INFO DRT-0033] met4 shape region query size = 19.
[INFO DRT-0033] via4 shape region query size = 0.
[INFO DRT-0033] met5 shape region query size = 0.
[INFO DRT-0165] Start pin access.
[INFO DRT-0078]   Complete 199 pins.
[INFO DRT-0081]   Complete 55 unique inst patterns.
[INFO DRT-0084]   Complete 59 groups.
#scanned instances     = 139
#unique  instances     = 61
#stdCellGenAp          = 1338
#stdCellValidPlanarAp  = 7
#stdCellValidViaAp     = 1056
#stdCellPinNoAp        = 0
#stdCellPinCnt         = 297
#instTermValidViaApCnt = 0
#macroGenAp            = 0
#macroValidPlanarAp    = 0
#macroValidViaAp       = 0
#macroNoAp             = 0
[INFO DRT-0166] Complete pin access.
[INFO DRT-0267] cpu time = 00:00:08, elapsed time = 00:00:04, memory = 113.47 (MB), peak = 299.69 (MB)

Number of guides:     663

[INFO DRT-0169] Post process guides.
[INFO DRT-0176] GCELLGRID X 0 DO 7 STEP 6900 ;
[INFO DRT-0177] GCELLGRID Y 0 DO 8 STEP 6900 ;
[INFO DRT-0028]   Complete FR_MASTERSLICE.
[INFO DRT-0028]   Complete Fr_VIA.
[INFO DRT-0028]   Complete li1.
[INFO DRT-0028]   Complete mcon.
[INFO DRT-0028]   Complete met1.
```

```
[INFO DRT-0028]   Complete via.
[INFO DRT-0028]   Complete met2.
[INFO DRT-0028]   Complete via2.
[INFO DRT-0028]   Complete met3.
[INFO DRT-0028]   Complete via3.
[INFO DRT-0028]   Complete met4.
[INFO DRT-0028]   Complete via4.
[INFO DRT-0028]   Complete met5.
[INFO DRT-0178] Init guide query.
[INFO DRT-0035]   Complete FR_MASTERSLICE (guide).
[INFO DRT-0035]   Complete Fr_VIA (guide).
[INFO DRT-0035]   Complete li1 (guide).
[INFO DRT-0035]   Complete mcon (guide).
[INFO DRT-0035]   Complete met1 (guide).
[INFO DRT-0035]   Complete via (guide).
[INFO DRT-0035]   Complete met2 (guide).
[INFO DRT-0035]   Complete via2 (guide).
[INFO DRT-0035]   Complete met3 (guide).
[INFO DRT-0035]   Complete via3 (guide).
[INFO DRT-0035]   Complete met4 (guide).
[INFO DRT-0035]   Complete via4 (guide).
[INFO DRT-0035]   Complete met5 (guide).
[INFO DRT-0036] FR_MASTERSLICE guide region query size = 0.
[INFO DRT-0036] FR_VIA guide region query size = 0.
[INFO DRT-0036] li1 guide region query size = 212.
[INFO DRT-0036] mcon guide region query size = 0.
[INFO DRT-0036] met1 guide region query size = 153.
[INFO DRT-0036] via guide region query size = 0.
[INFO DRT-0036] met2 guide region query size = 95.
[INFO DRT-0036] via2 guide region query size = 0.
[INFO DRT-0036] met3 guide region query size = 37.
[INFO DRT-0036] via3 guide region query size = 0.
[INFO DRT-0036] met4 guide region query size = 0.
[INFO DRT-0036] via4 guide region query size = 0.
[INFO DRT-0036] met5 guide region query size = 0.
[INFO DRT-0179] Init gr pin query.
[INFO DRT-0245] skipped writing guide updates to database.
[INFO DRT-0185] Post process initialize RPin region query.
[INFO DRT-0181] Start track assignment.
[INFO DRT-0184] Done with 307 vertical wires in 1 frboxes and 190 horizontal wires in 1 frboxes.
[INFO DRT-0186] Done with 24 vertical wires in 1 frboxes and 38 horizontal wires in 1 frboxes.
[INFO DRT-0182] Complete track assignment.
[INFO DRT-0267] cpu time = 00:00:00, elapsed time = 00:00:00, memory = 114.77 (MB), peak = 299.69 (MB)
[INFO DRT-0187] Start routing data preparation.
[INFO DRT-0267] cpu time = 00:00:00, elapsed time = 00:00:00, memory = 114.77 (MB), peak = 299.69 (MB)
[INFO DRT-0194] Start detail routing.
[INFO DRT-0195] Start 0th optimization iteration.
Completing 10% with 0 violations.
elapsed time = 00:00:01, memory = 122.46 (MB).
Completing 20% with 6 violations.
elapsed time = 00:00:01, memory = 123.35 (MB).
[INFO DRT-0199]   Number of violations = 6.
Viol/Layer        met2   met3
Metal Spacing        2      3
Short                1      0
[INFO DRT-0267] cpu time = 00:00:01, elapsed time = 00:00:01, memory = 478.16 (MB), peak = 478.16 (MB)
Total wire length = 1754 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 661 um.
Total wire length on LAYER met2 = 795 um.
Total wire length on LAYER met3 = 298 um.
Total wire length on LAYER met4 = 0 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 600.
Up-via summary (total 600):

----------------------
FR_MASTERSLICE      0
li1    296
met1    266
met2     38
met3      0
met4      0
----------------------
600


[INFO DRT-0195] Start 1st optimization iteration.
Completing 10% with 6 violations.
elapsed time = 00:00:00, memory = 478.16 (MB).
Completing 20% with 4 violations.
elapsed time = 00:00:00, memory = 482.85 (MB).
Completing 30% with 3 violations.
elapsed time = 00:00:00, memory = 482.85 (MB).
Completing 40% with 5 violations.
elapsed time = 00:00:00, memory = 482.85 (MB).
[INFO DRT-0199]   Number of violations = 5.
Viol/Layer        met1   met2
Metal Spacing        2      0
Short                2      1
[INFO DRT-0267] cpu time = 00:00:01, elapsed time = 00:00:01, memory = 482.85 (MB), peak = 482.85 (MB)
Total wire length = 1735 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 666 um.
Total wire length on LAYER met2 = 796 um.
Total wire length on LAYER met3 = 272 um.
Total wire length on LAYER met4 = 0 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 604.
Up-via summary (total 604):

----------------------
FR_MASTERSLICE      0
li1    296
met1    270
met2     38
met3      0
met4      0
----------------------
604


[INFO DRT-0195] Start 2nd optimization iteration.
Completing 10% with 5 violations.
elapsed time = 00:00:00, memory = 482.85 (MB).
Completing 20% with 5 violations.
elapsed time = 00:00:00, memory = 482.85 (MB).
Completing 30% with 5 violations.
elapsed time = 00:00:00, memory = 482.85 (MB).
Completing 40% with 5 violations.
elapsed time = 00:00:00, memory = 482.85 (MB).
[INFO DRT-0199]   Number of violations = 3.
Viol/Layer        met1   met2
Short                2      1
[INFO DRT-0267] cpu time = 00:00:01, elapsed time = 00:00:01, memory = 483.13 (MB), peak = 483.13 (MB)
Total wire length = 1744 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 667 um.
```

```
Total wire length on LAYER met2 = 805 um.
Total wire length on LAYER met3 = 270 um.
Total wire length on LAYER met4 = 0 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 607.
Up-via summary (total 607):

----------------------
FR_MASTERSLICE      0
li1    296
met1    273
met2     38
met3      0
met4      0
----------------------
607


[INFO DRT-0195] Start 3rd optimization iteration.
Completing 10% with 3 violations.
elapsed time = 00:00:00, memory = 483.13 (MB).
Completing 20% with 0 violations.
elapsed time = 00:00:00, memory = 483.13 (MB).
[INFO DRT-0199]   Number of violations = 0.
[INFO DRT-0267] cpu time = 00:00:00, elapsed time = 00:00:00, memory = 483.13 (MB), peak = 483.13 (MB)
Total wire length = 1757 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 676 um.
Total wire length on LAYER met2 = 808 um.
Total wire length on LAYER met3 = 273 um.
Total wire length on LAYER met4 = 0 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 607.
Up-via summary (total 607):

----------------------
FR_MASTERSLICE      0
li1    296
met1    271
met2     40
met3      0
met4      0
----------------------
607


[INFO DRT-0198] Complete detail routing.
Total wire length = 1757 um.
Total wire length on LAYER li1 = 0 um.
Total wire length on LAYER met1 = 676 um.
Total wire length on LAYER met2 = 808 um.
Total wire length on LAYER met3 = 273 um.
Total wire length on LAYER met4 = 0 um.
Total wire length on LAYER met5 = 0 um.
Total number of vias = 607.
Up-via summary (total 607):

----------------------
FR_MASTERSLICE      0
li1    296
met1    271
met2     40
met3      0
met4      0
----------------------
607
```

Start coding or generate with AI.

Double-click (or enter) to edit

```
display(drt)
```

```
────────────────────────────────────────── Render Image (w/ KLayout) ──────────────────────────────────────────
[16:13:07] VERBOSE  Running 'KLayout.Render'…                                                          step.py:1088
[16:13:07] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_bv4ja5ff/klayout-render.log…     step.py:1268
```

Time Elapsed: 11.08s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Fill Insertion

Finally, as we're done placing all the essential cells, the only thing left to do is fill in the gaps.

We prioritize the use of decap (decoupling capacitor) cells, which further supports the power distribution network, but when there aren't any small enough cells, we just use regular fill cells.

```
FillInsertion = Step.factory.get("OpenROAD.FillInsertion")

fill = FillInsertion(state_in=drt.state_out)
fill.start()
```

```
────────────────────────────────────────────────────────── Fill Insertion ──────────────────────────────────────────────────────────
[16:13:09] VERBOSE  Running 'OpenROAD.FillInsertion'…                                                                   step.py:1088
[16:13:09] VERBOSE  Logging subprocess to                                                                                step.py:1268
                    openlane_run/100-openroad-fillinsertion/openroad-fillinsertion.log…
Reading OpenROAD database at '/content/openlane_run/99-openroad-detailedrouting/MIMO.odb'…
Reading library file at '/root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/lib/sky130_fd_sc_hd__tt_025C_1v80.lib'…
Reading design constraints file at '/content/openlane_ipynb/openlane/scripts/base.sdc'…
[16:13:09] WARNING  [STA-0366] port 'clk' not found.                                                                    openroad.py:235
[INFO] Using clock clk…
[INFO] Setting output delay to: 2
[INFO] Setting input delay to: 2
[16:13:09] WARNING  [STA-0366] port 'clk' not found.                                                                    openroad.py:235
[INFO] Setting load to: 0.033442
[INFO] Setting clock uncertainty to: 0.25
[INFO] Setting clock transition to: 0.149999999999999994448884876874217297881841659545898437 5
[16:13:10] WARNING  [STA-0419] transition time can not be specified for virtual clocks.                                  openroad.py:235
[INFO] Setting timing derate to: 5%
[16:13:10] WARNING  [STA-0450] virtual clock clk can not be propagated.                                                 openroad.py:235
sky130_ef_sc_hd__decap_12 sky130_fd_sc_hd__decap_8 sky130_fd_sc_hd__decap_6 sky130_fd_sc_hd__decap_4
sky130_fd_sc_hd__decap_3 sky130_fd_sc_hd__fill*
[INFO DPL-0001] Placed 102 filler instances.
Setting global connections for newly added cells…
[INFO] Setting global connections...
Writing OpenROAD database to '/content/openlane_run/100-openroad-fillinsertion/MIMO.odb'…
Writing netlist to '/content/openlane_run/100-openroad-fillinsertion/MIMO.nl.v'…
Writing powered netlist to '/content/openlane_run/100-openroad-fillinsertion/MIMO.pnl.v'…
Writing layout to '/content/openlane_run/100-openroad-fillinsertion/MIMO.def'…
Writing timing constraints to '/content/openlane_run/100-openroad-fillinsertion/MIMO.sdc'…
```

Format	Path
nl	openlane_run/100-openroad-fillinsertion/MIMO.nl.v
pnl	openlane_run/100-openroad-fillinsertion/MIMO.pnl.v
def	openlane_run/100-openroad-fillinsertion/MIMO.def
odb	openlane_run/100-openroad-fillinsertion/MIMO.odb

```
display(fill)
```

```
────────────────────────────────────────────────────── Render Image (w/ KLayout) ──────────────────────────────────────────────────────
[16:13:10] VERBOSE  Running 'KLayout.Render'…                                                                            step.py:1088
[16:13:10] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_h_pbu19q/klayout-render.log…                      step.py:1268
```

Time Elapsed: 1.34s

Views updated:

- Verilog Netlist
- Powered Verilog Netlist
- Design Exchange Format
- OpenDB Database
- Design Constraints

Preview:

Parasitics Extraction a.k.a. Resistance/Capacitance Extraction (RCX)

This step does not alter the design- rather, it computes the Parasitic elements of the circuit, which have an effect of timing, as we prepare to do the final timing analysis.

The parasitic elements are saved in the **Standard Parasitics Exchange Format**, or SPEF. OpenLane creates a SPEF file for each interconnect corner as described in the Corners and STA section of the documentation.

```
RCX = Step.factory.get("OpenROAD.RCX")

rcx = RCX(state_in=fill.state_out)
rcx.start()
```

```
─────────────────────────────── Parasitic Resistance/Capacitance Extraction ───────────────────────────────
[16:13:11] VERBOSE  Running 'OpenROAD.RCX'…                                                    step.py:1088
[16:13:11] INFO     Running RCX for corners matching nom_*                                  openroad.py:1748
                    (/content/openlane_run/101-openroad-rcx/nom/rcx.log)…
[16:13:11] INFO     Running RCX for corners matching min_*                                  openroad.py:1748
                    (/content/openlane_run/101-openroad-rcx/min/rcx.log)…
[16:13:11] VERBOSE  Logging subprocess to openlane_run/101-openroad-rcx/nom/rcx.log…            step.py:1268
[16:13:11] VERBOSE  Logging subprocess to openlane_run/101-openroad-rcx/min/rcx.log…            step.py:1268
[16:13:12] INFO     Finished RCX for corners matching nom_*.                                openroad.py:1757
[16:13:12] INFO     Running RCX for corners matching max_*                                  openroad.py:1748
                    (/content/openlane_run/101-openroad-rcx/max/rcx.log)…
[16:13:12] VERBOSE  Logging subprocess to openlane_run/101-openroad-rcx/max/rcx.log…            step.py:1268
[16:13:12] INFO     Finished RCX for corners matching min_*.                                openroad.py:1757
[16:13:12] INFO     Finished RCX for corners matching max_*.                                openroad.py:1757
```

Format	Path
nl	openlane_run/100-openroad-fillinsertion/MIMO.nl.v
pnl	openlane_run/100-openroad-fillinsertion/MIMO.pnl.v
def	openlane_run/100-openroad-fillinsertion/MIMO.def
odb	openlane_run/100-openroad-fillinsertion/MIMO.odb
sdc	openlane_run/100-openroad-fillinsertion/MIMO.sdc
spef	nom_* openlane_run/101-openroad-rcx/nom/MIMO.nom.spef min_* openlane_run/101-openroad-rcx/min/MIMO.min.spef max_* openlane_run/101-openroad-rcx/max/MIMO.max.spef

Static Timing Analysis (Post-PnR)

STA is a process that verifies that a chip meets certain constraints on clock and data timings to run at its rated clock speed. See Corners and STA in the documentation for more info.

This step generates two kinds of files:

- `.lib` : Liberty™-compatible Library files. Can be used to do static timing analysis when creating a design with this design as a sub-macro.
- `.sdf` : Standard Delay Format. Can be used with certain simulation software to do *dynamic* timing analysis.

Unfortunately, the `.lib` files coming out of OpenLane right now are not super reliable for timing purposes and are only provided for completeness. When using OpenLane-created macros withing other designs, it is best to use the macro's final netlist and extracted parasitics instead.

```
STAPostPNR = Step.factory.get("OpenROAD.STAPostPNR")

sta_post_pnr = STAPostPNR(state_in=rcx.state_out)
sta_post_pnr.start()
```

```
──────────────────────────────────────── Static Timing Analysis (Post-PnR) ────────────────────────────────────────
[16:13:12] VERBOSE  Running 'OpenROAD.STAPostPNR'…                                                   step.py:1088
[16:13:12] INFO     Starting STA for the nom_tt_025C_1v80 timing corner…                            openroad.py:561
[16:13:12] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/nom_tt_025C_1v80/sta.log…
[16:13:12] INFO     Starting STA for the nom_ss_100C_1v60 timing corner…                            openroad.py:561
[16:13:12] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/nom_ss_100C_1v60/sta.log…
[16:13:13] INFO     Finished STA for the nom_tt_025C_1v80 timing corner.                            openroad.py:576
[16:13:13] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/nom_tt_025C_1v80/filter_unannotated.log…
[16:13:13] INFO     Finished STA for the nom_ss_100C_1v60 timing corner.                            openroad.py:576
[16:13:13] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/nom_ss_100C_1v60/filter_unannotated.log…
[16:13:14] INFO     Starting STA for the nom_ff_n40C_1v95 timing corner…                            openroad.py:561
[16:13:14] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/nom_ff_n40C_1v95/sta.log…
[16:13:14] INFO     Starting STA for the min_tt_025C_1v80 timing corner…                            openroad.py:561
[16:13:14] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/min_tt_025C_1v80/sta.log…
[16:13:16] INFO     Finished STA for the min_tt_025C_1v80 timing corner.                            openroad.py:576
[16:13:16] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/min_tt_025C_1v80/filter_unannotated.log…
[16:13:17] INFO     Starting STA for the min_ss_100C_1v60 timing corner…                            openroad.py:561
[16:13:17] INFO     Finished STA for the nom_ff_n40C_1v95 timing corner.                            openroad.py:576
[16:13:17] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/min_ss_100C_1v60/sta.log…
[16:13:17] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/nom_ff_n40C_1v95/filter_unannotated.log…
[16:13:18] INFO     Finished STA for the min_ss_100C_1v60 timing corner.                            openroad.py:576
[16:13:18] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/min_ss_100C_1v60/filter_unannotated.log…
[16:13:18] INFO     Starting STA for the min_ff_n40C_1v95 timing corner…                            openroad.py:561
[16:13:18] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/min_ff_n40C_1v95/sta.log…
[16:13:19] INFO     Starting STA for the max_tt_025C_1v80 timing corner…                            openroad.py:561
[16:13:19] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/max_tt_025C_1v80/sta.log…
[16:13:20] INFO     Finished STA for the max_tt_025C_1v80 timing corner.                            openroad.py:576
[16:13:20] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/max_tt_025C_1v80/filter_unannotated.log…
[16:13:20] INFO     Finished STA for the min_ff_n40C_1v95 timing corner.                            openroad.py:576
[16:13:20] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/min_ff_n40C_1v95/filter_unannotated.log…
[16:13:21] INFO     Starting STA for the max_ss_100C_1v60 timing corner…                            openroad.py:561
[16:13:21] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/max_ss_100C_1v60/sta.log…
[16:13:22] INFO     Starting STA for the max_ff_n40C_1v95 timing corner…                            openroad.py:561
[16:13:22] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/max_ff_n40C_1v95/sta.log…
[16:13:22] INFO     Finished STA for the max_ss_100C_1v60 timing corner.                            openroad.py:576
[16:13:22] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/max_ss_100C_1v60/filter_unannotated.log…
[16:13:25] INFO     Finished STA for the max_ff_n40C_1v95 timing corner.                            openroad.py:576
[16:13:25] VERBOSE  Logging subprocess to                                                             step.py:1268
                    openlane_run/102-openroad-stapostpnr/max_ff_n40C_1v95/filter_unannotated.log…
```

Corner/Group	Hold Worst Slack	Reg to Reg Paths	Hold TNS	Hold Vio Count	of whi… reg to reg	Setup Worst Slack	Reg to Reg Pat…	Setup TNS	Set… Vio Cou…	of which reg to reg	Max Cap Vio…	Max Slew Viol…
Overall	4.02…	N/A	0.0…	0	0	-0.1…	N/A	-0.3…	6	0	0	13
nom_tt_025C_1v80	4.16…	N/A	0.0…	0	0	2.77…	N/A	0.00…	0	0	0	0
nom_ss_100C_1v60	4.46…	N/A	0.0…	0	0	-0.1…	N/A	-0.2…	2	0	0	13
nom_ff_n40C_1v95	4.03…	N/A	0.0…	0	0	3.89…	N/A	0.00…	0	0	0	0
min_tt_025C_1v80	4.16…	N/A	0.0…	0	0	2.80…	N/A	0.00…	0	0	0	0
min_ss_100C_1v60	4.45…	N/A	0.0…	0	0	-0.0…	N/A	-0.1…	2	0	0	13
min_ff_n40C_1v95	4.02…	N/A	0.0…	0	0	3.91…	N/A	0.00…	0	0	0	0
max_tt_025C_1v80	4.17…	N/A	0.0…	0	0	2.75…	N/A	0.00…	0	0	0	0
max_ss_100C_1v60	4.47…	N/A	0.0…	0	0	-0.1…	N/A	-0.3…	2	0	0	13
max_ff_n40C_1v95	4.03…	N/A	0.0…	0	0	3.87…	N/A	0.00…	0	0	0	0

Corner/Group	Hold Worst Slack	Reg to Reg Paths	Hold TNS	Hold Vio Count	of which reg to reg	Setup Worst Slack	Reg to Reg Paths	Setup TNS	Setup Vio Count	of which reg to reg	Max Cap Violatio…	Max Slew Violati…
Overall	4.0281	N/A	0.0000	0	0	-0.1825	N/A	-0.3622	6	0	0	13
nom_tt_025C_1v80	4.1661	N/A	0.0000	0	0	2.7755	N/A	0.0000	0	0	0	0
nom_ss_100C_1v60	4.4669	N/A	0.0000	0	0	-0.1361	N/A	-0.2696	2	0	0	13
nom_ff_n40C_1v95	4.0302	N/A	0.0000	0	0	3.8964	N/A	0.0000	0	0	0	0
min_tt_025C_1v80	4.1606	N/A	0.0000	0	0	2.8000	N/A	0.0000	0	0	0	0
min_ss_100C_1v60	4.4577	N/A	0.0000	0	0	-0.0970	N/A	-0.1917	2	0	0	13
min_ff_n40C_1v95	4.0281	N/A	0.0000	0	0	3.9127	N/A	0.0000	0	0	0	0
max_tt_025C_1v80	4.1706	N/A	0.0000	0	0	2.7511	N/A	0.0000	0	0	0	0
max_ss_100C_1v60	4.4741	N/A	0.0000	0	0	-0.1825	N/A	-0.3622	2	0	0	13
max_ff_n40C_1v95	4.0321	N/A	0.0000	0	0	3.8797	N/A	0.0000	0	0	0	0

Format	Path	
nl	openlane_run/100-openroad-fillinsertion/MIMO.nl.v	
pnl	openlane_run/100-openroad-fillinsertion/MIMO.pnl.v	
def	openlane_run/100-openroad-fillinsertion/MIMO.def	
odb	openlane_run/100-openroad-fillinsertion/MIMO.odb	
sdc	openlane_run/100-openroad-fillinsertion/MIMO.sdc	
sdf	nom_tt_025C_1v80	openlane_run/102-openroad-stapostpnr/nom_tt_025C_1v80/MIMO__nom_tt_025C_1v80.sdf
	nom_ss_100C_1v60	openlane_run/102-openroad-stapostpnr/nom_ss_100C_1v60/MIMO__nom_ss_100C_1v60.sdf
	nom_ff_n40C_1v95	openlane_run/102-openroad-stapostpnr/nom_ff_n40C_1v95/MIMO__nom_ff_n40C_1v95.sdf
	min_tt_025C_1v80	openlane_run/102-openroad-stapostpnr/min_tt_025C_1v80/MIMO__min_tt_025C_1v80.sdf
	min_ss_100C_1v60	openlane_run/102-openroad-stapostpnr/min_ss_100C_1v60/MIMO__min_ss_100C_1v60.sdf
	min_ff_n40C_1v95	openlane_run/102-openroad-stapostpnr/min_ff_n40C_1v95/MIMO__min_ff_n40C_1v95.sdf
	max_tt_025C_1v80	openlane_run/102-openroad-stapostpnr/max_tt_025C_1v80/MIMO__max_tt_025C_1v80.sdf
	max_ss_100C_1v60	openlane_run/102-openroad-stapostpnr/max_ss_100C_1v60/MIMO__max_ss_100C_1v60.sdf
	max_ff_n40C_1v95	openlane_run/102-openroad-stapostpnr/max_ff_n40C_1v95/MIMO__max_ff_n40C_1v95.sdf
spef	nom_*	openlane_run/101-openroad-rcx/nom/MIMO.nom.spef
	min_*	openlane_run/101-openroad-rcx/min/MIMO.min.spef
	max_*	openlane_run/101-openroad-rcx/max/MIMO.max.spef
lib	nom_tt_025C_1v80	openlane_run/102-openroad-stapostpnr/nom_tt_025C_1v80/MIMO__nom_tt_025C_1v80.lib
	nom_ss_100C_1v60	openlane_run/102-openroad-stapostpnr/nom_ss_100C_1v60/MIMO__nom_ss_100C_1v60.lib
	nom_ff_n40C_1v95	openlane_run/102-openroad-stapostpnr/nom_ff_n40C_1v95/MIMO__nom_ff_n40C_1v95.lib
	min_tt_025C_1v80	openlane_run/102-openroad-stapostpnr/min_tt_025C_1v80/MIMO__min_tt_025C_1v80.lib
	min_ss_100C_1v60	openlane_run/102-openroad-stapostpnr/min_ss_100C_1v60/MIMO__min_ss_100C_1v60.lib

Stream-out

Stream-out is the process of converting the designs from the abstract formats using during floorplanning, placement and routing into a concrete format called GDSII (lit. Graphic Design System 2), which is the final file that is then sent for fabrication.

```
StreamOut = Step.factory.get("KLayout.StreamOut")

gds = StreamOut(state_in=sta_post_pnr.state_out)
gds.start()
```

```
────────────────────────────────────── GDSII Stream Out (KLayout) ──────────────────────────────────────
[16:13:26] VERBOSE  Running 'KLayout.StreamOut'…                                                  step.py:1088
[16:13:26] VERBOSE  Logging subprocess to openlane_run/103-klayout-streamout/klayout-streamout.log…  step.py:1268
[INFO] Clearing cells…
[INFO] Merging GDS files…
[INFO] Copying top level cell 'MIMO'…
[INFO] Checking for missing GDS…
[INFO] All LEF cells have matching GDS cells.
[INFO] Writing out GDS '/content/openlane_run/103-klayout-streamout/MIMO.klayout.gds'…
[INFO] Done.
```

Format	Path
nl	openlane_run/100-openroad-fillinsertion/MIMO.nl.v
pnl	openlane_run/100-openroad-fillinsertion/MIMO.pnl.v
def	openlane_run/100-openroad-fillinsertion/MIMO.def
odb	openlane_run/100-openroad-fillinsertion/MIMO.odb
sdc	openlane_run/100-openroad-fillinsertion/MIMO.sdc
sdf	nom_tt_025C_1v80 openlane_run/102-openroad-stapostpnr/nom_tt_025C_1v80/MIMO__nom_tt_025C_1v80.sdf
	nom_ss_100C_1v60 openlane_run/102-openroad-stapostpnr/nom_ss_100C_1v60/MIMO__nom_ss_100C_1v60.sdf
	nom_ff_n40C_1v95 openlane_run/102-openroad-stapostpnr/nom_ff_n40C_1v95/MIMO__nom_ff_n40C_1v95.sdf
	min_tt_025C_1v80 openlane_run/102-openroad-stapostpnr/min_tt_025C_1v80/MIMO__min_tt_025C_1v80.sdf
	min_ss_100C_1v60 openlane_run/102-openroad-stapostpnr/min_ss_100C_1v60/MIMO__min_ss_100C_1v60.sdf
	min_ff_n40C_1v95 openlane_run/102-openroad-stapostpnr/min_ff_n40C_1v95/MIMO__min_ff_n40C_1v95.sdf
	max_tt_025C_1v80 openlane_run/102-openroad-stapostpnr/max_tt_025C_1v80/MIMO__max_tt_025C_1v80.sdf
	max_ss_100C_1v60 openlane_run/102-openroad-stapostpnr/max_ss_100C_1v60/MIMO__max_ss_100C_1v60.sdf
	max_ff_n40C_1v95 openlane_run/102-openroad-stapostpnr/max_ff_n40C_1v95/MIMO__max_ff_n40C_1v95.sdf
spef	nom_* openlane_run/101-openroad-rcx/nom/MIMO.nom.spef
	min_* openlane_run/101-openroad-rcx/min/MIMO.min.spef
	max_* openlane_run/101-openroad-rcx/max/MIMO.max.spef
lib	nom_tt_025C_1v80 openlane_run/102-openroad-stapostpnr/nom_tt_025C_1v80/MIMO__nom_tt_025C_1v80.lib
	nom_ss_100C_1v60 openlane_run/102-openroad-stapostpnr/nom_ss_100C_1v60/MIMO__nom_ss_100C_1v60.lib
	nom_ff_n40C_1v95 openlane_run/102-openroad-stapostpnr/nom_ff_n40C_1v95/MIMO__nom_ff_n40C_1v95.lib
	min_tt_025C_1v80 openlane_run/102-openroad-stapostpnr/min_tt_025C_1v80/MIMO__min_tt_025C_1v80.lib
	min_ss_100C_1v60 openlane_run/102-openroad-stapostpnr/min_ss_100C_1v60/MIMO__min_ss_100C_1v60.lib
	min_ff_n40C_1v95 openlane_run/102-openroad-stapostpnr/min_ff_n40C_1v95/MIMO__min_ff_n40C_1v95.lib
	max_tt_025C_1v80 openlane_run/102-openroad-stapostpnr/max_tt_025C_1v80/MIMO__max_tt_025C_1v80.lib
	max_ss_100C_1v60 openlane_run/102-openroad-stapostpnr/max_ss_100C_1v60/MIMO__max_ss_100C_1v60.lib
	max_ff_n40C_1v95 openlane_run/102-openroad-stapostpnr/max_ff_n40C_1v95/MIMO__max_ff_n40C_1v95.lib
gds	openlane_run/103-klayout-streamout/MIMO.gds
klayout_gds	openlane_run/103-klayout-streamout/MIMO.klayout.gds

```
display(gds)
```

```
──────────────────────────────────────── Render Image (w/ KLayout) ────────────────────────────────────────
[16:13:27] VERBOSE  Running 'KLayout.Render'…                                                   step.py:1088
[16:13:27] VERBOSE  Logging subprocess to ../tmp/openlane_klayout_tmp_mk1fn4k7/klayout-render.log…  step.py:1268
```

Time Elapsed: 0.63s

Views updated:

- GDSII Stream
- GDSII Stream (KLayout)

Preview:

Design Rule Checks (DRC)

DRC determines that the final layout does not violate any of the rules set by the foundry to ensure the design is actually manufacturable- for example, not enough space between two wires, *too much* space between tap cells, and so on.

A design not passing DRC will typically be rejected by the foundry, who also run DRC on their side.

```
DRC = Step.factory.get("Magic.DRC")

drc = DRC(state_in=gds.state_out)
drc.start()
```

```
──────────────────────────────────────────────── Design Rule Checks ────────────────────────────────────────────────
[16:13:27] VERBOSE  Running 'Magic.DRC'…                                                                  step.py:1088
[16:13:27] VERBOSE  Logging subprocess to openlane_run/104-magic-drc/magic-drc.log…                       step.py:1268

Magic 8.3 revision 483 - Compiled on Sun Jun  2 18:57:41 UTC 2024.
Starting magic under Tcl interpreter
Using the terminal as the console.
Using NULL graphics device.
Processing system .magicrc file
Sourcing design .magicrc for technology sky130A ...
2 Magic internal units = 1 Lambda
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
ubm
Scaled tech values by 2 / 1 to match internal grid scaling
Loading sky130A Device Generator Menu ...
Loading "/content/openlane_ipynb/openlane/scripts/magic/wrapper.tcl" from command line.
Warning: Calma reading is not undoable!  I hope that's OK.
Library written using GDS-II Release 6.0
Library name: LIB
Reading "VIA_M2M3_PR".
Reading "VIA_M1M2_PR".
Reading "VIA_L1M1_PR_MR".
Reading "VIA_via2_3_2000_480_1_6_320_320".
Reading "VIA_via3_4_2000_480_1_5_400_400".
Reading "VIA_via4_5_2000_480_1_5_400_400".
Reading "sky130_fd_sc_hd__buf_2".
Reading "sky130_fd_sc_hd__conb_1".
Reading "sky130_fd_sc_hd__mux2_1".
Reading "sky130_fd_sc_hd__a31o_2".
Reading "sky130_fd_sc_hd__a21o_2".
Reading "sky130_fd_sc_hd__o211ai_2".
Reading "sky130_fd_sc_hd__o21ba_2".
Reading "sky130_fd_sc_hd__and2_2".
Reading "sky130_fd_sc_hd__o311ai_2".
Reading "sky130_fd_sc_hd__or3_2".
Reading "sky130_fd_sc_hd__o32a_2".
Reading "sky130_fd_sc_hd__or2_2".
Reading "sky130_fd_sc_hd__o211a_2".
Reading "sky130_fd_sc_hd__o31ai_2".
Reading "sky130_fd_sc_hd__a31oi_2".
Reading "sky130_fd_sc_hd__nor2_2".
Reading "sky130_fd_sc_hd__o22a_2".
Reading "sky130_fd_sc_hd__nand3_2".
Reading "sky130_fd_sc_hd__a21bo_2".
Reading "sky130_fd_sc_hd__o41a_2".
Reading "sky130_fd_sc_hd__and3b_2".
Reading "sky130_fd_sc_hd__and3_2".
Reading "sky130_fd_sc_hd__a21boi_2".
Reading "sky130_fd_sc_hd__o221ai_2".
Reading "sky130_fd_sc_hd__a2bb2o_2".
Reading "sky130_fd_sc_hd__a22oi_2".
Reading "sky130_fd_sc_hd__a21oi_2".
Reading "sky130_fd_sc_hd__nand2_2".
Reading "sky130_fd_sc_hd__o21ai_2".
Reading "sky130_fd_sc_hd__xor2_2".
Reading "sky130_fd_sc_hd__xnor2_2".
Reading "sky130_fd_sc_hd__o21a_2".
Reading "sky130_fd_sc_hd__and2b_2".
Reading "sky130_fd_sc_hd__nand2b_2".
Reading "sky130_fd_sc_hd__inv_2".
Reading "sky130_fd_sc_hd__tapvpwrvgnd_1".
Reading "sky130_fd_sc_hd__decap_6".
Reading "sky130_fd_sc_hd__decap_8".
Reading "sky130_fd_sc_hd__decap_4".
Reading "sky130_fd_sc_hd__fill_2".
Reading "sky130_fd_sc_hd__decap_3".
Reading "sky130_fd_sc_hd__fill_1".
Reading "sky130_ef_sc_hd__decap_12".
Reading "MIMO".
[INFO] Loading MIMO

DRC style is now "drc(full)"
Loading DRC CIF style.
```

SPICE Extraction for Layout vs. Schematic Check

This step tries to reconstruct a SPICE netlist from the GDSII file, so it can later be used for the **Layout vs. Schematic** (LVS) check.

```
SpiceExtraction = Step.factory.get("Magic.SpiceExtraction")

spx = SpiceExtraction(state_in=drc.state_out)
spx.start()
```

```
──────────────────────────────────────────────── SPICE Model Extraction ────────────────────────────────────────────
[16:13:29] VERBOSE  Running 'Magic.SpiceExtraction'…                                                       step.py:1088
[16:13:29] VERBOSE  Logging subprocess to                                                                  step.py:1268
                    openlane_run/105-magic-spiceextraction/magic-spiceextraction.log…

Magic 8.3 revision 483 - Compiled on Sun Jun  2 18:57:41 UTC 2024.
Starting magic under Tcl interpreter
Using the terminal as the console.
Using NULL graphics device.
Processing system .magicrc file
Sourcing design .magicrc for technology sky130A ...
2 Magic internal units = 1 Lambda
Input style sky130(): scaleFactor=2, multiplier=2
The following types are not handled by extraction and will be treated as non-electrical types:
ubm
Scaled tech values by 2 / 1 to match internal grid scaling
Loading sky130A Device Generator Menu ...
Loading "/content/openlane_ipynb/openlane/scripts/magic/wrapper.tcl" from command line.
> lef read /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef
Reading LEF data from file /root/.volare/sky130A/libs.ref/sky130_fd_sc_hd/techlef/sky130_fd_sc_hd__nom.tlef.
```