Computer Architecture II, Fall 2022, CAT Assignment

To start: take the CAT implementation, and modify as you would like or as necessary to be able to add the following instructions.

Please do each of the following:

1. Complete implementation of the "Store" instruction, show a small test program (example) to show that it works correctly.

2. Write a small (CAT) program to add two 1 x N vectors (that is add the corresponding values in two lists of numbers), for example:
   [1, 2, 3] + [4, 5, 6] ->
   -> [5, 7, 9]
   Where N will be less than 20
   Instrument the CAT VM to count number of instructions executed, clock cycles, as well as number of memory references

3. Implement (CAT) data hazard detection, as if the CAT were pipelined with a 5 stage pipeline,
   That is show that you can detect RAW data hazards (for this assignment, for the CAT implementation:
   Implement a scoreboard (or similar) to detect data hazards
   Show where these hazards exist (in the source asm/binary code), and the scoreboard results,
   Why these hazards exist, how long it is necessary to stall.
   All of the preceding should, of course, be implemented in code, show demo code to test your implementation, and results printed.

4. Implement control (branch) hazard detection on CAT (similar to the preceding)
   Show where these hazards exist (in the source asm/binary code), and the scoreboard results,
   Why these hazards exist, how long it is necessary to stall

   (Similarly, please implement in code, show demo code to test your implementation, and results printed.)

5. Implement one bit branch prediction for CAT (similar to preceding.)

6. Describe how a VLIW implementation with two slots VLIW instructions, could be:
   (a) implemented
   (b) show a demo test program
   (c) You DO NOT need to implement this, just describe, however you may receive bonus points if implemented

All work MUST be your own, you may use references IF the reference is provided.
Submission should be in: Code and a small writeup.