UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 5 Examination in Engineering: January 2024

Module Number: EE5260 **Module Name: Hardware Description Language**

[Three Hours]

[Answer all questions, each question carries 10 marks]

Q1 a) What are the key differences between programming languages for Central Processing Units (CPUs) and Hardware Description Languages (HDLs)?

[1.0 Mark]

b) (i). Compare the advantages and disadvantages of Application-Specific Integrated Circuits (ASICs) and Field-Programmable Gate Arrays (FPGAs).

[2.0 Marks]

(ii). Explain the significance of HDL in the Very Large Scale Integration (VLSI) design process.

[2.0 Marks]

c) (i). Name and describe two (02) main components of a VHDL design.

[1.0 Mark]

(ii). Why is drawing a black-box diagram when using VHDL to model digital circuits a good approach?

[1.0 Mark]

(iii). Write the VHDL entity declaration that describes the black-box diagram shown in Figure Q1.c.

[3.0 Marks]

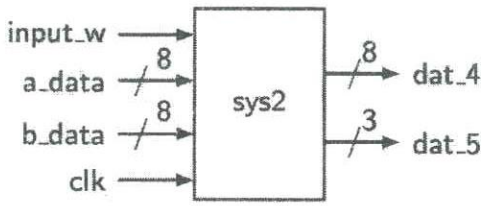

Figure Q1.c

Q2 a) Write VHDL models that implement the following Boolean functions using concurrent signal assignments.

(i). $F(A,B) = \bar{A}B + A + A\bar{B}$

(ii). $F(A,B,C,D) = (\bar{A}+B).(\bar{B}+C+\bar{D}).(\bar{A}+D)$

[3.0 Marks]

b) Write VHDL models that implement the following Boolean functions using conditional signal assignments.

(i). $F(A,B,C,D) = \bar{A}C\bar{D} + \bar{B}C + BC\bar{D}$

(ii). $F(A,B,C,D) = (\bar{A}+B).(\bar{B}+C+\bar{D}).(\bar{A}+C)$

[3.0 Marks]

c) Provide a VHDL model that can be used to implement the circuit shown in Figure Q2.c.

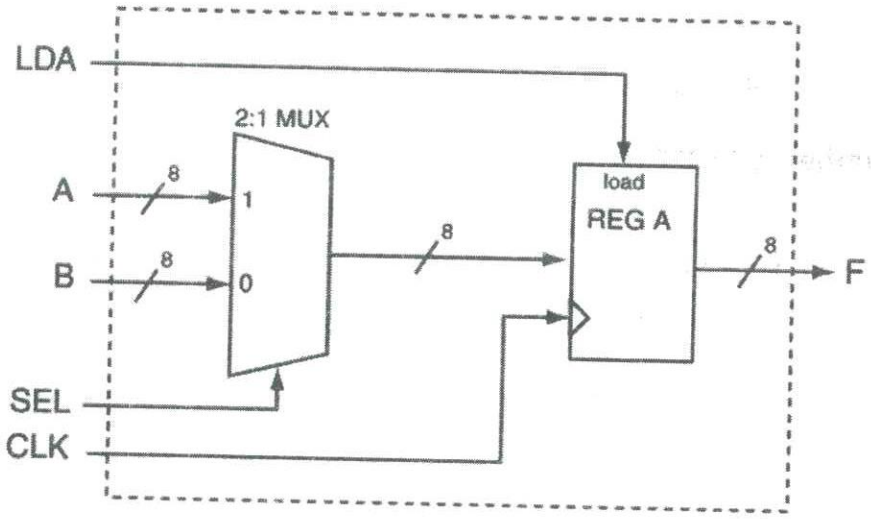

Figure Q2.c

[4.0 Marks]

Q3 a) Draw the basic flow involved in FPGA design and explain the "Synthesis" step.

[4.0 Marks]

b) Johnson counter, also known as the creeping counter, is an example of a synchronous counter. In the Johnson counter, the complemented (inverted) output of the last flip-flop (FF2) is connected to the input of the first flip-flop (FF0). Figure Q3.a shows a 3-bit Johnson counter. Table Q3.a represents the truth table of the specific counter.

(i). Copy Table Q3.a. into the answer sheet and fill in all the missing states of FF0, FF1, and FF2.

[1.0 Mark]

(ii). Draw the state diagram of a 3-bit up and down Johnson counter.

[2.0 Marks]

(iii). Write a Verilog module to implement a 3-bit up and down Johnson counter.

[3.0 Marks]

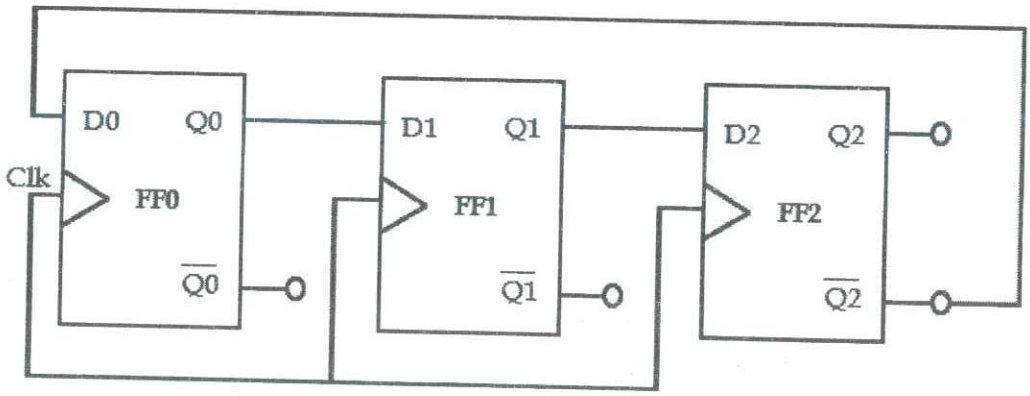

Figure Q3.a: A 3-bit Johnson Counter.

Table Q3.a: The truth table of the 3 – bit Johnson Counter.

Clk	FF0	FF1	FF2
0	0	0	0
1	1	0	0
2	1	1	0
⋮	⋮	⋮	⋮
	0	0	0

Q4 a) Briefly explain the "Blocking" and "Non-blocking" assignments of Verilog with examples.

[2.0 Marks]

b) Explain the "Incomplete specification" in Verilog designs.

[1.0 Mark]

c) (i). Design an 8-bit ALU in Verilog that supports addition, subtraction, AND, OR, and XOR operations. Provide the Verilog code for the ALU module.

[3.0 Marks]

(ii). Create a test bench to verify the functionality of the ALU designed in Q4.c.i. for different input combinations and operations (a single stimulus for each operation is adequate).

[4.0 Marks]

Q5 a) Explain the differences in the "always" block when included in a combinational design module and in a sequential design module.

[2.0 Marks]

b) (i). Write a Verilog module to implement a 4 to 1 multiplexer.

[2.0 Marks]

(ii). Design a Verilog module for an 8 to 1 multiplexer by using two 4 to 1 multiplexer designed in Q5.b.i and one 2 to 1 multiplexer.
(Hint: The inputs should be fed from the 4 to 1 multiplexer and the final output should be obtained through the 2 to 1 multiplexer.)

[4.0Marks]

(iii). Write a test bench to verify the design of the 8 to 1 multiplexer.

[2.0 Marks]