



UNIVERSITY OF RUHUNA

Faculty of Engineering

End-Semester 6 Examination in Engineering: September 2023

Module Number: EE6205

Module Name: Hardware Description Language
[Three Hours]

[Answer all questions, each question carries 10 marks]

- Q1 a)** i) Compare the advantages and disadvantages of Application-Specific Integrated Circuits (ASICs) and Field-Programmable Gate Arrays (FPGAs). [2.0 Marks]
ii) Explain the significance of Hardware Description Language (HDL) in the VLSI design process. [2.0 Marks]
iii) Explain the role of the Test Bench in VLSI design verification. [1.0 Mark]
- b) Draw the block diagram of the design process of an FPGA. [2.5 Marks]
- c) i) Briefly explain the netlist mapping and routing. [1.0 Mark]
ii) Briefly explain the timing optimization. [0.5 Marks]
- d) What are the key distinctions between programming languages for Central Processing Units (CPUs) and Hardware Description Languages (HDLs)? [1.0 Mark]

- Q2 a)** i) Name and describe two (02) main components in a VHDL design. [0.5 Marks]
ii) Why is it beneficial to create a black-box diagram when using VHDL for digital circuit modeling? [1.0 Mark]
iii) Provide the black-box diagram that is defined by the following VHDL entity declaration,

```
entity ckt_e is
port (
    RAM_CS, RAM_WE, RAM_OE : in std_logic;
    SEL_OP1, SEL_OP2 : in std_logic_vector(3 downto 0);
    RAM_DATA_IN : in std_logic_vector(7 downto 0);
    RAM_ADDR_IN : in std_logic_vector(9 downto 0);
    RAM_DATA_OUT : out std_logic_vector(7 downto 0));
end ckt_e;
```

[1.5 Marks]

- b) Write VHDL models that implement the following Boolean functions using concurrent signal assignment.
- $F(A, B) = \bar{A}\bar{B} + A + A\bar{B}$ [1.0 Mark]
 - $F(A, B, C, D) = (\bar{A} + B).(\bar{B} + C + \bar{D}).(\bar{A} + D)$ [2.0 Marks]
- c) Write VHDL models that implement the following Boolean functions using conditional signal assignment.
- $F(A, B, C, D) = \bar{A}C\bar{D} + \bar{B}C + BC\bar{D}$ [2.0 Marks]
 - $F(A, B, C, D) = (\bar{A} + B).(\bar{B} + C + \bar{D}).(\bar{A} + D)$ [2.0 Marks]

- Q3 a) i) Explain the difference between types 'wire' and 'reg' in Verilog. [1.0 Mark]
- ii) Explain the purpose of always blocks in Verilog and provide an example. [2.0 Marks]
- b) i) Design an 8-bit ALU in Verilog that supports addition, subtraction, AND, OR, and XOR operations. Provide the Verilog code for the ALU module. [3.0 Marks]
- ii) Create a testbench to verify the functionality of your ALU for different input combinations and operations (a single stimulus for each operation is enough). [4.0 Marks]

Q4 Figure Q4 shows a schematic diagram of a Serial-in Serial-out (SISO) Shift register.

- a) Write a VHDL code to implement the SISO Shift register shown in Figure Q4. [3.0 Marks]
- b) i) Explain the difference between blocking and non-blocking statements in Verilog. [1.0 Mark]
- ii) Write a Verilog code for a D flip-flop with an asynchronous reset. [1.5 Marks]
- iii) Write a Verilog code for a D flip-flop with a synchronous reset. [1.5 Marks]
- iv) Write a Verilog code to implement the SISO Shift register shown in Figure Q4. [3.0 Marks]

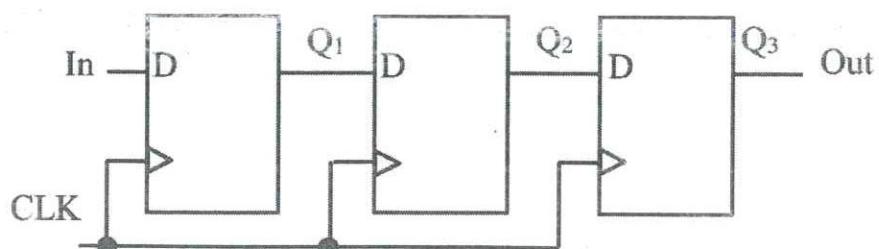
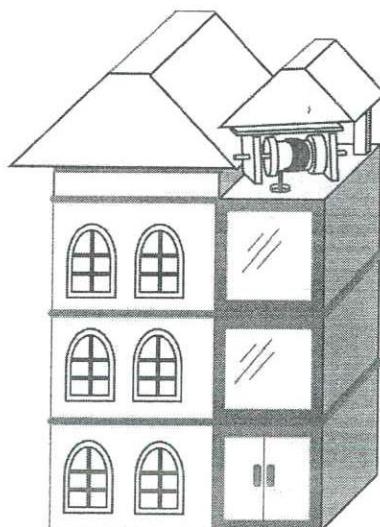


Figure Q4. Schematic diagram of a Serial-in Serial-out (SISO) Shift register.

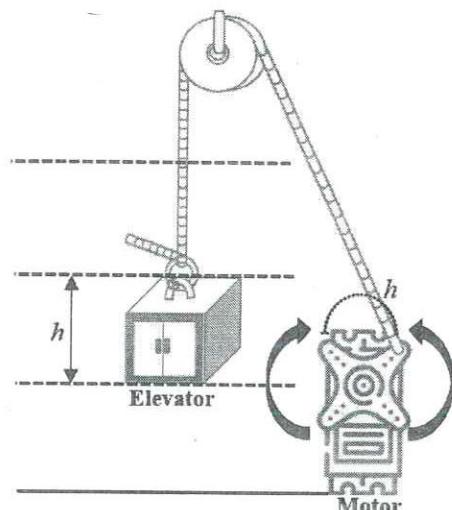
Q5 Design a control panel for an elevator installed in a three-story building (Figure Q5).

Assumptions:

- The elevator has a keypad with press buttons for each floor; only one button can be activated at a time.
- The elevator's door opens and closes automatically.
- The elevator is allowed to move only when the door is fully closed.



a) Building



b) Motor controlling

Figure Q5. Controlling an elevator installed in a three-story (three-floor) building.

- Define the states and the possible inputs in the problem statements. [2.0 Marks]
- i) Draw the finite state diagram with all the possible states and transitions. [2.0 Marks]
ii) If the elevator's behavior is controlled by a motor, include the motor rotation for the same state diagram. [1.0 Mark]
- Write the Verilog code to implement the finite state diagram. [5.0 Marks]