Lab Sheet

IA 3017 – Introduction to Field Programmable Gate Arrays

Department of Instrumentation & Automation Technology

University of Colombo

Practical 05 – Shift Registers

Introduction

A register stores data i.e. logic levels, zeros and ones. A shift register has the capability of shifting the data stored in the register from left to right or right to left. Shift registers consist of D flip-flops as shown in the figure below.

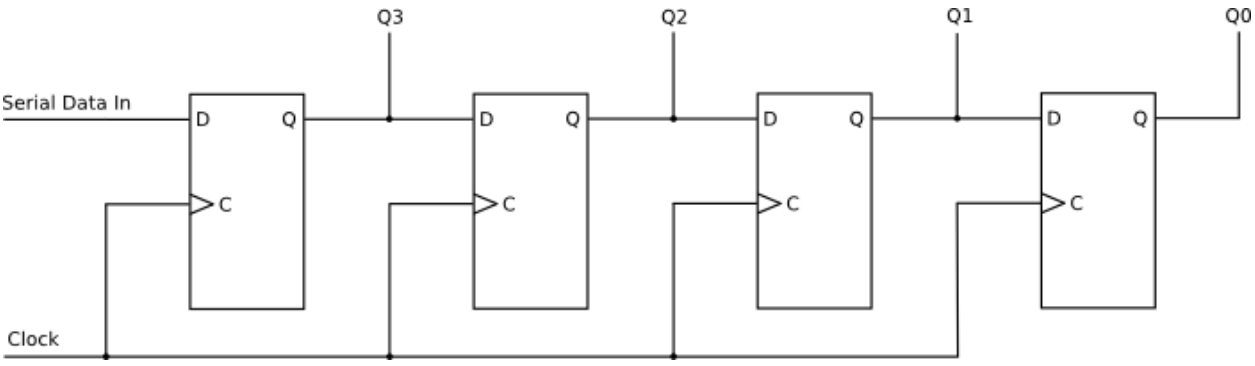

Figure 1 - Four-bit shift register

This is a four-bit shift register and therefore consists of four D flip-flops. This shift register is configured to shift data from the left to the right. Data is fed into the D input of the first flip-flop on the left. This data can be either a 0 or a 1 and will be shifted to the right on each rising edge of the clock pulse. Whatever the state of the data input when the rising edge of the clock pulse occurs will be the logic level that is shifted into the first flip-flop. The data in each flip-flop will be shifted to the flip-flop on its right when the rising edge of the clock pulse occurs.

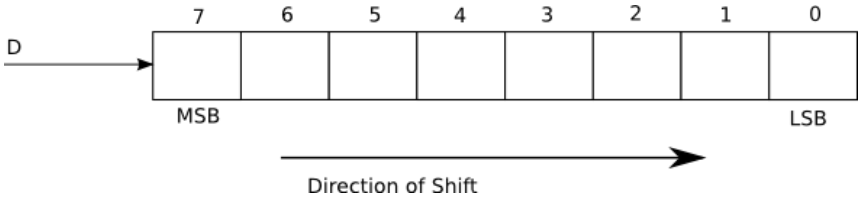

Figure 2 - Data direction of a shift register

The figure 2 shows an eight-bit shift register which data is shifted from left to right – from Most Significant Bit (MSB) to Least Significant Bit (LSB). It is also possible to shift data from right to left and to use the LSB as an input for serial data.

- **Experiment 01**
    - Construct a four-bit shift register circuit using a FPGA development board. Write the VHDL code and simulate the circuit using Modelsim-altera. Use 50 MHz clock input as clock pulse (PIN_M9)

- **Experiment 02**
    - Construct a eight-bit shift register circuit using a FPGA development board. Write the VHDL code and simulate the circuit using Modelsim-altera. Use 50 MHz clock input as clock pulse (PIN_M9)