



AES-ULTRA96-G

Revision:1

www.ultra96.org

AES-ULTRA96-G

Avnet Design Services

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Project Name: AES-ULTRA96-G PCB Rev: 1 BOM: 01 Variant: 00
 Doc Num: SCH-US1DEV Date: 3/9/2018 Time: 12:24:07 pm
 Sheet Title: Avnet Lead Sheet Size: B Sheet: 1 of 27

A

A

B

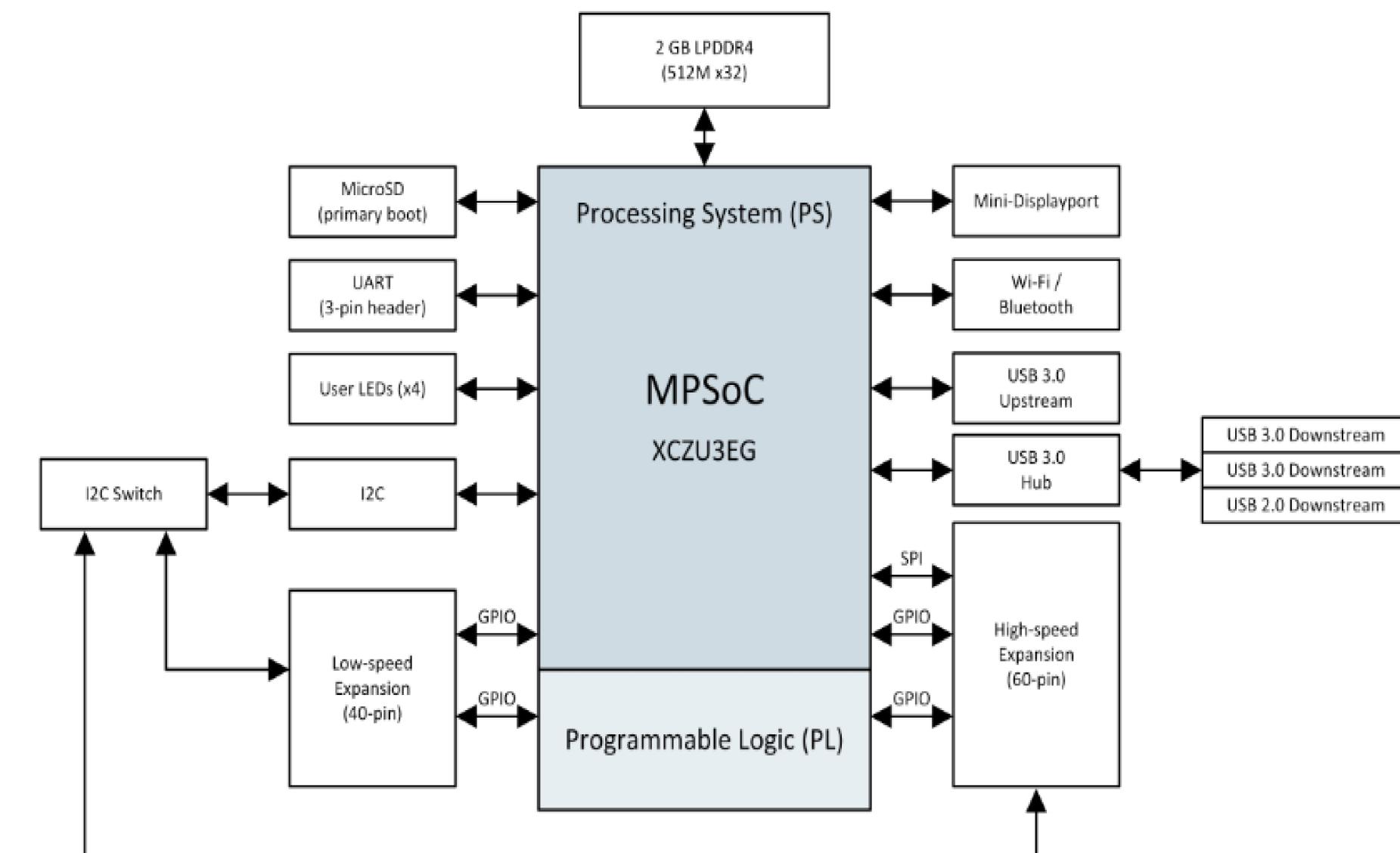
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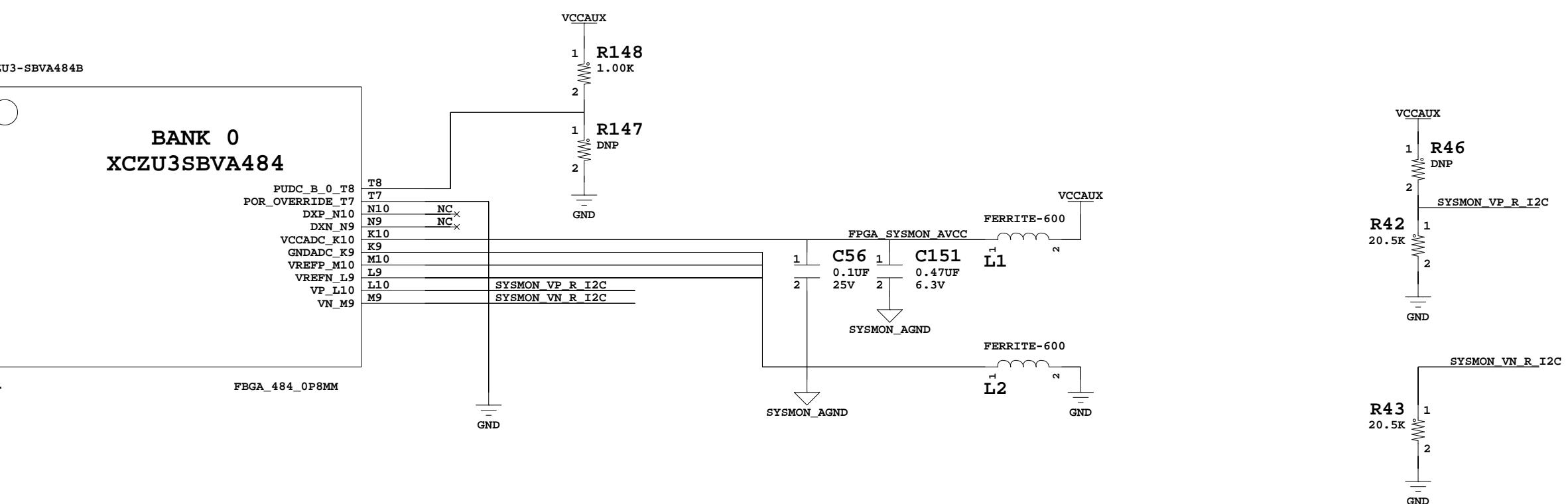
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C

D

D

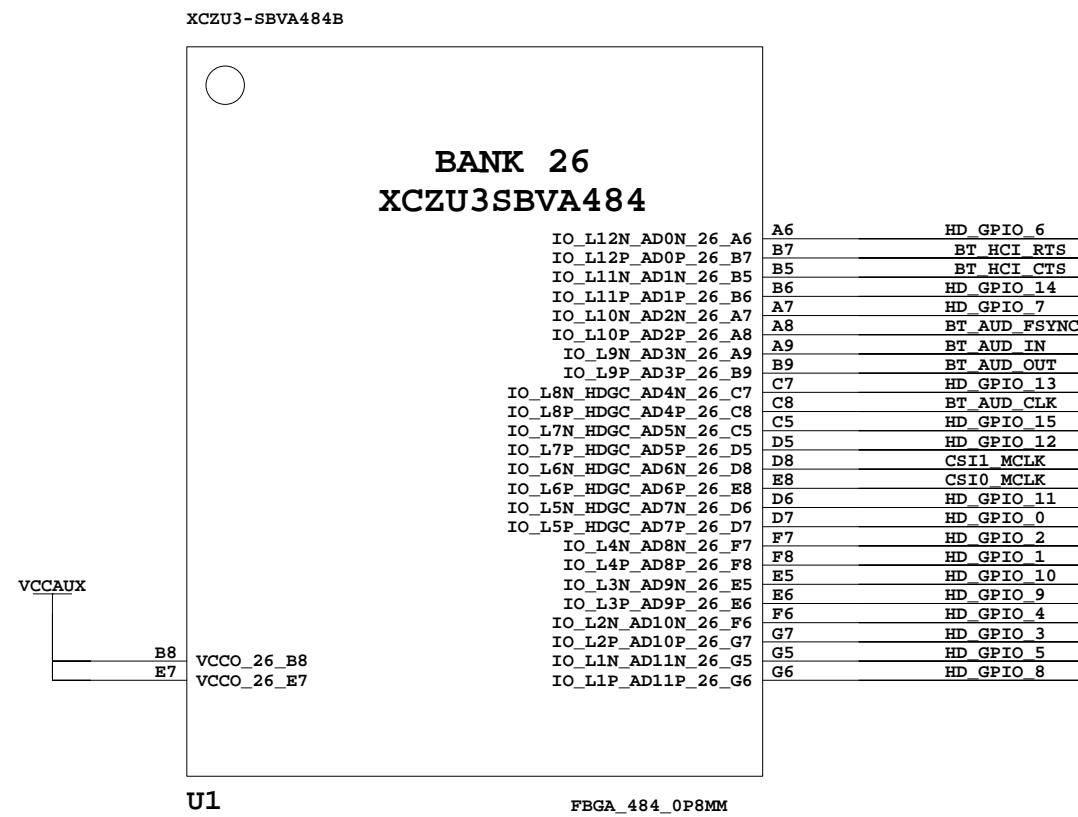




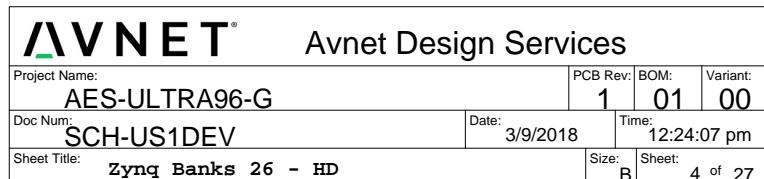
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Zynq Bank 0

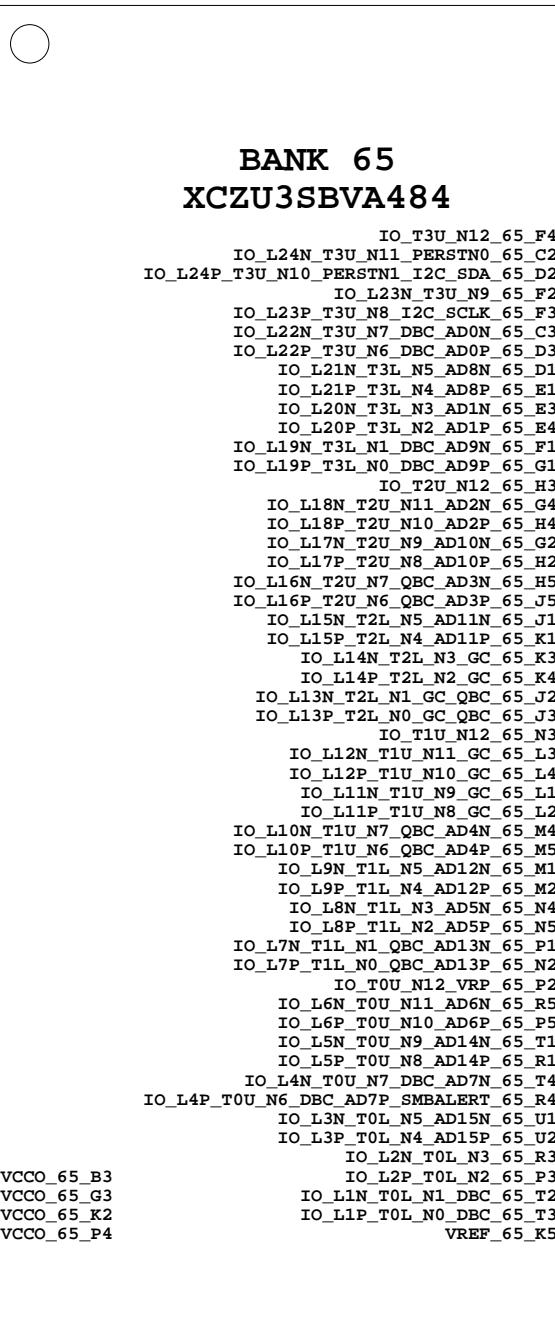
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Project Name:	AES-ULTRA96-G	PCB Rev:	BOM: 01 00 Variant:
Doc Num:	SCH-US1DEV	Date:	3/9/2018 Time: 12:24:07 pm
Sheet Title:	Zynq Bank 0	Size:	Sheet: B 3 of 27



Zyng Banks 26 - HD



XCZU3-SBVA484B



XCZU3-SBVA484B

BANK 66
XCZU3SBVA484

A2	HSIC_STR
A3	NC
A4	NC
B1	NC
B2	NC
B4	NC
C4	NC

U1 FBGA_484_0P8MM

R145
1 240 1/20W
2 1%

1 R145
2 240 1/20W
GND

Zynq Banks 65 66 - HP

AVNET Avnet Design Services	Project Name: AES-ULTRA96-G	PCB Rev.: 1	BOM: 01	Variant: 00
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XCZU3-SBVA484B

BANK 500
XCZU3SBVA484

PS_MIO25_Y6	MIO25_VBUS_DET
PS_MIO24_AB6	MIO24_SD0_DETECT
AB5	MIO23_GPIO_PB
AA6	MIO22_SD0_CLK_R
W6	MIO21_SD0_CMD_R
PS_MIO21_W6	MIO20_PS_LED0
PS_MIO20_AB4	MIO19_PS_LED1
PS_MIO19_AA4	MIO18_PS_LED2
PS_MIO18_Y5	MIO17_PS_LED3
PS_MIO17_AA3	MIO16_SD0_DAT3_R
PS_MIO16_Y3	MIO15_SD0_DAT2_R
PS_MIO15_Y4	MIO14_SD0_DAT1_R
PS_MIO14_W5	MIO13_SD0_DAT0_R
PS_MIO13_W3	MIO12_I2C_MUX_RESET_B
PS_MIO12_AB2	MIO11_SPI1_MOSI
PS_MIO11_W2	MIO10_SPI1_MISO
PS_MIO10_AA2	MIO9_SPI1_CS
PS_MIO9_V5	MIO8_BT_EN
PS_MIO8_V3	MIO7_WLAN_EN
PS_MIO7_V4	MIO6_SPI1_SCLK
PS_MIO6_Y1	MIO5_I2C1_SDA
AA1	MIO4_I2C1_SCL
U6	MIO3_UART0_TX_BT_HCI_RX
U5	MIO2_UART0_RX_BT_HCI_TX
V2	MIO1_UART1_RX
W1	MIO0_UART1_TX
U4	MIO0_UART1_TX

VCC_PSAUX

AA5
V6
VCCO_PSIO0_500_AA5
VCCO_PSIO0_500_V6

U1

FBGA_484_0P8MM

U1
FBGA_484_0P8MM

XCZU3-SBVA484B

BANK 501
XCZU3SBVA484

PS_MIO51_C13	MIO51_SD1_CLK
A13	MIO50_SD1_CMD
D13	MIO49_SD1_D3
A12	MIO48_SD1_D2
B12	MIO47_SD1_D1
C12	MIO46_SD1_D0
P5_MIO45_A11	MIO45_PS_GPIO1_5
B11	MIO44_PS_GPIO1_4
P5_MIO44_B11	MIO43_SPI0_MOSI
E13	MIO42_SPI0_MISO
P5_MIO42_D12	MIO41_SPI0_CS
B10	MIO40_PS_GPIO1_3
P5_MIO40_D11	MIO39_PS_GPIO1_2
C10	MIO38_SPI0_SCLK
P5_MIO38_C9	MIO37_PS_GPIO1_1
E11	MIO36_PS_GPIO1_0
D10	MIO35_POWER_KILL_B
E10	J20
F13	MIO34_PL_PWR_EN
E9	MIO33_PL_PWR_EN
F12	MIO32_PS_FP_PWR_EN
P5_MIO32_F12	MIO31_INA226_PMBUS_ALERT
F11	MIO30_G10
G10	MIO29_DP_AUX_IN
P5_MIO29_F9	MIO28_DP_HPD
F9	MIO27_DP_OE
G12	MIO26_POWER_INT_B
P5_MIO28_G12	MIO27_DP_AUX_OUT
G11	MIO26_POWER_AUX_IN
G9	MIO25_POWER_AUX_OUT

VCC_PSAUX

C11
F10
VCCO_PSIO1_501_C11
VCCO_PSIO1_501_F10

U1

FBGA_484_0P8MM

VCC_PSAUX
R23
1 4.70K

VCC_PSAUX
R160
1 4.70K
2
SW4
MIO23_GPIO_PB
B3U-1000P
GND

XCZU3-SBVA484B

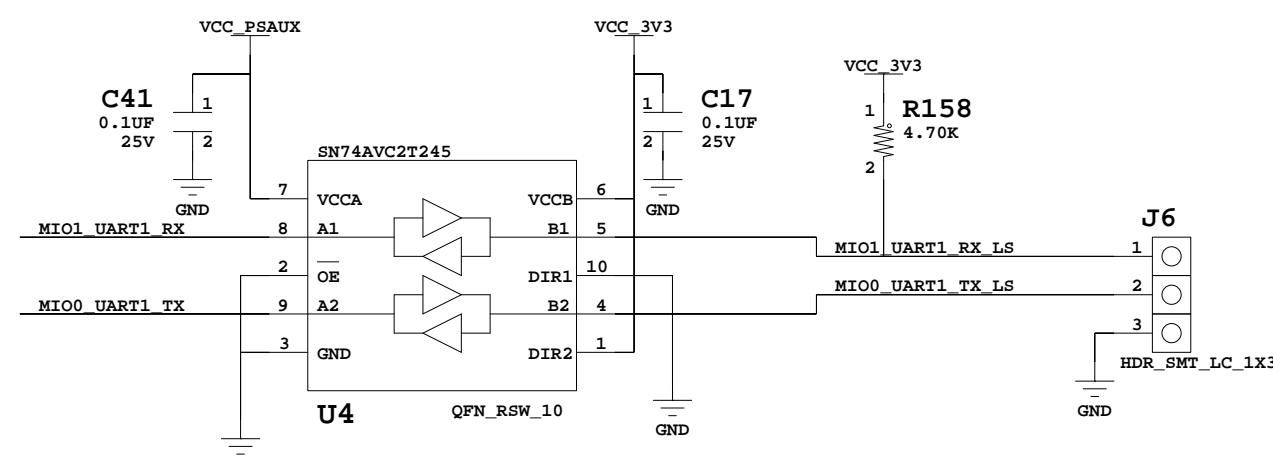
BANK 502
XCZU3SBVA484

B18	PMIC IRQ
F18	MIO76_WLAN_IRQ
P5_MIO75_B17	MIO75_USB1_DATA7
D18	MIO74_USB1_DATA6
D17	MIO73_USB1_DATA5
P5_MIO73_D17	MIO72_USB1_DATA4
P5_MIO72_C17	MIO71_USB1_DATA3
P5_MIO71_F17	MIO70_USB1_STP
P5_MIO70_A17	MIO69_USB1_A1
P5_MIO69_A16	MIO68_USB1_DATA1
P5_MIO68_B16	MIO67_USB1_NXT
P5_MIO67_G17	MIO66_USB1_DATA2
P5_MIO66_D16	MIO65_USB1_DIR
P5_MIO65_B15	MIO64_USB1_CLK
P5_MIO64_E16	MIO63_USB0_DATA7
P5_MIO63_F16	MIO62_USB0_DATA6
P5_MIO62_C15	MIO61_USB0_DATA5
P5_MIO61_G16	MIO60_USB0_DATA4
P5_MIO60_D15	MIO59_USB0_DATA3
P5_MIO59_E15	MIO58_USB0_STP
P5_MIO58_A14	MIO57_USB0_DATA1
P5_MIO57_B14	MIO56_USB0_DATA0
P5_MIO56_E14	MIO55_USB0_NXT
P5_MIO55_C14	MIO54_USB0_DATA2
P5_MIO54_G15	MIO53_USB0_DIR
P5_MIO53_F14	MIO52_USB0_CLK

VCC_PSAUX

C16
D14
VCCO_PSIO2_502_C16
VCCO_PSIO2_502_D14

U1

U1
FBGA_484_0P8MM

Zynq Banks 500 501 502 - MIO

AVNET	Avnet Design Services	Project Name: AES-ULTRA96-G	PCB Rev: 1	BOM: 01	Variant: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm			
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XCZU3-SBVA484B

BANK 503
XCZU3SBVA484

PS POR_B_K12
 PS_ERROR_STATUS_K18
 PS_ERROR_OUT_K16
 PS_SRST_B_K13
 PS_REF_CLK_H14
 PS_JTAG_TCK_H13
 PS_JTAG_TMS_J12
 PS_JTAG_TDO_J13
 PS_INIT_B_K15
 PS_PROG_B_K14
 PS_DONE_L12
 PS_PADI_H17
 PS_PAD0_J17
 PS_MODE3_H18
 PS_MODE2_H15
 PS_MODE1_H15
 PS_MODE0_J16

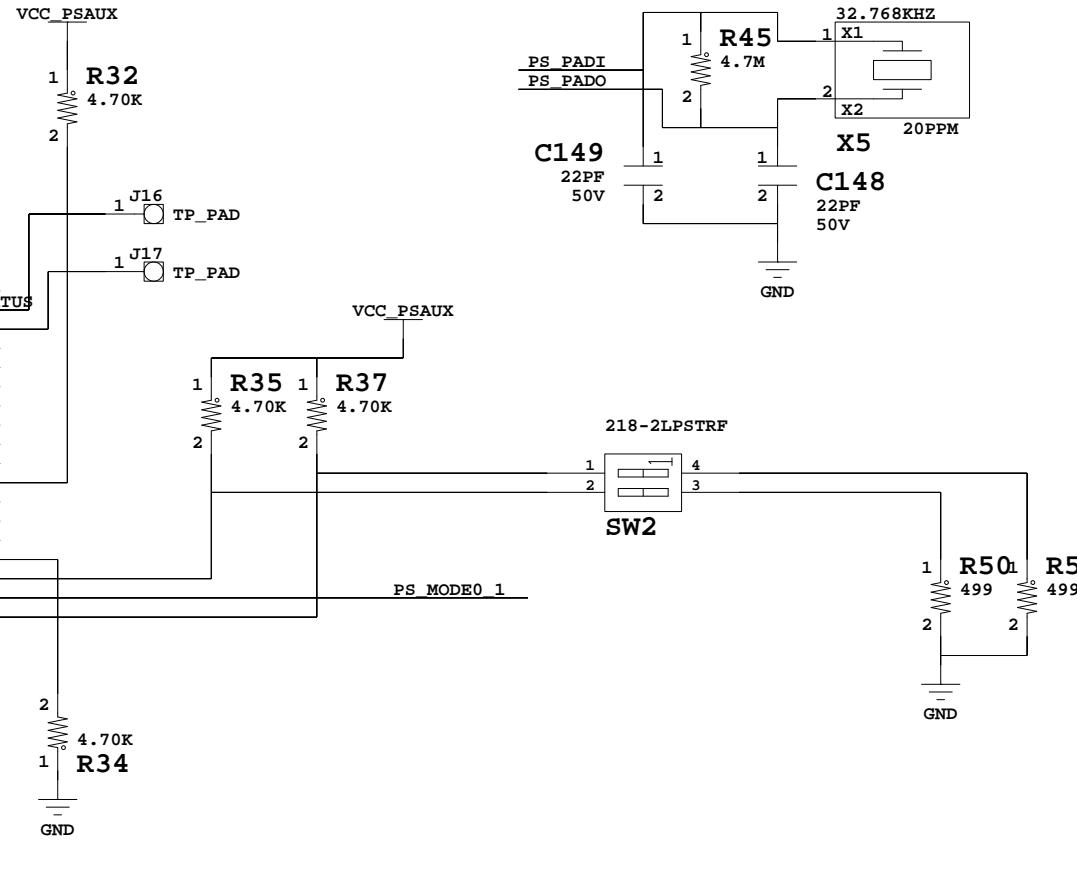
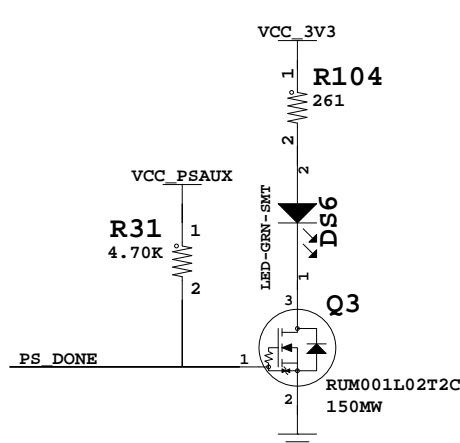
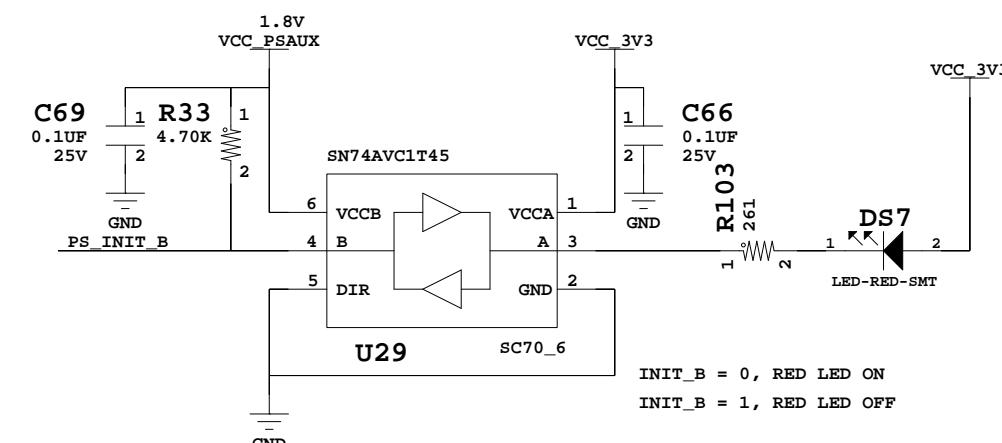
PS POR_B
 PS_ERROR_STATUS
 PS_ERROR_OUT
 PS_SRST_B
 PS_REF_CLK
 JTAG TCK
 JTAG TMS
 JTAG TDO
 JTAG TDI
 PS_INIT_B
 PS_PROG_B
 PS_DONE
 PS_PADI
 PS_PAD0
 PS_MODE3
 PS_MODE2

VCC_PSAUX

G13
H16VCCO_PSI03_503_G13
VCCO_PSI03_503_H16

FBGA_484_0P8MM

U1


PS_MODE0_1 is used to reset USB devices
BOOT MODE:
JTAG 11
SD 01
USB 00
**Zynq Banks 503 - Config**

Avnet Design Services			
Project Name:	PCB Rev:	BOM:	Variant:
AES-ULTRA96-G	1	01	00
Doc Num:	Date:	Time:	
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Sheet Title:	Zynq Banks 503 - Config	Size:	Sheet:
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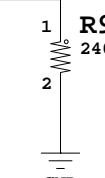
XCZU3-SBVA484B

BANK 504
XCZU3SBVA484

PS_DDR_CAA0	AA22	PS_DDR_A0_AA22	AB11	PS_DDR_DQ0
PS_DDR_CAA1	AB20	PS_DDR_A1_AB20	Y10	PS_DDR_DQ1
PS_DDR_CAA2	AB17	PS_DDR_A2_AB17	AB10	PS_DDR_DQ2
PS_DDR_CAA3	AB19	PS_DDR_A3_AB19	W10	PS_DDR_DQ3
PS_DDR_CAA4	AB21	PS_DDR_A4_AB21	AA8	PS_DDR_DQ4
PS_DDR_CAA5	AB16	PS_DDR_A5_AB16	Y8	PS_DDR_DQ5
	x NC	Y20	AB7	PS_DDR_DQ6
	x NC	Y19	AA7	PS_DDR_DQ7
	x NC	W17	AA11	PS_DDR_DQ8
	x NC	Y18	Y11	PS_DDR_DQ9
PS_DDR_CAB0	Y21	PS_DDR_A10_Y21	AA12	PS_DDR_DQ10
PS_DDR_CAB1	AA21	PS_DDR_A11_AA21	AB12	PS_DDR_DQ11
PS_DDR_CAB2	AA18	PS_DDR_A12_AA18	Y14	PS_DDR_DQ12
PS_DDR_CAB3	AA19	PS_DDR_A13_AA19	AA14	PS_DDR_DQ13
PS_DDR_CAB4	AA17	PS_DDR_A14_AA17	Y15	PS_DDR_DQ14
PS_DDR_CAB5	AA16	PS_DDR_A15_AA16	AB15	PS_DDR_DQ15
	x NC	Y16	W8	PS_DDR_DQ16
	x NC	W16	W7	PS_DDR_DQ17
	x NC	U17	V7	PS_DDR_DQ18
	x NC	V17	V10	PS_DDR_DQ19
	x NC	U15	U7	PS_DDR_DQ20
	x NC	T21	T9	PS_DDR_DQ21
	x NC	U19	U10	PS_DDR_DQ22
PS_DDR_RST_B	T18	PS_DDR_PARITY_U19	T10	PS_DDR_DQ23
	x NC	U16	U11	PS_DDR_DQ24
	x NC	W18	U12	PS_DDR_DQ25
PS_DDR_CS0_N	V22	PS_DDR_BG1_W18	W12	PS_DDR_DQ26
PS_DDR_CS1_N	U20	PS_DDR_CS_N0_V22	W11	PS_DDR_DQ27
PS_DDR_CKA_T	V20	PS_DDR_CS_N1_U20	V14	PS_DDR_DQ28
PS_DDR_CKA_C	W20	PS_DDR_CK0_V20	U14	PS_DDR_DQ29
PS_DDR_CKB_T	V18	PS_DDR_CK_N0_W20	W15	PS_DDR_DQ30
PS_DDR_CKB_C	V19	PS_DDR_CK1_V18	V15	PS_DDR_DQ31
PS_DDR_CKE0	U22	PS_DDR_CKE0_U22		
PS_DDR_CKE1	U21	PS_DDR_CKE1_U21	T22	NC
	x NC	W22	P22	NC
	x NC	W21	PS_DDR_ODT0_W22	×
		Y9	PS_DDR_ODT1_W21	PS_DDR_DQ65_P22
PS_DDR_DQSA0_T	AA9	PS_DDR_DQS_P0_Y9	P21	NC
PS_DDR_DQSA0_C	Y13	PS_DDR_DQS_N0_AA9	PS_DDR_DQ66_R21	NC
PS_DDR_DQSA1_T	AA13	PS_DDR_DQS_P1_Y13	PS_DDR_DQ67_P21	NC
PS_DDR_DQSA1_C	AA13	PS_DDR_DQS_N1_AA13	PS_DDR_DQ68_R18	NC
PS_DDR_DQSB0_T	V9	PS_DDR_DQS_P2_V9	P18	NC
PS_DDR_DQSB0_C	V8	PS_DDR_DQS_N2_V8	PS_DDR_DQ69_P18	NC
PS_DDR_DQSB1_T	V12	PS_DDR_DQS_P3_V12	PS_DDR_DQ70_N18	NC
PS_DDR_DQSB1_C	V13	PS_DDR_DQS_N3_V13	PS_DDR_DQ71_N19	NC
	x NC	P20		
	x NC	R20		
VCCO_PSDDR	Y22	VCCO_PSDDR_504_Y22	AB9	PS_DDR_DMA0
	Y17	VCCO_PSDDR_504_Y17	AB14	PS_DDR_DMA1
	V21	VCCO_PSDDR_504_V21	U9	PS_DDR_DMB0
	V16	VCCO_PSDDR_504_V16	W13	PS_DDR_DMB1
	T20	VCCO_PSDDR_504_T20	R19	NC
	P19	VCCO_PSDDR_504_P19		
	AB18	VCCO_PSDDR_504_AB18		
		PS_DDR_ZQ_T19	T19	LPDDR4_PS_ZQ

U1

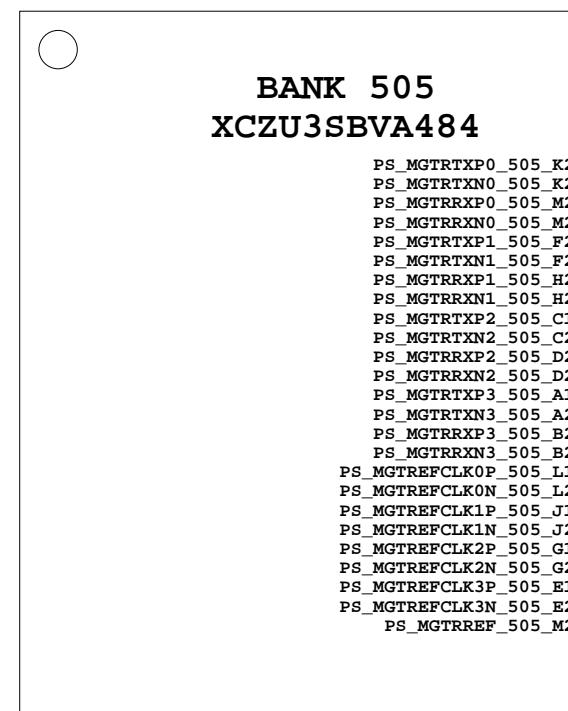
FBGA_484_0P8MM



Zynq Bank 504 - Memory

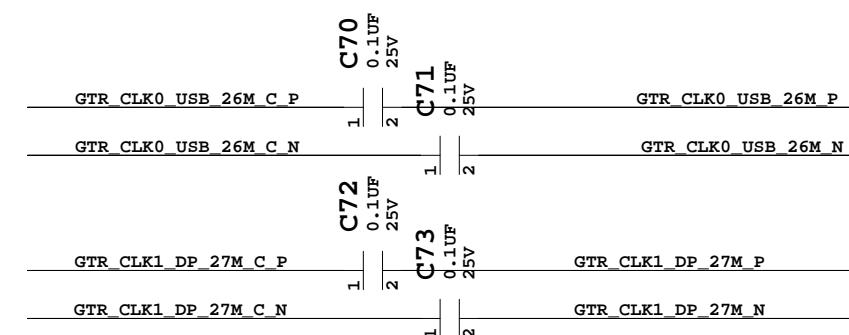
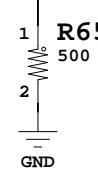
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Project Name:	AES-ULTRA96-G	PCB Rev:	BOM: 01 00
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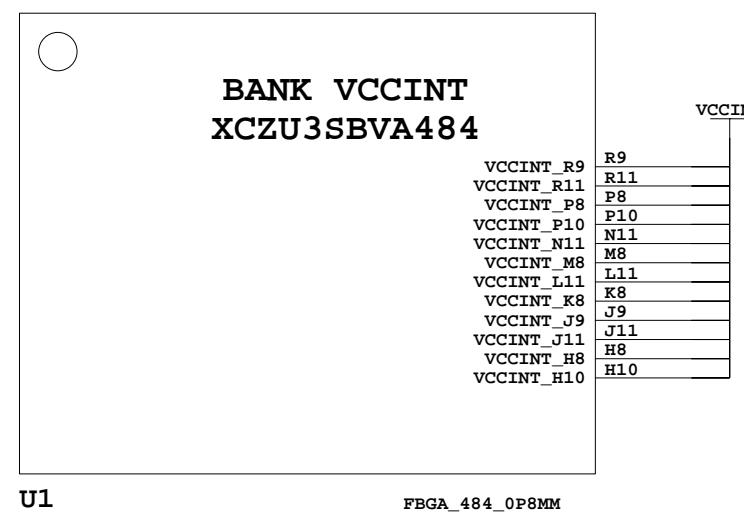
U1

FBGA_484_0P8MM

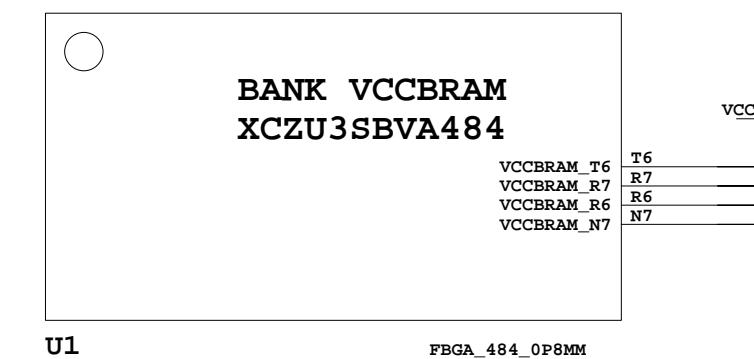
**Zynq Banks 505 - GTR**

Avnet Design Services			
Project Name:	PCB Rev:	BOM:	Variant:
AES-ULTRA96-G	1	01	00
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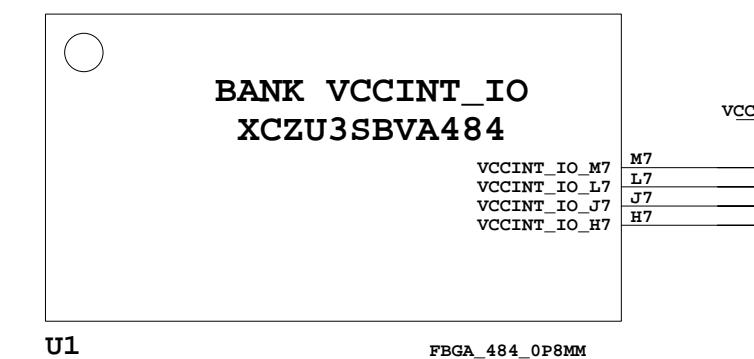
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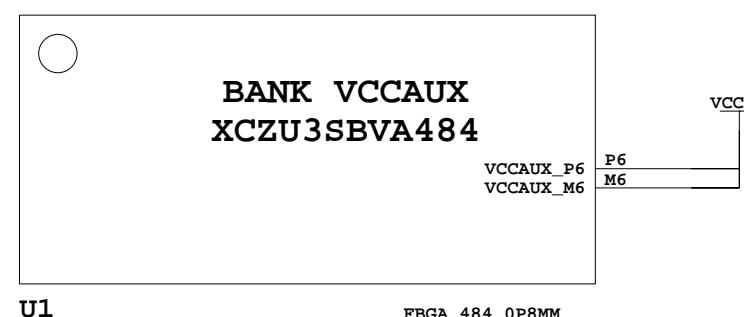
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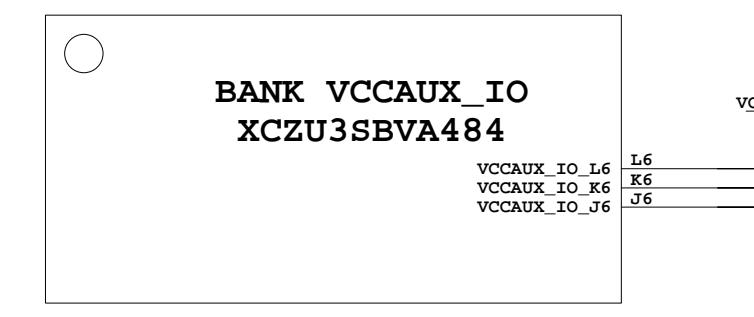
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XCZU3-SBVA484B

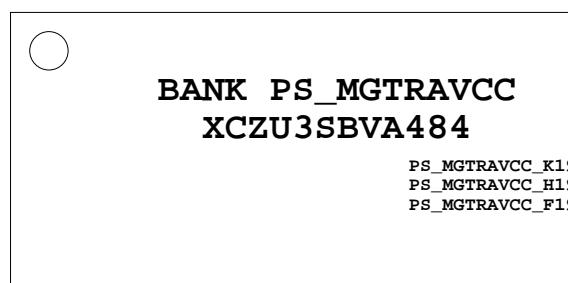


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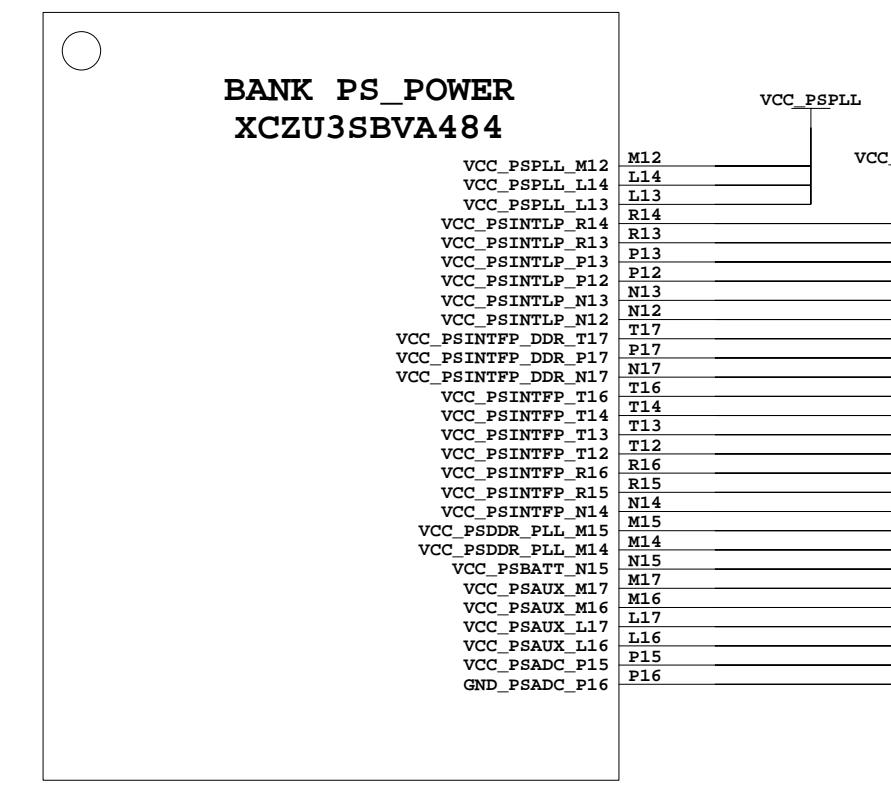
**Zynq Power 1**

Avnet Design Services			
Project Name:	AES-ULTRA96-G	PCB Rev:	BOM: 1 01 00 Variant:
Doc Num:	SCH-US1DEV	Date:	3/9/2018 Time: 12:24:07 pm
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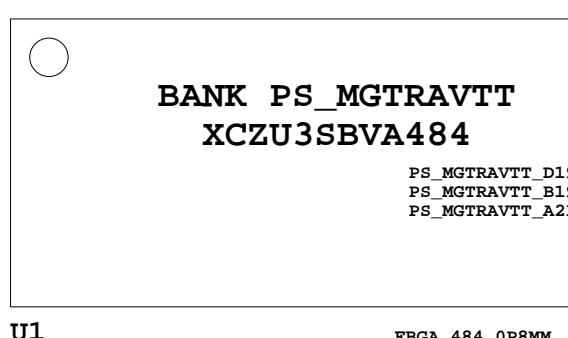
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XCZU3-SBVA484B

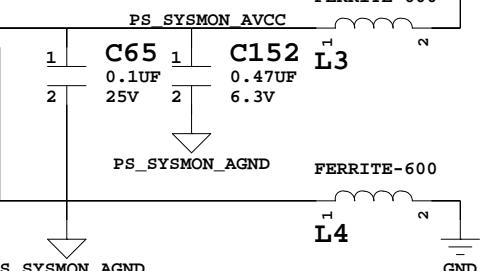


XCZU3-SBVA484B



VCC_PSAUX

FERRITE-600



Zynq Power 2

Avnet Design Services			
Project Name:	AES-ULTRA96-G	PCB Rev:	BOM: 01 00 Variant:
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A

B

C

D

A

B

C

D

U1

FBGA_484_0P8MM

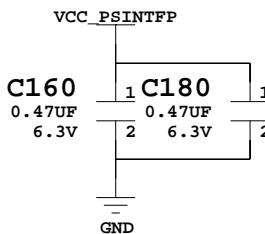
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A10	GND_A10
A15	GND_A15
A18	GND_A18
A19	GND_A22
A22	GND_A5
A5	GND_AA10
AA10	GND_AA15
AA15	GND_AA20
AA20	GND_AB1
AB1	GND_AB13
AB13	GND_AB22
AB22	GND_AB3
AB3	GND_AB8
AB8	GND_B13
B13	GND_B20
B20	GND_C1
C1	GND_CL8
C18	GND_C21
C21	GND_C22
C22	GND_C6
C6	GND_D20
D20	GND_D4
D4	GND_D9
D9	GND_E12
E12	GND_E17
E17	GND_E18
E18	GND_E2
E2	GND_E21
E21	GND_E22
E22	GND_F15
F15	GND_F20
F20	GND_F5
F5	GND_G18
G18	GND_G21
G21	GND_G22
G22	GND_G8
G8	GND_H1
H1	GND_H11
H11	GND_H20
H20	GND_H6
H6	GND_H9
H9	GND_J10
J10	GND_J14
J14	GND_IT8
J18	GND_J21
J21	GND_J22
J22	GND_J4
J4	GND_J8
J8	GND_K11
K11	GND_K17
K17	GND_K20
K20	GND_K7
K7	GND_L15
L15	GND_L18
L18	GND_L21
L21	GND_L22
L22	GND_L5
L5	GND_L8
L8	GND_M11
M11	GND_M13
M13	GND_M18
M18	GND_M19
M19	GND_M3
M3	GND_N6
N6	GND_N1
N1	GND_N16
N16	GND_N20
N20	GND_N21
N21	GND_N22
N22	GND_P7
P7	GND_P9
P9	GND_R10
R10	GND_R12
R12	GND_R17
R17	GND_R2
R2	GND_R22
R22	GND_R8
R8	GND_T11
T11	GND_T15
T15	GND_T5
T5	GND_U13
U13	GND_U18
U18	GND_U3
U3	GND_V8
V8	GND_V1
V1	GND_V11
V11	GND_W14
W14	GND_W19
W19	GND_W4
W4	GND_W9
W9	GND_Y12
Y12	GND_Y2
Y2	GND_Y7
Y7	GND_GND

Zynq GND

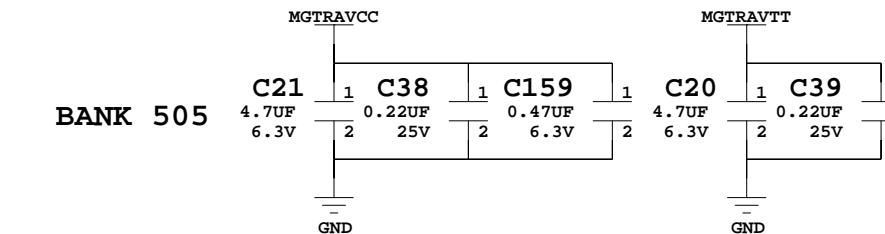
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Project Name: AES-ULTRA96-G	PCB Rev.: 1	BOM: 01
Doc Num: SCH-US1DEV	Date: 3/9/2018	Variant: 00
Sheet Title: Zynq GND	Time: 12:24:07 pm	
		Size: B
		Sheet: 12 of 27

XCZU3-SBV484B

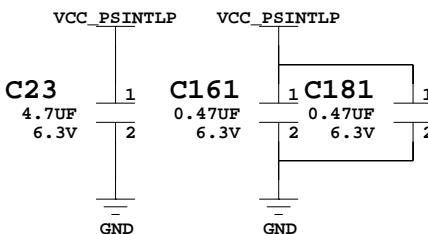
XCZU3-SBV484
BANK GND



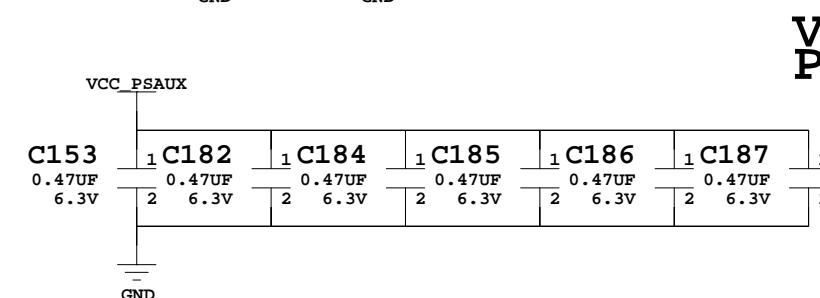
VCCPSINTFP



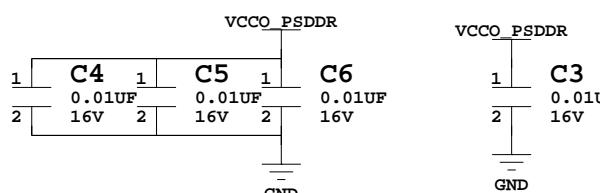
MGTRAVCC/AVTT



VCCPSINTLP

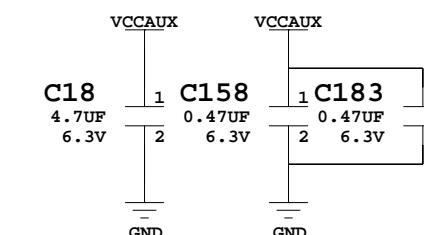
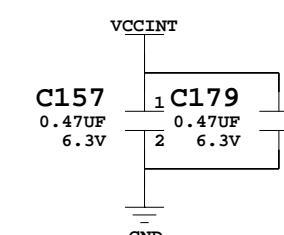
VCCPSAUX/PSADC/PSDDRPLL
PSIO1-3

PL VCCINT/VCCBRAM



VCCPSDDR

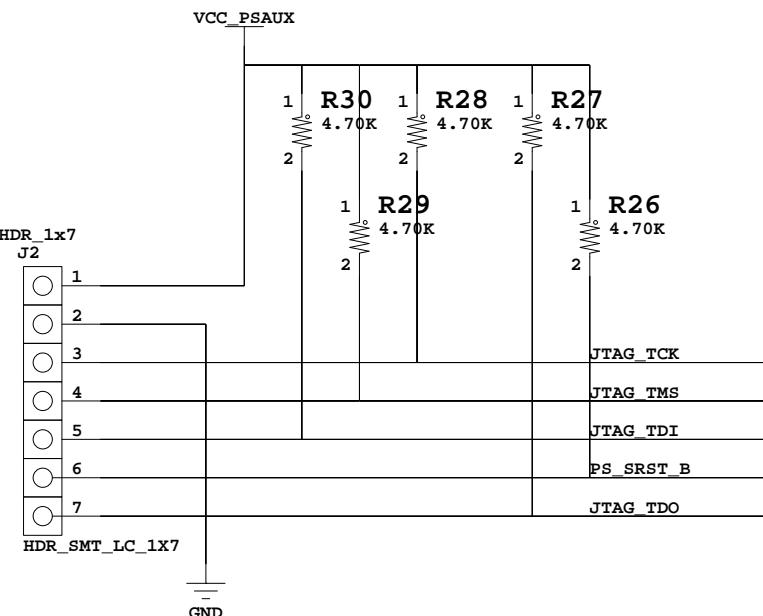
Place this cap directly under U1



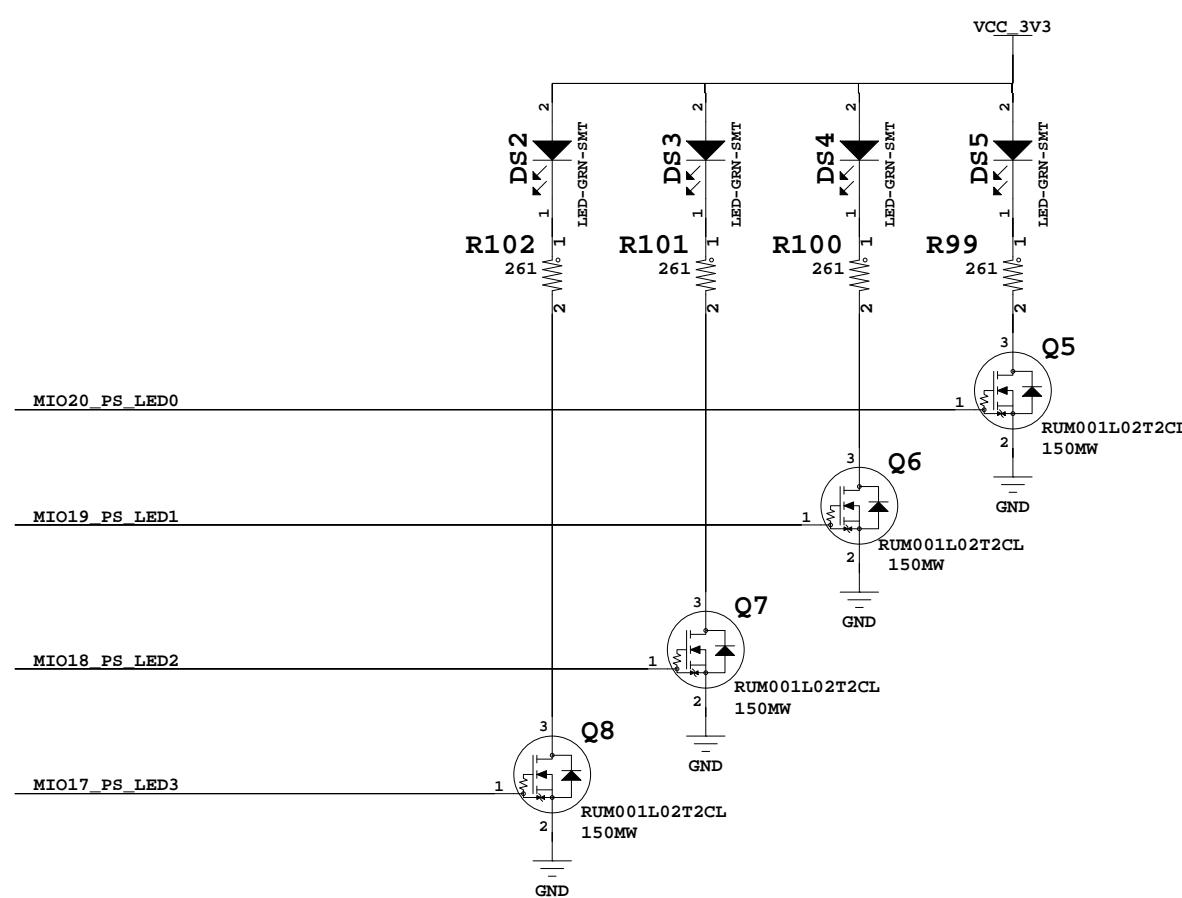
PL VCCAUX / VCCAUX_IO

Zynq Decoupling

Avnet Design Services			
Project Name:	AES-ULTRA96-G	PCB Rev:	BOM: 01 00
Doc Num:	SCH-US1DEV	Date:	Time: 12:24:07 pm
Sheet Title:	Zynq Decoupling	Size:	Sheet: B 13 of 27



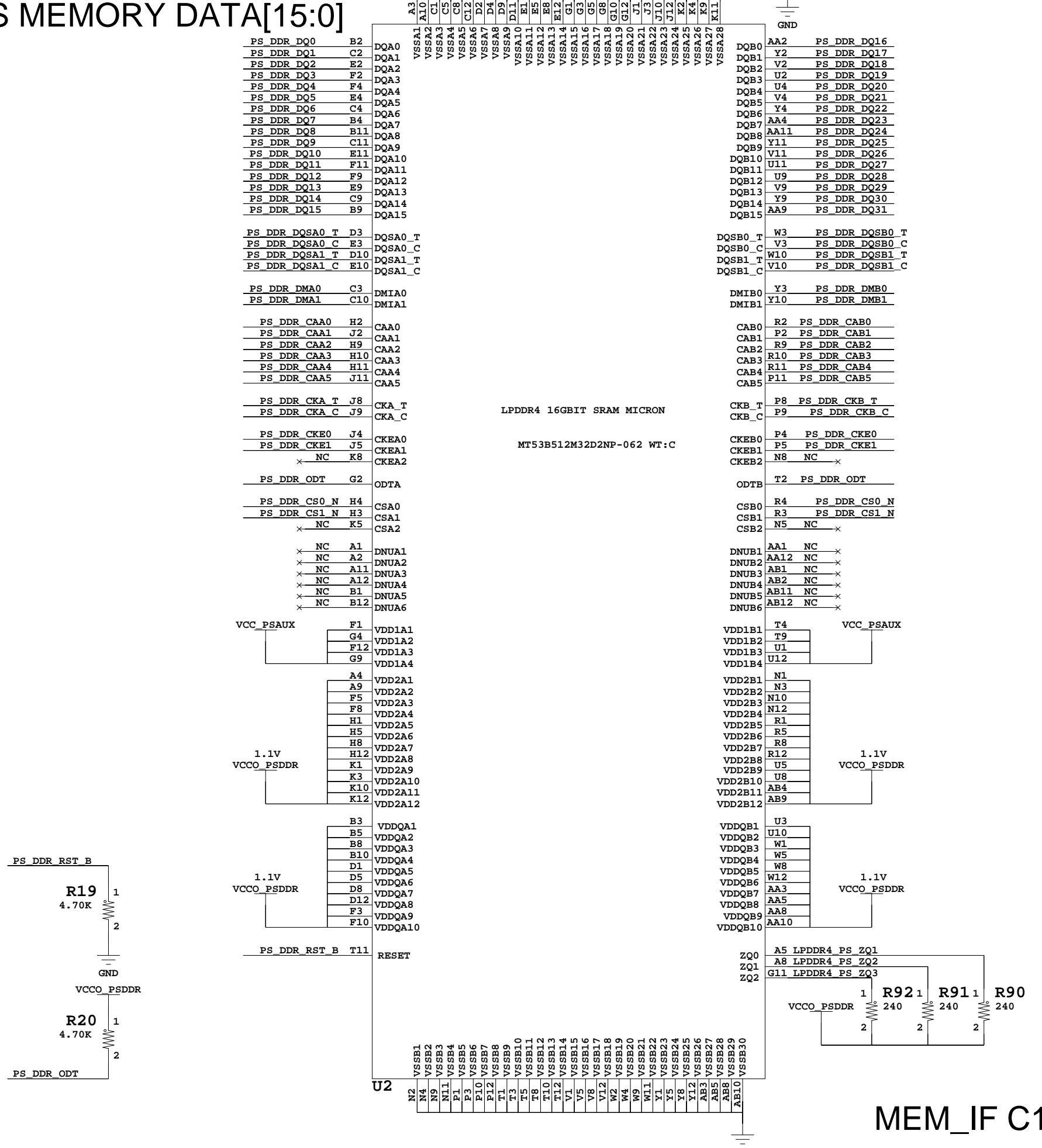
JTAG on Bottomside



JTAG Headers - LEDs

Avnet Design Services			
Project Name:	PCB Rev:	BOM:	Variant:
AES-ULTRA96-G	1	01	00
Doc Num:	Date:	Time:	
SCH-US1DEV	3/9/2018	12:24:07 pm	
Sheet Title:	Size:	Sheet:	
JTAG Headers - LEDs	B	14 of 27	

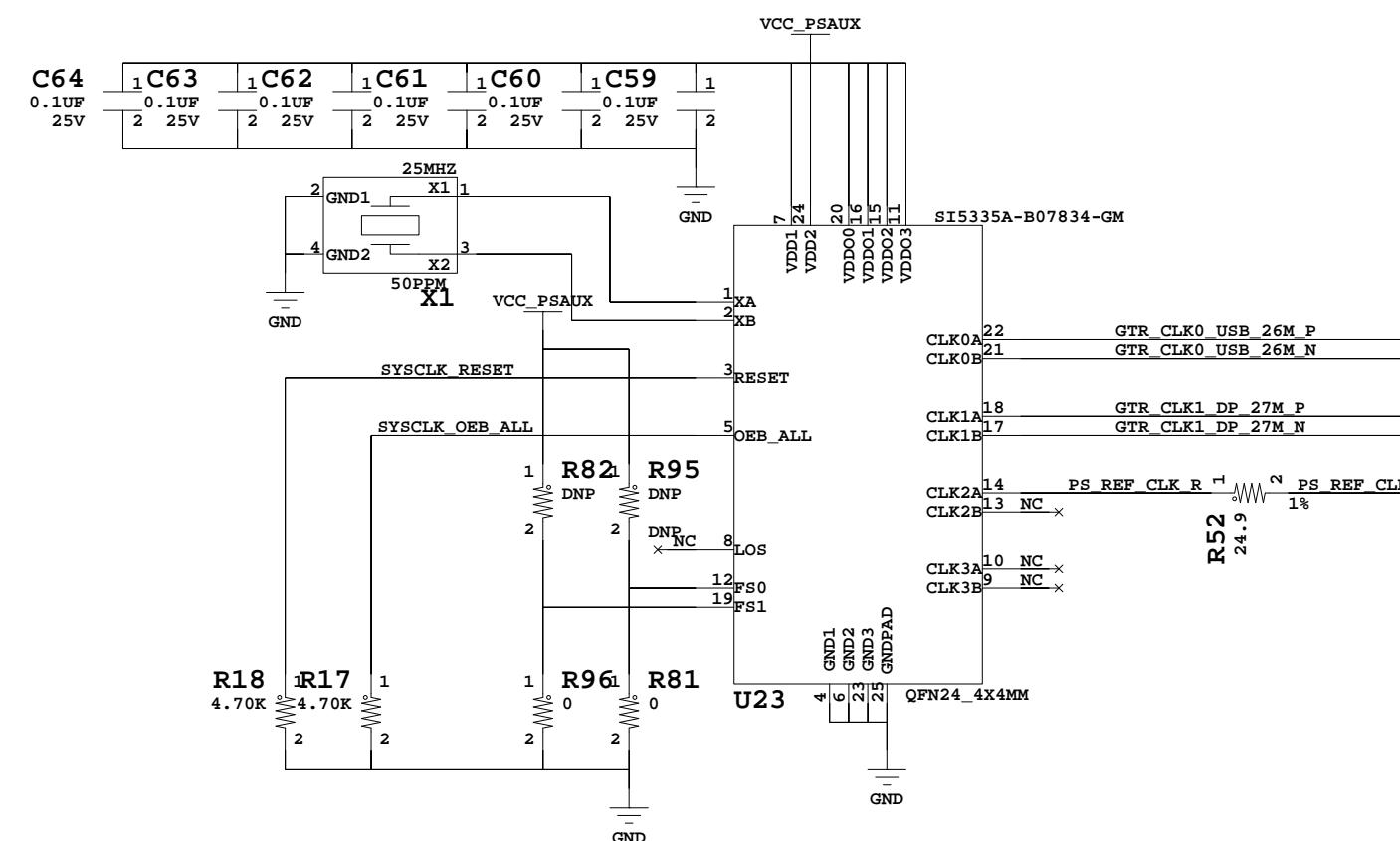
LPDDR4 PS MEMORY DATA[15:0]



MEM_IF C1

40 OHM INTERFACE
PS LPDDR4 DRAM

AVNET Avnet Design Services		Project Name: AES-ULTRA96-G	PCB Rev: BOM: 1 01 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm	
Sheet Title: PS LPDDR4 DRAM	Size: B	Sheet: 15 of 27	



26MHz LVDS

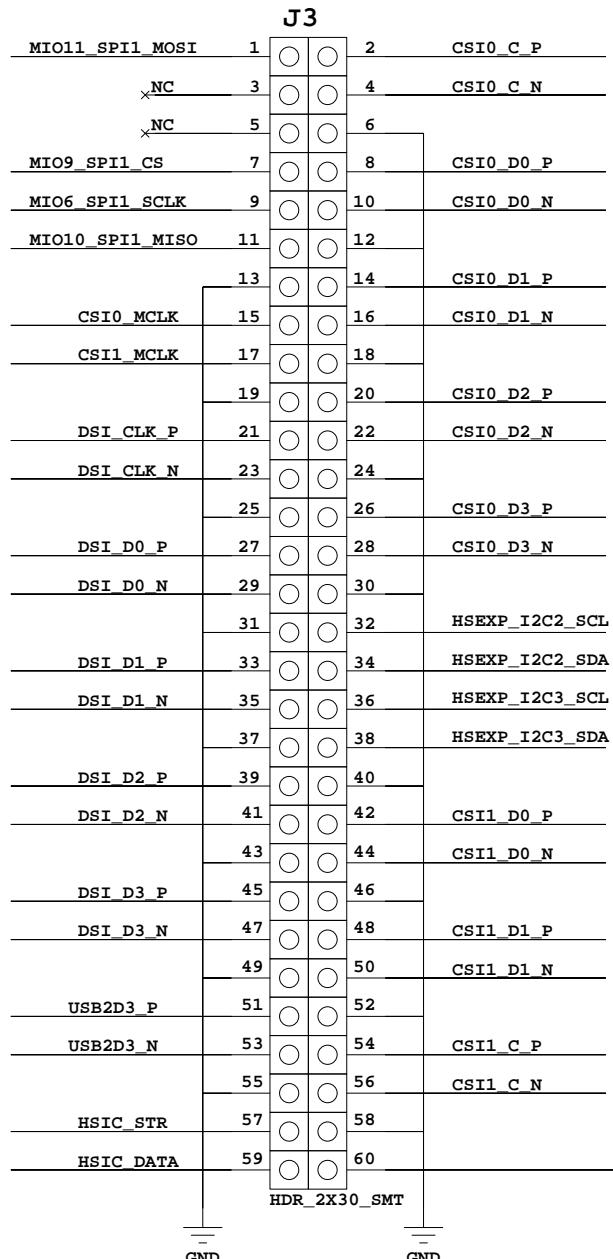
27MHz LVDS

**33.333333MHz LVCMOS
(100/3)**

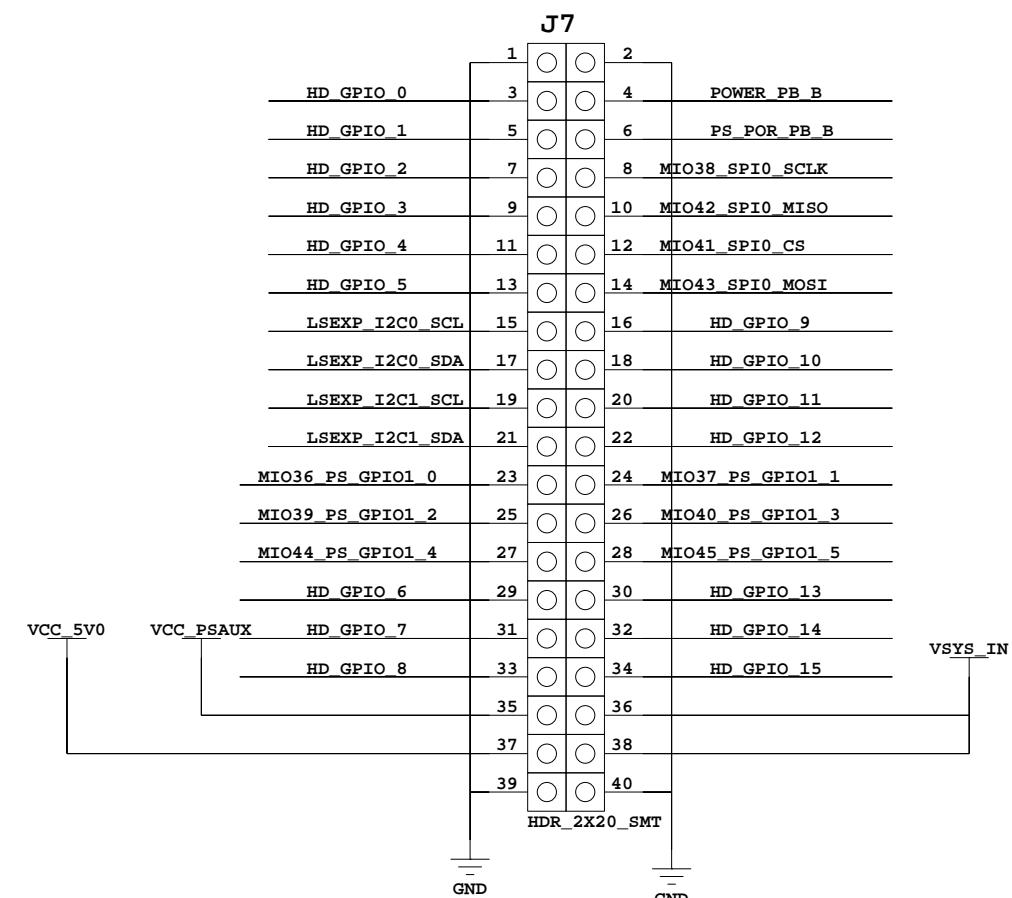
Fixed Clocks

Avnet Design Services		
Project Name: AES-ULTRA96-G	PCB Rev: 01	BOM: 00
Doc Num: SCH-US1DEV	Date: 3/9/2018	Time: 12:24:07 pm
Sheet Title: Fixed Clocks	Size: B	Sheet: 16 of 27

**SPI shared with HS header
Different CS signals**



VCC_PSAUX
1 R124
100K
1/20W
2 1%



Expansion Headers

AVNET® Avnet Design Services		Project Name:	AES-ULTRA96-G	PCB Rev:	BOM:	Variant:
		Doc Num:	SCH-US1DEV	Date:	1	01 00
		Sheet Title:	Expansion Headers		Time:	12:24:07 pm
		Size:	B	Sheet:	17	of 27

1

2

3

4

5

6

A

A

B

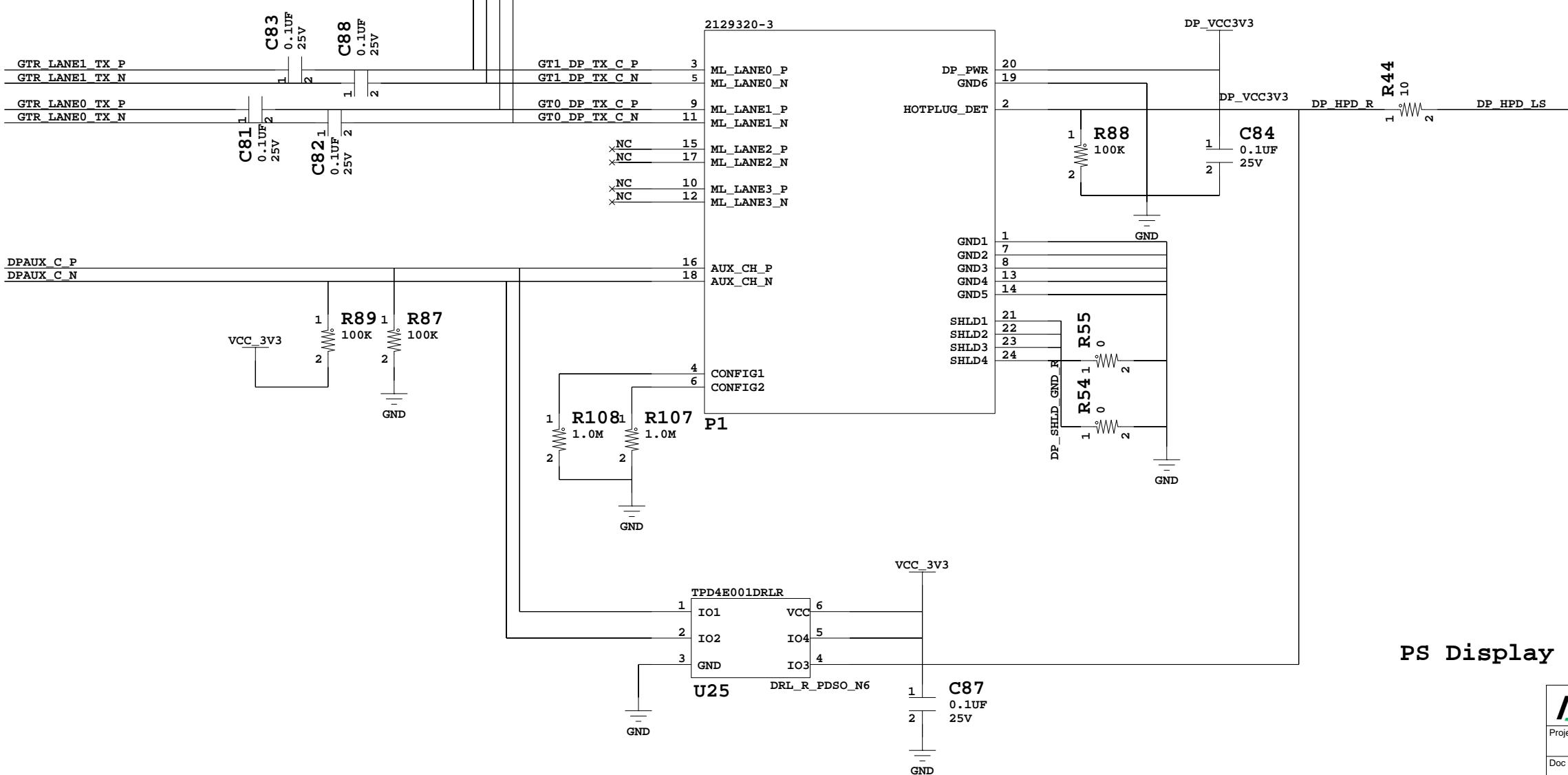
B

C

C

D

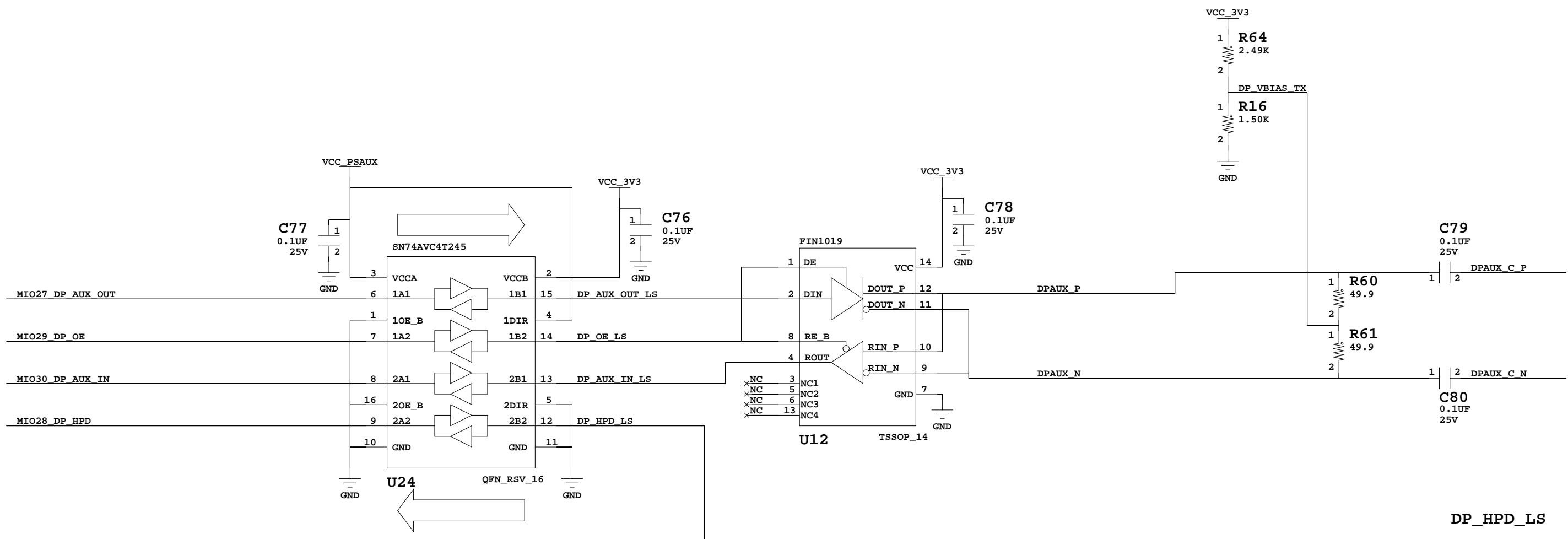
D



PS Display Port Connector

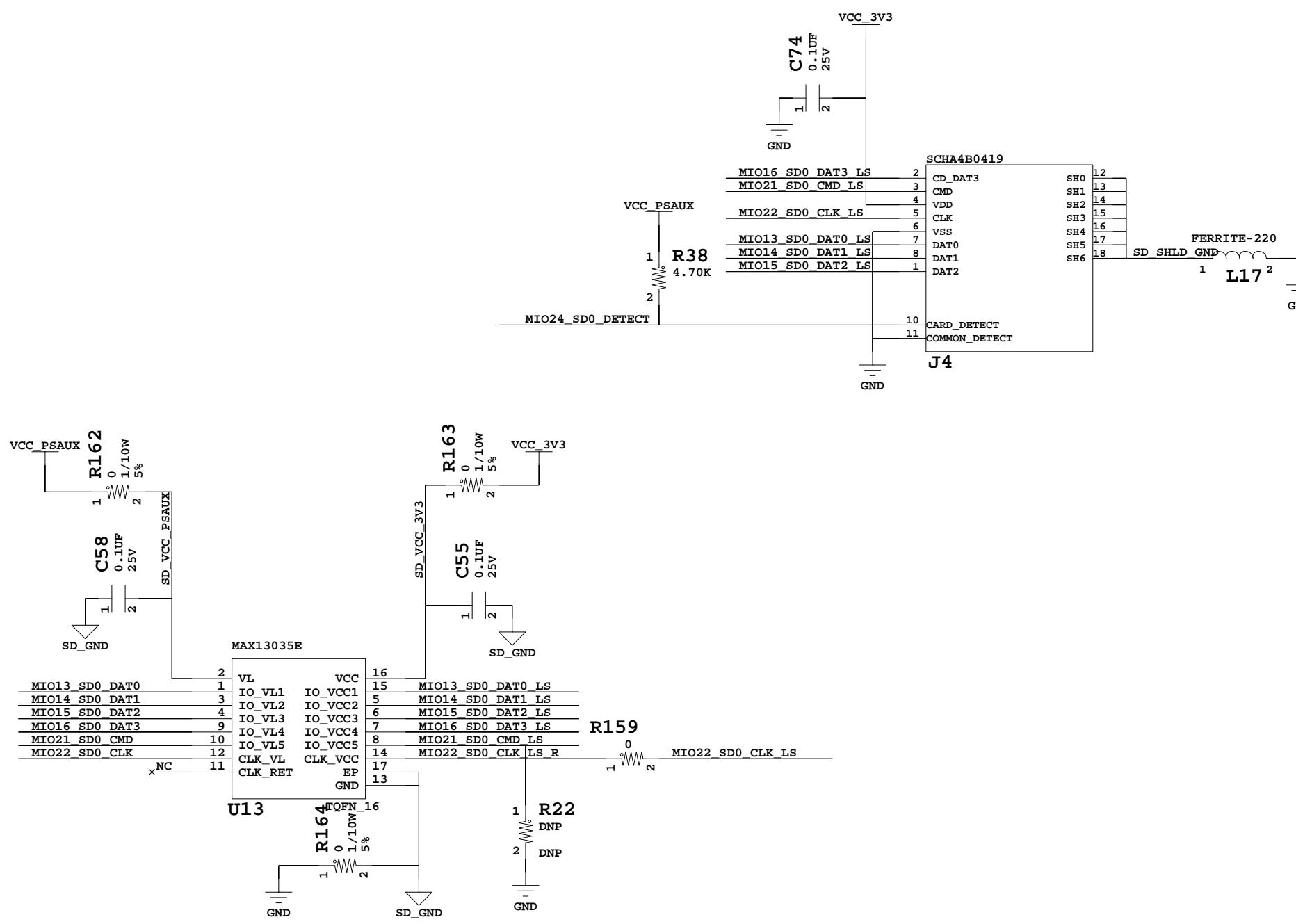
Avnet Design Services		
Project Name:	PCB Rev:	BOM: Variant:
AES-ULTRA96-G	1	01 00
Doc Num:	Date:	Time:
SCH-US1DEV	3/9/2018	12:24:07 pm
Sheet Title:	PS Display Port Connector	Size: Sheet:
	B	18 of 27

A

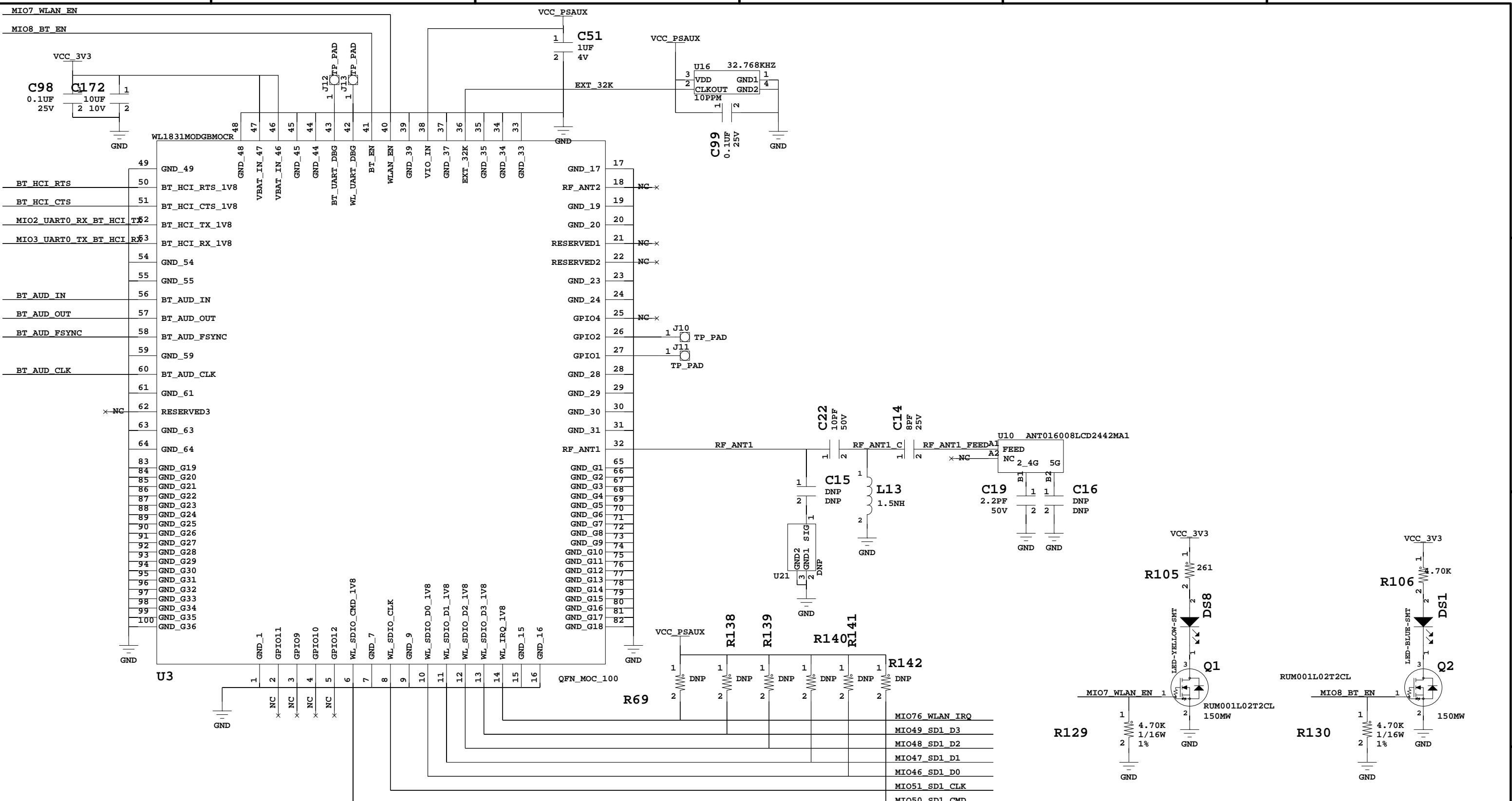


PS Display Port IO

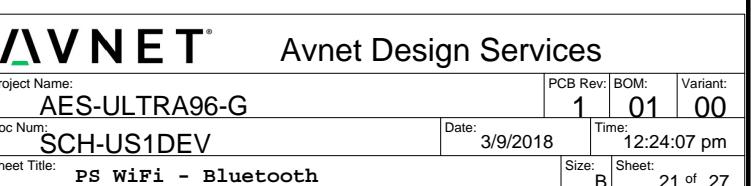
Avnet Design Services		
Project Name:	PCB Rev:	BOM:
AES-ULTRA96-G	1	01 00
Doc Num:	Date:	Variant:
SCH-US1DEV	3/9/2018	12:24:07 pm
Sheet Title:	Size:	Sheet:
PS Display Port IO	B	19 of 27

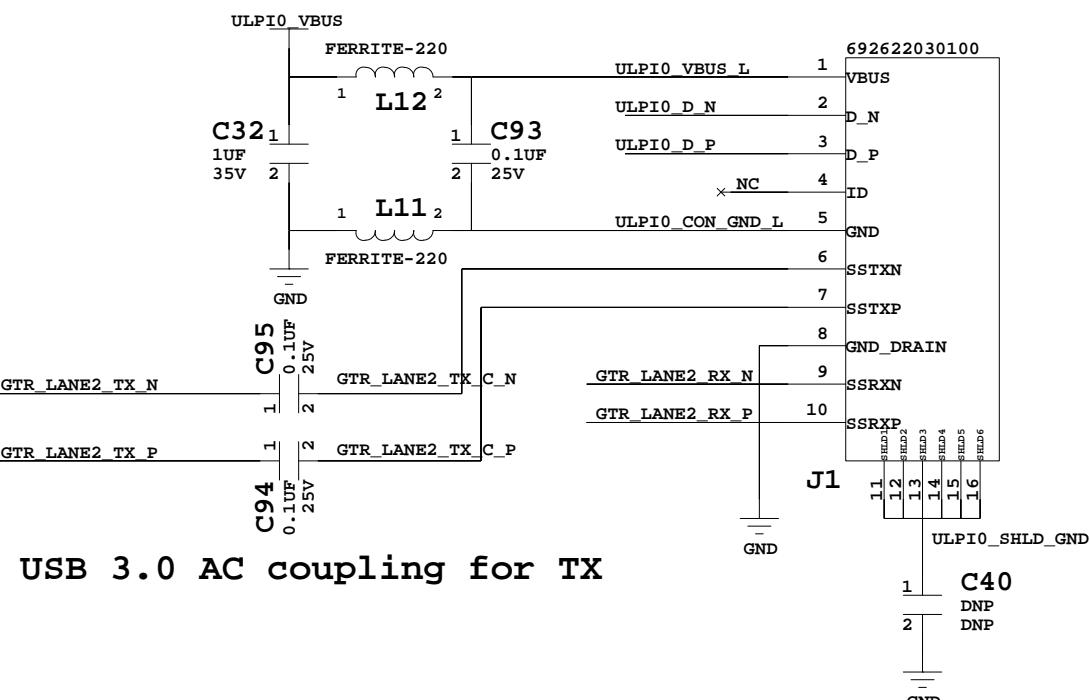
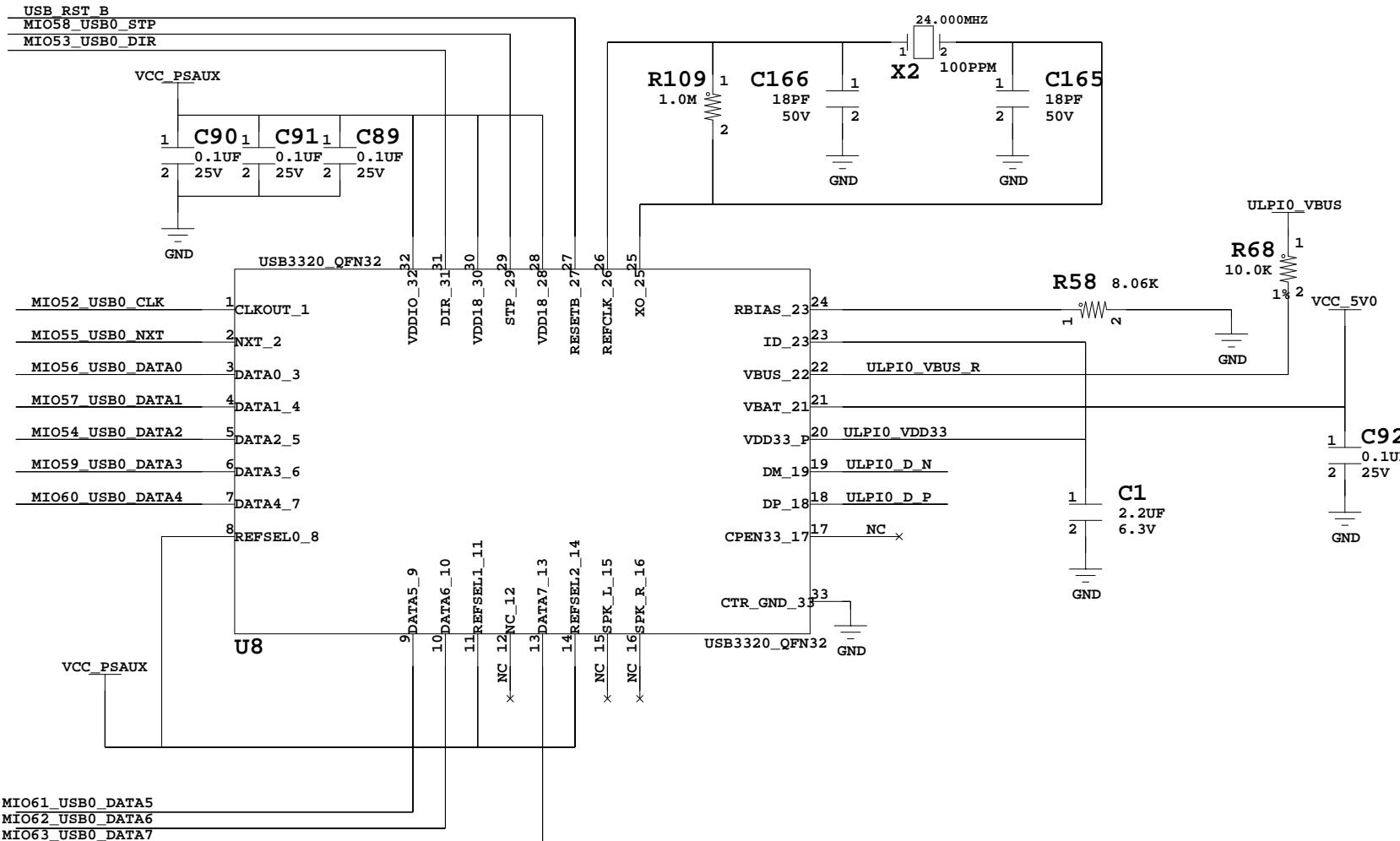


Avnet Design Services		
Project Name:	AES-ULTRA96-G	PCB Rev: BOM: Variant:
Doc Num:	1 01 00	
Sheet Title:	SCH-US1DEV	Date: 3/9/2018 Time: 12:24:07 pm
Size:	B	Sheet: 20 of 27



PS WiFi - Bluetooth



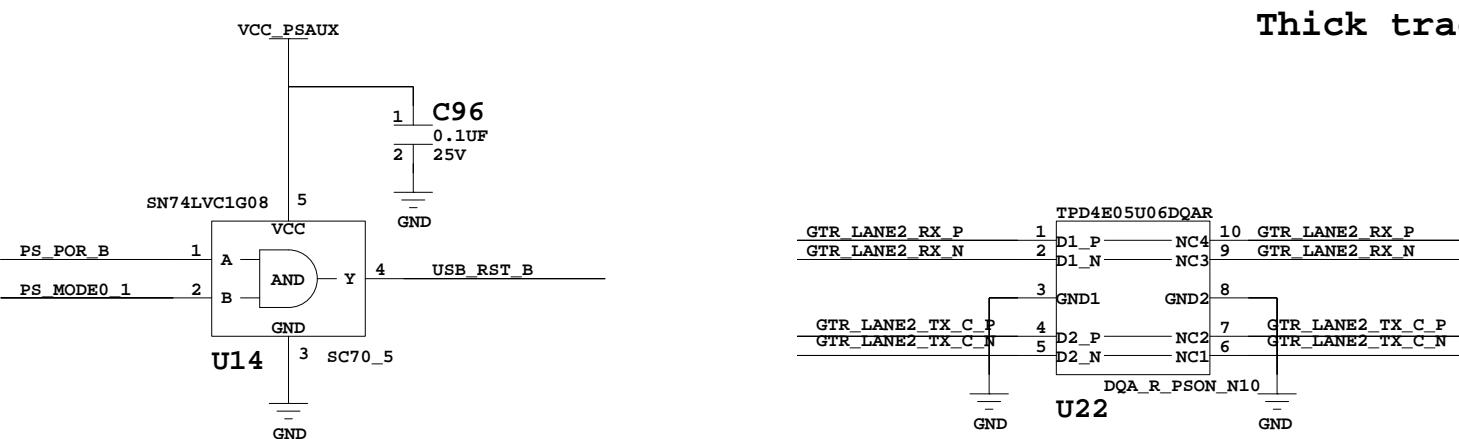


USB 3.0 AC coupling for TX

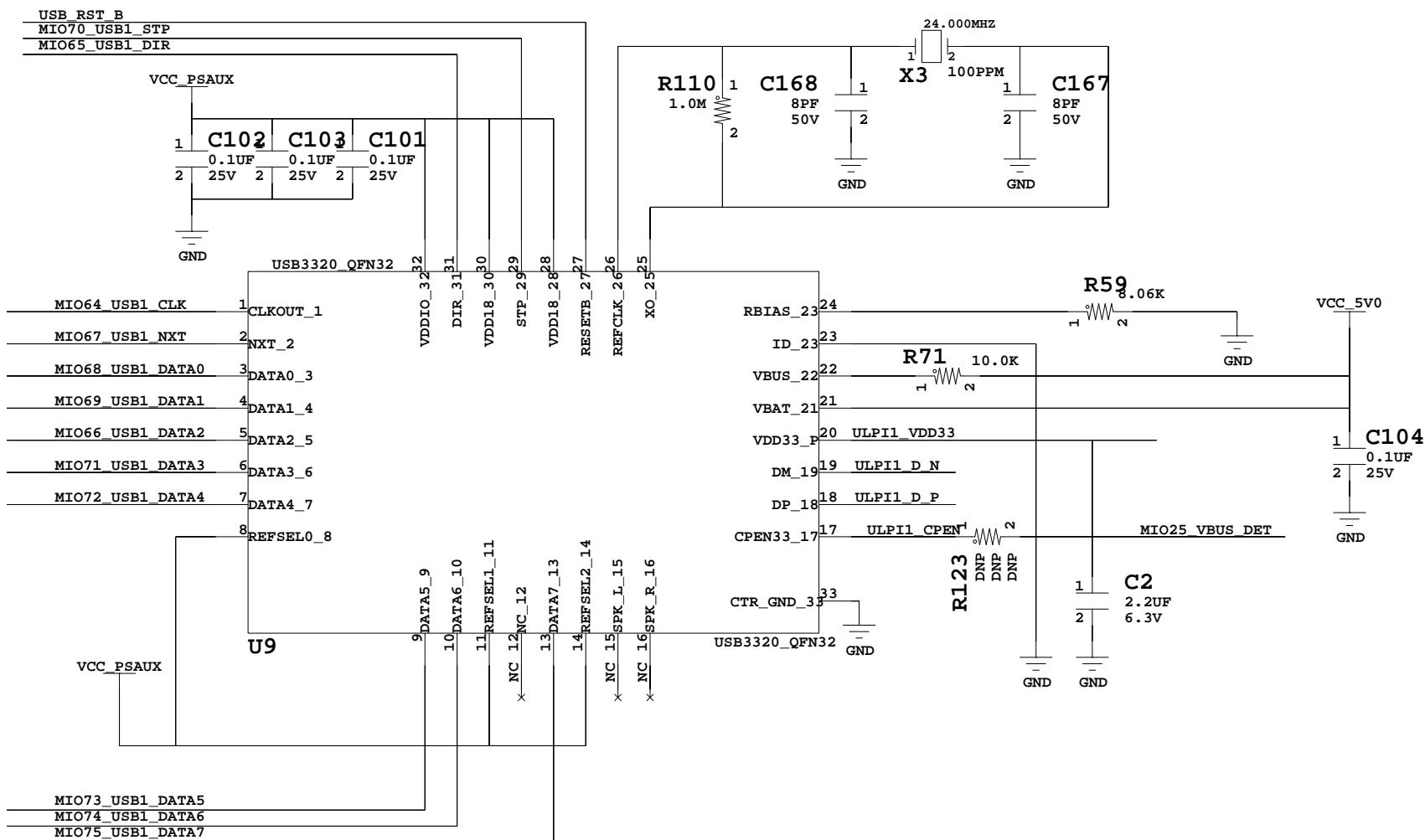
90 ohm impedance for USB 2.0 ULPI_D_P/N,

100 ohm for USB 3.0 USB_SSTX_P/N, USB_SSRX_P/N

Thick trace for ULPI_VBUS and related nets



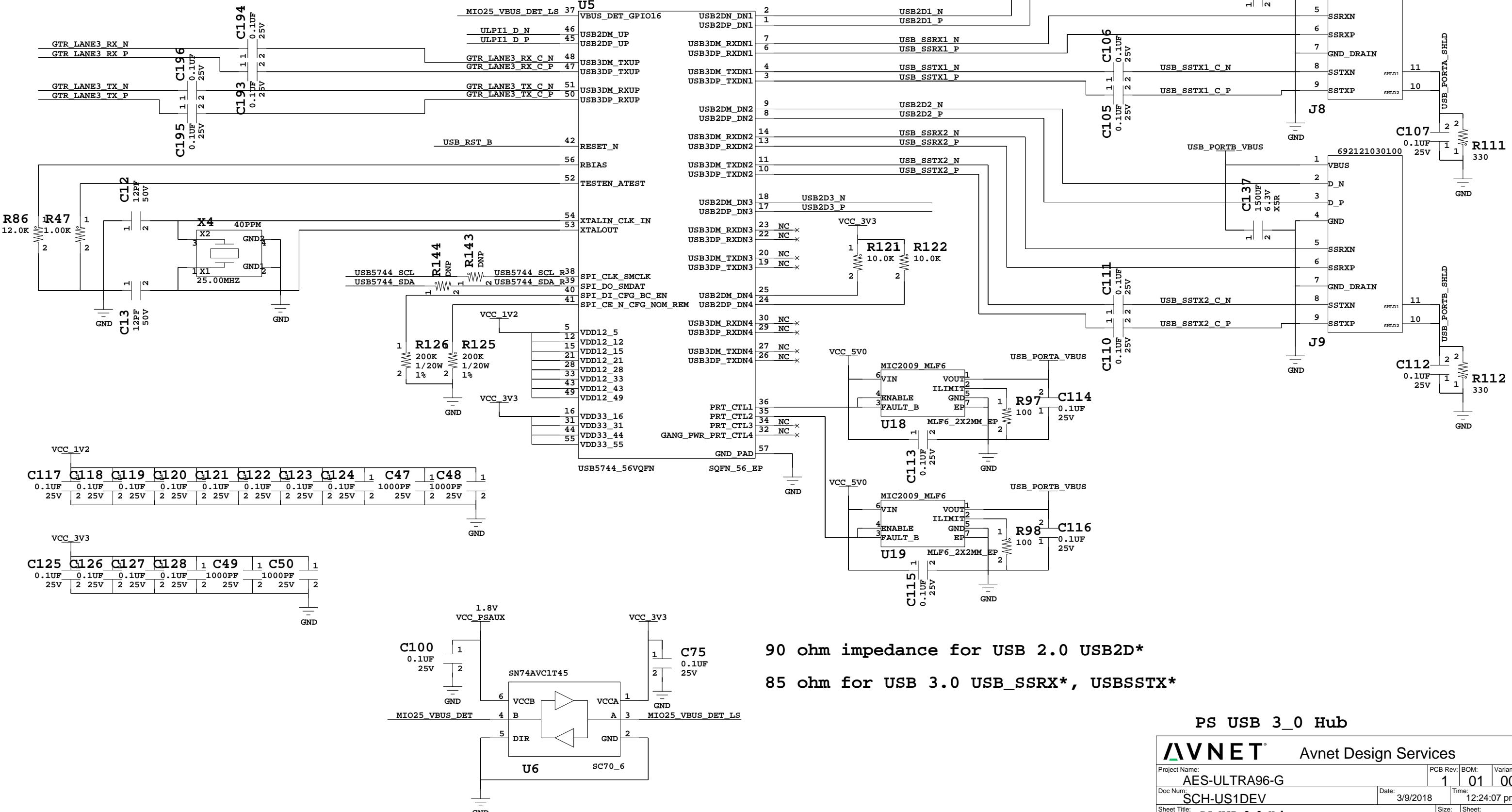
PS USB 3_0 ULPI Upstream

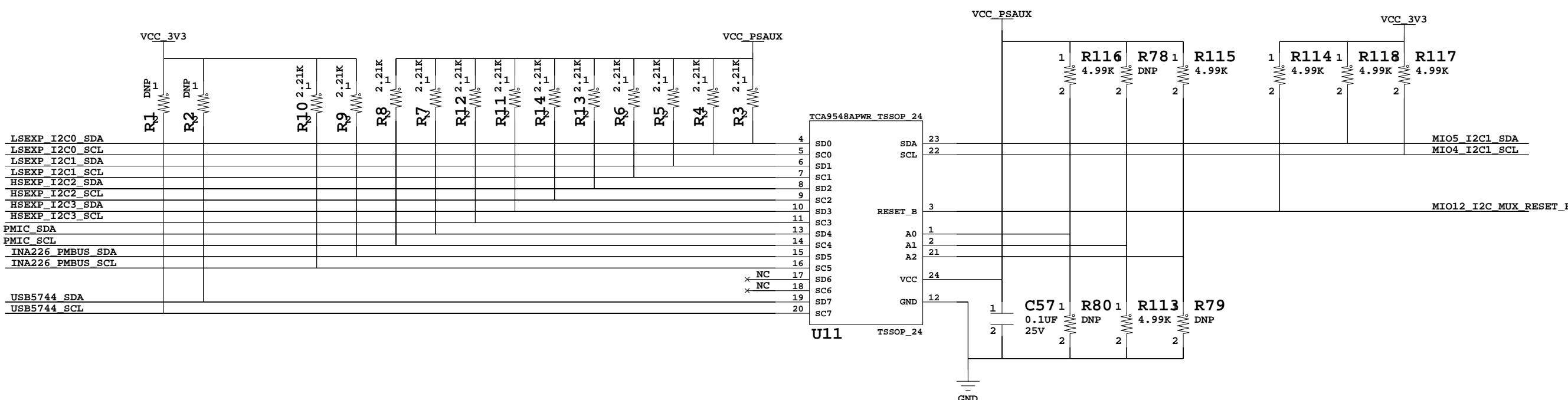


90 ohm impedance for USB 2.0 ULPI_D_P/N,

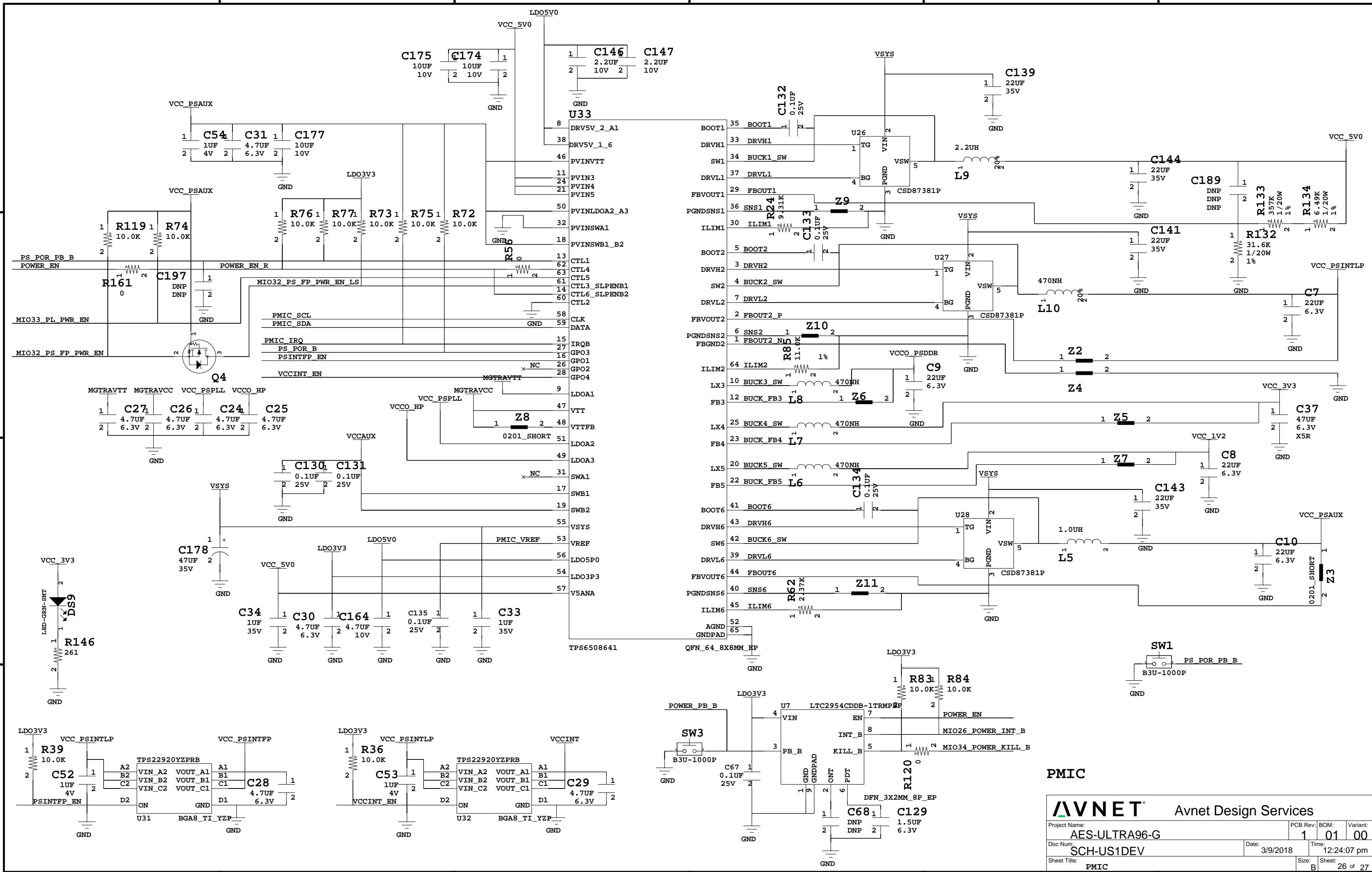
100 ohm for USB 3.0 GTR_LANE3*

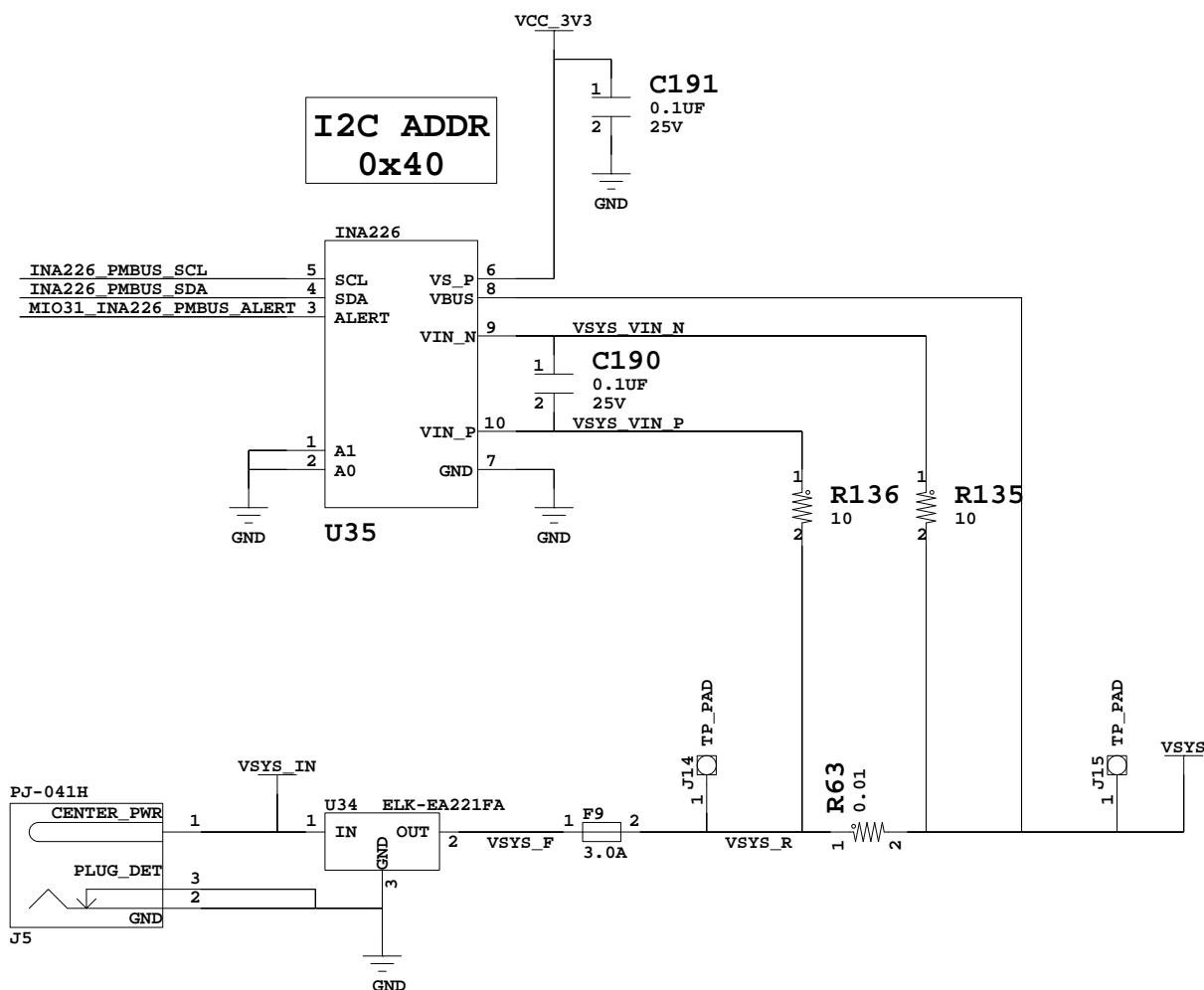
USB 3.0: Connect TX to RX, add AC coupling



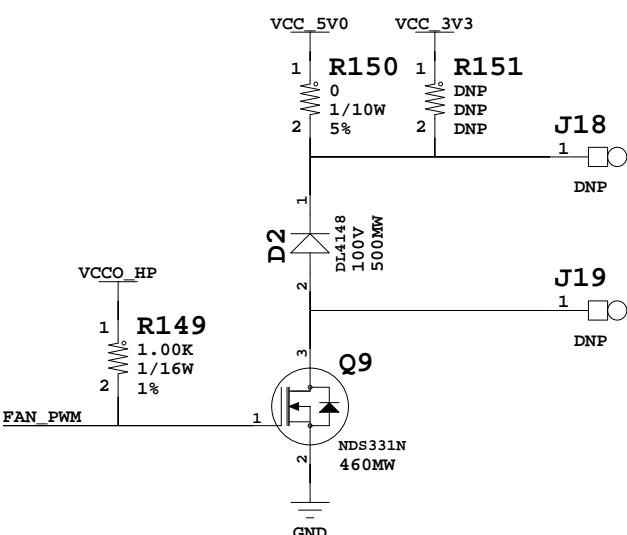
**I2C MUX**

AVNET® Avnet Design Services		
Project Name:	PCB Rev:	BOM:
AES-ULTRA96-G	1	01
Doc Num:	Date:	Variant:
SCH-US1DEV	3/9/2018	12:24:07 pm
Sheet Title:	Size:	Sheet:
I2C MUX	B	25 of 27





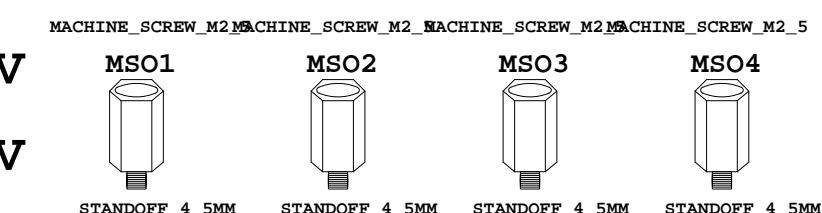
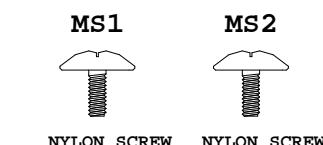
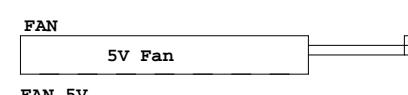
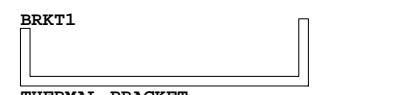
Fan wires, place near board edge



RAIL

RAIL	VOLTAGE
VCC_PSINTFP	0.85V
VCC_PSINTLP	0.85V
VCC_PSPPLL	1.20V
VCC_PSAUX	1.80V
VCC_PSDDR	1.10V
MGTRAVCC	0.90V
MGTRAVTT	1.80V
VCCINT	0.85V
VCCAUX	1.80V
VCCO_HP	1.20V
VCC_5V0	5.00V
VCC_3V3	3.30V
VCC_1V2	1.20V
LDO5V0	5.00V
LDO3V3	3.30V
USB_PORTA_VBUS	5.00V
USB_PORTB_VBUS	5.00V
DP_VCC3V3	3.30V

Power Connector - Mounting Holes



STANDOFF_4_5MM STANDOFF_4_5MM STANDOFF_4_5MM STANDOFF_4_5MM

