

PHYS 479 Final Report

Flip-Chip fabrication and testing

A. Silberstein, T. Martz-Oberlander, Z. Berkson-Korenberg, J. Mainville, and G. Gervais
McGill University
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The study of the integer (IQHE) and fractional (FQHE) quantum Hall effects constitutes one of the largest areas of research in condensed matter physics in the 21st century. The goal of this project is to fabricate a topological Qubit on a semiconductor by leveraging non-Abelian states, such as the 5/2 FQHE. We have assembled a Flip-Chip device, which gates a GaAs wafer while not degrading its electron mobility. We will then perform the wanted measurements on the device.

I. INTRODUCTION

The Nobel prize winning discovery of the quantum Hall effect in 1980 by Klaus von Klitzing [1] marked a turning point in condensed matter physics as it showed that electronic resistance could be defined precisely in terms of fundamental constants, even in a disordered and irregular sample. The search for a robust Qubit is central to the field of Quantum computing as the fragility of current Qubit is the main bottleneck of current quantum computers. The theorized non-Abelian state of the 5/2 Fractional Quantum Hall Effect (FQHE) could form the basis for a more robust topological Qubit.

II. THEORY BACKGROUND

Theoretical context will first be given to motivate the project starting with the Quantum Hall Effect, two dimensional electron gases, anyons and finally anyon interferometry. An overview of the experimental design will then follow. The measurement setup and the measurements taken will be presented. These involve evaluating the quality of each contact on the wafers, measuring gate leakage, and testing the ability of the gates to form a potential barrier on the wafers.

A. Hall effect

Consider a rectangular thin conducting material in the $x - y$ plane. If a current is applied across the material in the x direction and a magnetic field is applied in the z direction, the Lorenz force $F = q(\mathbf{v} \times \mathbf{B})$ will cause the moving charge to deviate in the y direction. The result is a voltage difference in the y direction called the Hall Voltage, $V_H = BI/ne$ [2], where n is the electron density and e the charge of an electron. From Ohm's law, the Hall resistance is $R_H = B/ne$. In this classical regime, a linear relationship between R_H and B is expected. We will be interested in how this effect changes in the quantum mechanical regime.

B. Two-dimensional electron gas

In our case, the conducting material called the wafer is made of a Aluminum Gallium Arsenide/Gallium arsenide (AlGaAs/GaAs) heterostructure. Physically, this corresponds to a thin ($\sim nm$) layer of GaAs between two layers of AlGaAs. The AlGaAs has a larger bandgap [3] than the GaAs so the energy of the conducting band in the GaAs is lower than in the AlGaAs. Hence, the electrons in the conducting band of the AlGaAs fall into the conduction band of the GaAs. When the thermal energy given by $k_B T$, where k_B is Boltzmann constant and T is the temperature, is less than this difference in conducting band energies, the electrons are stuck in the thin GaAs layer. This structure called a *Quantum well* restricts the conducting electrons to the thickness of the GaAs ($\sim nm$). The system is therefore called a 2D electron gas. One important metric of a wafer is its *electron mobility* defined as $\mu := v_d/E$ where v_d is the drift velocity and E is the electric field. A higher electron mobility leads to better overall performance. In the case of field-effect transistors, this means an increase in its frequency [4].

C. Quantum Hall Effect

In a 2DEG, at high B and low T , the linear relationship between R_H and B breaks down.

In the presence of the magnetic field, the energy states of the electrons collapse onto orbits of quantized radii called Landau levels (LLs). Each LL is separated by an energy of

$$\Delta E = \hbar\omega_c = \frac{\hbar e B}{m^*} \quad (1)$$

where \hbar is the Planck constant divided by 2π , ω_c is the cyclotron frequency, and m^* is the electron mass [5].

The number of electrons per LL (per unit area) is given by

$$d = \frac{\Phi}{\Phi_0 A} = \frac{Bh}{e} \quad (2)$$

where $\Phi = \mathbf{B} \cdot A\hat{z} = BA$ is the magnetic flux that is quantized by units of $\Phi_0 = h/e$ [6], and A is the area

of the 2DEG sample. Hence, for every additional $\Phi_0 A$ passing through the sample, each LL has room for one more electron. At low temperature, the Fermi level is the highest energy level that an electron can occupy, therefore at fixed B , the LLs of energy below the Fermi level are accessible and are thus filled by electrons [5]. From equation (1), as B increases so does d meaning that new states for electrons at lower energy LLs are available. The electrons at the higher LLs will therefore fill these states, leaving the higher energy LLs partially unfilled. Thus, at certain points B_i when sweeping the magnetic field, an integer i of LLs will be exactly filled [2]. This would require $n = di$. In this case, solving for B in equation (2) yields

$$B_i = \frac{\Phi_0 d}{A} = \frac{hd}{eA} = \frac{nh}{ie} \quad (3)$$

where h is Planck's constant. At this magnetic field, the Hall Resistance from before becomes quantized since

$$R_H = \frac{B_i}{ne} = \frac{h}{ie^2} \quad (4)$$

now depends on the inter i . This discreteness is shown in blue in Figure 1. At these specific values of B , near absolute zero, electron scattering is not possible as the lower energy states are all filled while the higher energy states are not accessible. This translates to no dissipation and therefore no resistance, $R_x = 0$ [6] (see the purple line in Figure 1). However, straight lines at fractional values

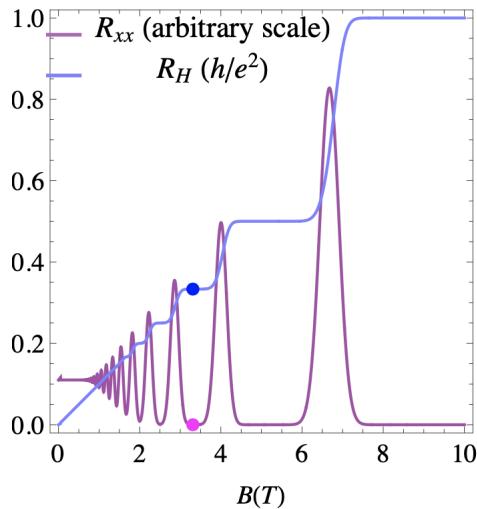


FIG. 1: Snapshot from a Mathematica applet illustrating the quantization of Hall resistance R_H and vanishing of longitudinal resistance R_{xx} in the quantum Hall regime (after work by G. Jelbert and N. Walet). We see that the plateaus correspond to an integer number of Landau levels filled. [2].

of i such as $1/3, 2/5, 3/7$, have also been observed [7], meaning that, for example, when the lowest energy LL is only $1/3$ filled, a slight increase in B does not modify R_H .

The electron model is no longer sufficient to explain this Fractional Quantum Hall Effect (FQHE). Quasiparticles called anyons which obey anyonic (fractional) statistics are required, they obey neither Fermi-Dirac nor Bose-Einstein statistics. When the denominator of the fraction is odd, these results can be explained by Laughlin states [8][9] and the *hierarchical model* [10]. However, a $5/2$ state was observed by R. Willet *et al.* [11] which breaks this rule.

D. $5/2$ state of the FQHE

To explain this special $5/2$ state, the Moore-Read Pfaffian [12] and anti-Pfaffian [13] models suggest that the anyons obey non-abelian statistics [14]. In two dimensions, the motion of n anyons in space time can be represented by the Braid group \mathbb{B}_n shown in Figure 2[14]. The vertical direction of the page would be time, the horizontal direction would be a spatial dimension, and into-the-page (not visible) would be the second spatial dimension. For instance, σ_1 would mean that *anyon*₁ and *anyon*₂ have swapped positions, they performed a *braiding exchange operation*. While an electron has 2 degrees of freedom, spin-up and spin-down, an anyon obeying non-Abelian statistics would have non-integer degrees of freedom such as $\sqrt{2}$. This could form the basis of a topological Qubit for a quantum computer [2].

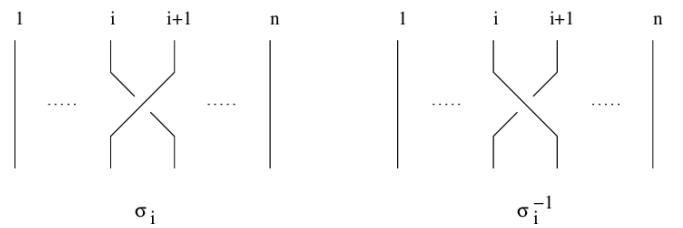


FIG. 2: Illustration of the elements of the Braid group \mathbb{B}_n . σ_i represents string i crossing behind string $i + 1$ while σ_i^{-1} represents string $i + 1$ crossing behind string i . For example a traditional infinite hair braid would be $\prod_{i=1}^{\infty} \sigma_i^{-1} \sigma_i$.

The goal of this project is to learn more about anyonic statistics through their experimental measurement. The experiment would attempt to perform a braiding operation of anyons by having two anyons travelling along the same trajectory separate and then latter recombine. One could then measure the acquired phase difference [2]. This is analogous to interferometry but with anyons instead of photons.

E. Topological conductors

To perform optical interferometry, one must have precise control over the light beam. Similarly, for anyon interferometry, precise control of the current is required (since anyons are charged particles). In a magnetic field, this is possible by taking advantage of the topological properties of conductors. As seen in Figure 3, in a conductor subjected to a perpendicular magnetic field, the trajectory of a single charged particle not near an edge, looks like a circular orbit. It therefore doesn't contribute to any macroscopic current. However, at the edge, the charged particle completes half circles as a potential barrier is formed by the edge. These charged particles therefore contribute to a current on the edge of the sample (see the green line in Figure 3). The result is that under a magnetic field, a conducting sample will have an edge current going around the sample. This phenomena is independent of sample shape which is what makes it *topological*. Any potential barrier restricting the charged particles will cause the edge current, this includes a voltage from a nearby conductor such as gold gates.

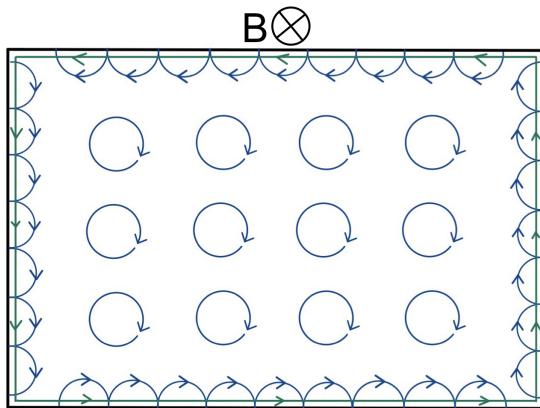


FIG. 3: Conductor under a perpendicular magnetic field. The trajectory of the charged particles at certain positions is seen in blue. The net induced current in in green, it is along the edge.

F. Anyon interferometry

Precise control of the current can therefore be achieved by applying a voltage on gates placed right above the 2DEG. Since the role of the gates is to control the current in the 2DEG while not directly exchanging particles with it, a thin insulating layer is required between the 2DEG and the gates. This is done by the top AlGaAs layer since, due to the low temperature, electrons are not able to reach its conducting band. To split the current, gates separated by a distance on the nanometer scale are used, these are called Quantum Point Contacts (QPCs). When the voltage applied to these gates is tuned just right,

as seen in Figure 4a, the quasiparticles starting in the bottom left have a non zero probability of following the blue, red or green paths. By comparing the different phase acquired at each of the four corners of the 2DEG, one is able to measure the interference between anyons as they perform braiding exchange operations and travel along different paths before recombining [2]. In the case of a perpendicular magnetic field, the phase difference $\Delta\phi$ is given by

$$\Delta\phi = \frac{e^* BS}{\hbar} \quad (5)$$

where e^* is the effective charge of the particle and S is the area of the central region [2]. This interference results in oscillation of the measured R_H . The period of this oscillation reveals the charge of the quasiparticles. It is theorised that this charge is $e/4$ for an anyon [2].

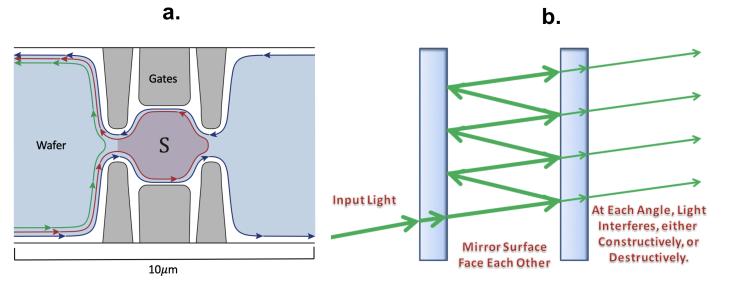


FIG. 4: **a.** Illustration of the different possible channels that current can take. In blue is the region of the 2DEG accessible to electrons. In white is the region of the 2DEG that is not accessible to the electrons due to the voltage applied to the gates. The gates are in grey. The edge currents are shown by the blue, red and green lines. In reality, these three lines all overlap the blue line as they must be at the edge. Interference occurs between the reflected (green, leftmost) and transmitted (red, encircling the central area) edge currents. The phase accumulated by the transmitted current can be tuned by a modification of the central area S [2]. **b.** Illustration of an optical Fabry-Perot interferometer. The input light is reflected or transmitted by the inner mirror multiple times. The transmitted light is then recombined with a lens (not shown in diagram). [15].

This anyon interferometer is named a Fabry-Perot interferometer due to its similarity with an optical Fabry-Perot interferometer (see Figure 4b) where a semi-transparent mirror and non-transparent mirror face each other. When a photon hits the semi-transparent mirror, it has a non zero probability of traversing the mirror or being reflected. Interference then occurs when the different beams are recombined with a lens.

III. FLIP-CHIP DEVICE

The goal of the experiment is to build such a device. The 2DEG wafers are supplied by Sandia National Laboratories (NM) or L.N. Pfeiffer at Princeton. Then, the gates must be placed on the 2DEG. The straightforward method of doing this is through Electron Beam Lithography (EBL) directly on the wafer. However, this can damage the wafer. Therefore, the gates are deposited on a slab of sapphire that is then mechanically attached to the top of the wafer. This method of gating wafers was developed in the Gervais Lab and is called the Flip-Chip method [2].

To perform the experiment, one must be able to measure the current at the four corners of the wafer as well as supply voltages to the gates. So wires must be connected to all these points. The main step in the assembly process consists of soldering wires from the wafer and gates to a PCB which will connect to the hardware in the cryogenic freezer. Due to the sensitivity of the measurements, these wires must be gold wires of diameter $25\mu\text{m}$ or $50\mu\text{m}$. The soldering process is therefore challenging. When mounting the gates onto the 2DEG, the proximity between the gates and the 2DEG is crucial. It is essential that the surface of the 2DEG is free of any dust particles that could prevent the gates from laying extremely flat on the wafer. The assembly process must be done in the clean room (McGill Nanotools Microfab) to avoid contaminating the wafer with dust particles. As the very tip of the gates are only approximately $1\mu\text{m}$, they are prone to burning by electrostatic discharge. It is therefore important to always be grounded during the assembly process. At the start of the semester, training in the clean room was required. Next, the work consisted of learning and practicing the steps involved in the assembly process. After the wires between the pins and contacts on the wafer and gates are soldered, the next step was to apply downwards pressure on the sapphire to ensure contact between the surface of the wafer and the gates on the sapphire. This was done by placing a sapphire top plate above the current sapphire with the gates. This top plate is then held down by screws attached to the PCB [2]. The final device is shown in Figure 5.

Unfortunately there were several issues with the device such as small scratches on the surface of the wafer, burnt gates and some issues with a few of the contacts on the wafer. Therefore other simpler devices assembled by T. Martz-Oberlander, as depicted in Figure 6, were instead put on the dilution fridge.

The first device (Figure 6a) is a High-Electron-Mobility Transistor (HEMT). The gates consist of a simple gold bar across the center of the wafer. The second device (Figure 6b) is similar to the Flip-Chip but with only one gate on each side instead of three.

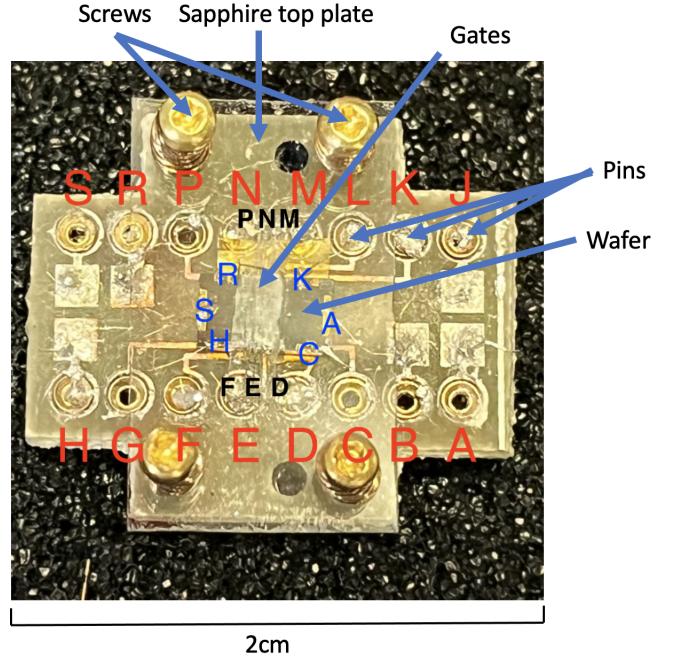


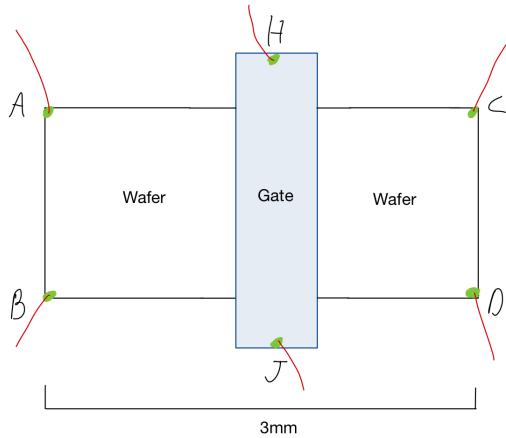
FIG. 5: Image of the Flip-Chip from above. The wafer is at the center with gold wires soldered to each corner. The other ends of the wires are soldered to pins on the PCB. The sapphire with the gates is seen on top of the wafer with the gates being on the bottom side as they are in contact with the wafer. As seen in Figure 4a, there are three distinct traces on each side, these get much wider as they get further from the center. These 6 traces, 3 on each side are visible. At the far end of the sapphire, each of the 6 traces has a gold wire soldered to it which is also soldered a pin on the PCB. The 4 screws hold down a sapphire top plate which ensures the contact between the gates and the wafer.

IV. MEASUREMENT SETUP

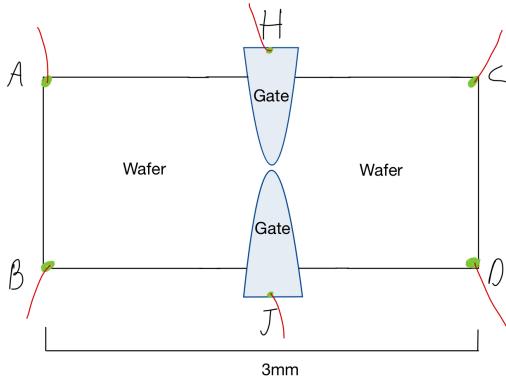
The devices are put in a dilution fridge as seen in Figure 7a. A diagram of the inside of the fridge is shown in Figure 7b.

The devices are placed at the center of the fridge where it says sample on the diagram. Each pin on the device which is labelled by a letter has a direct connection to one of the switches on the breakout box (Figure 8) labelled by the same letter. Each contact on the wafer and gates can be directly interacted with through the gold wires, pins and breakout box. On the breakout box, each pin has a switch to the left and right. The right switch (labelled PIN) controls whether the connection is grounded (switch down) or floating (which means not grounded) (switch up).

To close the fridge three different metal cans are attached from inside out in growing sizes. The first one is inside the second which is inside the third. A pump is



(a) First device. This device is called a High-Electron-Mobility Transistor (HEMT) as it acts as a transistor. Applying a current to the gates controls whether current can flow through the wafer. This defines two states: ON or OFF.



(b) Second device. The two gates form a Quantum Point Contact (QPC) at the center as they are separated by a distance on the order of a μm .

FIG. 6: Simplified diagrams of the two devices in the fridge. The PCB and pins are not depicted. The letter associated with each contact is different on the real device. In red are the gold wires which are connected to the pins on the PCB. In green are the indium solder joints. The gates are above the wafer.

then used to create a vacuum. The cooling process can then begin using Helium-3. After approximately one day, the temperature reaches 0.1K.

V. DEVICE TESTING

Before more complex measurements can take place, we first check that the device works as intended. First, the quality of each contact on the wafer is tested. Second, the existence of gate leakage between the gates and the wafer is tested. Finally, the ability of the gates to act as

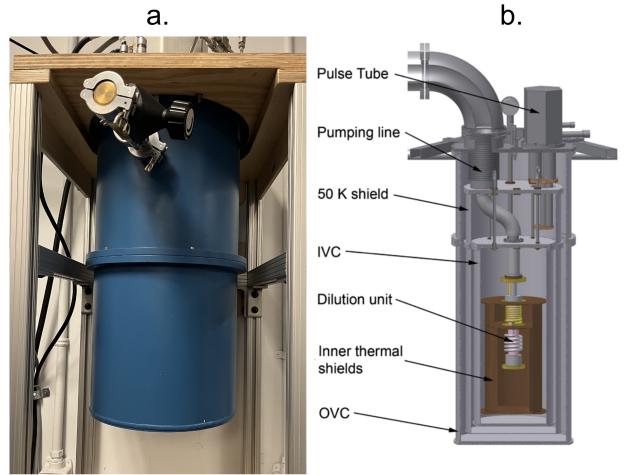


FIG. 7: a. Closed dilution fridge containing the devices. b. Diagram showing the components inside the dilution fridge. IVC (Inner vacuum chamber), OVC (Outer vacuum chamber). The devices are located at the very bottom, below the dilution unit [16].



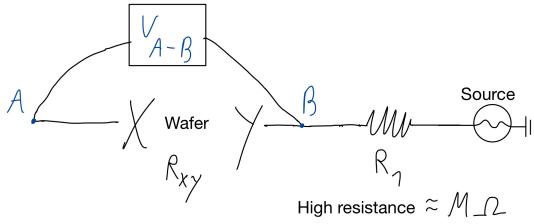


FIG. 9: Circuit diagram of a 2 point resistance measurement between contacts (arbitrary) X and Y on the wafer.

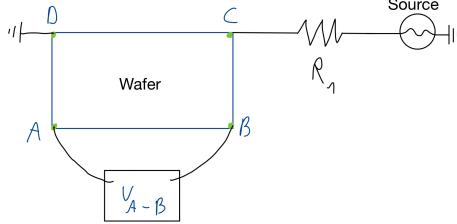


FIG. 10: Circuit diagram of a 4 point measurement where current is applied to the top right of the wafer, the top left corner is grounded, the resistance between contacts (arbitrary) A and B can then be deduced from the measured voltage difference V_{A-B} .

In this case the geometry of the contacts is very important. By taking various four point contact measurements one can calculate the sheet resistance of the wafer. The results of these measurements for the HEMT device is shown in Table 1. It is clear that contact W is defective as the measured resistance measurements using that contact are abnormally high. No 4pt measurements were thus taken with contact W. The very low $\sim \Omega$ 4pt resistance measurement on the other contacts indicate that these are working properly.

Contacts	2pt Resistance (Ω)	4pt Resistance (Ω)
V-Z	572	3.7
Y-X	806	4.0
Y-Z	828	3.4
V-X	548	3.0
Y-V	1053	1.4
Z-X	334	4.0
W-X	$1.5 \cdot 10^6$	N/A
W-Z	$1.5 \cdot 10^6$	N/A
W-U	$3.4 \cdot 10^6$	N/A
W-V	$1.5 \cdot 10^6$	N/A

TABLE I: 2 point and 4 point resistance measurements across the contacts on the wafer.

Next, we test for the existence of a gate leakage between the gates and the wafer. The role of the gates is to apply a potential barrier to the wafer. The gates must

therefore be extremely close to the wafer but there must be no continuity between them. The circuit used for this test is shown in Figure 11.

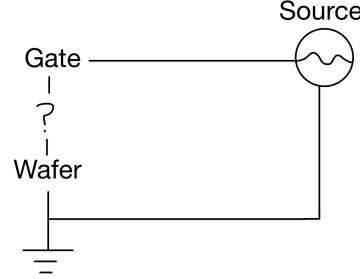


FIG. 11: Circuit to test for a leakage between the gates and the wafer. The source applies a small voltage to the gates while measuring the current from the circuit. If there is no continuity between the gates and the wafer the current in the circuit will be 0.

As voltage to the gates first travels through the gold wires, one possible explanation for a leak could be if a gate wire (a wire connected to the gates) was in contact with a wafer wire (a wire connected to one of the contacts on the wafer gates).

The third test determines if the gates are close enough to the wafer to act as a potential barrier. While measuring the conductance between opposite sides of the wafer, a voltage is applied to the gates. As this voltage increases a potential barrier should be created in the wafer which hinders current from flowing through the wafer. A large drop in conductance is therefore expected. This is called a pinch-off conductance measurement. A successful measurement is shown in figure 12. The result of this measurement on the device depicted in Figure 6b is shown in Figure 13.

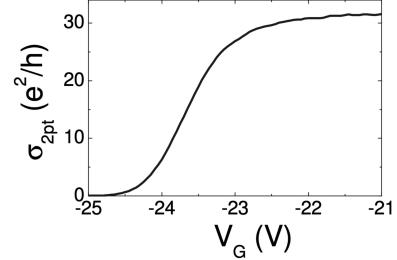


FIG. 12: Pinch-off conductance measurement on a similar device [17]. As the absolute value of the voltage increases a steep drop in conductance is observed.[17]

Although a drop in conductance has been observed, it is not large enough to come from a potential barrier from the gates. It is rather due to a leakage current between the top gate and the wafer. Further measurements are

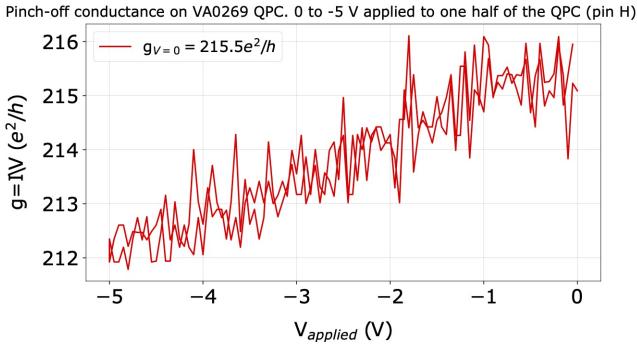


FIG. 13: Pinch-off conductance measurement on the device depicted in Figure 6b. The voltage is applied to only one of the two gates, the top one in the diagram, through pin H. As the absolute value of the voltage increases a small drop in conductance is observed.

therefore required.

VI. CONCLUSION

The objective of the project was to assemble a Flip-Chip device and perform measurements on it. This first objective was completed as seen in Figure 5. The measurements were however conducted on similar devices which are depicted in Figure 6. Testing of each solder joint on the wafer was done through many resistance measurements using the circuit shown in Figure 8. Then, testing for a current leak between the gates and the wafer was made using the circuit shown in Figure 11. Finally,

we test whether or not the gates indeed work as a gate for the current. This is done by measuring conductance across the wafer as the absolute value of the voltage is increased, this pinch-off conductance measurement was unsuccessful as seen by comparing Figures 12 and 13. During the summer, many Flip-Chip devices will be built so that measurements using the Fabry-Perot anyon interferometer can take place. The first important measurement is of the pinch off conductance across the QPC's that should be quantized by units of e^2/h [18]. Next, measurement of the Integer and Fractional QHEs can take place while sweeping the magnetic field. Finally, the goal would be to see experimental evidence of the braiding exchange operations of anyons at the 5/2 state through the use of the Fabry-Perot interferometer. The interest in this 5/2 state stems from the potential application to quantum computing as the non-Abelian exchange properties of the anyons could form the basis of a topological Qubit.

Another goal would be a capacitance measurement between the gates and the wafer while sweeping the magnetic field. Drops in capacitance are expected at integer filling factors [19].

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