

Operation of Altera DE2-115 Board and Quartus II software

1. Altera DE2-115 Board

As the logic circuit is more and more complex, implementation of circuit will have difficulties. Cause the difficult to achieve. Therefore, we use the DE2-115 board to emulate the logic circuit for realize the operation of circuit. The DE2-115 board has many features that allow the user to implement a wide range of designed circuits, from simple circuits to various multimedia projects. In addition to these hardware features, the DE2-115 board has software support for standard I/O interfaces and a control panel facility for accessing various components. Also, software is provided for a number of demonstrations that illustrate the advanced capabilities of the DE2-115 board. In order to use the DE2-115 board, the user has to be familiar with the Quartus II software. The necessary knowledge can be acquired by reading the tutorials *Getting Started with Altera's DE2-115 Board* and *Quartus II Introduction* (which exists in three versions based on the design entry method used, namely Verilog, VHDL or schematic entry). These tutorials are provided in the directory *DE2_115_tutorials* on the **DE2-115 System CD-ROM** that accompanies the DE2-115 board and can also be found on Altera's DE2-115 web pages.

A photograph of the DE2-115 board is shown in Figure 1. It depicts the layout of the board and indicates the location of the connectors and key components.

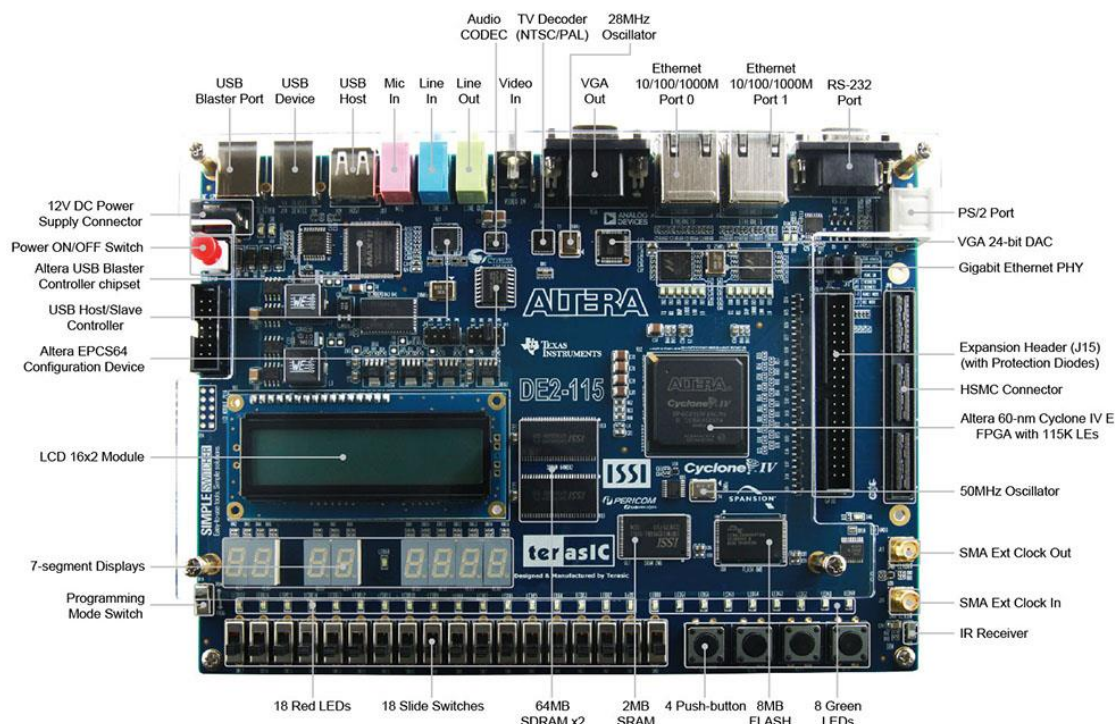


Figure 1. The DE2-115 Board

Table 1 below Altera DE2-115 experimental platform specification list:

Table 1. Altera DE2-115 Specification

FPGA	<ul style="list-style-type: none"> ● AlteraCyclone® IV EP4CE115 ● Altera Serial Configuration device – EPCS64
I/O	<ul style="list-style-type: none"> ● USB Blaster (on board) for programming and user API control; both JTAG and Active Serial (AS) programming modes are supported ● SD Card socket ● 50-MHz oscillator and 28.63-MHz oscillator for clock sources ● 24-bit CD-quality audio CODEC with line-in, line-out, and microphone-in jacks ● VGA DAC (10-bit high-speed triple DACs) with VGA-out connector ● 2 TV Decoder (NTSC/PAL/SECAM) and TV-in connector ● 10/100 Ethernet Controller with a connector ● USB Host/Slave Controller with USB type A and type B connectors ● RS-232 transceiver and 9-pin connector ● PS/2 mouse/keyboard connector ● IrDA transceiver ● 1 SMA connector
Memory	<ul style="list-style-type: none"> ● 128MB (32Mx32bit) SDRAM ● 2MB (1Mx16) SRAM ● 8MB (4Mx16) Flash with 8-bit mode ● 32Kbit EEPROM
Switches, light-emitting diodes	<ul style="list-style-type: none"> ● 18 switches and 4 push-buttons ● 18 red and 9 green LEDs ● Eight 7-segment displays

2. Quartus II software operation

Start the Quartus II software. You should see a display similar to the one in Figure 2. This display consists of several windows that provide access to all the features of Quartus II software, which the user selects with the computer mouse. Most of the commands provided by Quartus II software can be accessed by using a set of menus that are located below the title bar.

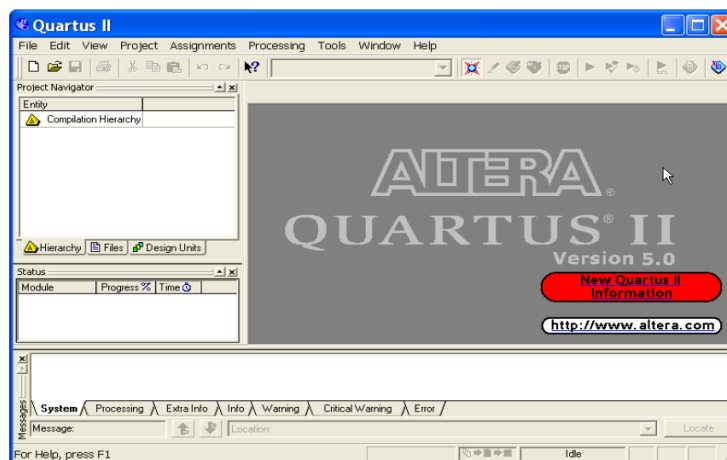


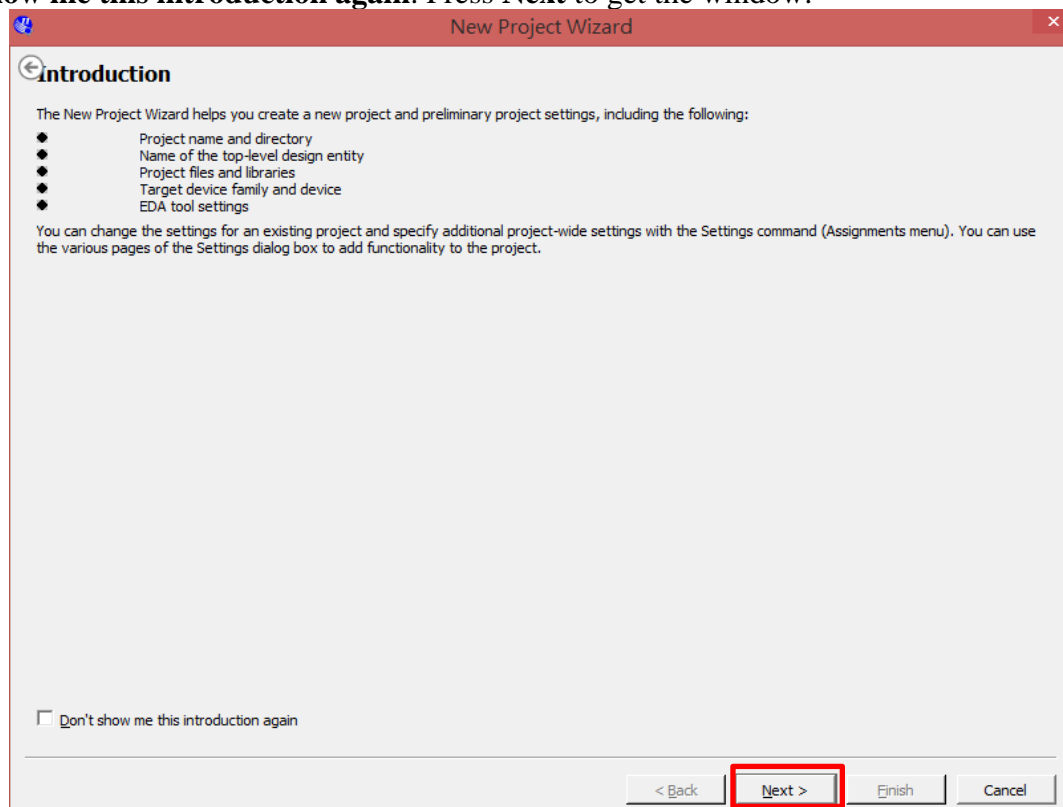
Figure 2. The main Quartus II display.

2.1 Project creation and programming

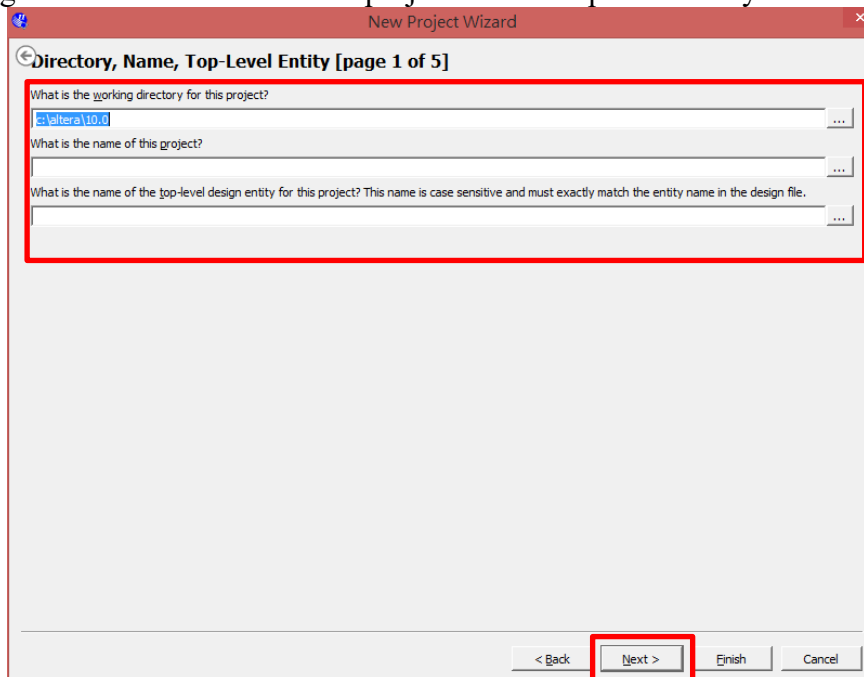
Step 1: Select **File > New Project Wizard** to reach the window, which indicates the capability of this wizard.



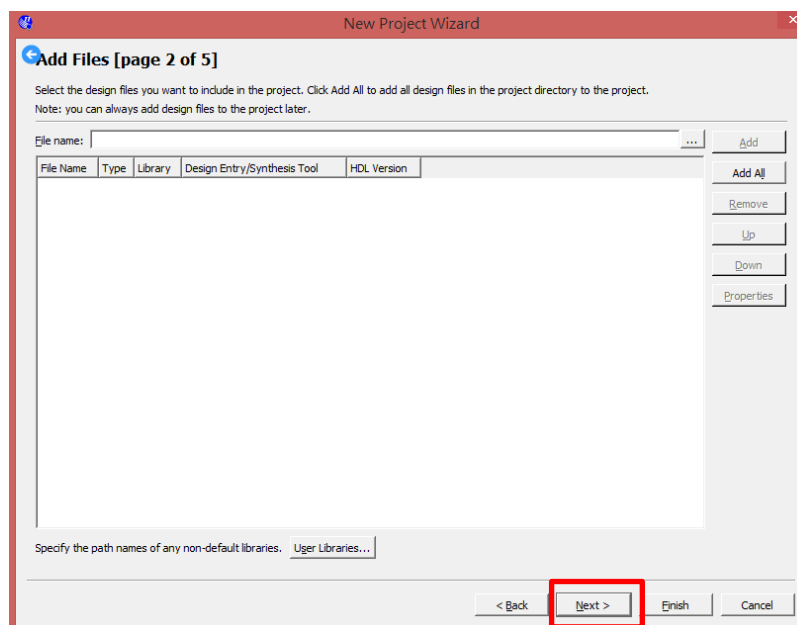
Step 2: You can skip this window in subsequent projects by checking the box **Don't show me this introduction again**. Press **Next** to get the window.



Step 3: Set the working directory to be *introtutorial*; of course, you can use some other directory name of your choice if you prefer. The project must have a name, which is usually the same as the top-level design entity that will be included in the project. Choose light as the name for both the project and the top-level entity. Press **Next**.



Step 4: The wizard makes it easy to specify which existing files (if any) should be included in the project. Assuming that we do not have any existing files, click **Next**.



Step 5: We have to specify the type of device in which the designed circuit will be implemented. Choose Cyclone IV E as the target device family. We can let Quartus II software select a specific device in the family, or we can choose the device explicitly. We will take the latter approach. From the list of available devices, choose the device called EP4CE115F29C7 which is the FPGA used on Altera's DE2 board. Press **Next**.

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family

Family: Cyclone IV E

Devices: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements
EP4CE75F29I7	1.2V	75408	427	2810880	400
EP4CE115F23C7	1.2V	114480	281	3981312	532
EP4CE115F23C8	1.2V	114480	281	3981312	532
EP4CE115F29C7	1.2V	114480	529	3981312	532
EP4CE115F29C8	1.2V	114480	529	3981312	532
EP4CE115F29I7	1.2V	114480	529	3981312	532

Companion device

HardCopy:

☐ Limit DSP & RAM to HardCopy device resources

< Back Next > Finish Cancel

Step 6: The user can specify any third-party tools that should be used. A commonly used term for CAD software for electronic circuits is *EDA tools*, where the acronym stands for Electronic Design Automation. This term is used in Quartus II messages that refer to third-party tools, which are the tools developed and marketed by companies other than Altera. Since we will rely solely on Quartus II tools, we will not choose any other tools. Press **Next**.

EDA Tool Settings [page 4 of 5]

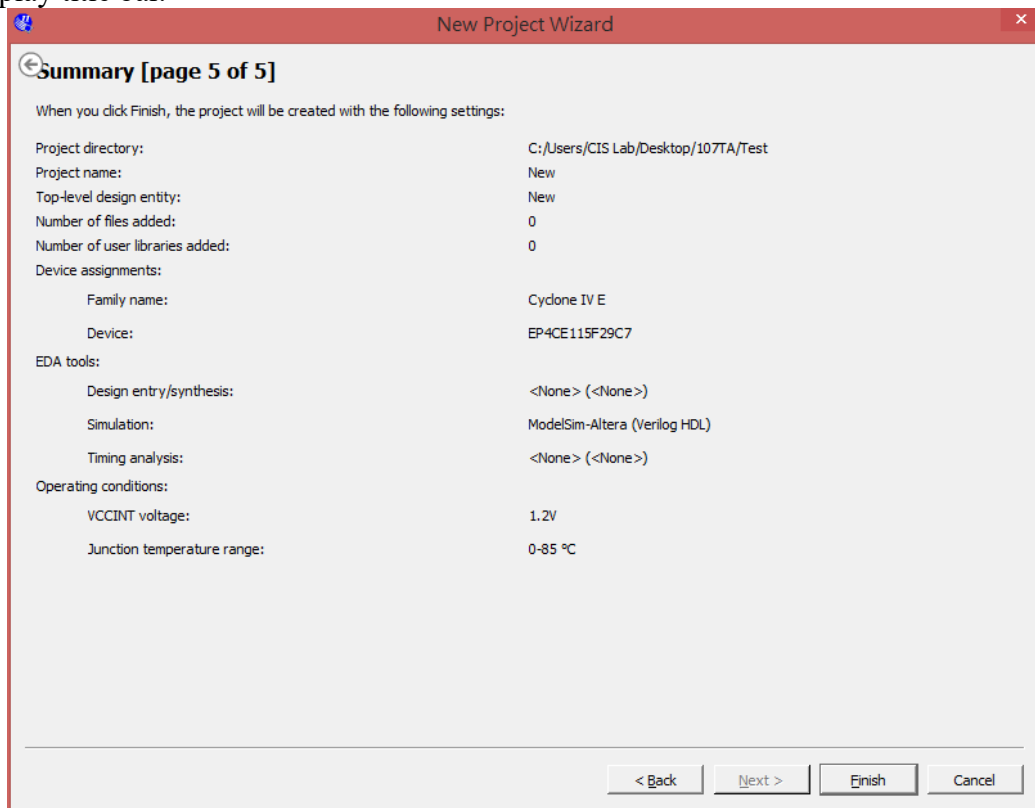
Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

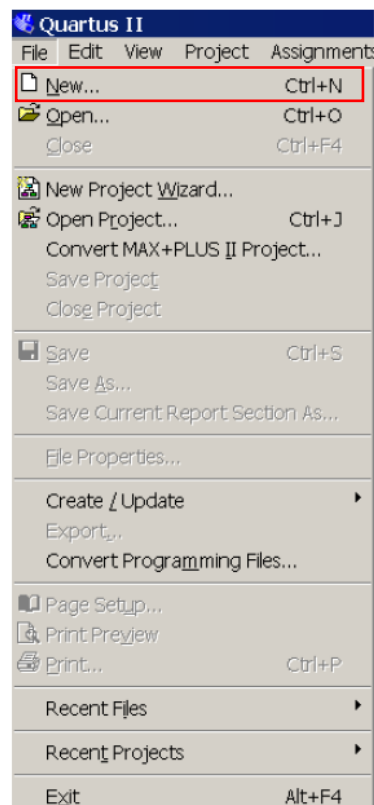
Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	Verilog HDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Timing Analysis	<None>	<None>	<input type="checkbox"/> Run this tool automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

< Back Next > Finish Cancel

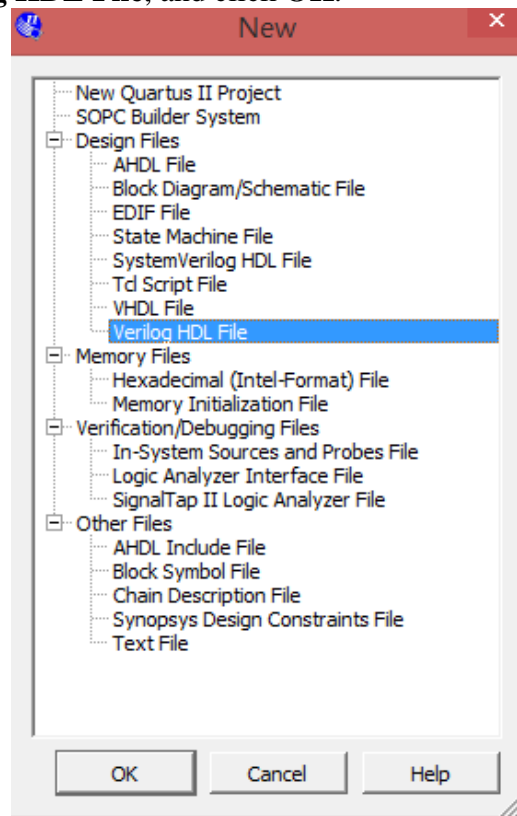
Step 7: A summary of the chosen settings appears in the screen. Press **Finish**, which returns to the main Quartus II window, but with light specified as the new project, in the display title bar.



Step 8: Select **File > New** to get the window.



Step 9: Choose **Verilog HDL File**, and click **OK**.

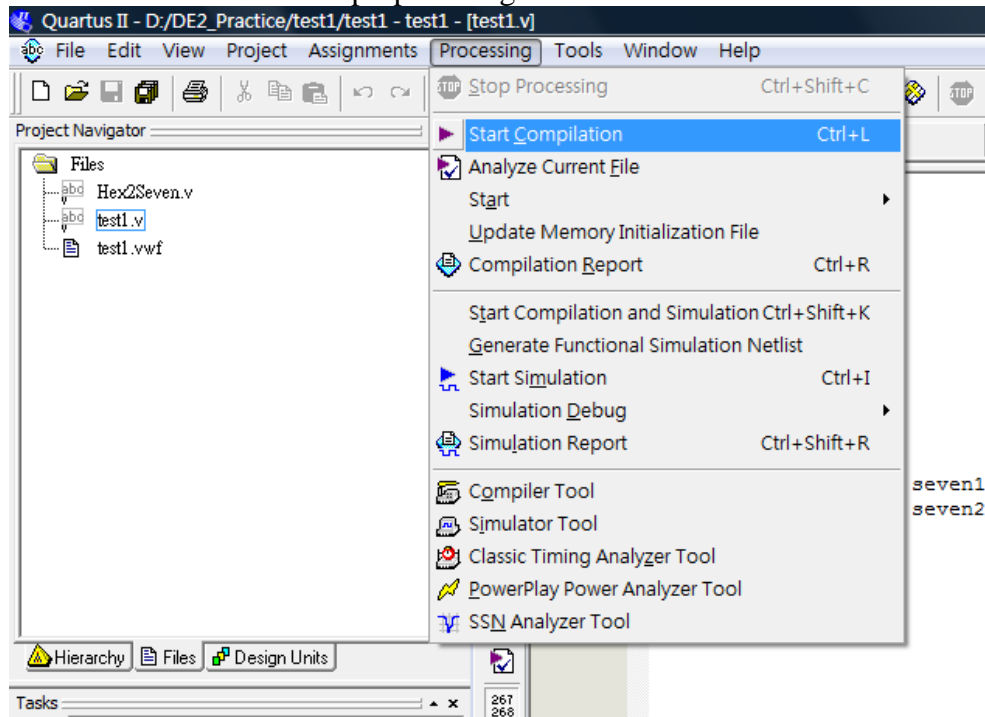


Step 10: Open a new document window, then you can start to write Verilog program.

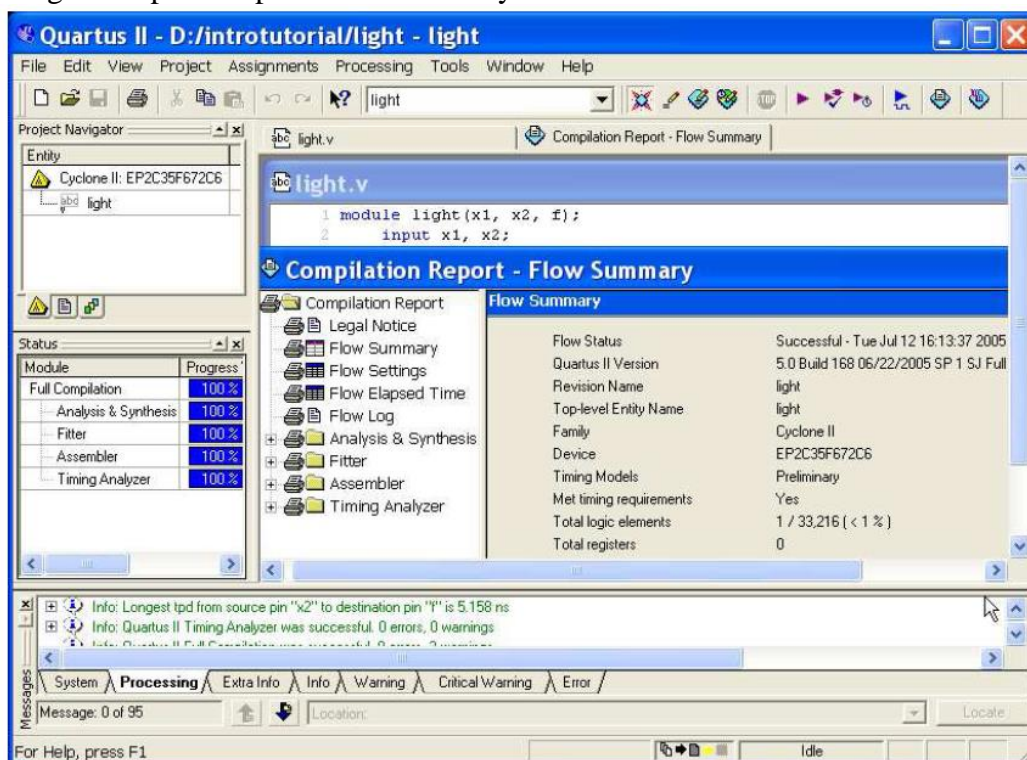


2.2 Compiling

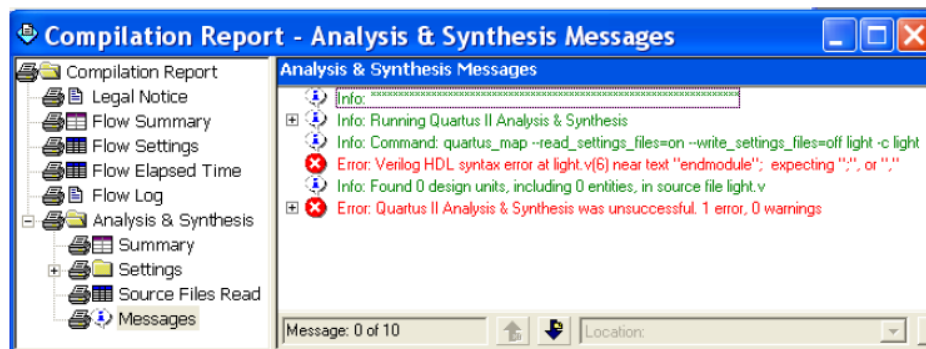
Step 1: Run the Compiler by selecting Processing > Start Compilation, or by clicking on the toolbar icon that looks like a purple triangle.



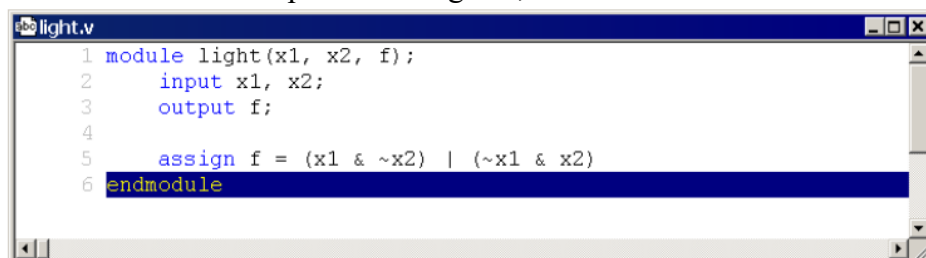
Step 2: When the compilation is finished, a compilation report is produced. A window showing this report is opened automatically.



Step 3: Expand the Analysis & Synthesis part of the report and then select Messages to have the messages displayed as shown in following figure. Double-click on the first error message.



Step 4: The error in this example is missing a “;”.

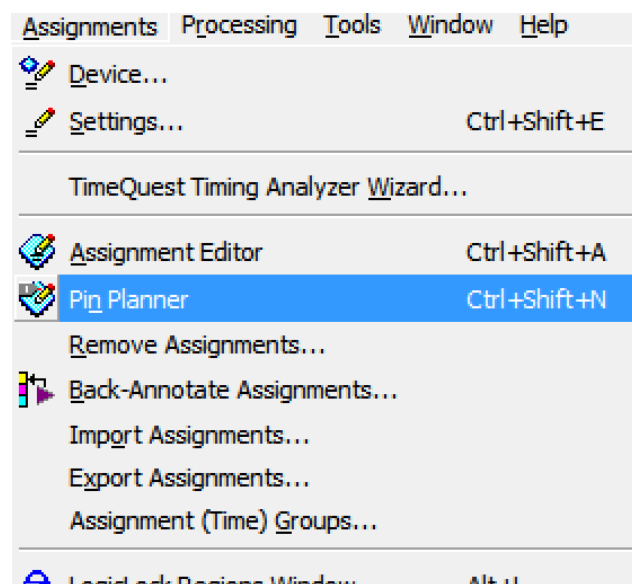


Step 5: Compiling complete.

2.3 Pin Assignment

If we want the program controls the hardware on the board (e.g, Toggle switch, LED, or Seven-segment) , we must set the assignment the pin.

Step 1: After compilation completed. Under 「Assignments」 we select 「Pin Planner」.



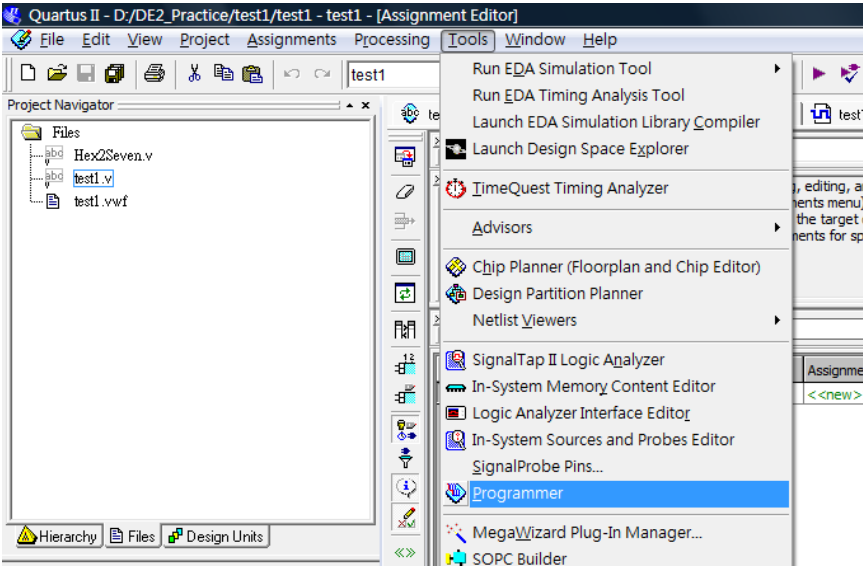
Step 2: Display all variable name in the Node Name field after Compiling complete then following the Pin Table fill up to Location field by corresponding Pin.

Node Name	Direction	Location
seg1[7]	Output	PIN_M24
seg1[6]	Output	PIN_H22
seg1[5]	Output	PIN_J22
seg1[4]	Output	PIN_L25
seg1[3]	Output	PIN_L26
seg1[2]	Output	PIN_E17
seg1[1]	Output	PIN_F22
seg1[0]	Output	PIN_G18
seg2[7]	Output	
seg2[6]	Output	PIN_AA14
seg2[5]	Output	PIN_AG18
seg2[4]	Output	PIN_AF17
seg2[3]	Output	PIN_AH17

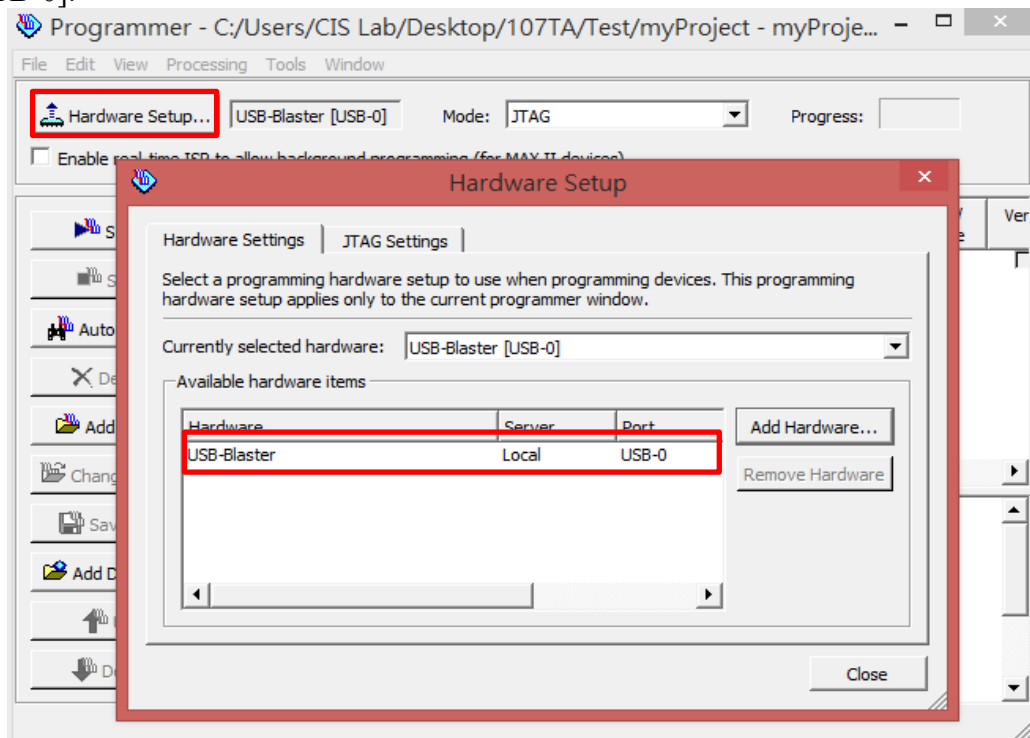
Step 3:Complete Assign.

2.4 JTAG Programming

Step 1: Select 「Tools」 > 「Programmer」 .



Step 2: Click the 「Hardware Setup」 on the up left corner then select 「USB-Blaster [USB-0]」.



Step 3: Back to Programmer window, check whether the compiled program (.sof or .pof) is already in the list. Also, check 「Program/Configure」 whether is selected. It can choose JTAG (the switch set RUN) or ASP (the switch set PROG) for the Mode. Press 「Start」 button for programming. (JTAG is like 「Pseudo programming」 . After reboot the power, the board will back to the initial state. ASP is opposite to JTAG, after reboot the board, it will not recover to the before programming) .

