DEPARTMENT OF ELECTRONICS AND ELECTRICAL COMMUNICATION ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

Date: **20 April 2018**, ~~FN~~/AN, Time: 3 Hrs., Full Marks: **100**, No. of Students: **704** (Non-ECE branches); End Spring Semester-2018, Sub. No.: **EC21101**, Sub. Name: **Basic Electronics**

Instructions

- **All waveform sketches / diagrams must be neatly drawn and clearly labeled.** Answers must be brief and to the point.
- The final answers (numerical values with unit) should be **underlined** or enclosed within box with unit.
- **For every Question No., start your answer from a new page.**
- **Avoid writing answers of the various parts of a single question at different locations in your answer-script.**
- For any value related to any device parameter or circuit parameter, which you may find not given with a problem, assume suitable value for such parameter.
- **No Queries will be entertained. Candidate may make necessary assumptions, if so required.**

Question 1 (1x 10 = 10 marks)

(i) Bipolar Junction Transistor name suggest
(a) It has two junctions
(b) Both electrons and holes constitute the current
(c) only electrons constitute the current
(d) none of these

(ii) A BJT is biased in forward active mode where the base current I_B is 2.8 μA, and the emitter current is 325 μA. The β and the collector current I_c are
(a) 116, 322 μA
(b) 115, 325 μA
(c) 115, 322 μA
(d) 116, 322 μA

(iii) The PMOS refers to
(a) p-type substrate and n-channel
(b) n-type substrate and p-channel
(c) p-type substrate and p-channel
(d) n-type substrate and n-channel

(iv) Threshold gate voltage of NMOS in enhancement mode is
(a) positive
(b) negative
(c) zero
(d) depends on drain voltage

(v) MOSFET is
(a) current controlled device
(b) voltage controlled device
(c) both current and voltage controlled device
(d) none of these

(vi) A MOSFET has
(a) three terminals
(b) four terminals
(c) two terminals
(d) five terminals

(vii) Which is the doping order of Emitter, Base and Collector in a BJT?
(a) moderately, lightly and heavily
(b) heavily, moderately and lightly
(c) lightly, heavily and moderately
(d) heavily, lightly and moderately

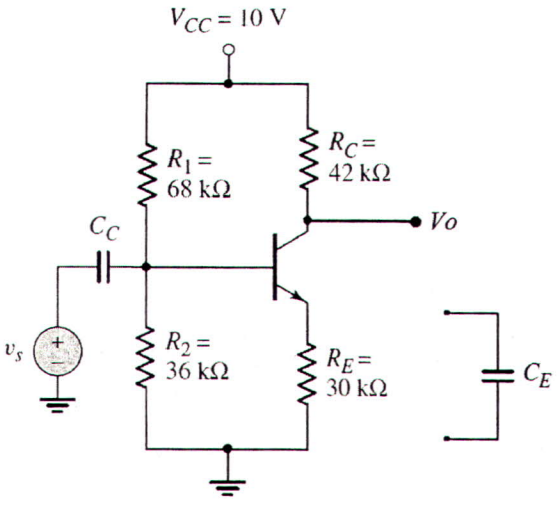
(viii) An op-amp has
(a) high CMRR
(b) infinite open-loop gain
(c) large bandwidth
(d) all of these

(ix) The closed loop gain of a non-inverting operational amplifier
(a) decreases with increase in finite open loop op-amp gain
(b) is never less than unity
(c) has the inverting input terminal at virtual ground
(d) all of these

(x) Which is the correct statement? (ABD: Avalanche Breakdown; ZBD: Zener Breakdown)
(a) $V_{ABD} < V_{ZBD}$
(b) $V_{ABD} > V_{ZBD}$
(c) $V_{ABD} = V_{ZBD}$
(d) $V_{ABD} \leq V_{ZBD}$

Question 2.

Consider the circuit (shown on the right side) of a CE amplifier with voltage divider biasing. Consider the coupling and emitter capacitors to be ideal working as short circuits for AC signals. The transistor at work is silicon based with $V_{BE}(on) = 0.7V$ and $V_{CE}(sat)=0.2V$, and the emitter capacitor is not connected to the circuit yet. Consider the β of the transistor as 50.



(a) If bias stability is assumed, find the error committed by this assumption as a percentage of the calculated DC output voltage. **(2+2+3+1=8 marks)**

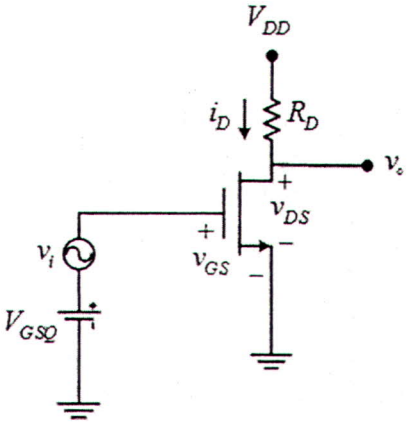
(b) Draw the hybrid-π transistor model based small-signal equivalent current amplifier circuit with proper labeling assuming infinite early voltage and calculate the transconductance of the circuit. **(2+2+2=6 marks)**

(c) If the resistance offered to the AC emitter current amplified by the resistance reflection rule needs to be at least 20 times larger than the diffusion resistance (r_π), find the maximum AC voltage gain that can be achieved for the correct hybrid-π circuit from the part (b) using the emitter capacitor without decreasing the resistance offered to the DC emitter current. **(2+4=6 marks).**

Question 3

(a). An NMOS transistor has parameters $V_{TN} = 0.8\,V, k_n' = 80\ \mu A/V^2$, and $\lambda = 0$. (i) Determine the drain current I_D for a width-to-length ratio $(W/L) = 3.125$ and $g_m = 0.5\,mA/V$ when biased in the saturation region. (ii) Calculate the required value of V_{GS}. **(2+2=4 marks)**

(b). An n-channel MOSFET is biased in the saturation region at a constant V_{GS}. The drain current is $I_D = 0.20\,mA$ at $V_{DS} = 2\,V$ and $I_D = 0.22\,mA$ at $V_{DS} = 4\,V$. Determine the value of λ and r_o. **(3+2 =5 marks).**

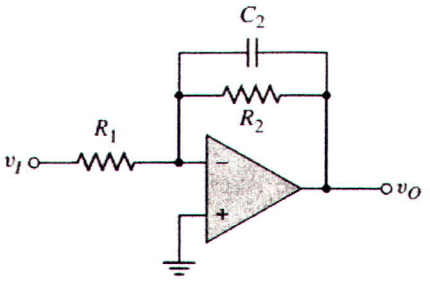


(c). For the circuit shown in the figure, the transistor parameters are: $V_{TN} = +0.8\,V, \lambda = 0015\,V^{-1}$, and $k_n' = 60\mu A/V^2$. Let $V_{DD} = 10\,V$, (i) Determine the transistor width-to-length ratio (W/L) and the resistance R_D such that $I_{DQ} = 0.5\,mA, V_{GS} = 2\,V$ and $V_{DSQ} = 6\,V$. (ii) Calculate g_m and r_o. (iii) What is the small-signal voltage gain $A_v = v_o / v_i$?

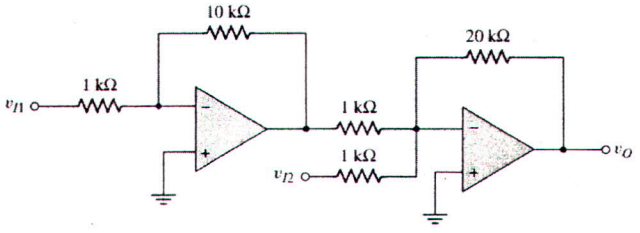
(4+4+3=11 marks)

Question 4

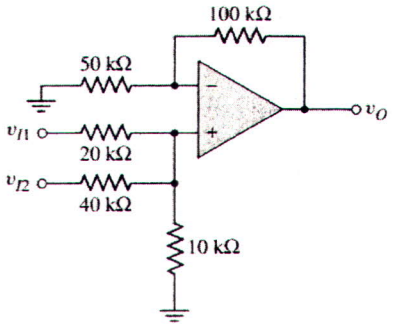
(a) The circuit shown in figure (right side) represents which type of filter? Obtain the gain expression. What is the gain at dc (i.e. ω=0)?. At what frequency is the magnitude of the voltage gain a factor of $\sqrt{2}$ less than that of dc value? **(1+4+1+2=8 marks)**



(b) Consider the circuit shown in figure shown in right. Derive the expression for the output voltage v_o in terms of v_{I1} and v_{I2}. Determine the v_o for v_{I1}=5mV and v_{I2} = (−25−50sinωt) mV. **(5+3=8 marks)**



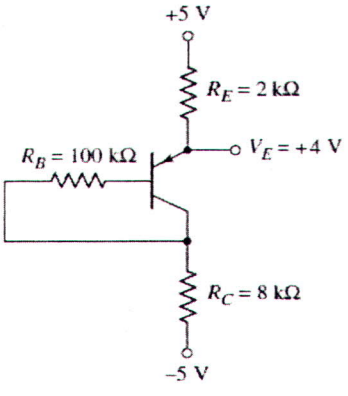
(c) Consider a non-inverting ideal op-amp. Derive the expression of v_o as a function of v_{I1} and v_{I2}. Find v_o for v_{I1}=0.2V and v_{I2}=0.3V. **(5+2 =7 marks)**



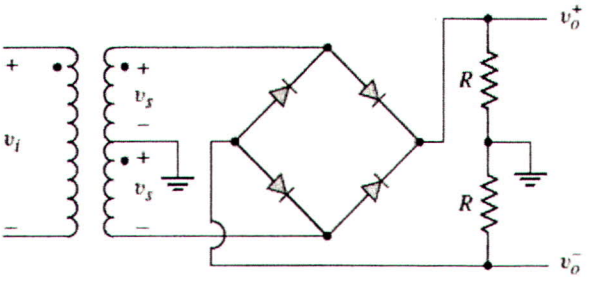
(d) Obtain the closed-loop gain for a non-inverting operational amplifier if the open-loop gain (or open-loop differential gain) is finite and is given by A_{od}. If the R_1 and R_2 (feedback resistor) have the values of 10 kΩ and 120 kΩ, find the closed-loop gain for (i) A_{od} = 1000 and (ii) $A_{od}=10^5$. **(5+2 =7 marks)**

Question 5

(a) For the circuit given in the adjacent figure, using the given DC voltage conditions, determine the value of β, and the collector current. Find the change in collector current if R_B is changed to 150kΩ. **(6+4 =10 marks)**



(b) The circuit in figure (right side) is a complementary output rectifier. If $v_s = 26\sin\left[2\pi(60)t\right]$ volts, sketch the output waveforms v_o^+ and v_o^- versus time, assuming V_γ = 0.6 V for each diode. **(5 marks)**



Question 6

Discuss the physics behind the origin of finite slope in the output characteristics of BJT (in active mode) and MOSFET (in saturation mode). Use suitable diagrams and mathematics to justify your answer. Give a brief explanation. **(2+2+1=5 marks)**

End of Question Paper