Course: Basic Electronics (EC21101)

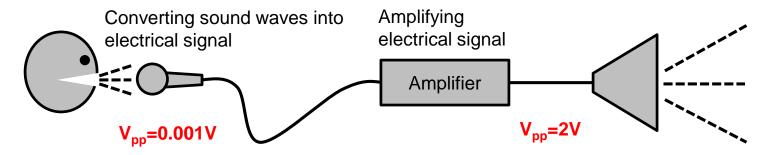
Course Instructor: Prof. Kapil Debnath

# **Lecture 5: Bipolar Junction Transistor**

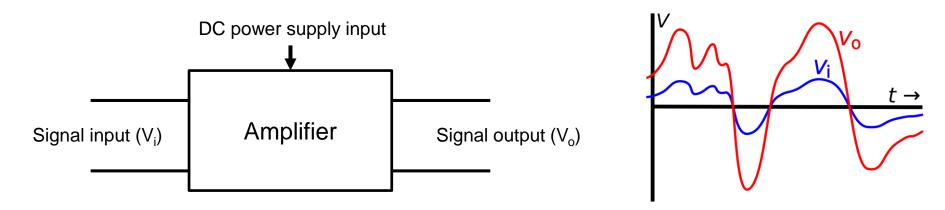
- Contact Email: k.debnath@ece.iitkgp.ac.in
- website: <a href="https://kdebnath8.wixsite.com/nanophotonics">https://kdebnath8.wixsite.com/nanophotonics</a>
- Office: R314, ECE Dept, Discussion time: Friday 5pm

# **Amplifier**

Amplifier is one of the most important components in any electronic system. Following is an example of a microphone-speaker system. The voltage that is generated at the output of a microphone usually is of the order of few mVs, whereas for the speaker to work the voltage level required at the input terminal of the speaker is of the order of few Vs. Therefore we need to amplify the voltage level from mVs range to Vs range.



Amplifiers can increase the power of a signal (a time-varying voltage or current signal). Unlike any component that we discussed so far (except transformer), amplifier is a two-port electronic circuit that uses electric power from a power supply to increase the amplitude of a signal applied to its input terminals, producing a proportionally greater amplitude signal at its output.

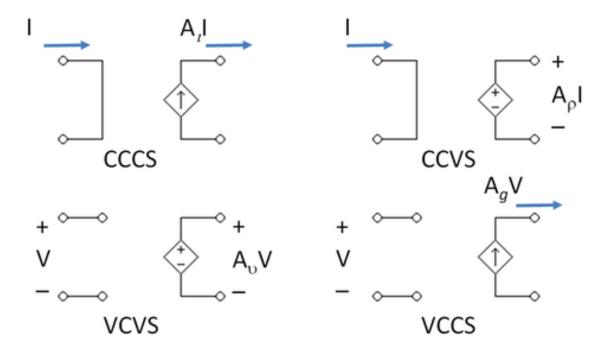


## Dependent source

In order to understand amplifier fully we need to have some basic knowledge of dependent voltage and current sources.

A dependent source is a voltage source or a current source whose value depends on a voltage or current elsewhere in the network. There are four types of dependent sources:

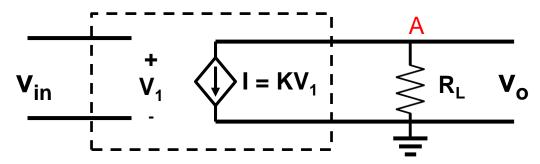
- Voltage-controlled voltage source (VCVS)
- 2. Voltage-controlled current source (VCCS)
- 3. Current-controlled current source (CCCS)
- 4. Current-controlled voltage source (CCVS)



The current and voltage from these sources remains unaffected by the load condition

## Dependent source

Let us consider a Voltage-controlled current source (VCCS). The voltage that controls the current source is connected to the input signal and the dependent current source is feeding the load resistance. The output voltage is measured across the load resistance.

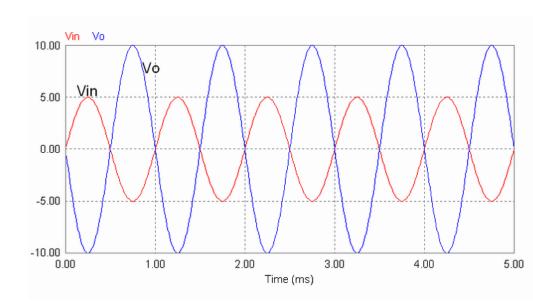


If we apply KCL at point A we get:

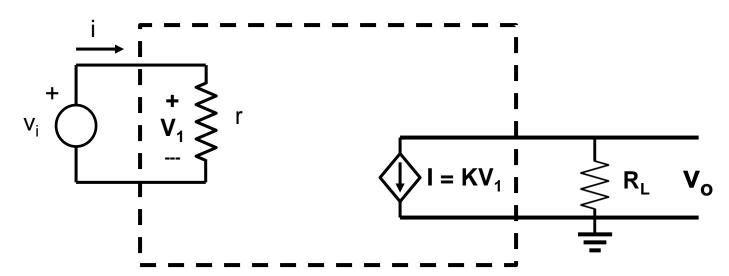
$$\frac{V_o}{R_L} + KV_1 = 0$$

$$\Rightarrow V_o = -R_L K V_{in}$$

If we have  $R_L$  and K such that  $R_L K > 1$ , we have an amplification of the input signal. Therefore we can argue that we can achieve amplification with a dependent source.



# Dependent source: example



#### **Input terminal**

$$v_i = 10 \ mV$$

$$i_i = 10 \, \mu A$$

Power delivered to the system:

$$P_i = 10 \ mV \times 10 \ \mu A = 0.10 \mu W$$

#### **Output terminal**

If 
$$R_L=10K\Omega$$
 and  $K=100mA/V$  
$$V_o=-100\frac{mA}{V}\times 10~mV\times 10~K\Omega=10~V$$
 
$$V_o=10~V$$

Power delivered to the load:

$$P_i = 10 V \times 1 mA = 10 mW$$

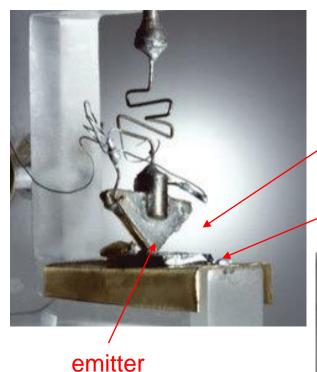
## Component for dependent source (Amplifier)

The components that we discussed so far, i.e. resistor, capacitor, inductor, transformer, diode can not operate as a voltage dependent source. In a transformer although we can vary the secondary coil voltage by altering the turn ratio, the total power that is transferred from primary coil to the secondary one is fixed. In order to realize a voltage dependent source or an amplifier we need a new device, known as transistor. There are two types of transistors available:

- 1. Bipolar Junction Transistor (BJT)
- 2. Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

In this lecture and what follows we will consider BJT and its operation.

#### First BJT

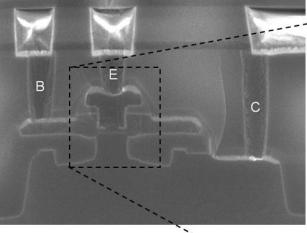


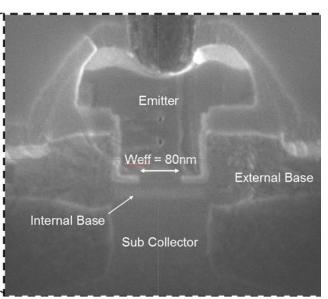
Collector

invented in December 1947 By John Bardeen and Walter Brattain and William Shockley Nobel prize in 1956

base

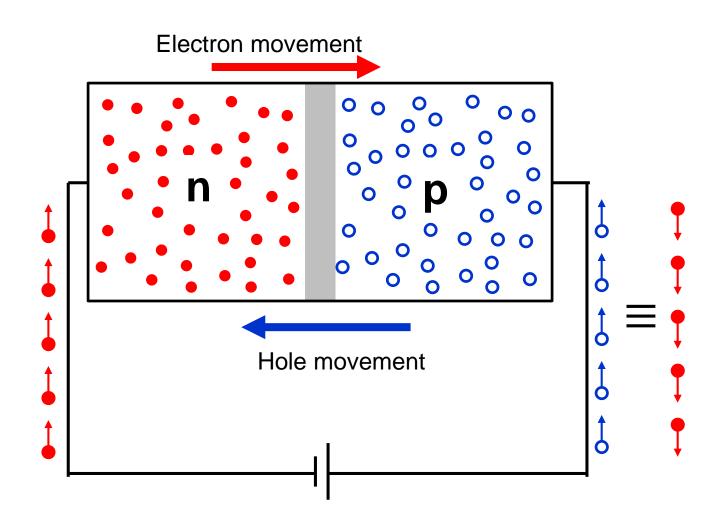
Today's BJT



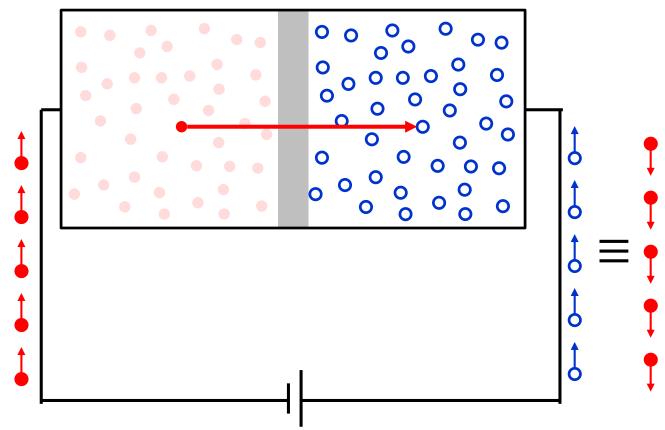


**IMEC** 

#### Carrier flow in a forward bias pn junction:



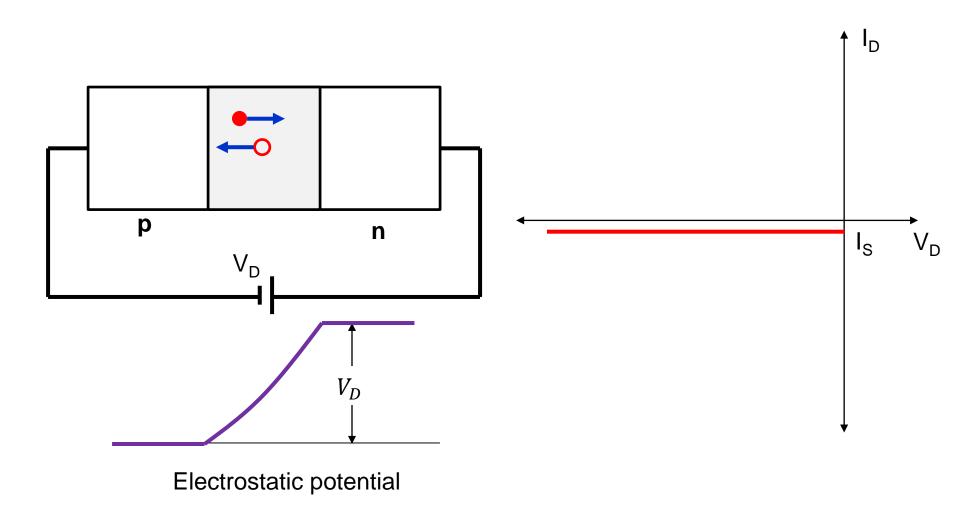
#### Carrier flow in a forward bias pn junction:



- Because of the forward biasing of the junction the electrons will diffuse into the p-side.
- After travelling for a while electrons will eventually recombine with holes.
- Holes on p-side and electrons on n-side will be replenished by the voltage source.

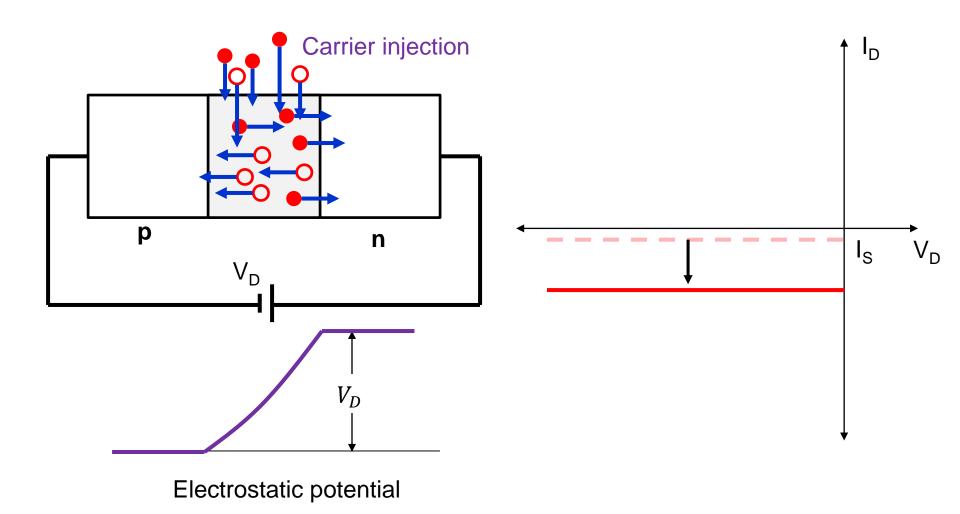
#### **Carrier injection:**

Diode under reverse bias, very few free carriers to contribute to the current flow



#### **Carrier injection:**

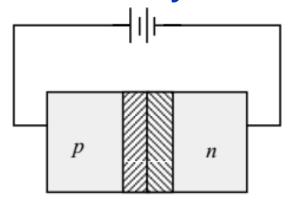
When electrons and hole are somehow injected into the depletion region, there is an increase in the diode current



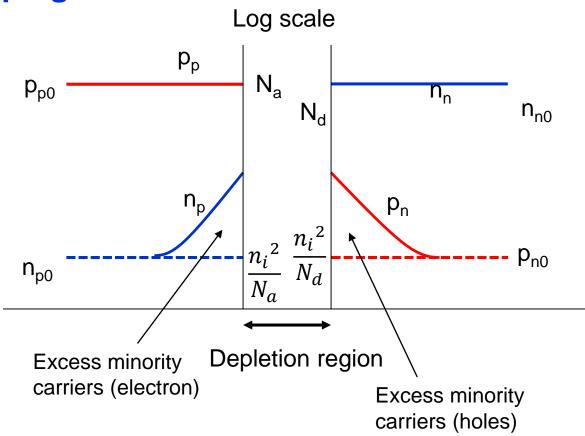
#### Effect of asymmetric doping:

When a pn junction is formed by joining two equally doped p and n-type semiconductor materials, under forward bias both electrons and holes contribute equally to the current flow through the junction. However when one side is doped heavily in comparison to other, for example a pn<sup>++</sup> junction, where the p side is doped with 10<sup>15</sup>/cm<sup>3</sup> boron atoms and the n side is doped with 10<sup>18</sup>/cm<sup>3</sup> phosphorous atoms, the current through the junction will be almost entirely due to movement of electrons.

#### Effect of asymmetric doping:

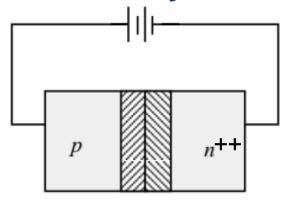


Similar doping on p and n side

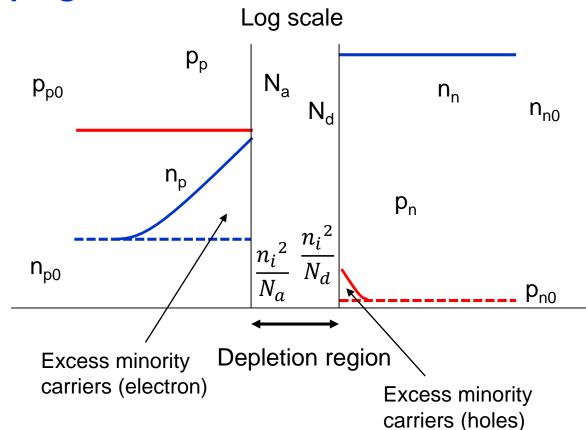


Current is due to both electrons and holes

#### **Effect of asymmetric doping:**

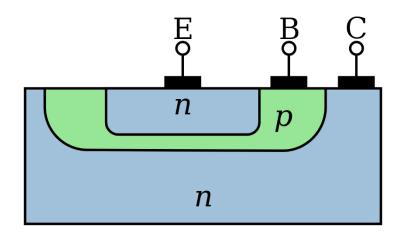


n side heavily doped

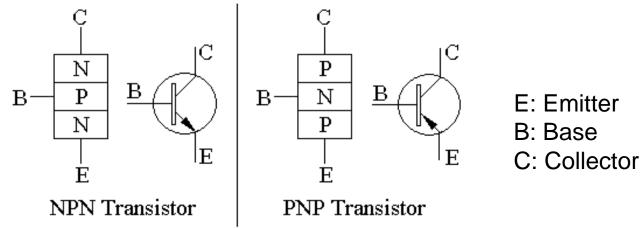


Current is primarily due to <u>electrons</u>

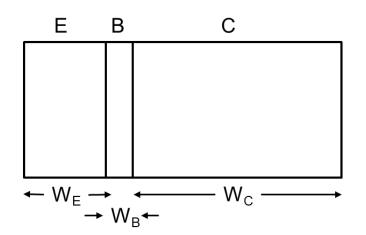
Unlike a diode, BJT is a three terminal device and has three semiconductor sections. A simplified schematic cross-sectional diagram of a BJT is shown below.



There are two variations of BJTs: pnp type and npn type. Schematic and circuit symbol of both types of BJT is shown below.



The relative size and the level of doping in individual parts of the BJT plays an important role in the operation of the device. The doping concentration in different parts of a BJT is substantially different. For example, the impurity concentration in the emitter, base and collector may be of the order of 10<sup>19</sup>, 10<sup>16</sup> and 10<sup>15</sup> /cm<sup>3</sup> respectively. Also *the distance* between the two junctions (base-collector and base-emitter) are kept very low by keeping the base region very narrow. Whereas the collector region is kept largest.



$$W_B \ll W_E \ll W_C$$
  
 $N_E \ll N_B, N_C$ 

$$N_E \ll N_B, N_C$$

#### **Understanding the BJT symbol**

In both the symbols, an arrow is placed between the base and the emitter and the arrow points towards the direction of current flow when the junction is in forward bias. For a npn BJT, the arrow points from base to emitter and for a pnp BJT, the arrow points from emitter to base

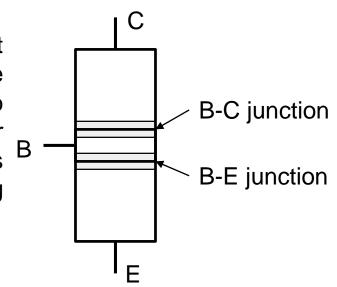






**PNP Transistor** 

Recall, in diode we only had one pn junction and it operates when a positive bias is applied to the p-side with respect to the n-side. However, here we have two junctions, one between the base and emitter and another between base and collector. Since, the device now has two junctions, there can be four possible biasing conditions:



- 1. Both junctions are forward bias
- 2. Both junctions are reversed bias
- 3. B-C in forward bias and B-E in reverse bias
- 4. B-E in forward bias and B-C in reverse bias

Fortunately, one out of these four combinations actually useful for achieving amplification and that is:

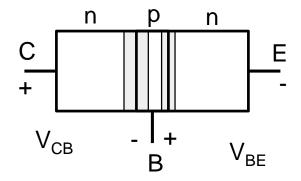
#### Base-Emitter in forward bias and Base-Collector in reverse bias

This biasing configuration is called forward-active operating mode, or simply active region of operation.

In the active region of operation,

For a npn BJT, the base should be more positively biased than the emitter and the collector should be more positively biased than the base.

For a pnp BJT, the emitter should be more positively biased than the base and the base should be more positively biased than the collector.



C P N P E V BE

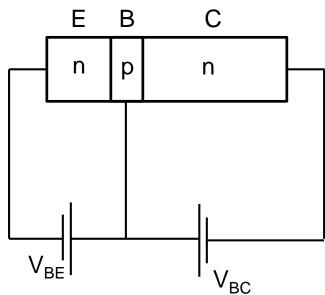
V<sub>BE</sub> is positive

V<sub>CB</sub> is negative

V<sub>BE</sub> is negative

V<sub>CB</sub> is positive





B-C in forward bias and B-E in reverse bias

Reverse-active

Both junctions are forward bias

Saturation

Saturation and cut-off regions are used for logic operations

- Forward active region is used for amplification
- Reverse active regions are generally avoided

Both junctions are reverse bias

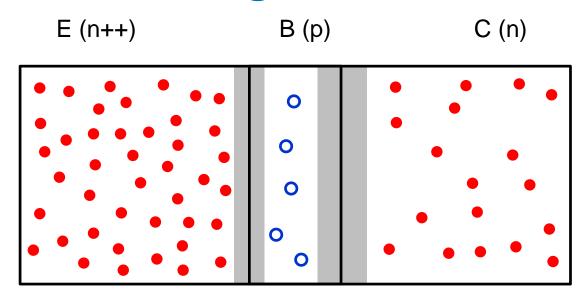
Cut-off

B-E in forward bias and B-C in reverse bias

forward-active

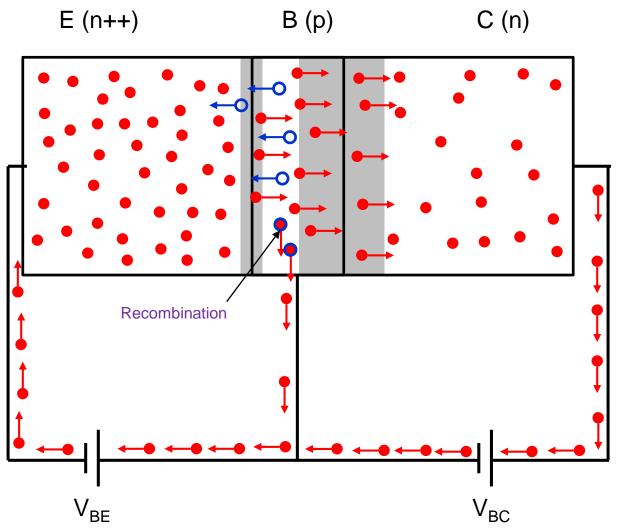
What should be map for pnp transistor?

## **Charge Carrier flow: Equilibrium**



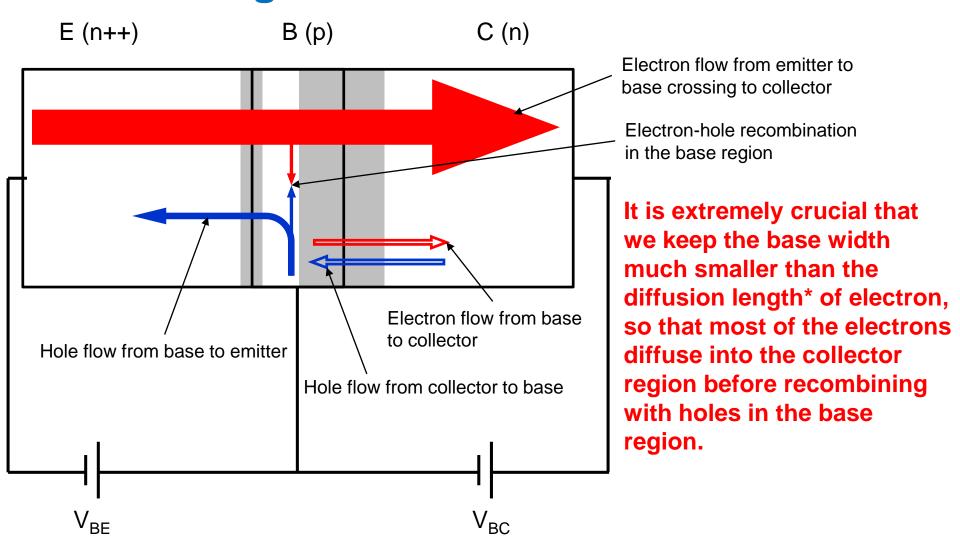
Under equilibrium condition due to potential barrier at each junction no carrier flows from one part of the device to another.

## **Charge Carrier flow: Active Bias**



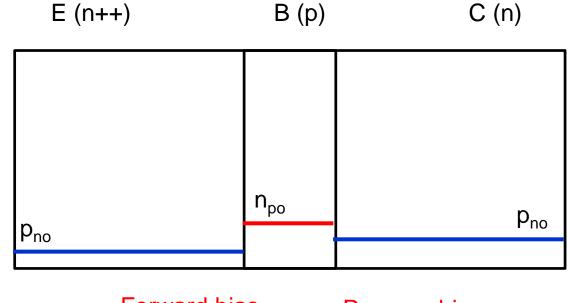
- As the reverse bias is applied to base-collector junction very few carriers cross this junction from collector to base
- As the forward bias is applied to base-emitter junction, mainly electrons will start flowing from emitter to base region (because of asymmetric doping).
- Remember the base region is very small
- Once the electrons from emitter enters the base region, they either recombine with the holes in the base region, thus contributes to the base current.
- Or they cross the base region and enters into the base-collector depletion region. Once the electrons enters the depletion region, due to the electric field electrons get swept away into the collector region, thus contributing to the collector current.

## **Charge Carrier flow: Active Bias**



\*diffusion length: average length an electron (or hole) travels before recombining with a hole (or electron)

## Minority carrier concentration

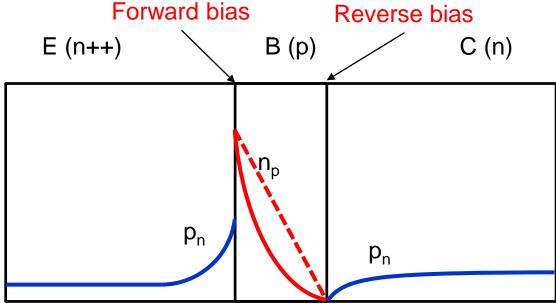


#### **Equilibrium**

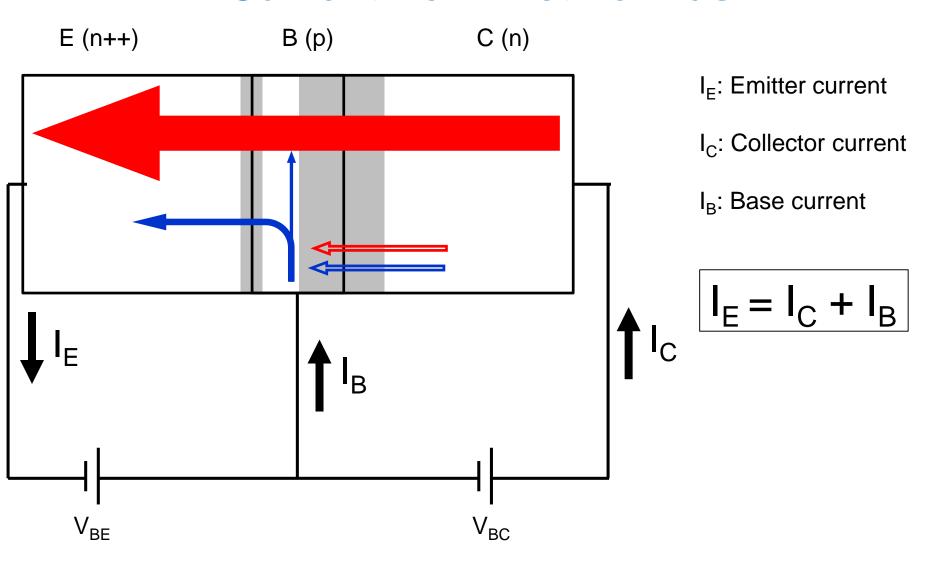


No recombination ----

With recombination -



#### **Current flow: Active Bias**



#### **Observations:**

- a) Since the B-E junction is forward biased, the current through the junction is an exponential function of the B-E voltage (recall current through a forward bias pn diode). So we can expect that both  $I_E$  and  $I_B$  will increase exponentially with increase in the junction voltage  $V_{BE}$ .
- b) When the B-E junction is open circuited, and B-C junction is reversed bias, only a small amount of current flows between collector and base terminal due to reverse saturation current.
- c) When the B-E junction is forward biased and B-C junction is reversed bias, the emitter current has two components (current due to electron from emitter to base and current due to holes from base to emitter). If we consider no recombination is taking place in the base region, all the electrons diffusing from the emitter region to base region will be injected into the collector region. So the collector current becomes almost equal to the emitter current.
- d) The base current also consists of two components:
  - a) Holes diffusing from the base region to emitter region. Due to asymmetric doping (emitter heavily doped and base lightly doped) this current is much smaller than the current due to electron diffusing from emitter region to the base region.
  - b) Holes supplied to the base region to recombine with the electrons diffusing from the emitter region. Since the base width is very small, most of the electrons from emitter migrates to the collector region before recombining with the holes in the base region. So this current component is also very small.

The collector current consists of two components:

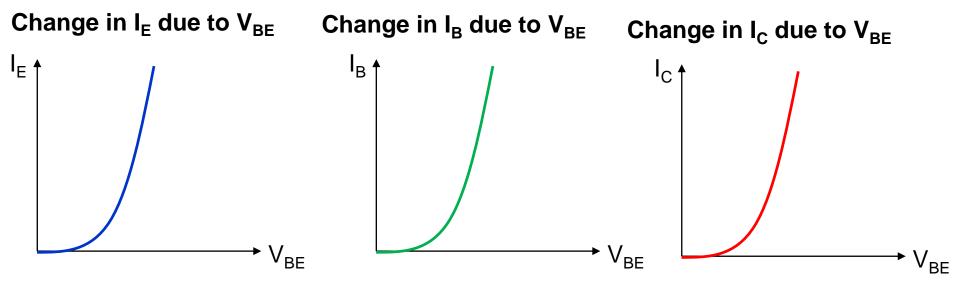
- a) Current due to electrons migrating from emitter via base to collector region
- b) Reverse saturation current due to reverse biased base-collector junction

Since the reverse saturation current is typically very small (nA or less), the collector current will be mainly due to the electrons coming from the emitter.

So we can write

$$I_C \propto I_E$$

Since I<sub>E</sub> varies exponentially with the base-emitter voltage, we can expect the collector current should also vary in the same fashion.

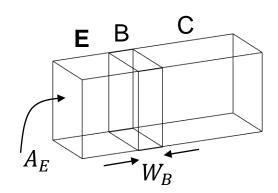


- ➤ Since the emitter current is an exponential function of the base-emitter junction, the collector current also becomes an exponential function of the same junction. If we ignore the small reverse saturation current due to the base-collector junction, the current at the collector terminal only depends on the base-emitter junction voltage and not on the base-collector junction voltage. Therefore, this device appears to be working as a constant current source and the current depends on a voltage somewhere else in the system.
- ▶ I<sub>C</sub> is expressed in terms of V<sub>BE</sub> as:

$$I_C = I_S \left( e^{\frac{V_{BE}}{\eta V_T}} - 1 \right)$$

Where the proportionality constant  $I_S$  is expressed as:

$$I_S = \frac{eA_E D_n n_i^2}{W_B N_B}$$



Where

e is the electron charge,  $A_E$  is the cross-sectional area of the emitter region,  $D_n$  is the diffusion constant of electron,  $n_i$  is the intrinsic carrier concentration,  $W_B$  is the width of the base region and  $N_B$  is the doping level in the base region.

▶ I<sub>C</sub> can be expressed in terms of I<sub>F</sub> as:

$$I_C = \alpha I_E$$

- The collector current is slightly smaller than the emitter current. For a good transistor,  $\alpha$  is very close to unity. This parameter  $\alpha$  is called <u>common-base current gain</u>.
- ➤ Since the base current I<sub>B</sub> also varies exponentially with the base-emitter voltage, we can expect a linear relationship between I<sub>C</sub> and I<sub>B</sub>.

$$I_C = \beta I_B$$

 $\beta$  is known as **common-emitter current gain**.

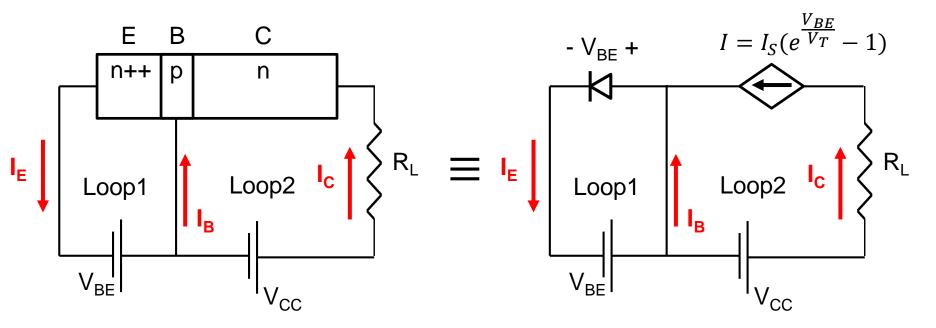
- ightharpoonup Typical values of  $\alpha$  is  $0.98 \le \alpha \le 0.99$
- $\triangleright$  Typical values of β is  $50 \le \beta \le 400$
- > The relationship between different current components are:

$$I_E = I_C + I_B$$

$$\Rightarrow \frac{I_C}{\alpha} = I_C + \frac{I_C}{\beta}$$

$$\Rightarrow \beta = \frac{\alpha}{1-\alpha}$$

## BJT as voltage dependent current source

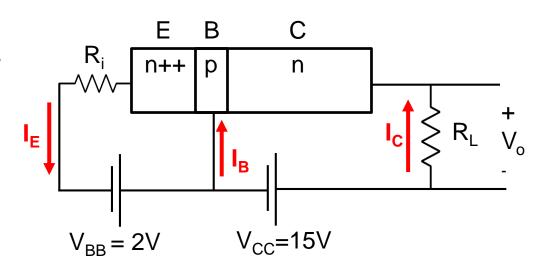


- ➤ The base-emitter junction is simply a forward biased diode. So we can replace this with a diode in loop1.
- ➤ In the collector side, the current I<sub>C</sub> does not depend on the voltage V<sub>BC</sub>. Rather it depends on the voltage across the base-emitter junction V<sub>BE</sub>. We can replace this section with a dependent current source.
- ➤ Interesting to note here that the current through the load resistance R<sub>L</sub> is fixed and does not depend to the voltage V<sub>CC</sub> rather depends on V<sub>BE</sub>. As we will see later this is the basis of amplification in BJTs.

## BJT as a voltage amplifier

Lets consider a silicon BJT in the above circuit. This biasing condition is called common base configuration, since the base is common to both the loops.

Ri=1K $\Omega$  and R<sub>L</sub>=5K $\Omega$ 



- ➤ The base-emitter junction is in forward bias with V<sub>BE</sub>=0.7V (assuming piecewise linear model).
- Current I<sub>E</sub> can be found by using KVL in the input loop as:

$$V_{BB} - V_{BE} - I_E R_i = 0$$

From this equation we get I<sub>F</sub> as:

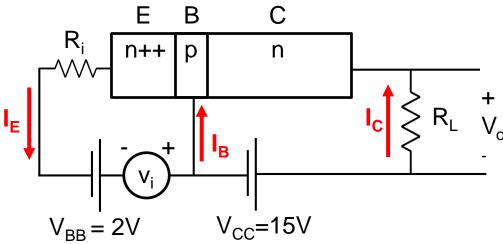
$$I_E = 1.3 mA$$

If we take  $\alpha = 0.98$ , then  $I_C = 0.98 \times 13 mA = 1.274 mA$ Hence

$$V_o = -R_L I_C = 5K\Omega \times 1.274 mA = 6.37V$$

## BJT as a voltage amplifier

Lets add a sinusoidal voltage source to the input loop with  $v_i = 0.2\sin(\omega t)$ .



- When  $v_i = 0.2V$ , the base-emitter junction is still in forward bias with  $V_{BE} = 0.7V$  (since we assumed piecewise linear model).
- ➤ In this case, again current I<sub>F</sub> can be found by using KVL in the input loop as:

$$V_{BB} + v_{i,max} - V_{BE} - I_E R_i = 0$$

From this equation we get  $I_E$  as:

$$I_E = 1.5mA$$

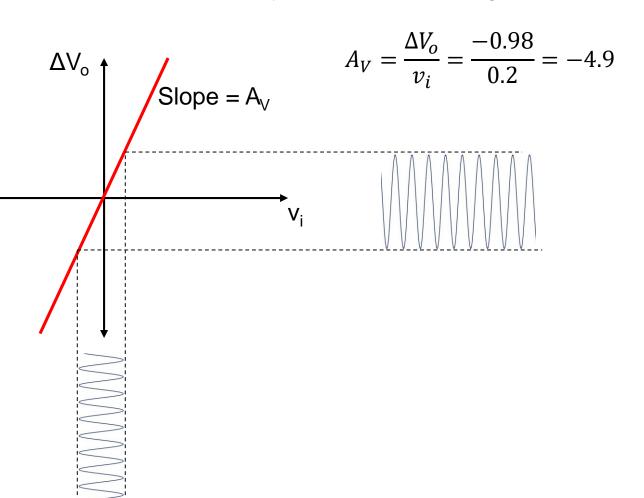
If we take  $\alpha = 0.98$ , then  $I_C = 0.98 \times 1.5 mA = 1.47 mA$ 

Hence

$$V_0 = -R_L I_C = -5K\Omega \times 1.47mA = -7.35V$$

## BJT as a voltage amplifier

- For a input voltage of 0.2V, the output voltage changed from 6.37V to 7.35V, i.e. 0.98V.
- Therefore, we can say that the input voltage has been amplified by



#### Summary: BJT current-voltage relationships in active region

$$I_C = \beta I_B$$

$$I_E = I_C + I_B$$

 $\beta \equiv$  common-emitter current gain.

$$I_C = \alpha I_E$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

 $\alpha \equiv$  common-base current gain.

 $\alpha$  is always very close but less than 1

#### For npn transistor

#### For pnp transistor

$$I_C = I_S e^{V_{BE}/V_T}$$

$$I_C = I_S e^{V_{EB}/V_T}$$

$$I_E = \frac{I_C}{\alpha} = \frac{I_S}{\alpha} e^{V_{BE}/V_T}$$

$$I_E = \frac{I_C}{\alpha} = \frac{I_S}{\alpha} e^{V_{EB}/V_T}$$

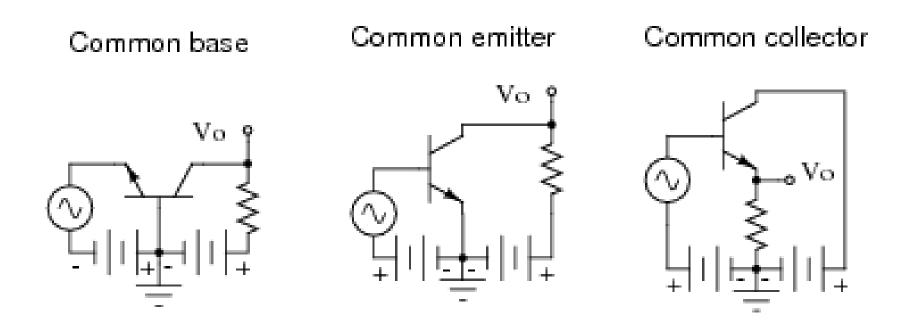
$$I_B = \frac{I_C}{\beta} = \frac{I_S}{\beta} e^{V_{BE}/V_T}$$

$$I_B = \frac{I_B}{\beta} = \frac{I_S}{\beta} e^{V_{EB}/V_T}$$

## **BJT Biasing**

An amplifier is a two port device, i.e. it requires four terminals for operation: input port consist of two terminals and output port consist of two terminals. BJT, however, has 3 terminals, i.e. emitter, base, collector. So, when a BJT is used as an amplifier, one of the three terminals becomes common to both input and output port. Hence we can have three different biasing configurations:

- a) Common-base (CB) configuration: base is common to both input output port
- b) Common-emitter (CE) configuration: emitter is common to both input output port
- c) Common-collector (CC) configuration: base is common to both input output port



## Common-base (CB) configuration

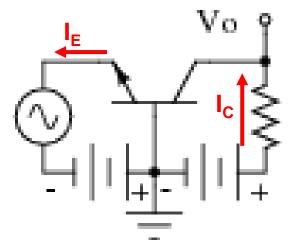
In a CB configuration, the base terminal is common to both input port and the output port.

The examples discussed in the previous slides consider a CB biasing configuration.

In CB configuration, although we saw that we can get voltage amplification, we can not get any current amplification, since, the output current  $I_C$  is always less than  $I_E$  and the relationship between them is:

$$I_C = \alpha I_E$$

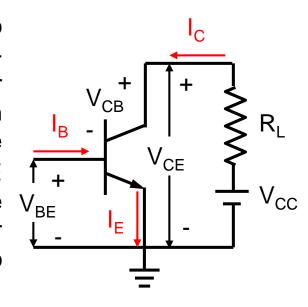
This is why  $\alpha$  is called common-base current gain.



Most commonly used biasing configuration for amplification is the common emitter configuration. In CE configuration, we can achieve both voltage as well as current gain. So, in the following slides we will mainly discuss CE configuration.

## Common-emitter (CE) configuration

In a CE configuration, the emitter terminal is common to both the input port as well as the output port. For forward-active region of operation, we require the base-emitter junction to be forward biased, i.e.  $V_{BE}$  should be greater than the cut-in voltage  $(V_{\gamma})$  of the base-emitter diode and the base collector junction to be reversed bias. In CE configuration, even though we have direct access to the base-emitter junction (as shown in figure), the base-collector junction is biased indirectly by applying a positive voltage to collector terminal with respect to the emitter terminal.



From the figure, we can write:

$$V_{CE}-V_{CB}-V_{BE}=0$$
 Hence,  $V_{CB}=V_{CE}-V_{BE}$ 

For a npn transistor, as shown in the figure, for active region of operation we need  $V_{BE}$  to be more than the cutin voltage (i.e. $V_{BE(ON)} > V_{\gamma}$ ) of the base-emitter diode (for Silicon  $V_{\gamma} \approx 0.6V - 0.7V$ ) and the base-collector voltage  $V_{CB}$  to be zero or negative. Which means,  $V_{CE} \geq V_{BE(ON)}$ .

## **Ideal Characteristics**

For the CE configuration,  $V_{BE}$  and  $I_{B}$  are the input variables and  $V_{CE}$  and  $I_{C}$  are the output variables.

As we discussed earlier,  $I_B$  varies exponentially with  $V_{BE}$ .

$$I_B = \frac{I_B}{\beta} = \frac{I_S}{\beta} e^{V_{BE}/V_T}$$

If  $V_{BE} > V_{\gamma}$  and  $V_{CE} \ge V_{BE}$ , the transistor goes into active region of operation and for an ideal transistor,  $I_{C}$  remains independent of  $V_{CE}$  and only depends on  $I_{B}$ .

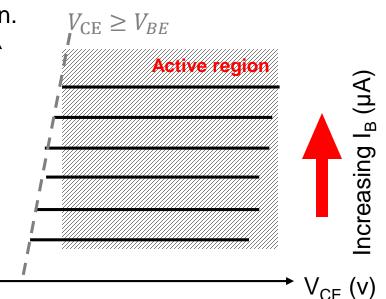
$$I_C = \beta I_B$$

This is why  $\beta$  is called common-emitter current gain.

 $I_{C}$  (mA)

## **Active region:**

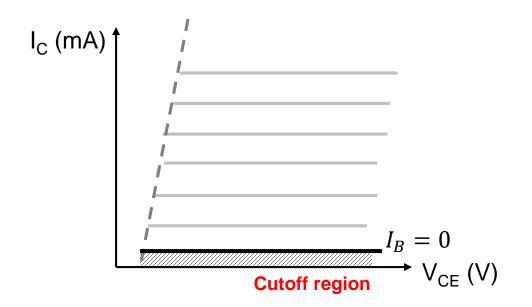
The figure shows the output current-voltage relationship. For an ideal transistor,  $I_C$  only depends on  $I_B$  and not on  $V_{CE}$ .



## **Cutoff region**:

When  $V_{BE} < V_{\gamma}$ ,  $I_B = 0$ , hence no current flows (except a very small amount of reverse saturation current due to reverse biased base-collector) in the output loop

$$I_C = \beta I_B \approx 0$$



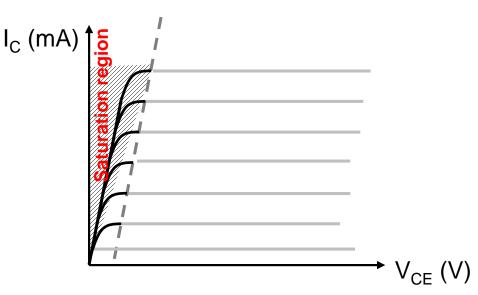
## Saturation region:

When both the base-emitter and base-collector junctions are forward biased, i.e.  $V_{BE} > V_{\gamma}$  and  $V_{CB} < V_{\gamma}$ , the collector current  $I_{C}$  no longer remains independent of  $V_{CE}$  and starts to vary linearly with  $V_{CE}$ .

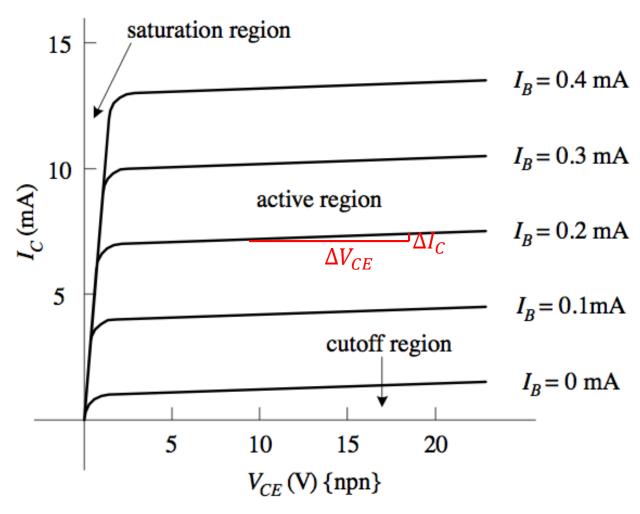
We have

$$V_{CE} = V_{CB} + V_{BE}$$

Since, for a forward bias junction the diode voltage is close to the cutin voltage ( $\sim$ 0.6V-0.7V),  $V_{CE}$  is also remains in few tenths of volts. For silicon BJTs  $V_{CE}\sim$ 0.2V. Hence saturation region is very close to zero voltage axis, where all the current rapidly reduces to zero. In this region the  $I_{C}$  is approximately given by  $V_{CC}/R_{C}$  and independent of base current. Under this situation, normal transistor action is lost and it acts like a small ohmic resistance.



Output characteristics of a real npn transistor in CE configuration

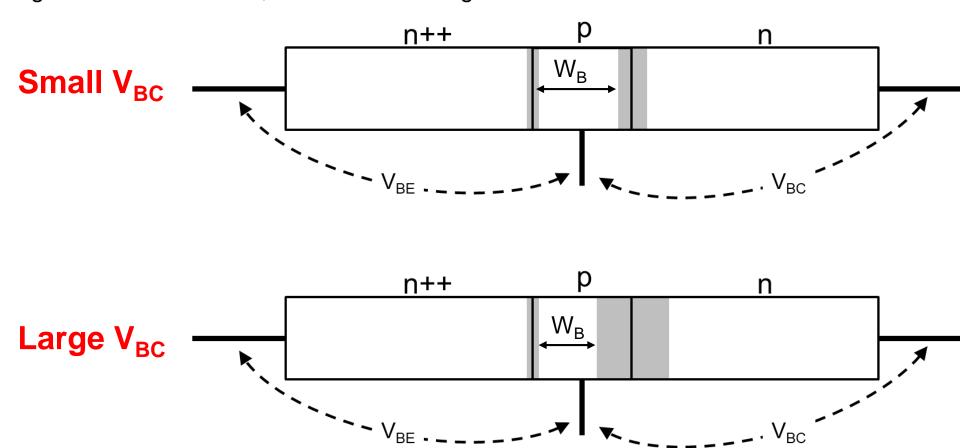


Notice nonzero slope in the active region

# **Early Effect: Base width modulation**

To understand the nonzero slope of the output curve in active region we have to revisit the operation of a BJT under forward-active region.

Since the base-emitter junction is forward biased, the depletion region is small, on the other hand the depletion region at base-collector junction is large, because of reverse bias. As the reverse bias voltage at base-collector junction increases, the depletion region further increases, as shown in the figure.

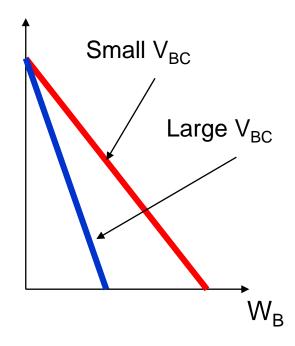


# **Early Effect: Base width modulation**

As the base-collector depletion region increases with large  $V_{BC}$  the effective base width reduces. This  $n_p$  phenomenon of modulation of base width by the collector voltage is known as *Early effect* (named after J. M. Early).

Decrease in  $W_B$  with increasing  $V_{BC}$  has three consequences:

- a) Since the effective base width reduced, there is less chance for recombination within the base region. Hence  $\alpha$  increases with increasing  $V_{BC}$ .
- b) The concentration gradient of minority carriers in the base region (for npn transistor it is electron) increases, as shown in figure.
- c) For a very large value of V<sub>BC</sub> the base width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is known as *punch* through.



# **Early Effect: Base width modulation**

Due to the early effect,  $I_C$  increases with  $V_{BC}$  in the active region. When the output curves are extrapolated to zero current, they meet at a point on the negative voltage axis, at  $V_{BC} = -V_A$ .  $V_A$  is called *Early voltage*. Typically ranges between 50 to 300V.

The linear dependence of  $I_C$  on  $V_{CE}$  in active region can be described by

$$I_C = I_S e^{V_{BE}/V_T} \left( 1 + \frac{V_{CE}}{V_A} \right)$$

Notice the term  $\left(1 + \frac{V_{CE}}{V_A}\right)$  represents the change in  $I_C$  due to Early effect.

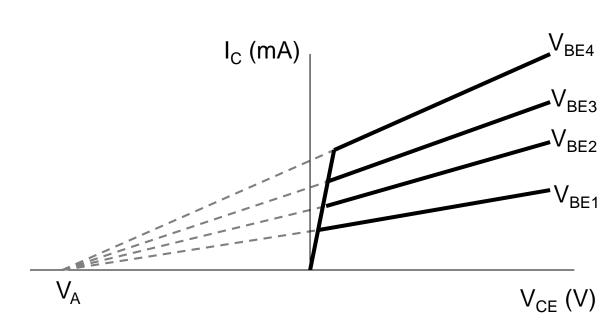
The nonzero slope of the output curves indicate that the output resistance  $r_o$  looking into the collector is finite and can be determined from:

$$\left. \frac{1}{r_o} = \frac{\partial I_C}{\partial V_{CE}} \right|_{V_{BE} = constant}$$

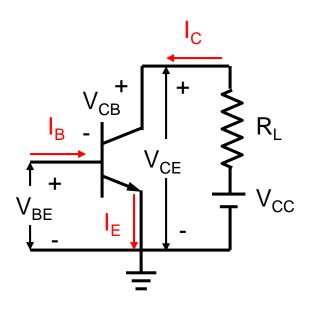
i.e.

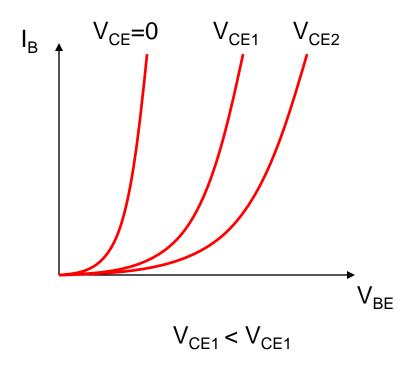
$$r_o \approx \frac{V_A}{I_C}$$

This output resistance plays a important role in amplifier design.



The input characteristic is between the base-emitter voltage  $V_{BE}$  and  $I_{B}$ . as shown in figure. When the emitter and collector terminals are shorted, i.e.  $V_{CE} = 0$ , the input characteristic is essentially that of a forward biased diode. As the  $V_{CE}$  increases, due to the Early effect, the base width reduces, causing the  $I_{B}$  to reduce for the same  $V_{BE}$ . As a result the input characteristic curve shifts towards higher value of  $V_{BE}$  as  $V_{CE}$  increase.





# DC analysis of BJT circuits

Two of the primary applications of BJTs are amplification and switching (logic gates). Both of these application require DC biasing of the transistors. DC analysis of a BJT circuit allows us to choose the appropriate values of currents and voltages (such as  $I_B$ ,  $V_{BE}$ ,  $I_C$  and  $V_{CE}$ ) in order to perform certain operation reliably.

For example, for amplification the overall circuit needs to be designed in such a way that the transistor remains in forward-active mode for the entire range of input signal. And also the output varies linearly with the input signal.

Whereas, for logic operations the transistor should switch between the saturation region and active region.

## **Common-emitter circuit**

Figure shows a simple biasing circuit for a CE configuration and its DC equivalent circuit.

In active mode of operation, the base-emitter diode needs to be forward biased, i.e.  $V_{BE} = V_{\gamma}$  (considering an ideal diode).

Hence the base current becomes:

$$I_B = \frac{V_{BB} - V_{\gamma}}{R_B}$$

In the collector terminal,

The collector current

$$I_C = \beta I_B$$

And

$$V_{CE} = V_{CC} - I_C R_C$$

These equations are valid when  $V_{BB} > V_{\gamma}$  and  $V_{CE} \geq V_{BE}$ 

## Power dissipation in the transistor

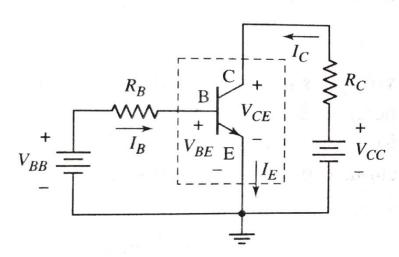
The total power dissipation in the transistor can be expressed as

$$P_T = I_B V_{\gamma} + I_C V_{CE}$$

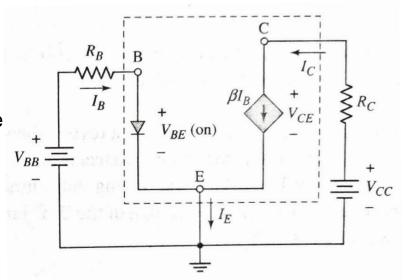
Usually  $I_B \ll I_C$  and  $V_{\gamma} \ll V_{CE}$ 

So

$$P_T \approx I_C V_{CE}$$



## DC equivalent circuit



# **Load line and Q-point**

From the previous example, it is obvious that the DC values of various current and voltages dictate the circuit behaviour to perform certain function, such as amplification. One of the simplest way to visualize the status of a transistor in a circuit is by using load line. Remember, similar analysis we have also done for diodes.

Consider the BJT in CE configuration. For the input loop (i.e. B-E portion of the circuit), we can write:

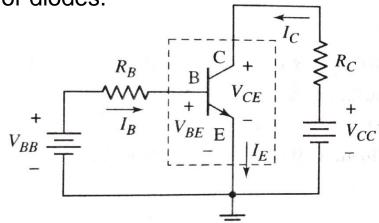
$$I_B = \frac{V_{BB}}{R_B} - \frac{V_{BE}}{R_B}$$

This is an equation of a straight line and if we superimpose this curve onto the input characteristic of the BJT, the intersection would give us the operating base current  $I_B$  and base-emitter voltage  $V_{BF}$ .

Similarly for the output loop, we can write

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C}$$

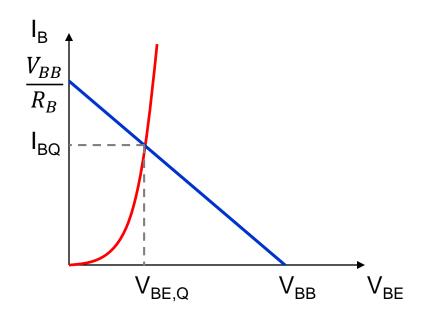
If we superimpose this curve onto the output characteristic of the BJT, the intersection would give us the operating collector current  $I_C$  and collector-emitter voltage  $V_{CE}$ .

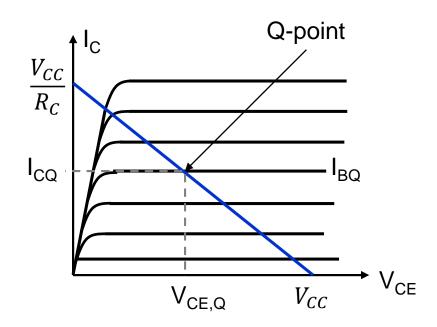


# **Load line and Q-point**

## Input variables

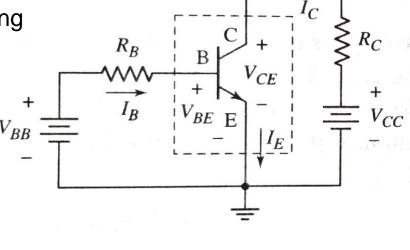
## **Output variables**

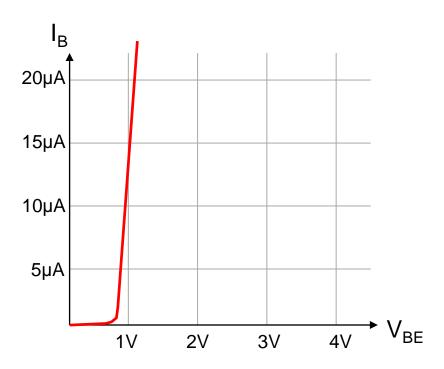


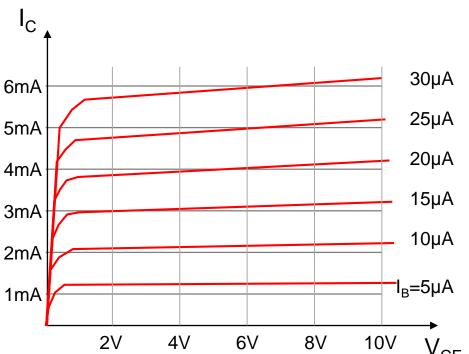


Q-point ( $I_{CQ}$  and  $V_{CE,Q}$ ) tells the region of operation of the transistor, i.e. whether the transistor is in active or saturation or cutoff region.

Consider the CE circuit with an npn transistor having the following input output characteristics.







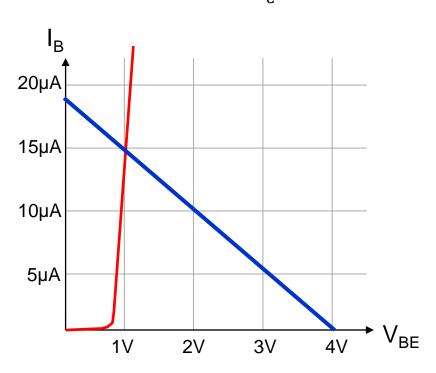
#### Case 1:

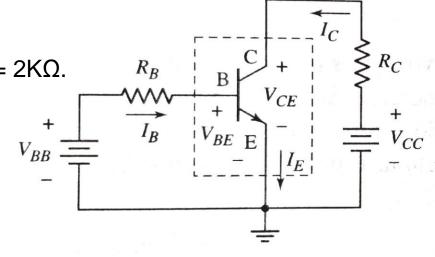
Consider  $V_{BB} = 4V$ ,  $R_B = 220K\Omega$ ,  $V_{CC} = 10V$ ,  $R_C = 2K\Omega$ .

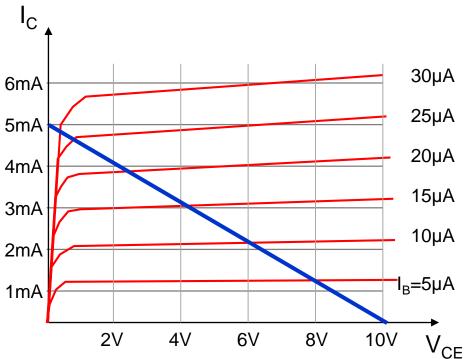
The load lines are

Input load line:  $I_B = \frac{V_{BB} - V_{BE (ON)}}{R_B}$ 

Output load line:  $I_C = \frac{V_{CC} - V_{CE}}{R_C}$ 



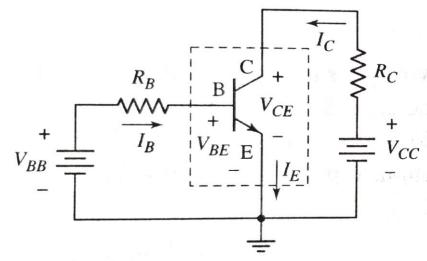


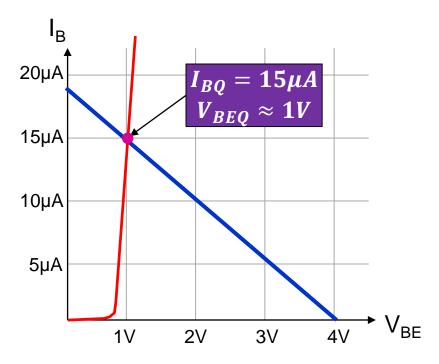


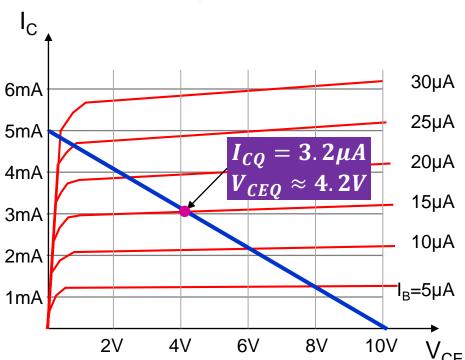
## Case 1:

$$V_{BB} = 4V$$
,  $R_B = 220K\Omega$ ,  $V_{CC} = 10V$ ,  $R_C = 2K\Omega$ .

Q-point is almost at the center of the output characteristic, allowing us to use larger input signal variation.



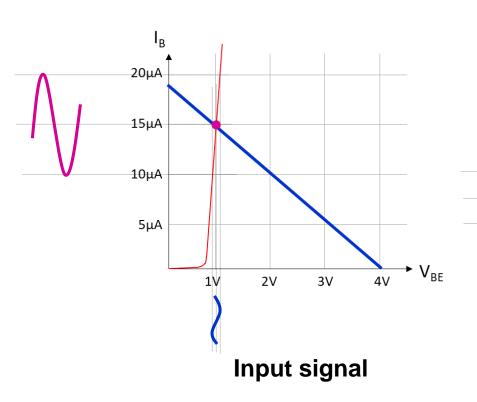


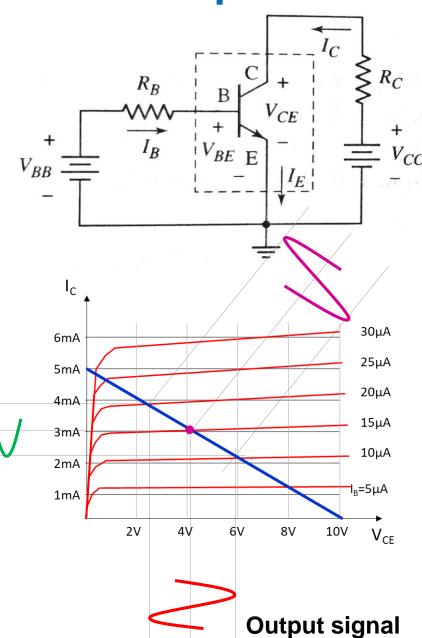


#### Case 1:

 $V_{BB} = 4V$ ,  $R_B = 220K\Omega$ ,  $V_{CC} = 10V$ ,  $R_C = 2K\Omega$ .

Input signal amplified with no distortion





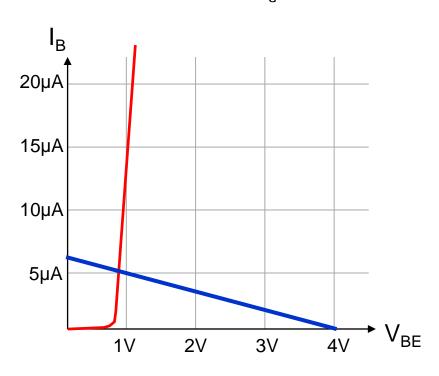
#### Case 2:

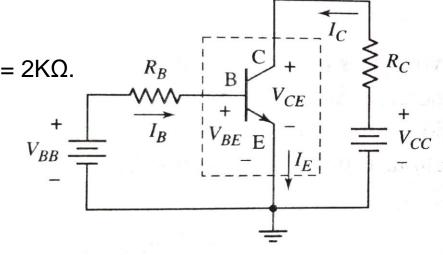
Consider  $V_{BB} = 4V$ ,  $R_{B} = 650K\Omega$ ,  $V_{CC} = 10V$ ,  $R_{C} = 2K\Omega$ .

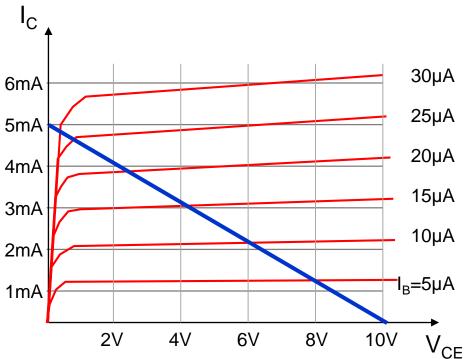
The load lines are

Input load line:  $I_B = \frac{V_{BB} - V_{BE (ON)}}{R_B}$ 

Output load line:  $I_C = \frac{V_{CC} - V_{CE}}{R_C}$ 



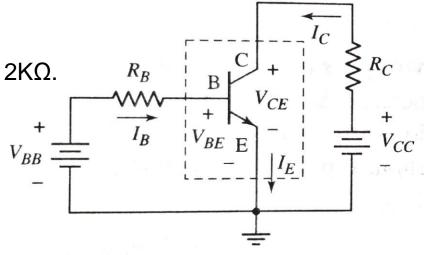


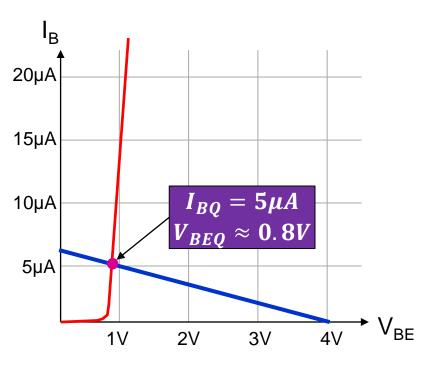


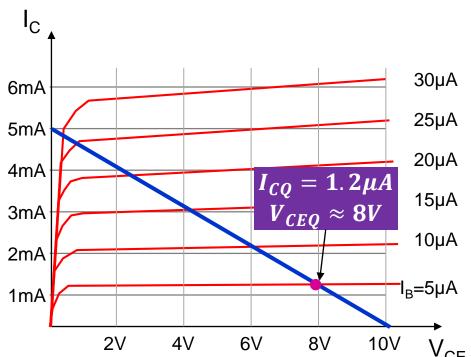
#### Case 2:

Consider  $V_{BB} = 4V$ ,  $R_{B} = 650K\Omega$ ,  $V_{CC} = 10V$ ,  $R_{C} = 2K\Omega$ .

Q-point is now close to the cut off regions, as a result the negative cycle of the signal may get clipped.



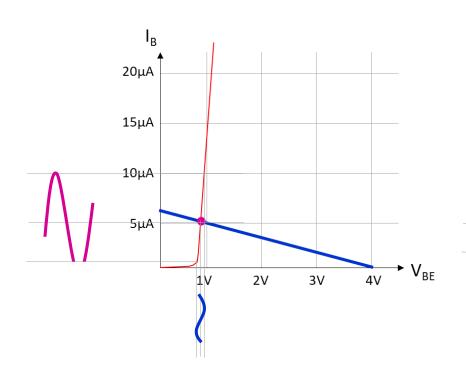


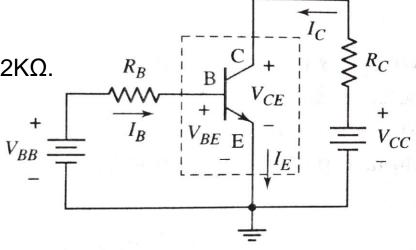


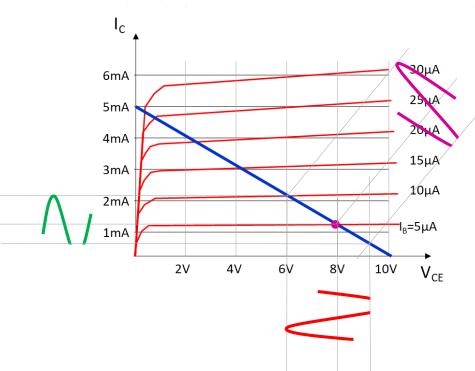
#### Case 2:

Consider  $V_{BB} = 4V$ ,  $R_B = 650K\Omega$ ,  $V_{CC} = 10V$ ,  $R_C = 2K\Omega$ .

Input signal amplified with distortion

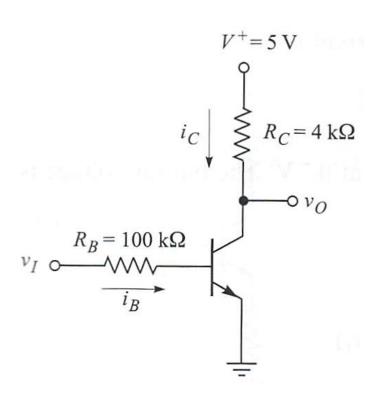






Another more direct approach to visualize the operation of a BJT circuit or the state of a transistor is by using a plot of the transfer characteristics (output voltage versus input voltage).

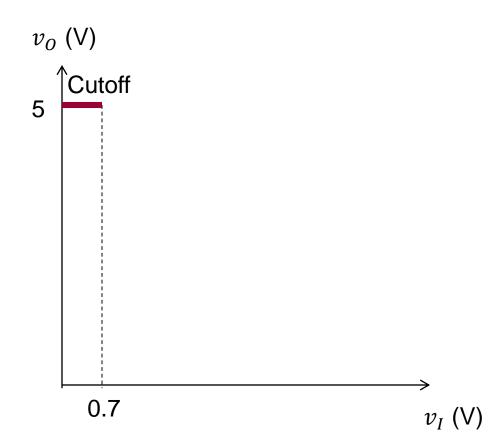
Let's consider the following circuit.



Assume  $V_{BE(ON)} = 0.7V$ ,  $\beta = 120$ ,  $V_{CE(sat)} = 0.2V$ 

In this circuit,  $v_o = V_C = V_{CE}$ 

- Initially, the transistor is in cutoff mode because Vi is too small to turn on the diodes.
   In cut off mode, there is no current flow.
- Then as V<sub>I</sub> starts to be bigger than V<sub>BE(ON)</sub> the transistor operates in forward-active mode.



## **B-E Loop**

$$100I_B + V_{BE} - v_I = 0$$

$$\Rightarrow I_B = \frac{v_I - 0.7}{100}$$

## C-E Loop

$$I_{C}R_{C} + v_{O} - 5 = 0$$

$$\Rightarrow I_{C} = \frac{5 - v_{O}}{4}$$

$$\Rightarrow \beta I_{B} = \frac{5 - v_{O}}{4} \quad \beta = 120$$

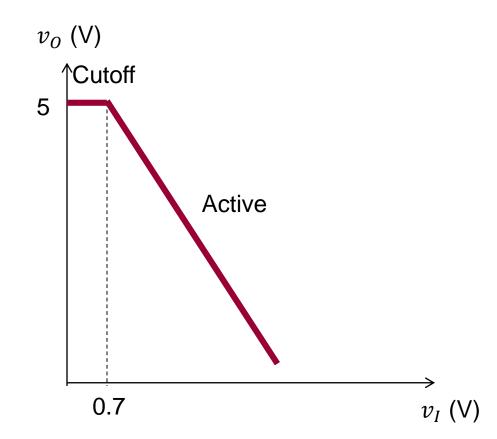
$$\Rightarrow I_{B} = \frac{5 - v_{O}}{480}$$

Equating these two equations:

$$\frac{v_I - 0.7}{100} = \frac{5 - v_O}{480}$$

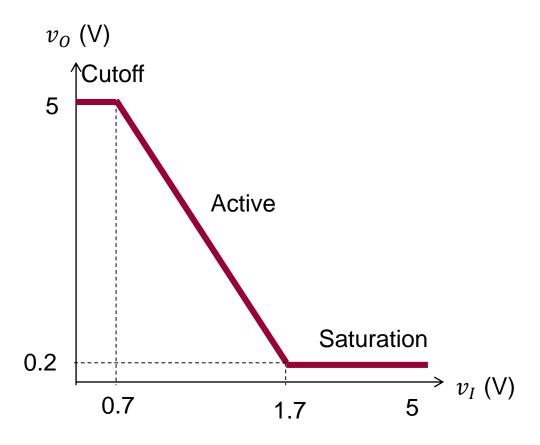
$$\Rightarrow v_O = \frac{-480v_I + 836}{100}$$

A linear equation with negative slope



However, as you increase Vi even further, it reaches a point where both diodes start to become forward biased – transistor is now in saturation mode.

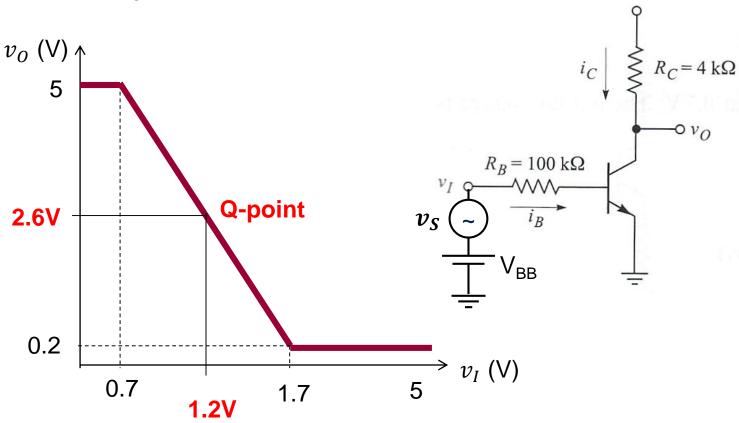
In saturation mode,  $v_O = V_{CE(sat)} = 0.2V$ .



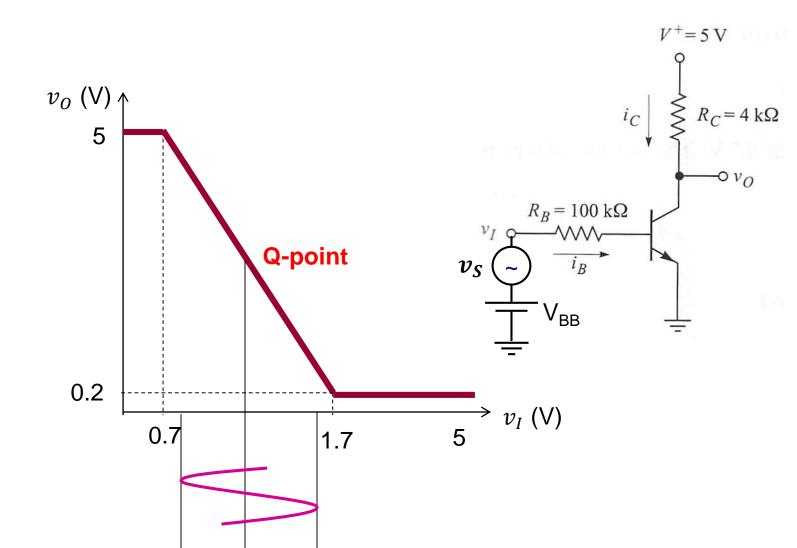
Let us now introduce an AC signal  $v_i$  (which needs to be amplified) at the input port along with a DC voltage  $V_{\rm BB}$ .

$$v_S = 0.4 \sin(2\pi 50t), V_{BB} = 1.2V$$

The Q-point is shown in the figure:



With the AC signal the input signal will also vary with time from  $v_I = (1.2 + 0.4)V = 1.6V$  to  $v_I = (1.2 - 0.4)V = 0.8V$ 



Since the entire input signal is within the linear range of voltage transfer characteristic:

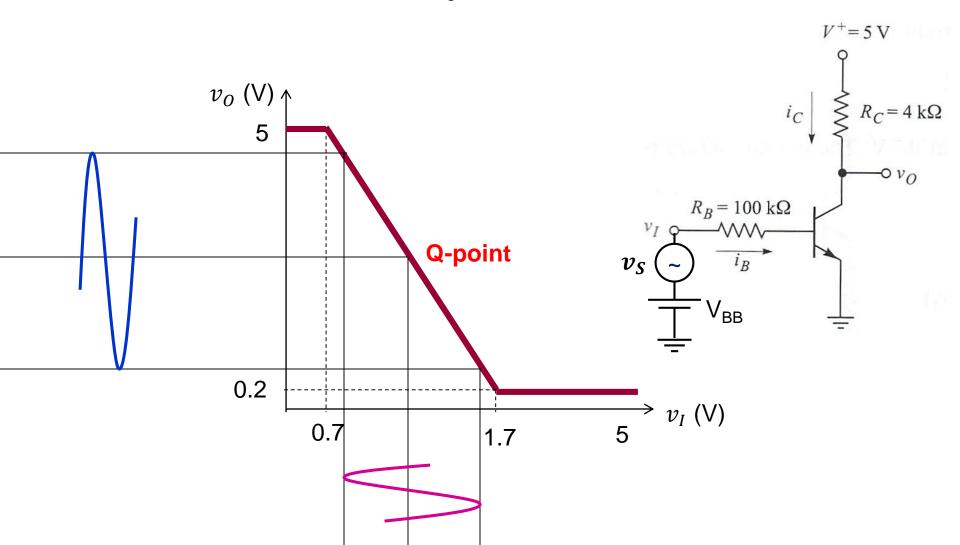
$$v_{O,max} = \frac{-480 \times v_{I,min} + 836}{100} = \frac{-480 \times 0.8 + 836}{100} = 4.52V$$

$$v_{O,min} = \frac{-480 \times v_{I,max} + 836}{100} = \frac{-480 \times 1.6 + 836}{100} = 0.68V$$

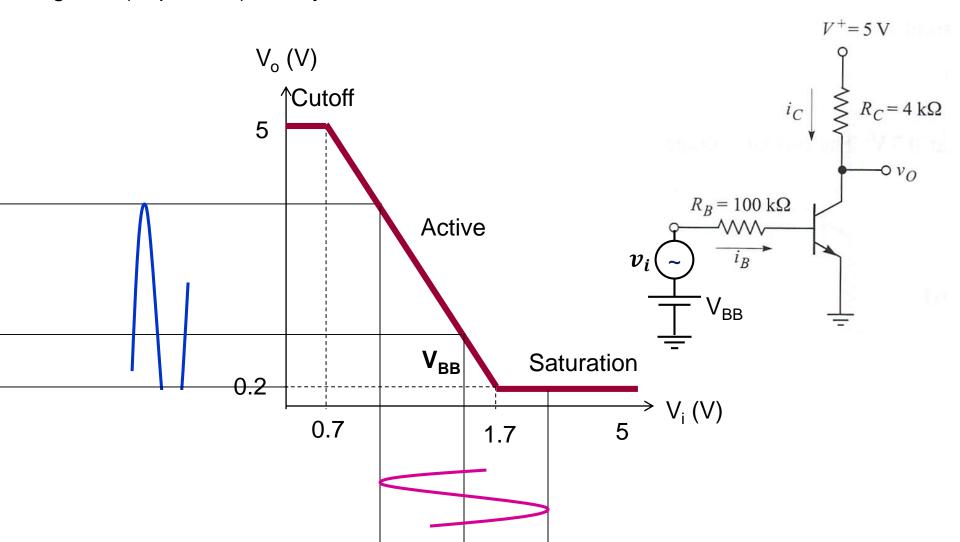
$$v_{O} \text{ (V)}$$

As a result  $\Delta v_O = 0.68 - 4.52 = 3.84V$ 

Thus the voltage amplification is  $A_v = \frac{\Delta v_O}{v_S} = \frac{-3.84}{0.8} = -4.8$ 



The DC sources plays an important role, if the DC bias is chosen close to saturation (or cut off) region, for the same input voltage swing, the output will be clipped in the negative (or positive) half cycle, as shown below.



# **Various Biasing circuits**

From the previous discussion it is obvious that the DC values of input ( $I_B$ ,  $V_{BE}$ ) and output variables ( $I_C$ ,  $V_{CE}$ ) or in other words the position of the Q-point of a transistor plays an important role in its operation as an amplifier.

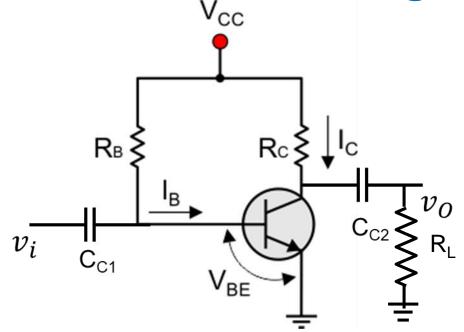
In order to create a linear amplifier, we must keep the transistor in the forward-active mode, establish a Q-point near the center of the load line and couple the time varying input signal to the base.

The amplifier biasing circuit discussed in the previous slides is not a very practical design for two main reasons:

- 1. The signal source is not grounded
- 2. There may be situations where you do not want a DC base current flowing through the signal source.

Therefore, in this section we will discuss various alternative biasing schemes.

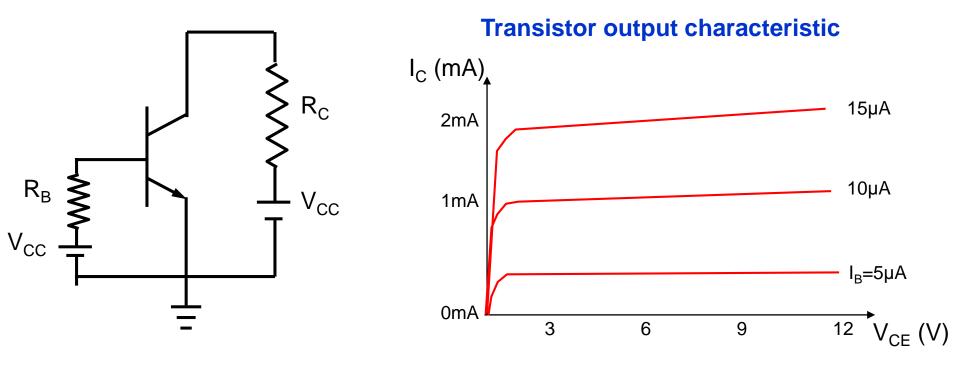
# Fixed base (or Single base) resistor biasing



#### Notice:

- $C_{C1}$  and  $C_{C2}$  are called coupling capacitors (typical values range between 1-10µF). These are called coupling capacitors. They act as open circuit for DC voltages.  $C_{C1}$  isolates the signal source from the DC base current.  $C_{C2}$  removes any DC component from the output voltage.
- If the frequency of the input signal is large enough and  $C_{C1}$  and  $C_{C2}$  are large enough, the input signal can be coupled to the base through  $C_{C1}$  and amplified AC signal can be transferred to the load with little attenuation.
- Here only one DC bias source V<sub>CC</sub> is used. By choosing correct values of R<sub>B</sub> and R<sub>C</sub> we can control the junction voltages.

# Fixed base (or Single base) resistor biasing DC equivalent circuit



If  $V_{CC}$  = 12 V and the Q-point need to be  $I_C$  = 1mA and  $V_{CEQ}$  = 6V, find the values of  $R_B$  and  $R_C$ . Assume  $\beta$  = 100 and  $V_{BE(ON)}$  = 0.7V.

# Fixed base (or Single base) resistor biasing

From the output circuit we can find the value of R<sub>C</sub>

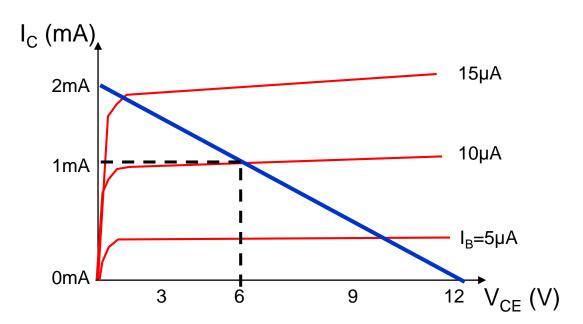
$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CO}} = 6k\Omega$$

The base current:

$$I_B = \frac{I_{CQ}}{\beta} = 10\mu A$$

The base resistance:

$$R_B = \frac{V_{CC} - V_{BE(ON)}}{I_{BO}} = 1.13 \text{M}\Omega$$



## Fixed base (or Single base) resistor biasing

This fixed base biasing configuration although simple, has two major draw backs:

1. Large base resistance: In order to keep the base current in the range of few  $\mu$ A, the base resistance value lies in the range of M $\Omega$ . This resistance is too large to be used in integrated circuits.

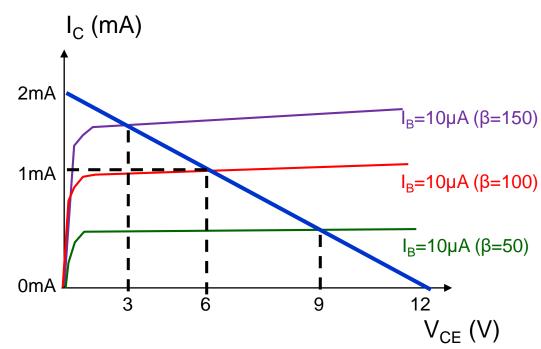
2. Bias instability: in this configuration the Q-point is not stable against any variation in the  $\beta$ 

value.

#### Change in Q-point as $\beta$ changes:

 $\beta$  of a transistor may change for various reasons. For the transistor used in this example, although the nominal value of  $\beta$  is considered to be 100, the  $\beta$  value may vary in the range of 50-150.

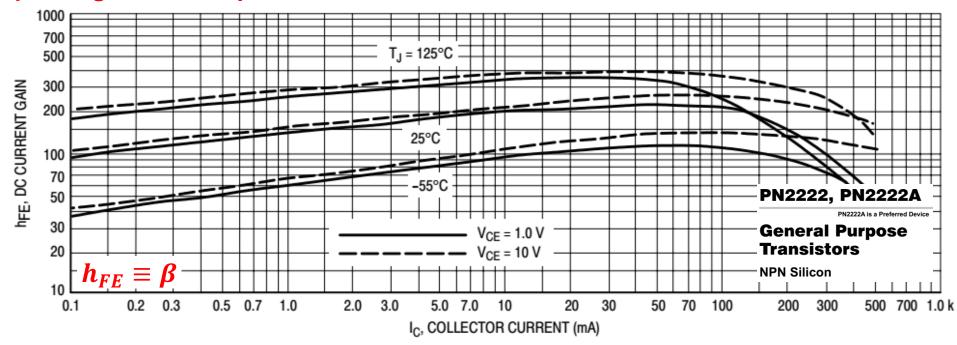
Since the base current does not depend on  $\beta$ , rather on  $V_{CC}$  and  $R_B$ , it remains constant against any fluctuation of  $\beta$ . However the output characteristic curve will change as the  $\beta$  value changes. As a result the Q-point will vary accordingly.

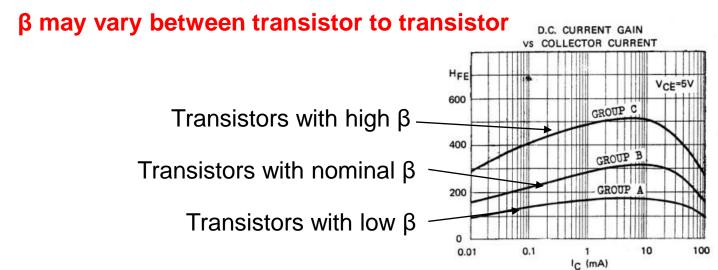


β		50	100	150
Q-point values	I <sub>CQ</sub>	0.5mA	1mA	1.5mA
	$V_{\sf CEQ}$	9V	6V	3V

## Transistor datasheet: variation of β with temperature

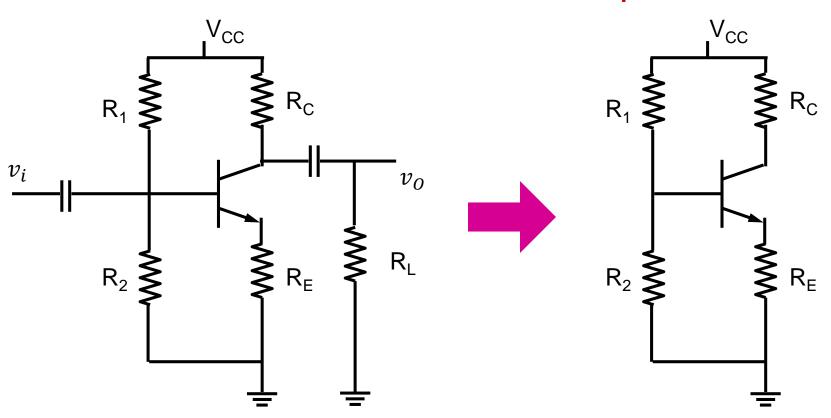
## **β** changes with temperature





## Voltage divider biasing for bias stability

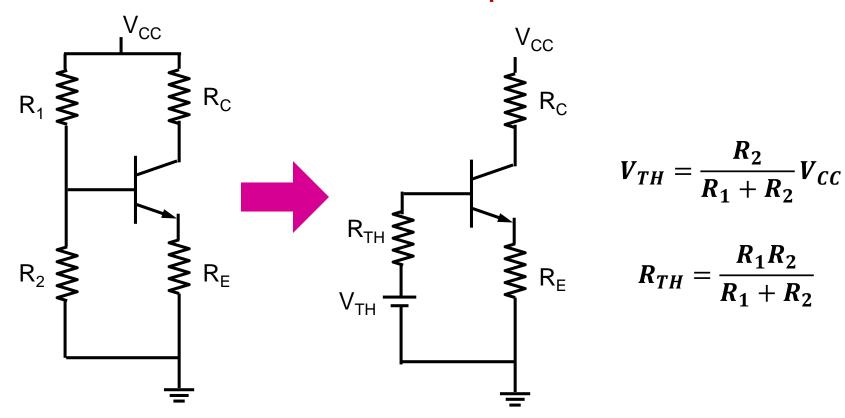
## DC equivalent circuit



## Voltage divider biasing for bias stability

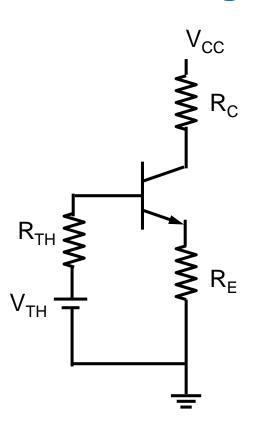
## DC equivalent circuit

## Thevenin equivalent circuit



Notice here since the voltage applied to the base depends on the ratio between  $R_1$  and  $R_2$  rather than their individual values, we have complete flexibility in choosing the values of  $R_1$  and  $R_2$ .

## Voltage divider biasing for bias stability



Apply KCL in B-E loop:

$$V_{TH} = I_{BQ}R_{TH} + V_{BE(ON)} + I_{EQ}R_E$$

If the transistor is biased in the forward-active mode, then

$$I_{EQ} = (1 + \beta)I_{BQ}$$

Therefore the base current becomes

$$I_{BQ} = \frac{V_{TH} - V_{BE(ON)}}{R_{TH} + (1 + \beta)R_E}$$

Hence the collector current becomes

$$I_{CQ} = \beta I_{BQ} = \frac{\beta (V_{TH} - V_{BE(ON)})}{R_{TH} + (1 + \beta)R_E}$$

If 
$$R_{TH} \ll (1+\beta)R_E$$

$$I_{CQ} pprox rac{eta(V_{TH} - V_{BE(ON)})}{(1 + eta)R_E}$$
 and normally  $eta \gg 1$ 

Therefore  $I_{CQ}$  becomes

$$I_{CQ} \cong \frac{(V_{TH} - V_{BE(ON)})}{R_F}$$

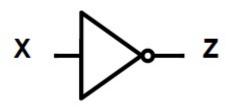
Notice here that the quiescent collector current has essentially become a function of the bias voltage ( $V_{CC}$ ) and the emitter resistance  $R_E$ . Hence any variation in  $\beta$  will have minimum effect on the Q-point

In practice  $R_{TH} = 0.1(1 + \beta)R_E$  is considered to avoid excessive power dissipation in R<sub>1</sub> and R<sub>2</sub>

# **BJT** in Digital logic gates

Another primary use of transistors is in logic gates. In logic gates transistors are either used in saturation mode or cutoff mode. While for amplification we try to avoid going into saturation and cutoff region, for logic operation we stay out of active region.

## **NOT** gate

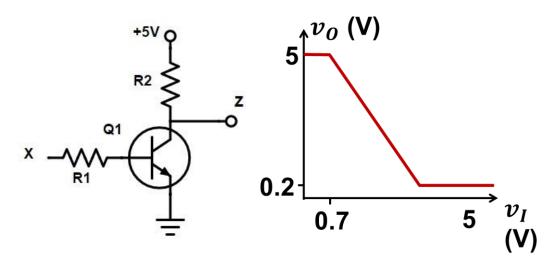


In a NOT gate when the input is 1 (high voltage) the output is 0 (low voltage)

#### **Truth Table**

Input	Output	
X	Z	
0	1	
1	0	

## **NOT** gate circuit realization

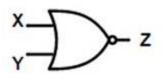


When X is 5V (Logic 1), Z is 0.2 (Logic 0)

When X is 0V (Logic 0), Z is 5 (Logic 1)

# **BJT** in Digital logic gates

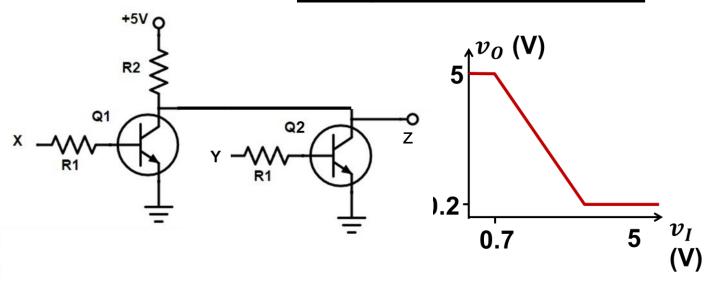
## **NOR** gate



#### **Truth Table**

Inputs		Outputs	
X	Υ	Z	
0	0	1	
0	1	0	
1	0	0	
1	1	0	

## NOR gate circuit realization



- When both X and Y are 0V (logic 0), both the transistors Q1 and Q2 are cut off, hence z is 5V (Logic 1).
- When X is 0V (logic 0) and Y is 5V (logic 1), Q1 is in cut off and Q2 is in saturation, hence z is 0.2V (Logic 0).
- When X is 5V (logic 1) and Y is 0V (logic 0), Q1 is in saturation and Q2 is in cut off, hence z is 0.2V (Logic 0).
- When both X and Y are 5V (logic 1), Q1 as well as Q2 are in saturation, hence z is 0.2V (Logic 0).

# **BJT in Digital logic gates**

What logic operations can be performed with the following circuits?

