(D)

DEPARTMENT OF ELECTRONICS AND ELECTRICAL COMMUNICATION ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

Date: **24 April 2017**, ~~FN~~/AN, Time: 3 Hrs., Full Marks: **100**, No. of Students: **677** (Non-ECE branches); End Spring Semester-2017, Sub. No.: **EC21101**, Sub. Name: **Basic Electronics**

Instructions

- **All waveform sketches / diagrams must be neatly drawn and clearly labeled**. Answers must be brief and to the point.
- The final answers (numerical values with unit) should be **underlined** or enclosed within box with unit.
- **For every Question No., start your answer from a new page.**
- **Avoid writing answers of the various parts of a single question at different locations in your answer-script.**
- For any value related to any device parameter or circuit parameter, which you may find not given with a problem, assume suitable value for such parameter.
- **No Queries will be entertained. Candidate may make necessary assumptions, if so required.**

Question 1 (MCQ), [1x20 = 20 marks]

1. The bubble in the symbol of a NOR gate represents
(a) Complement (b) Negation (c) Invert (d) All

2. The NOR and OR gates, respectively, are considered as
(a) Universal logic gates (b) Universal and basic logic gates (c) Basic logic gates (d) Basic and universal gates

3. Which of the following is minimized expression of $A(A+B)$?
(a) A (b) B (c) AB (d) $A+B$

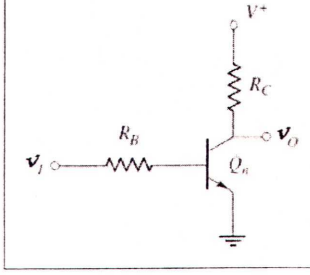
4. The decimal equivalent of the binary number 1.1101 is
(a) 1.625 (b) 1.725 (c) 1.7125 (d) 1.8125

5. In an *npn* BJT, the magnitude V_A of the early voltage can be
(a) $v_{CB} = V_A$ (b) $v_{CB} = -V_A$ (c) $v_{CE} = V_A$ (d) $v_{CE} = -V_A$

6. An *npn* BJT with common cut-in voltage V_γ, in the reverse active mode, satisfies
(a) $v_{BE} < V_\gamma, v_{CE} > v_{BE} + V_\gamma$ (b) $v_{BE} < V_\gamma, v_{CE} > v_{BE} - V_\gamma$
(c) $v_{BE} < V_\gamma, v_{CE} < v_{BE} - V_\gamma$ (d) $v_{BE} < V_\gamma, v_{CE} < v_{BE} + V_\gamma$

7. The use of ideal bypass capacitor in a BJT based CE-amplifier circuit is
(a) to ensure that current from DC source meant for biasing do not pass through the signal source
(b) to achieve bias stability without reduction in the small signal voltage gain
(c) to reduce the signal attenuation effect of the transistor's internal capacitances
(d) to reduce loading effects due smaller load impedances

8. In the circuit given below, where Q_n is in forward active mode, the phase difference between the input and output signals changing with time is



(a) 90 degrees
(b) 0 degrees
(c) 270 degrees
(d) 180 degrees

9. At room temperature, Aluminum (Al) with 3 valence electrons is a

(a) donor impurity (b) acceptor impurity (c) intrinsic semi-conductor (d) none of the above

10. A glowing LED is essentially

(a) a reverse biased diode with direct band gap (b) a reverse biased diode with indirect band gap

(c) a forward biased diode with direct band gap (d) a forward biased diode with indirect band gap

11. For the same input sinusoidal signal, the difference in the peak voltage magnitude obtained at the output of a bridge and a center-tap full-wave rectifiers comprising diodes with cut-in voltage V_γ is

(a) V_γ (b) $V_{peak} - V_\gamma$ (c) $2V_\gamma$ (d) 0

12. The current and voltage across a non-ideal pn-junction diode are

(a) not related (b) inversely proportional to each other

(c) proportional to each other when the voltage is in log-scale (d) proportional to each other when the current is in log-scale

13. The capacitance of a diode increases in

(a) forward bias (b) reverse bias (c) in both biasing modes (d) none

14. For a BJT to be used as a CE amplifier, it is preferred

(a) both p-n junctions are forward-biased (b) E-B reverse bias and C-B forward bias

(c) E-B forward bias and C-B reverse bias (d) both E-B and E-B reverse bias

15. Clampers are circuits which

(a) take away some portion of the applied signal (b) shifts the applied signal to a different dc level

(c) doesn't make any change in the applied signal (d) none

16. For a BJT CE amplifier, the base current is one hundredth of the collector current, and the emitter current is 10.1 mA, the base and the collector currents are, respectively

(a) 99 μA, 9.9 mA (b) 10 mA, 0.1 mA (c) 0.1 mA, 10 mA (d) 0.1 μA, 10 mA

17. For an ideal OPAMP, the CMRR is

(a) finite (b) infinite (c) zero (d) none

18. The unity gain OPAMP buffer can be realized by

(a) inverting configuration (b) non-inverting configuration

(c) both inverting and non-inverting configurations (d) none

19. In realizing OPAMP as an integrator (working at low frequencies as well), the feedback circuit should have

(a) a capacitor (b) a resistor

(c) both capacitor and resistor in parallel (d) both capacitor and resistor in series

20. The output of an inverting OPAMP which has resistances ratio (R_F/R_1) of 10 is fed into the non-inverting OPAMP with feedback resistance ratio of 20. The overall voltage gain of this cascaded amplifier configuration is

(a) 46.4 dB (b) 20 dB (c) 26.4 dB (d) none

Question 2.

A. Study the Common Emitter amplifier circuit in Fig. 2a, where the capacitor acts ideally and the transistor's early voltage is high enough to be considered infinite.

(i) Consider that the circuit is changed by removing the capacitor and by replacing the voltage divider biasing with a biasing through an additional voltage (say, V_{BB}) in series with v_s. Mathematically deduce and show the difference in the small-signal gain due to the change by drawing the Hybrid-π transistor model based on small-signal equivalent circuits and explain briefly (not more than 100 words) the effect of the change on the gain. **[8 + 2 = 10 marks]**

(ii) If an emitter resistor is added to the circuit (in Fig. 2a), show that a type of small signal gain stability can be achieved. **[5 marks]**

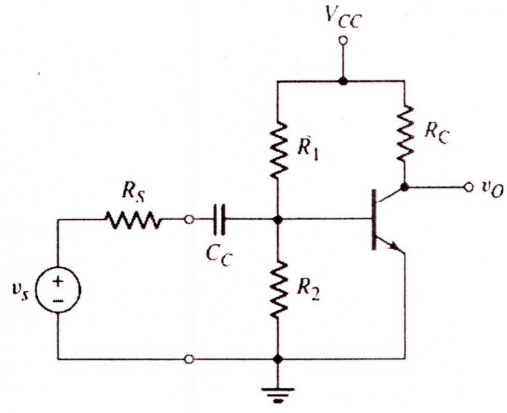


Fig. 2a

B. Study the Common Emitter amplifier circuit in Fig. 2b, where the capacitors act ideally, the DC collector and emitter currents can be considered same, and the transistor's early voltage is high enough to be considered infinite. Assume that the resistors R_1 and R_2 are set in such a way that maximum symmetrical swing is achieved maintaining bias stability and the transistor in forward-active mode with $v_{CE} \geq 0.5V$ & $i_C \geq 0.25mA$. Find the maximum values that v_{CE} and i_C reaches. **[5 marks]**

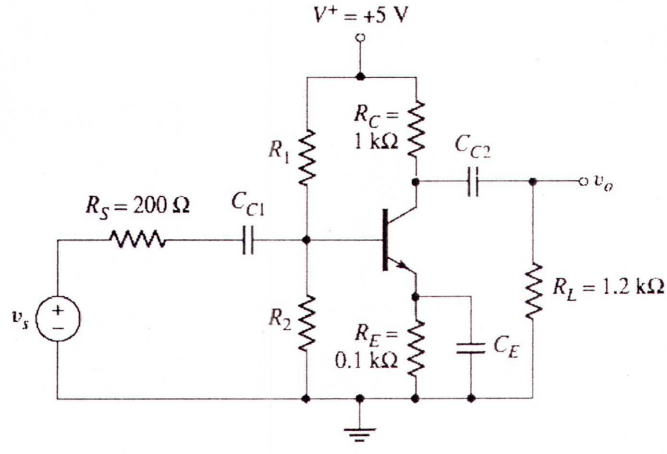


Fig. 2b

Question 3

A. Calculate the CMRR in dB of the differential amplifier circuit shown in Fig. 3a. What is the full form of CMRR? **[8 marks]**

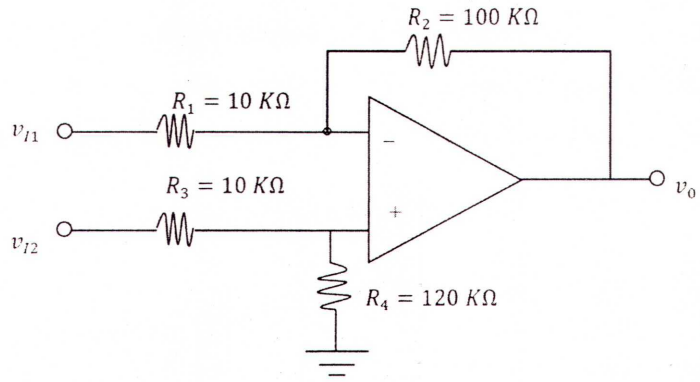


Fig. 3a

B. Consider the circuit made of ideal OPAMPs as shown below in Fig. 3b. Let $R_1 = 20\ k\Omega$, $R_2 = 120\ k\Omega$, $R_3 = 15\ k\Omega$ and $R_4 = 75\ k\Omega$. If $v_I = 0.2V$, calculate v_{01}, v_0, i_1, i_2, i_3 and i_4. Determine the current into or out of the output terminal of each OPAMP. **[7 marks]**

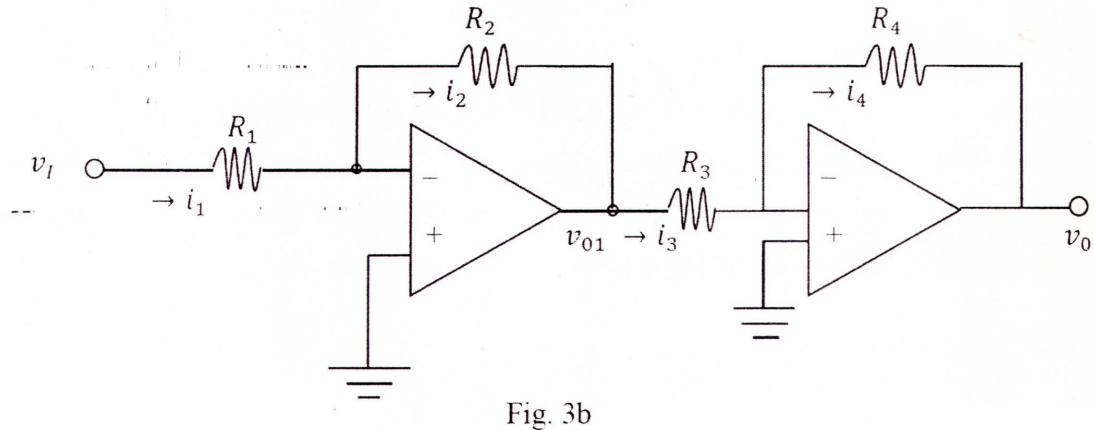


Fig. 3b

C. Find the closed loop voltage gain of the circuit shown in Fig. 3c. **[5marks]**

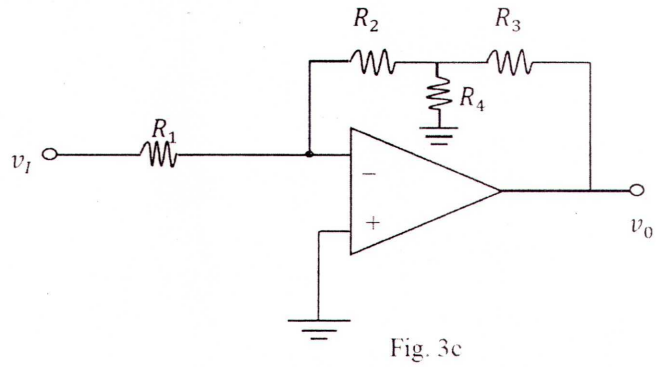
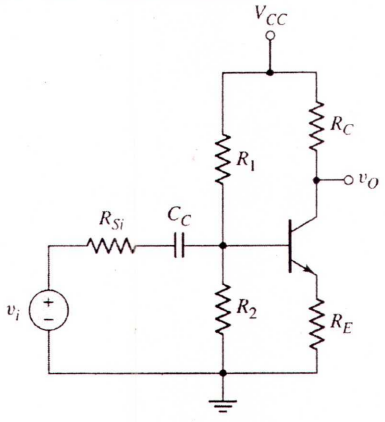


Fig. 3c

Question 4

A. Obtain an average dc output voltage in a full-wave rectifier, assuming diodes to be ideal. **[5 marks]**

B. For the CE BJT amplifier circuit (given below), draw its hybrid-π equivalent model. Obtain the corner frequency and maximum gain provided by the circuit. Consider: R_1=51.2 kΩ, R_2=9.6 kΩ, R_C=2 kΩ, R_E=0.4 kΩ, R_{Si} = 0.1 kΩ, C_C= 1μF, V_{BE} (on) =0.7 V, β=100, V_A =∞ , and V_{CC} =10 V. **[15 marks]**



Question 5

A. State De Morgan's Theorems by considering three variables in your representations. Consider that you need 2-input AND gate, 2-input OR gate and 2-input Ex-OR gate in some circuit realization while you have only 2-input NAND gates in your stock. Show how you can use these 2-input NAND gates to fulfill your need. **[2+4 marks]**

B. A digital system has a 4-bit input $B_3B_2B_1B_0$ that can vary from 0000 to 1111. The system generates an output, $Y = 1$ when the equivalent decimal input is greater than 9, else $Y = 0$.

(i) Write the truth table that represents the digital system and give the minterm and maxterm based representations of output as a Boolean function of the input. [**3 marks**]

(ii) Use Karnaugh Map to give minimized representations in sum-of-product and product-of-sum forms for this system and draw corresponding circuit diagrams. [**6 marks**]

(iii) How does the minimized expressions change if Y is either 0 or 1 when the equivalent decimal input is 10 or 11, while other things remain same? **[2 marks]**

C. Show how the decimal number 25.625 can be represented in binary in fixed point representation? How the same can be represented in hexadecimal? **[2+1 marks]**

End of Question Paper