Course: Basic Electronics (EC21101)

Course Instructor: Prof. Kapil Debnath

Lecture 7: MOSFET

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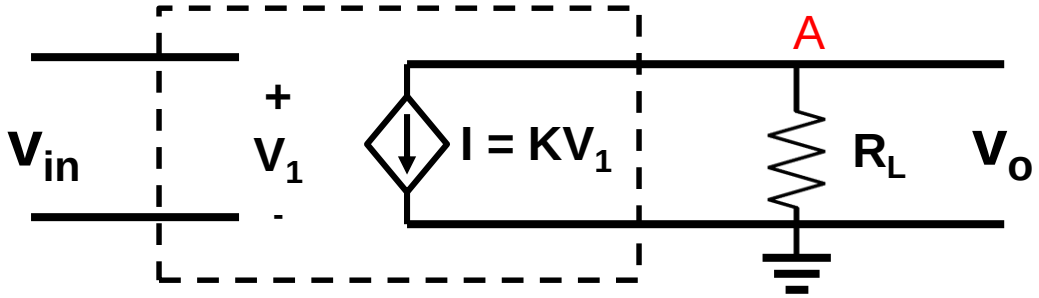
Dependent source as amplifier

Let us consider a Voltage-controlled current source (VCCS). The voltage that controls the current source is connected to the input signal and the dependent current source is feeding the load resistance. The output voltage is measured across the load resistance.

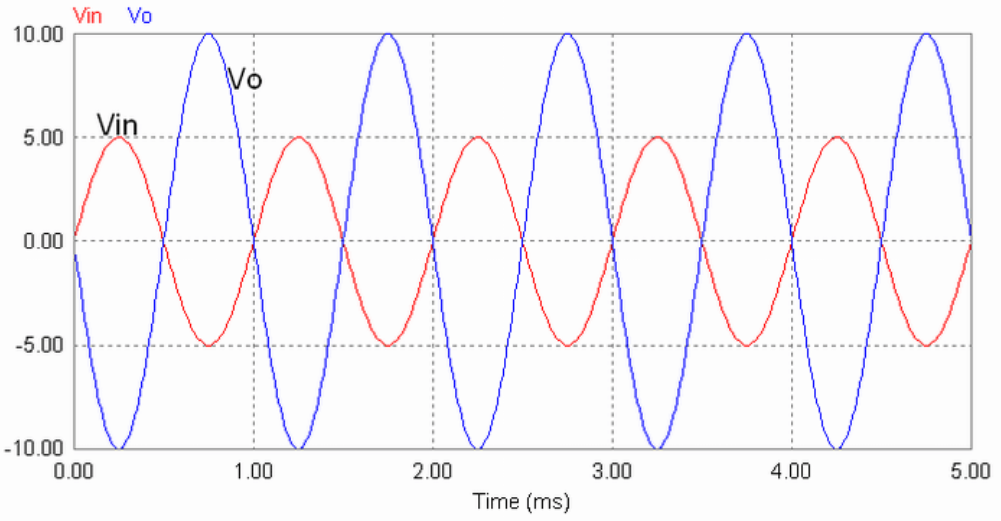


If we apply KCL at point A we get:

$$\frac{V_o}{R_L} + KV_1 = 0$$

$$\Rightarrow V_o = -R_L K V_{in}$$

If we have R_L and K such that $R_L K > 1$, we have an amplification of the input signal. Therefore we can argue that we can achieve amplification with a dependent source.



Dependent source realization

In order to realize a dependent source i.e. an amplifier we need a new device, known as transistor. There are two types of transistors available:

1. **B**ipolar **J**unction **T**ransistor (BJT)
2. **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor (MOSFET)

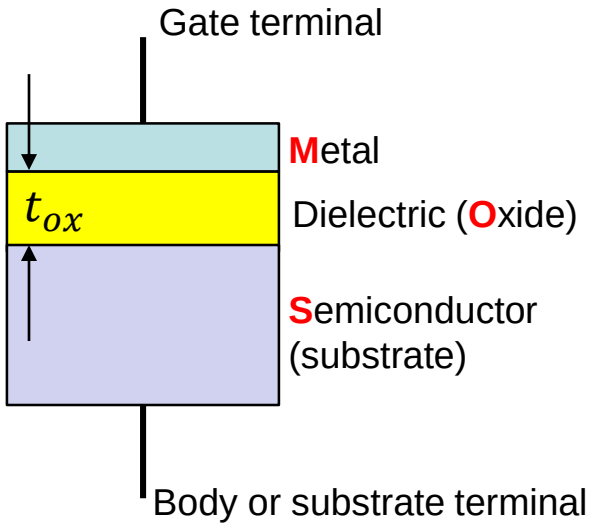
We have already covered BJT in the previous lectures, now we will briefly discuss the structure and behaviour of MOSFETs.

MOSFTEs have several advantages over BJTs, some of them are:

1. High input impedance
2. Smaller size
3. Low power consumption
4. Efficient switching
5. More stable to thermal changes

Basic MOS structure

The basic MOS (metal-oxide-semiconductor) structure consists of an insulating layer (oxide) sandwiched between a metal layer and a semiconductor layer. The structure is very similar to a parallel metal plate capacitor, hence the basic MOS structure is also called a MOS capacitor. Here one point to remember is that unless the semiconductor is heavily doped, the conductivity is much lower than that of metal.



Once some voltage is applied across the gate terminal and the body (substrate) terminal, we expect charges to accumulate on both sides of the dielectric region. The accumulated charge is given by:

$$Q = CV$$

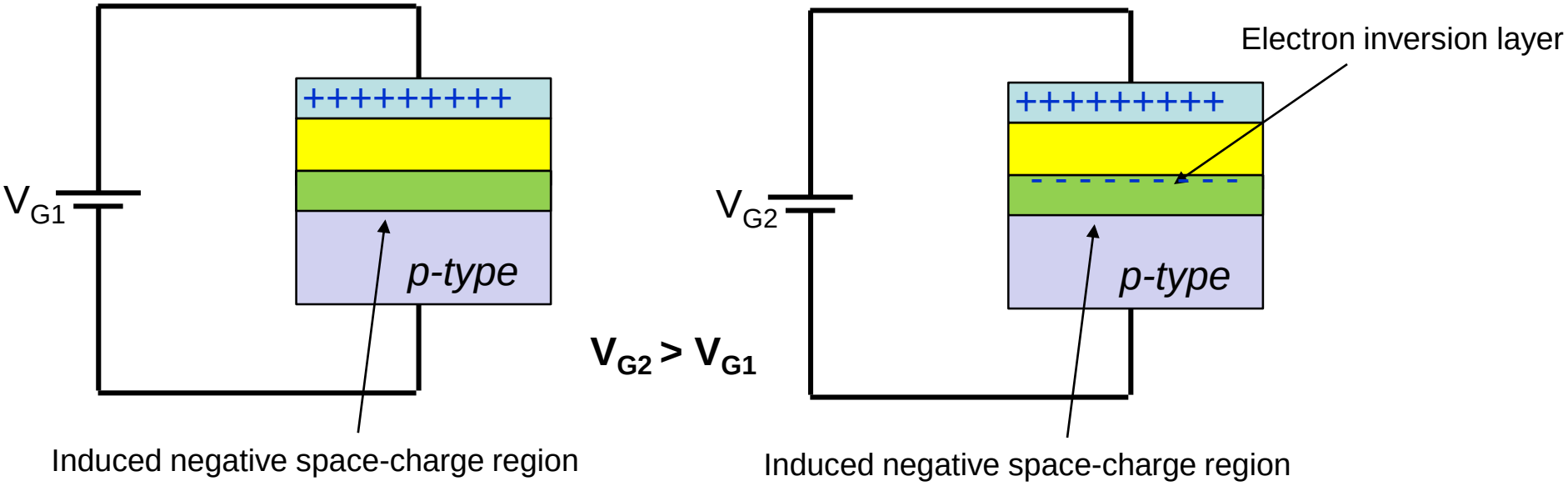
Where the capacitance is expressed as:

$$C = \varepsilon_{ox} \frac{A}{t_{ox}}$$

ε_{ox} is the dielectric permittivity, A is the cross-sectional area and t_{ox} is the thickness of the oxide layer

MOS capacitor with p-type substrate

Let us first consider a MOS capacitor with p-type substrate. As you know, p-type semiconductor has more holes than electrons. When a positive bias is applied to the gate terminal with respect to the substrate, holes near the dielectric-semiconductor interface moves away from the interface leaving behind negative ions. Thus a negative space charge region is created. When a larger positive voltage is applied, minority carrier electrons in the p-type semiconductor are attracted to the oxide-semiconductor interface. As the applied field further increases the electron density near the interface also increases. After certain applied voltage the electron concertation becomes more than the hole concentration of the p-type substrate. This phenomenon is called **inversion**. i.e. near the dielectric-semiconductor interface the p-type semiconductor turns into an n-type semiconductor. This region where the electron concentration becomes more than the hole concentration is called an **electron inversion layer or channel**. We can have the same effect in an n-type semiconductor MOS by applying a negative bias to the gate terminal.



MOS capacitor with p-type substrate

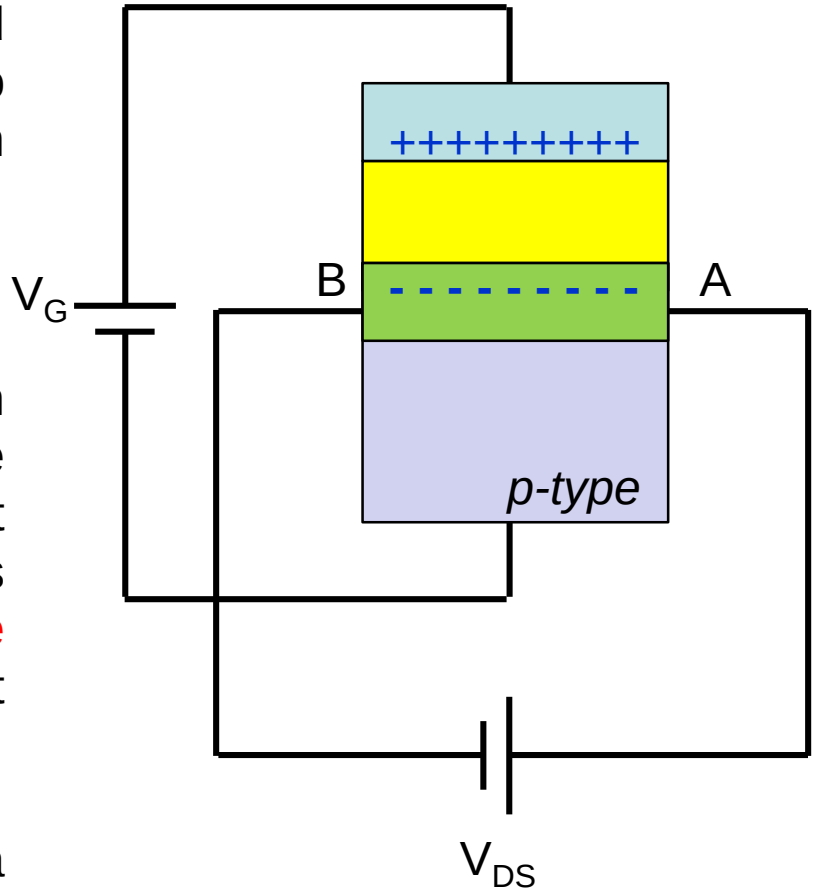
What if now we apply a voltage across the substrate as shown?

It should be obvious that due to the applied voltage V_{DS} the electrons will move along B to A direction and we will have a current flow from A to B.

Now if we increase V_G what will happen?

Since due to increase in V_G electron density in the channel region will increase and hence the resistance of the region decrease. As a result the current flow will increase. Thus this structure can be considered as a voltage dependent current source where the current from A to B depends on voltage V_G.

This is the basic operating principle of a MOSFET.

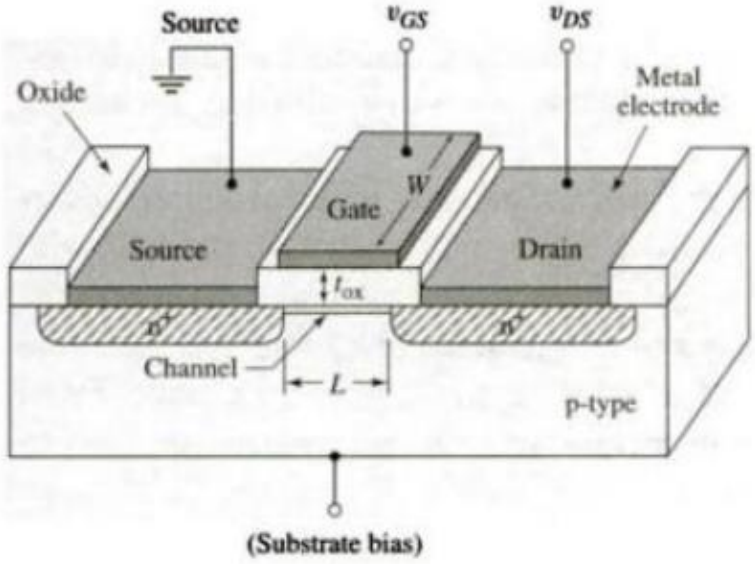


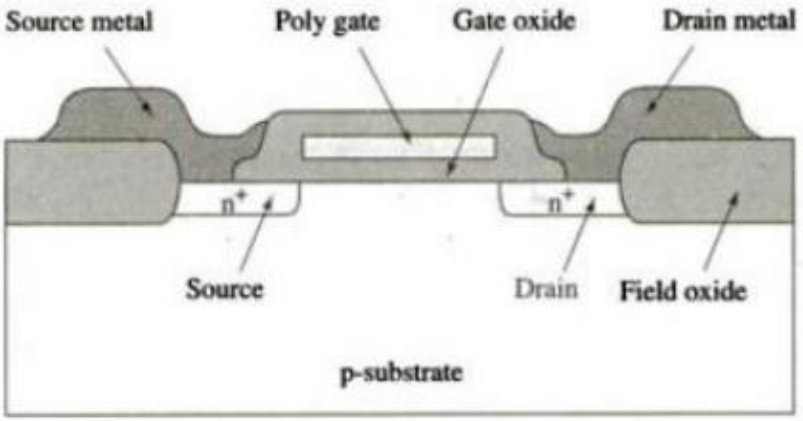
n-channel Enhancement-mode MOSFET

The mechanism described in the previous slide for current flow through the inversion layer in a MOS capacitor can be used to create a transistor. For most of the electronic devices, especially for integrated circuits, it is impractical to use electrical contacts on the side of the devices (such as point A and B).

Figure shows a simplified cross-section of a MOS field-effect transistor. As you can notice the gate, oxide and p-type substrate or body is same as the MOS capacitor. In addition we now have to n-regions, called source terminal and drain terminal. When no voltage is applied to the gate with respect to the body, no current can flow between source and drain. But due to an applied voltage at the gate when an inversion layer is created that allows the flow of charge through the inversion layer, also called the channel region. Since certain voltage must be applied to the gate terminal in order to create the inversion layer, this type of MOSFETs are called enhancement mode MOSFET.

n-channel Enhancement-mode MOSFET



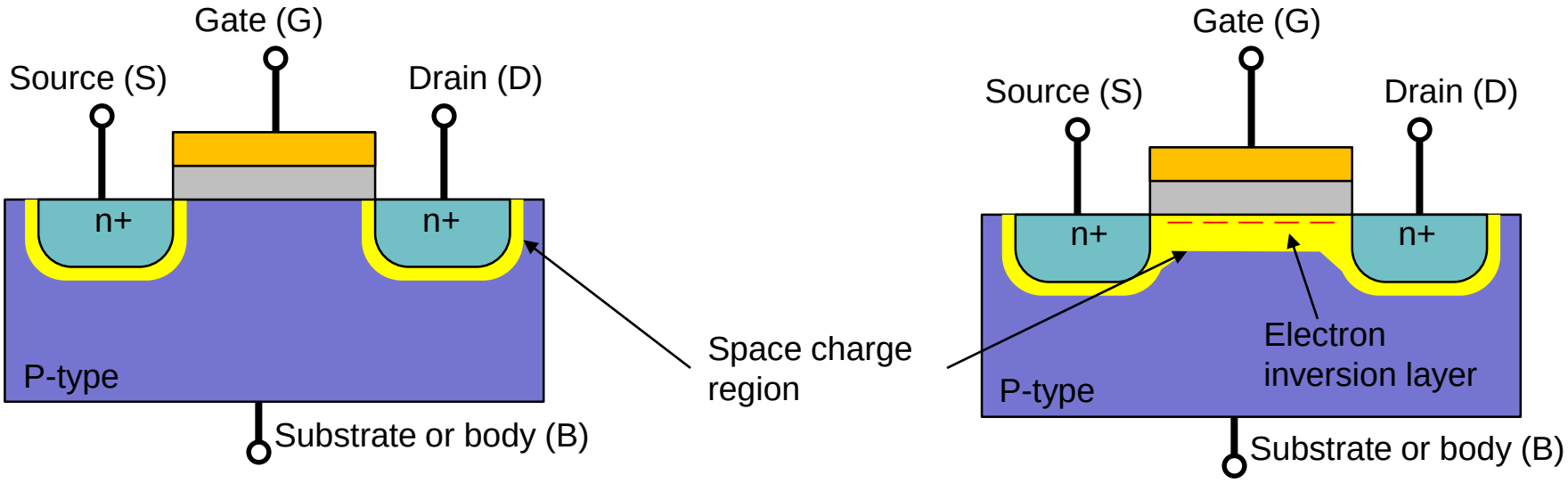


- Channel length, $L \sim 1$ μm
- Oxide length, $t_{ox} \sim 400$ Angstrom
- NMOS (*carriers are electrons*)

p-type substrate, two n-regions (n-source, n-drain)
Positive Gate voltage

n-MOSFET basic transistor operation

When zero bias is applied between the gate and body, the source and drain terminals are separated by the p-region. This is equivalent to two back-to-back diodes. Under such condition no current flows between the source and drain terminals. When a large voltage is applied to the gate an electron inversion layer is created close to the oxide-semiconductor interface and this layer connects the n-source to the n-drain. Since the free carriers in the inversion layer are electrons this device is also called n-channel MOSFET (NMOS). The source terminal supplied the carriers that flow through the channel and the drain terminal allows th4 carriers to drain from the channel. The magnitude of the current through the channel depends on the amount of charge in the inversion layer, which in tern is a function of the applied gate voltage. Since the gate terminal is separated from the channel by the oxide layer, there is no gate current. Similarly, since the channel and substrate are separated by a space charge region, there is essentially no current through the substrate.

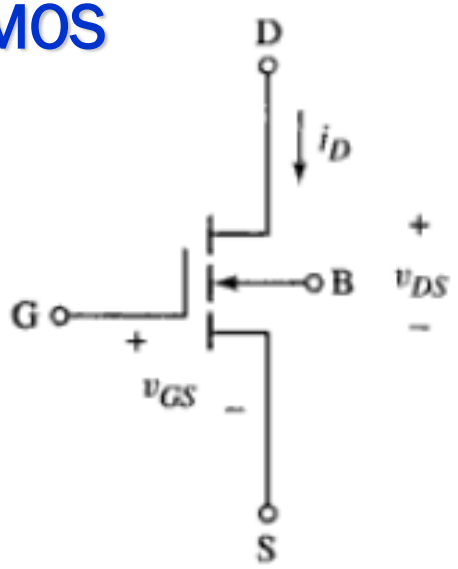


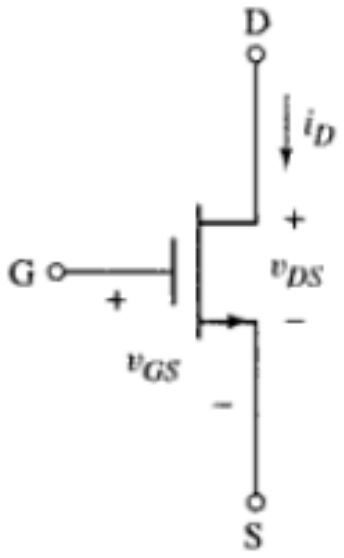
No bias applied

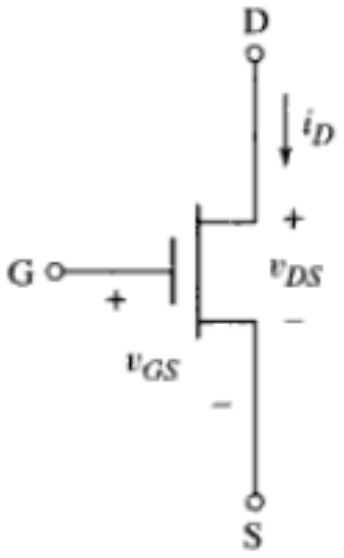
Bias applied

Symbols

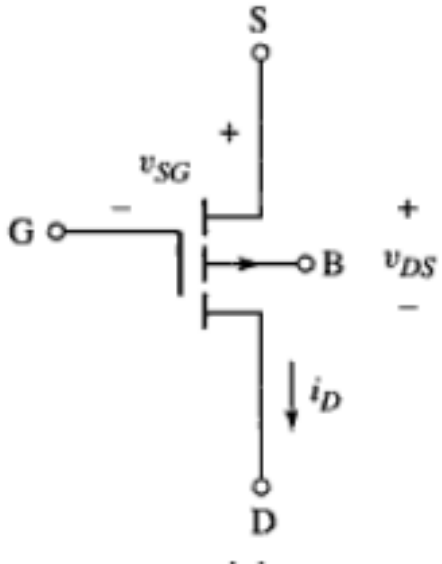
NMOS

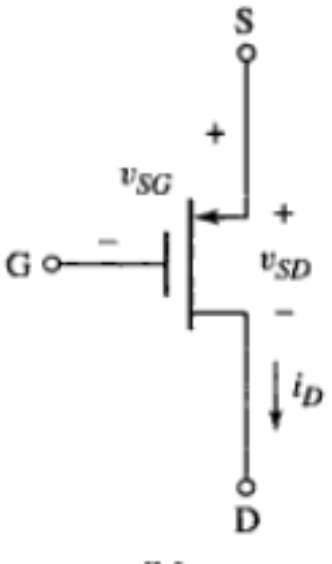


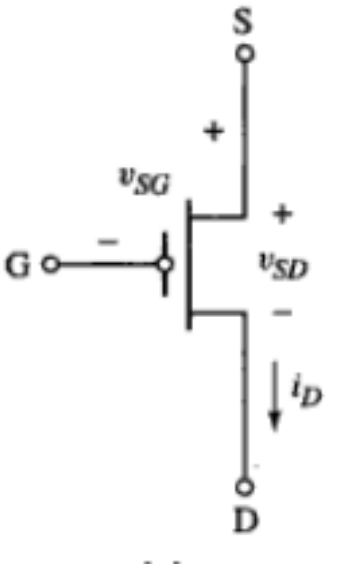




PMOS





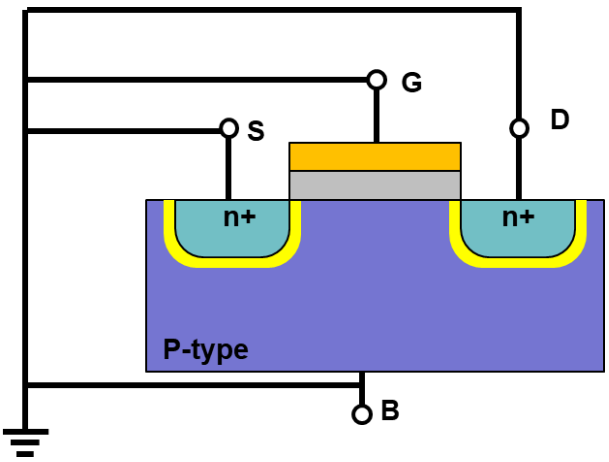


Ideal NMOS current-voltage characteristics

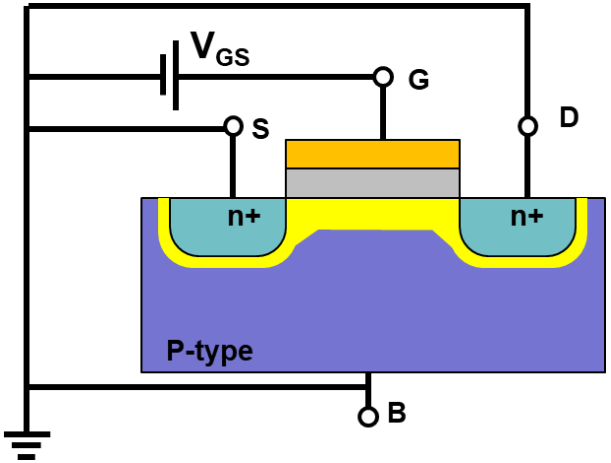
Let us first consider that all the terminals are grounded expect the gate terminal, where we apply certain positive voltage V_{GS}. When V_{GS} increases first a depletion layer is formed near the oxide-semiconductor interface. As V_{GS} further increases inversion layer starts to form and above a certain value of V_{GS} the electron density in the inversion layer becomes more than the majority (hole) density in the substrate. That voltage is called threshold voltage, V_{TN}.

As the gate voltage increases beyond V_{TN} electron density increases in the inversion layer, i.e. in the channel region. Thus the resistance between source and drain terminal decreases.

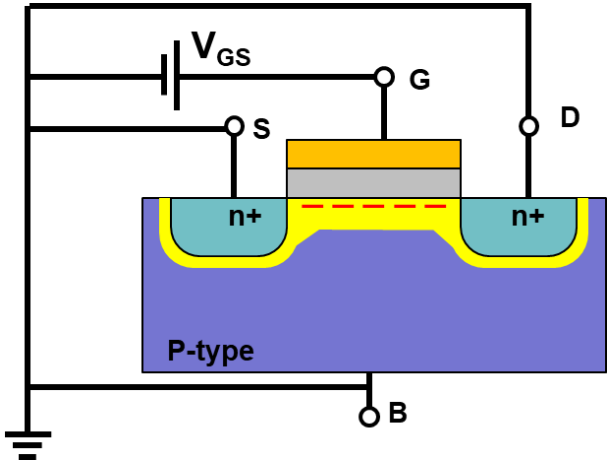
No applied voltage



$V_{GS} < V_{TN}$



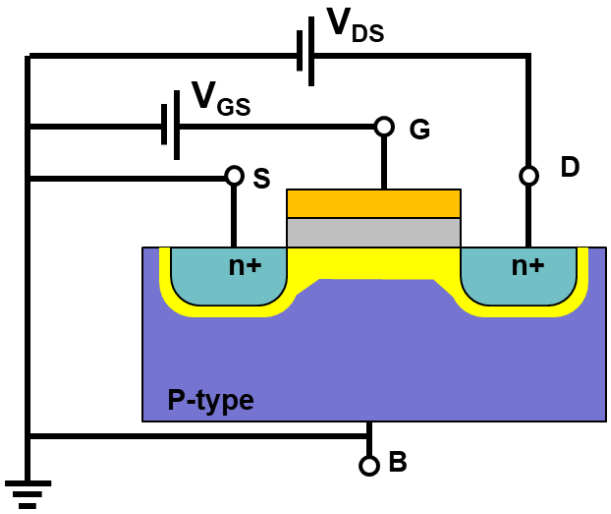
$V_{GS} > V_{TN}$



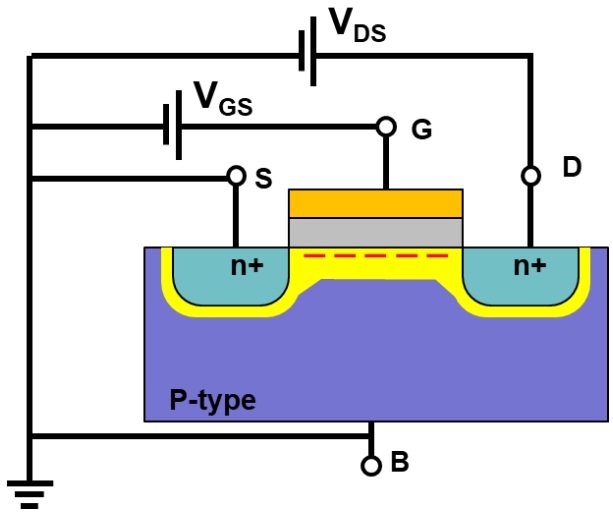
Ideal NMOS current-voltage characteristics

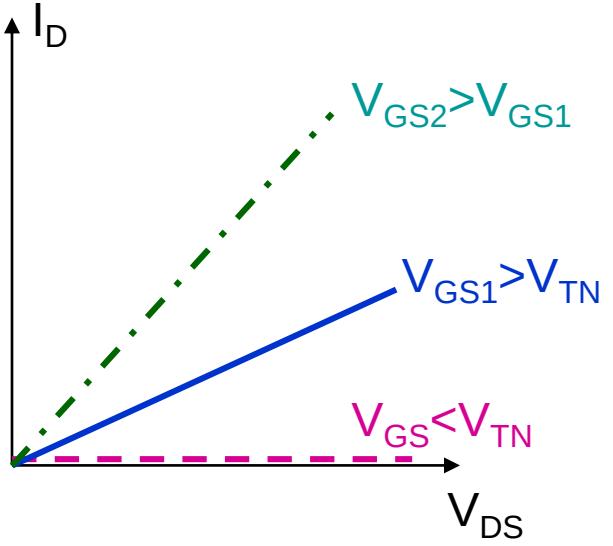
Let us now also apply a positive voltage to the drain with respect to source.
When the gate voltage is less than V_{TN}, essentially no current flows from drain to source, because there is no inversion layer is formed which can connect the source and drain terminals. Therefore for any value of drain to source voltage V_{DS} the current through the channel is zero.
When V_{GS} increases beyond V_{TN}, current will flow between drain and source. For small value of drain to source voltage V_{DS}, the current through the channel I_D increases linearly with V_{DS}.
As the V_{GS} further increases, due to increased electron density in the channel the channel resistance decreases and hence the slope of the I_D-V_{DS} curve increases.

$V_{GS} < V_{TN}$

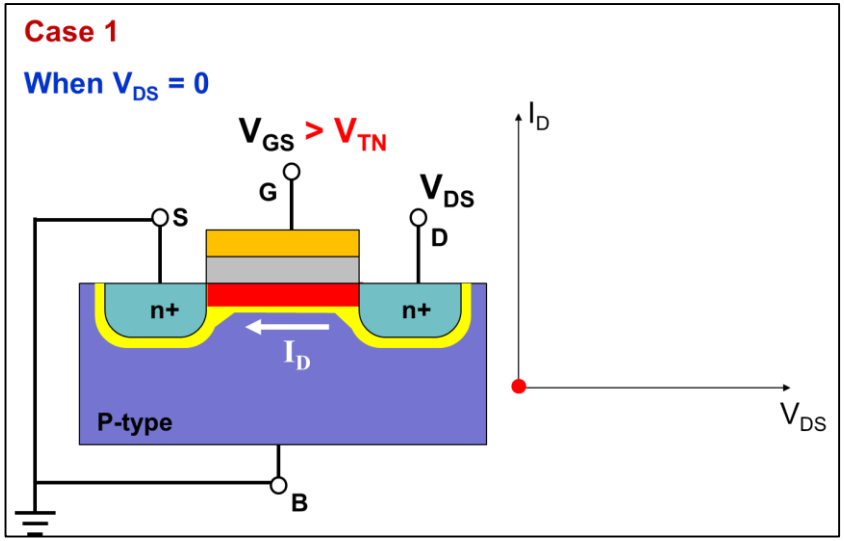


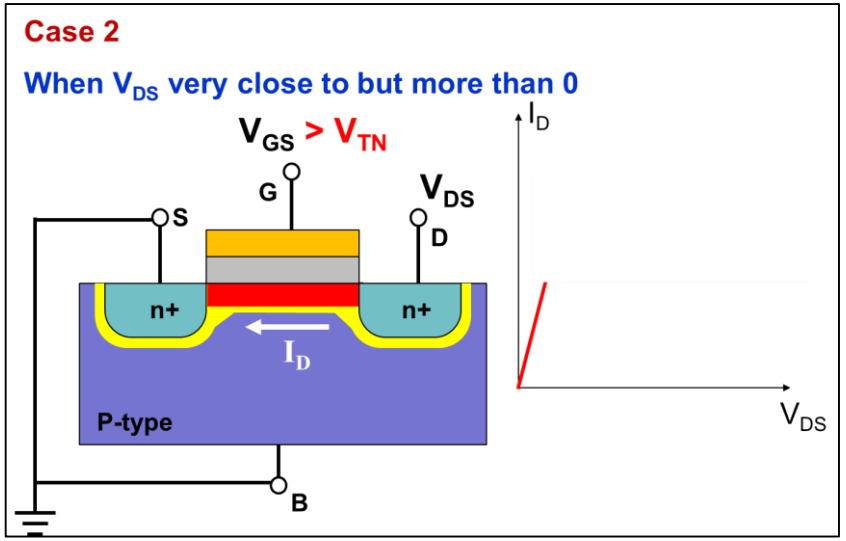
$V_{GS} > V_{TN}$

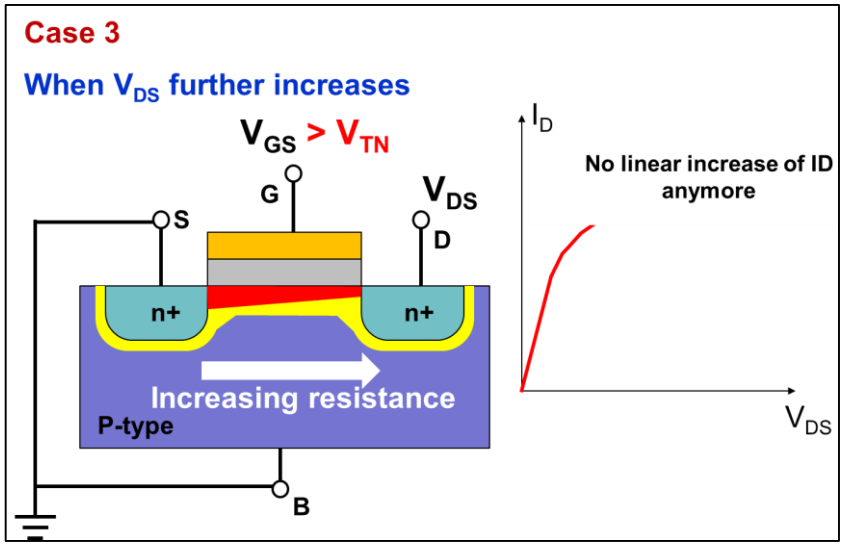


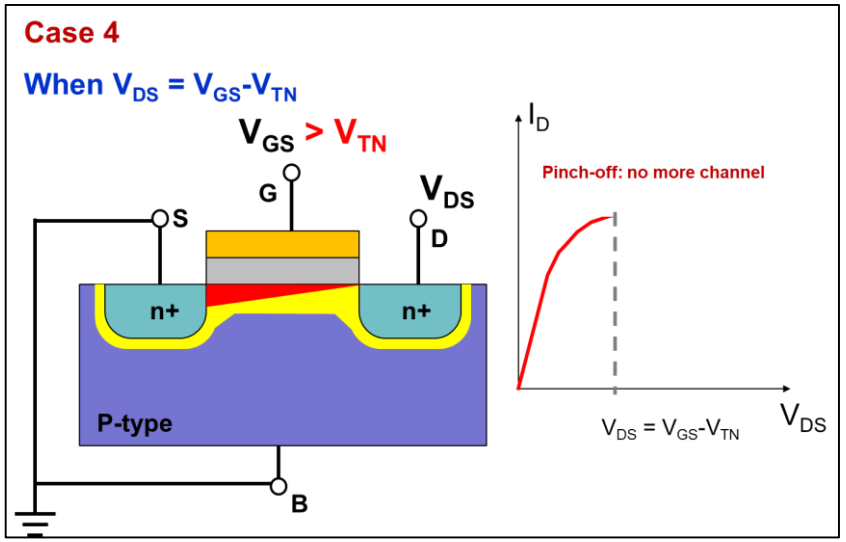


Ideal NMOS output IV characteristics

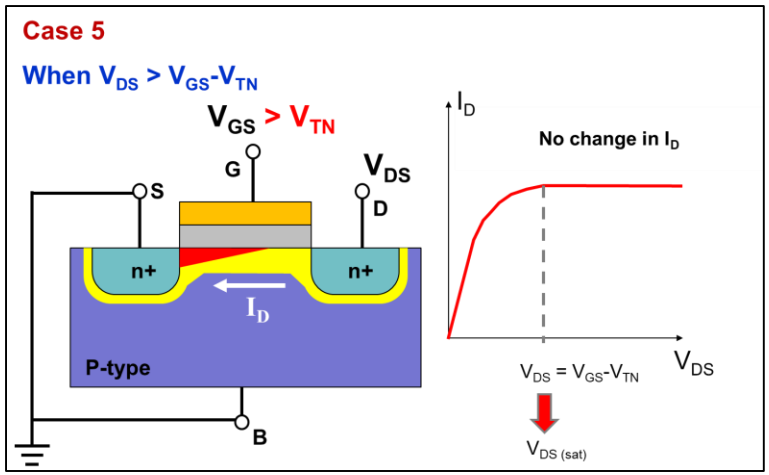


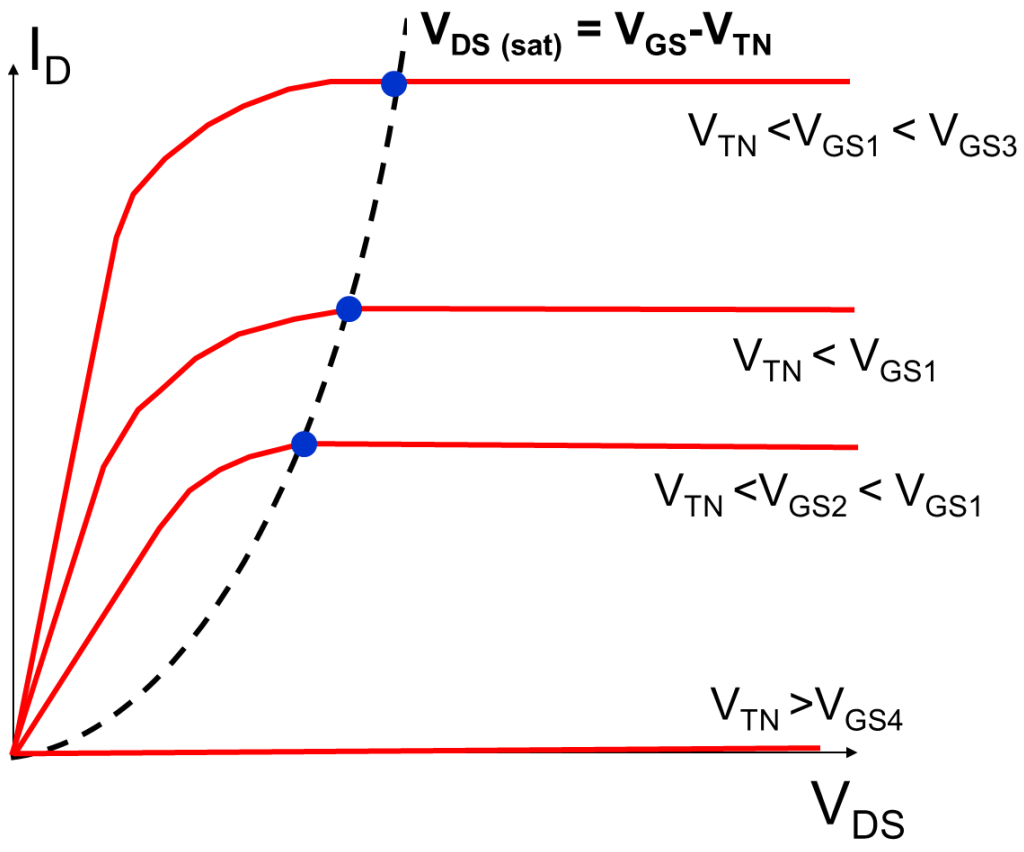




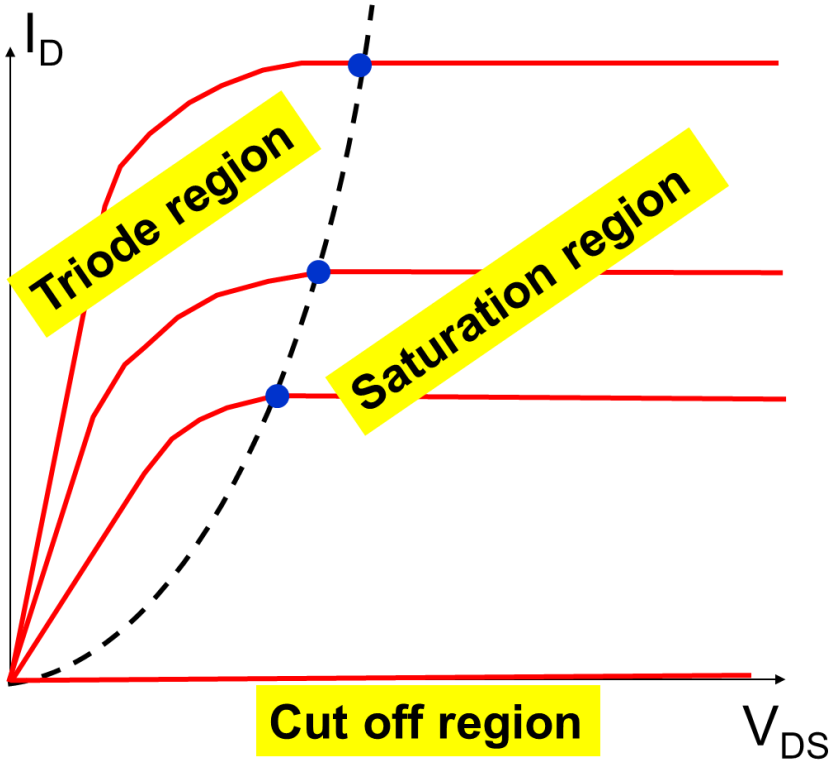


Ideal NMOS output IV characteristics





Ideal NMOS output IV characteristics



Triode region:

$$I_D = K_n\left[2(V_{GS} - V_{TN})V_{DS} - {V_{DS}}^2\right]$$

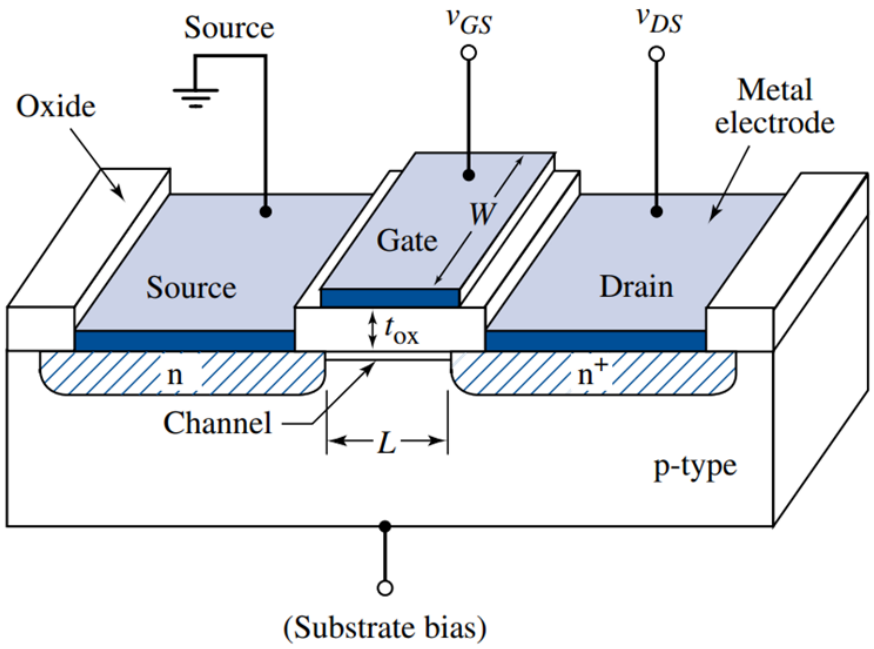
Saturation region:

$$I_D = K_n(V_{GS} - V_{TN})^2$$

Cut off region:

$$I_D = 0$$

Ideal NMOS output IV characteristics



Conduction parameter

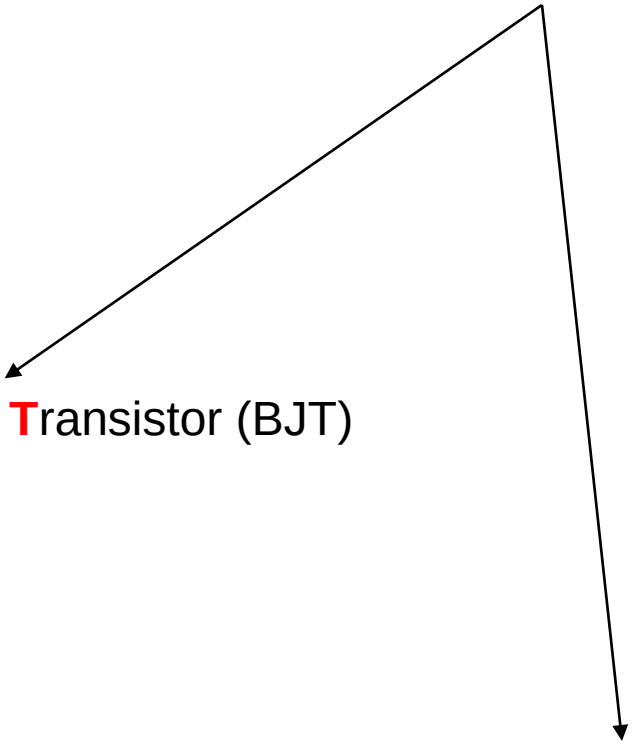
$$K_n = \frac{W\mu_n C_{ox}}{2L}$$

Unit = mA/V^2

$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ (capacitance per unit area)

Appendix
class slides

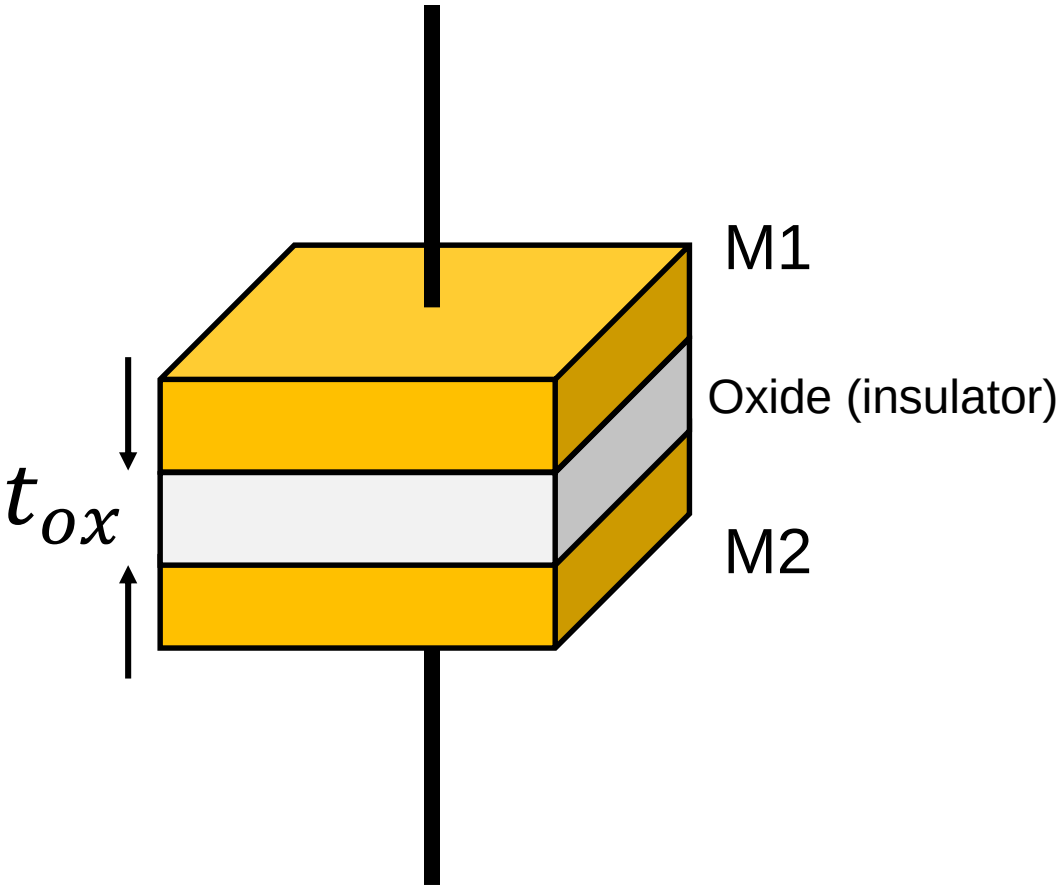
Transistors

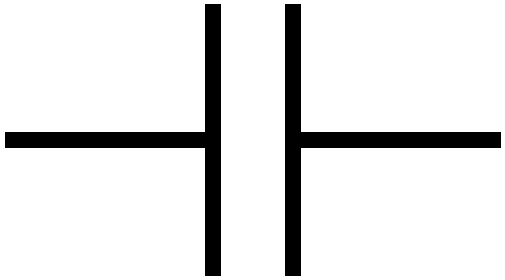


Bipolar **J**unction **T**ransistor (BJT)

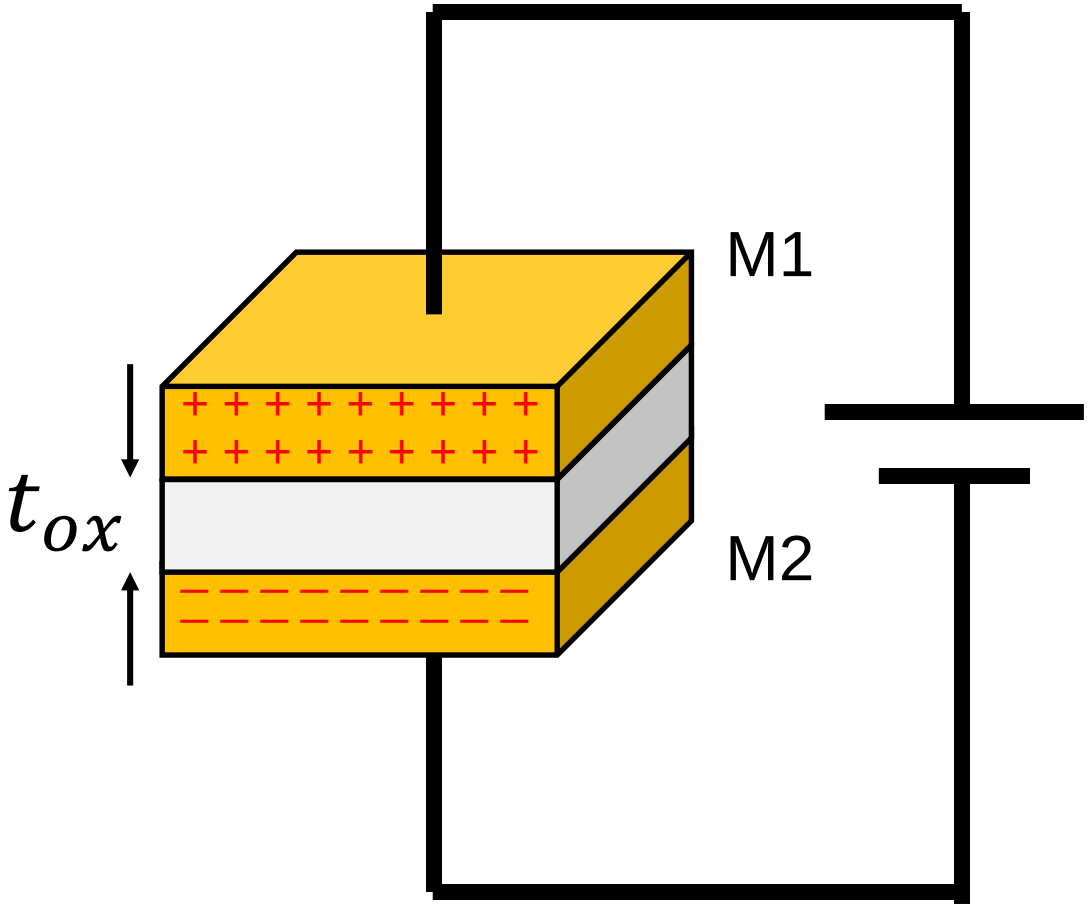
Metal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor (MOSFET)

Conventional capacitor

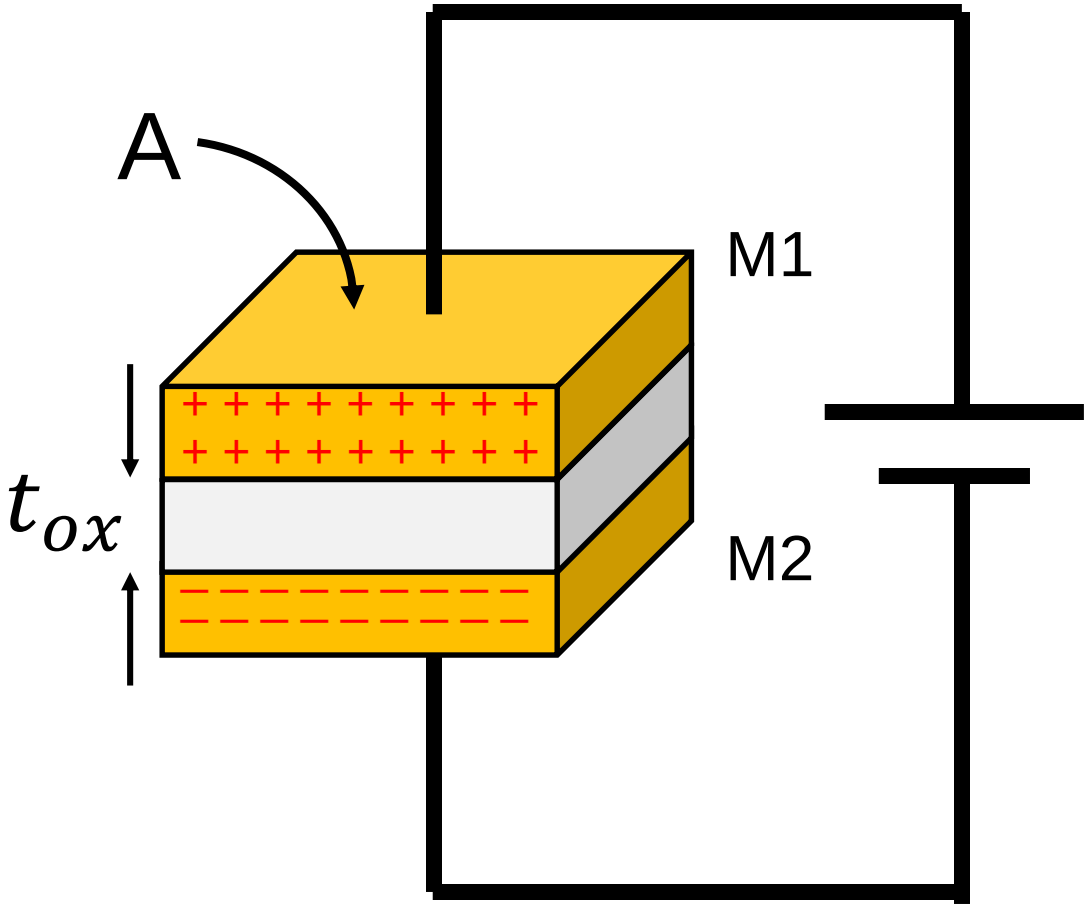




Conventional capacitor



Conventional capacitor

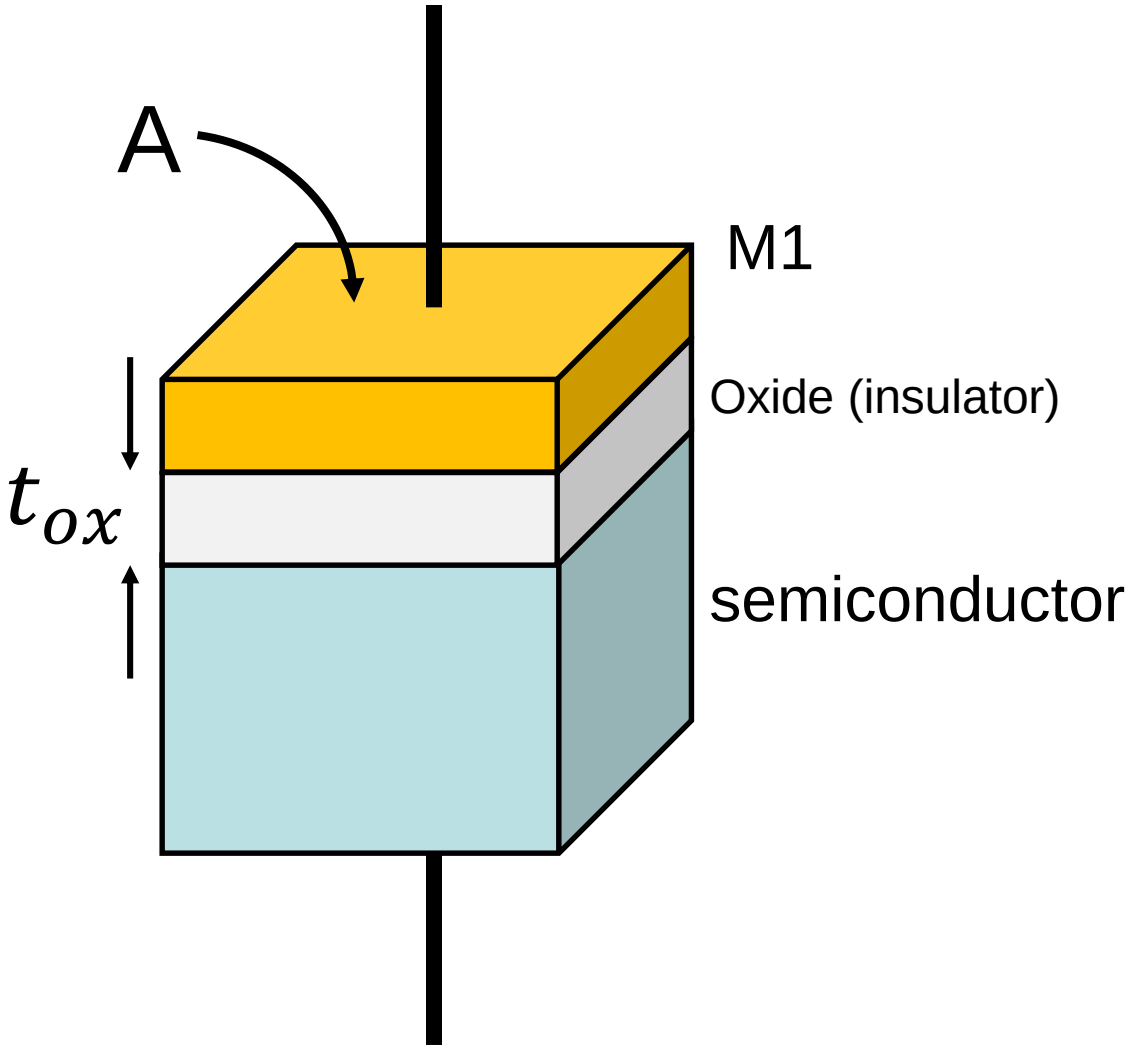


Stored charge

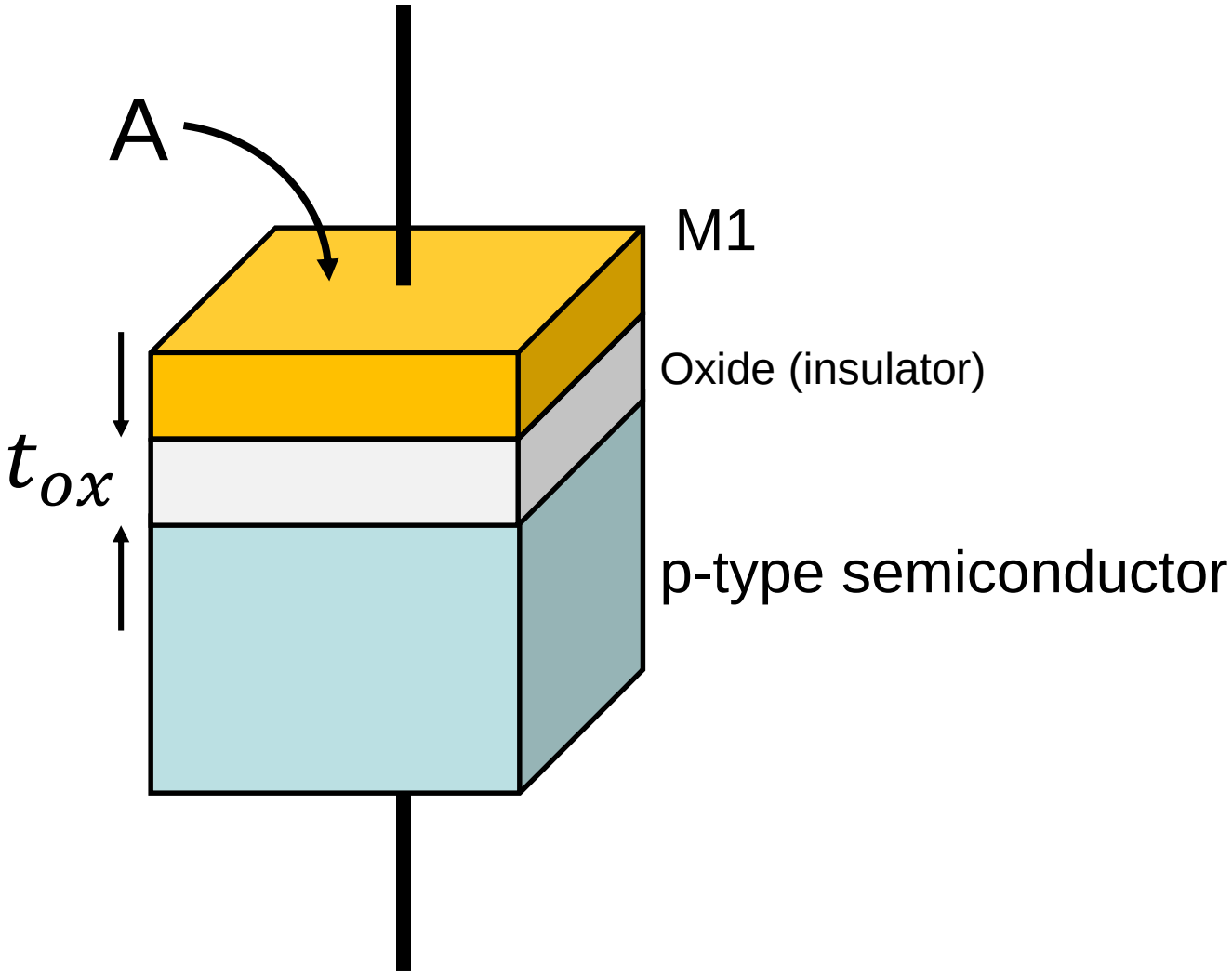
$$Q = CV$$

$$C = \varepsilon_{ox} \frac{A}{t_{ox}}$$

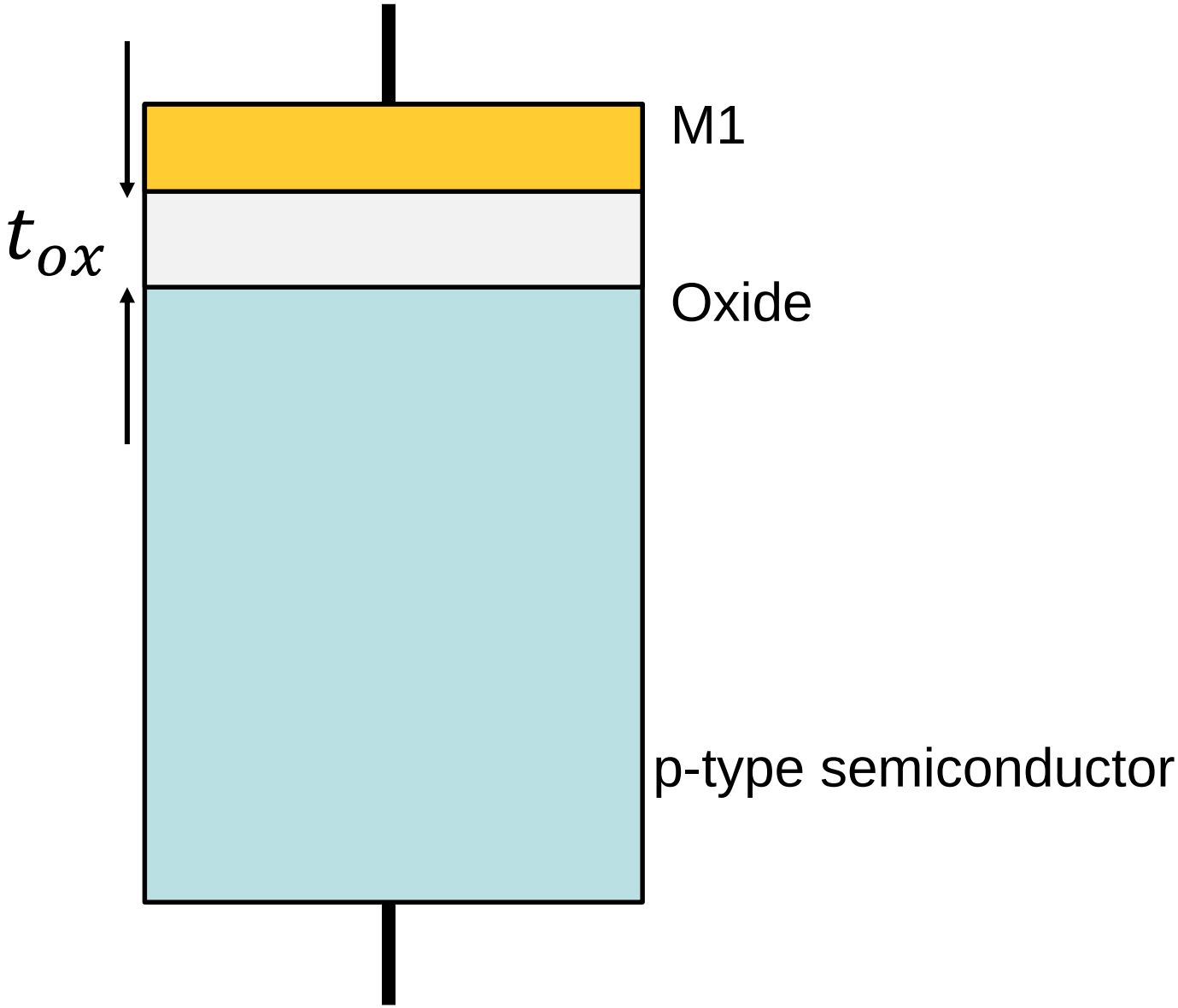
Metal Oxide Semiconductor capacitor



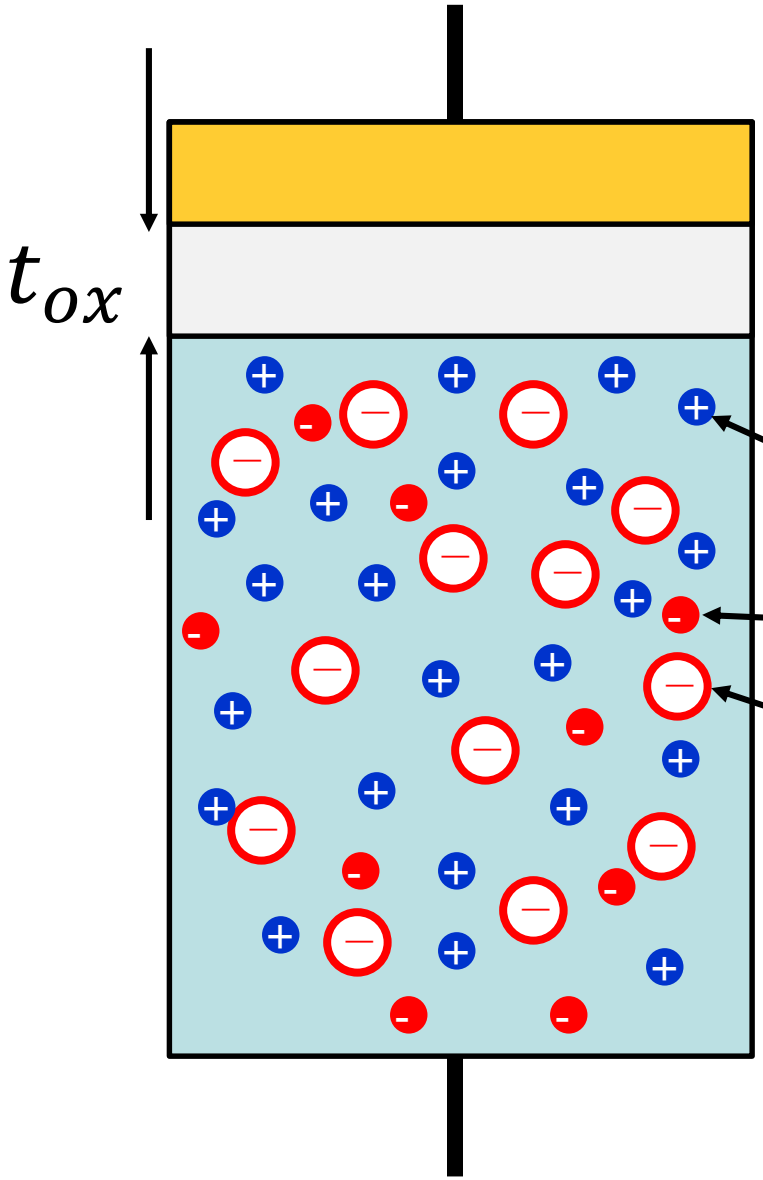
Metal Oxide Semiconductor capacitor



Metal Oxide Semiconductor capacitor



Metal Oxide Semiconductor capacitor

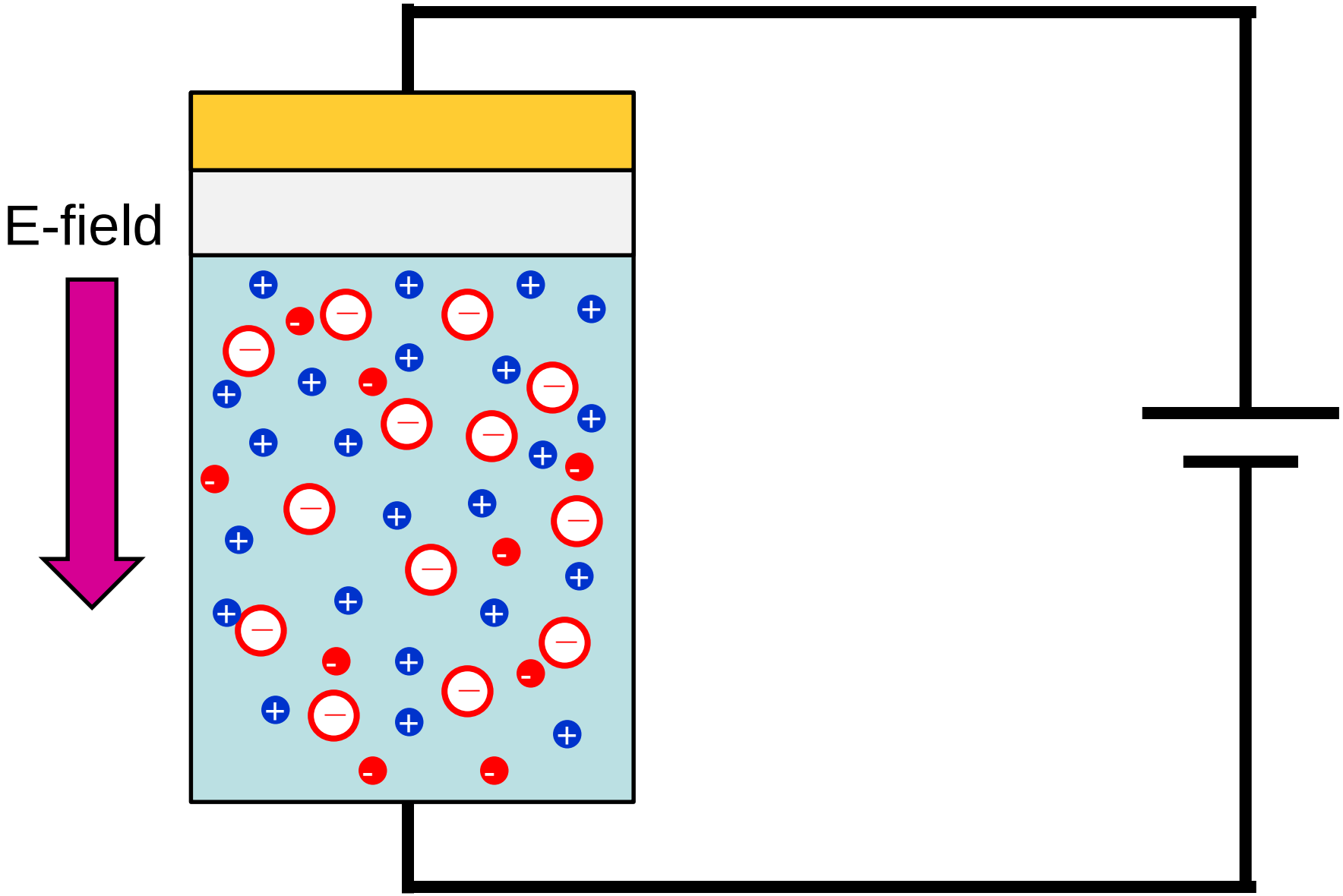


$$p = 10^{15}/cm^3$$

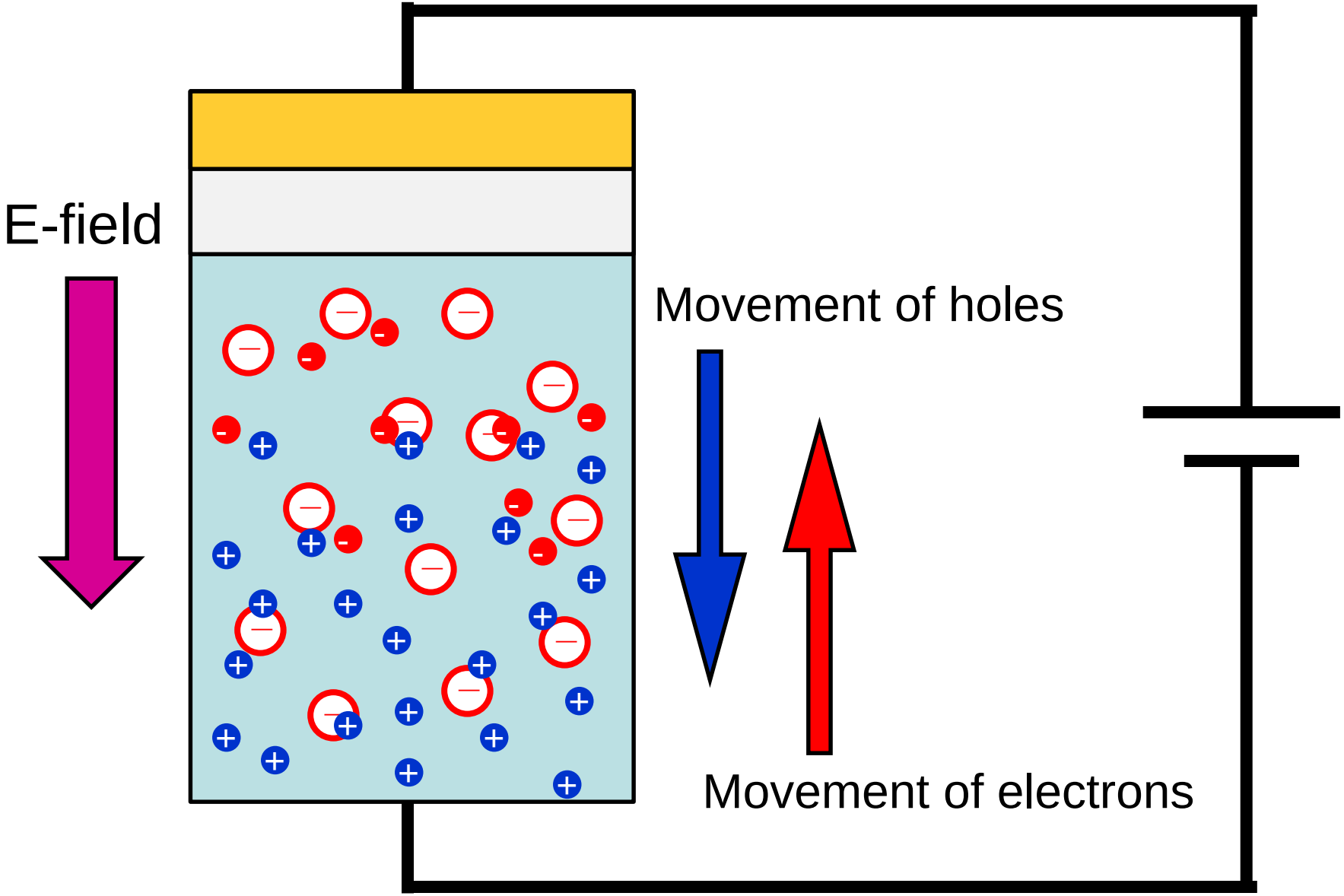
$$n_i = 10^{10}/cm^3$$

$$n = 10^5/cm^3$$

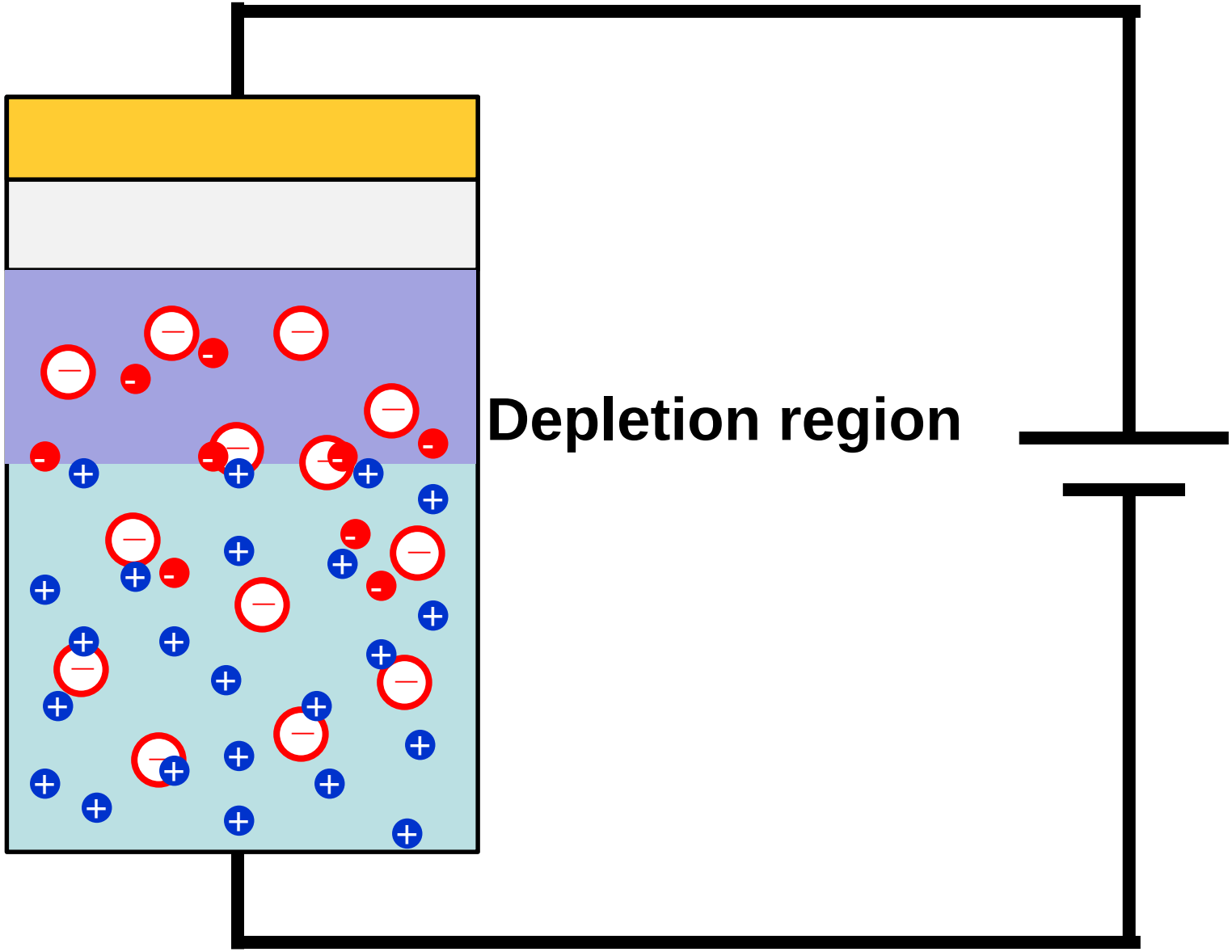
Metal Oxide Semiconductor capacitor



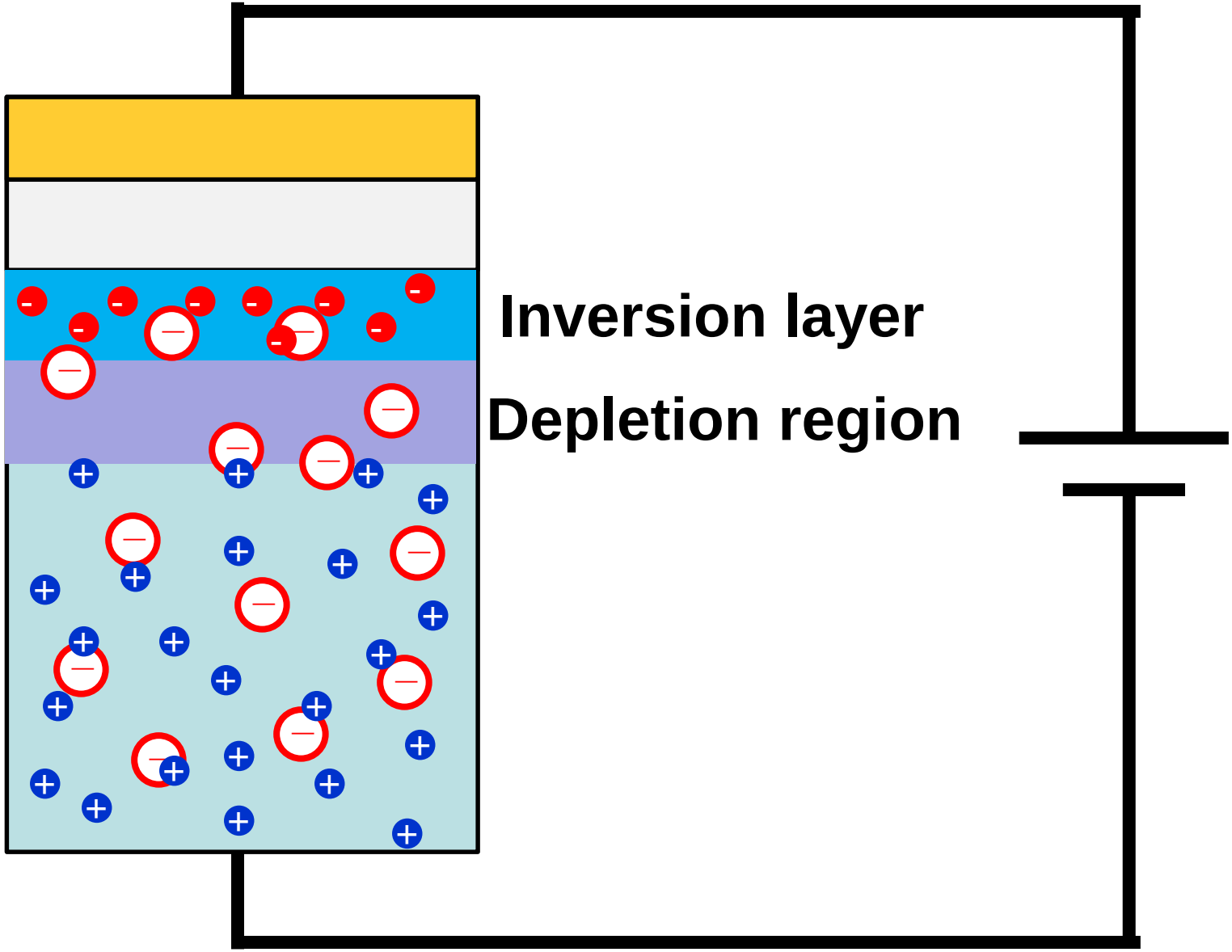
Metal Oxide Semiconductor capacitor



Metal Oxide Semiconductor capacitor



Metal Oxide Semiconductor capacitor

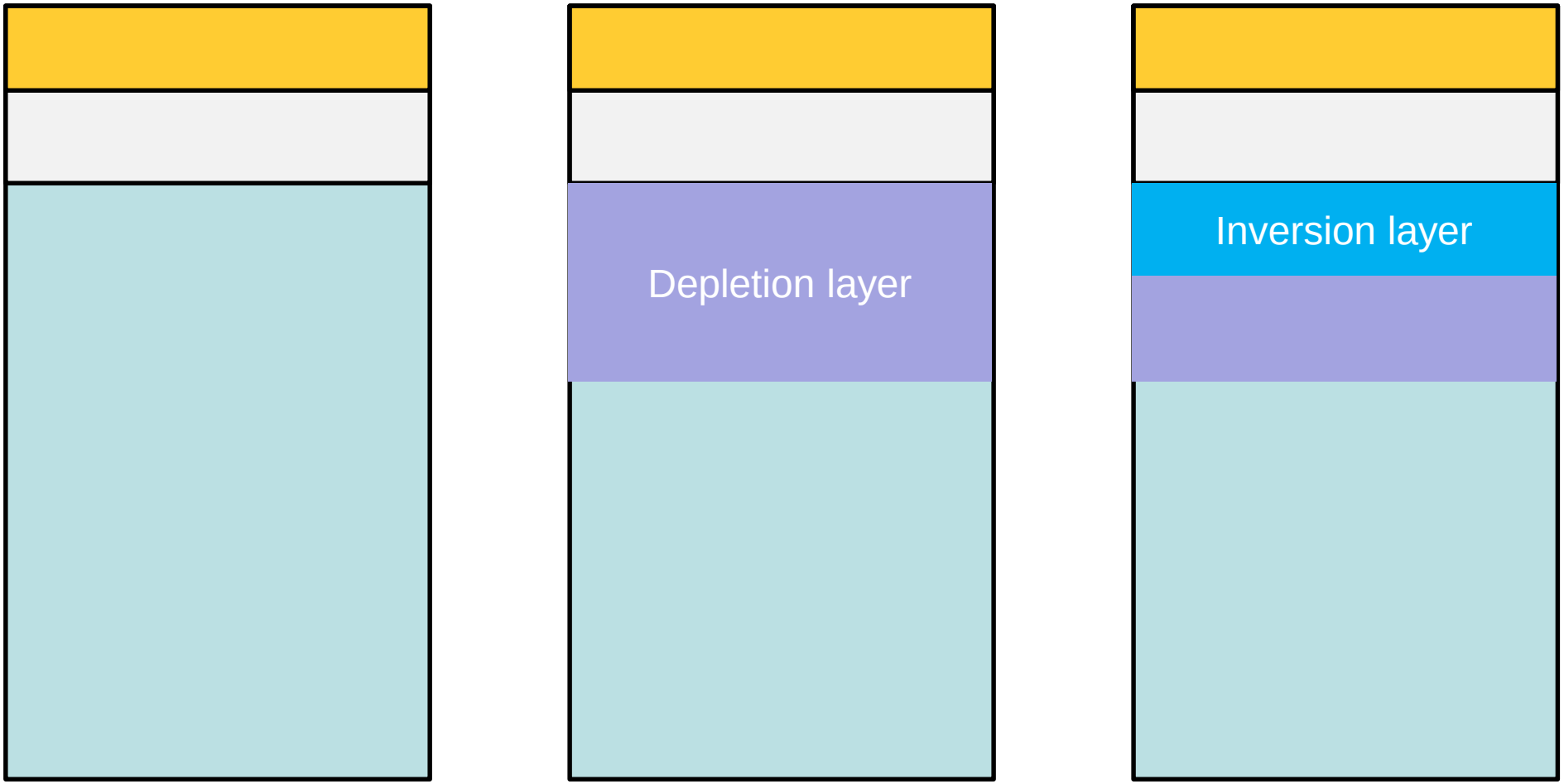


Metal Oxide Semiconductor capacitor

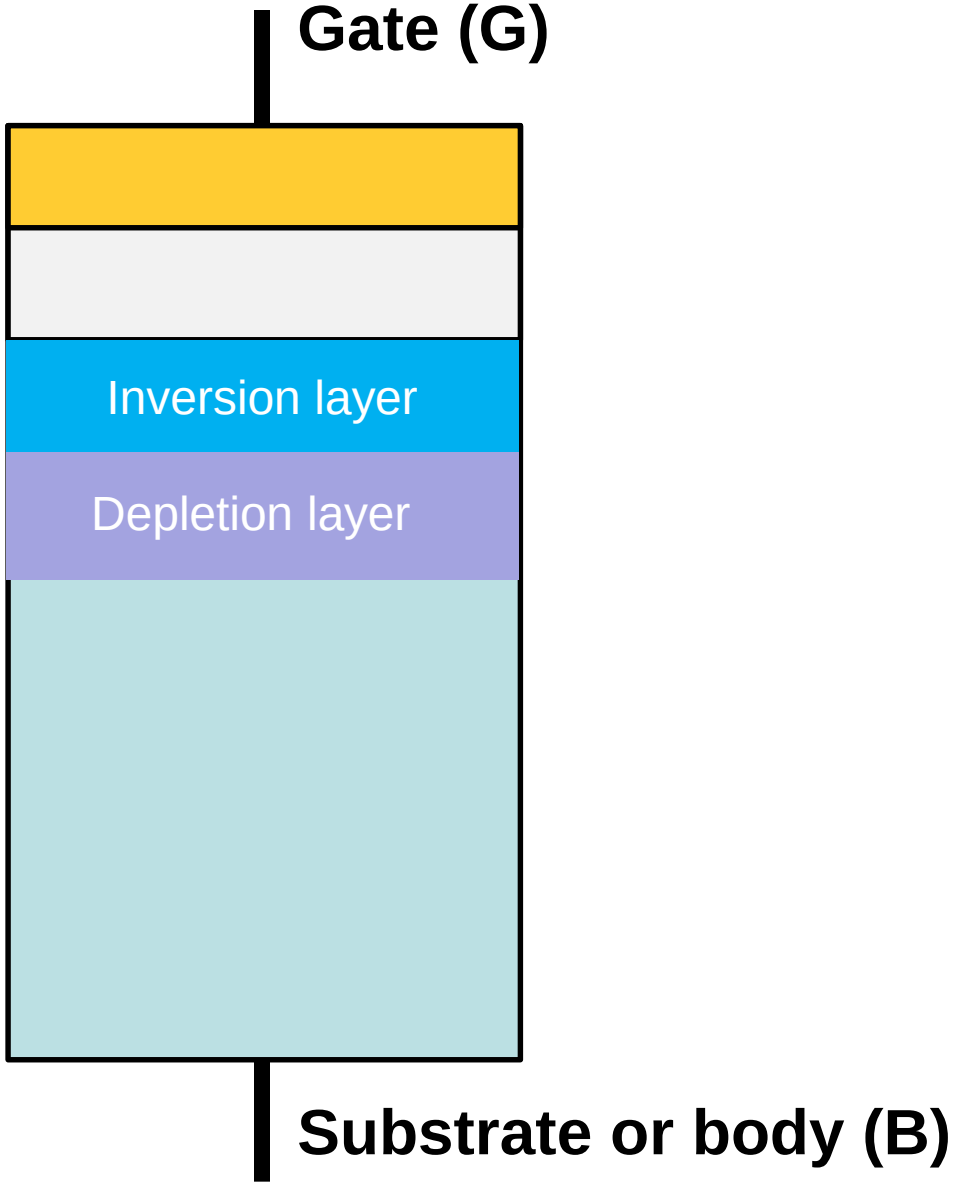
No applied voltage

With applied voltage

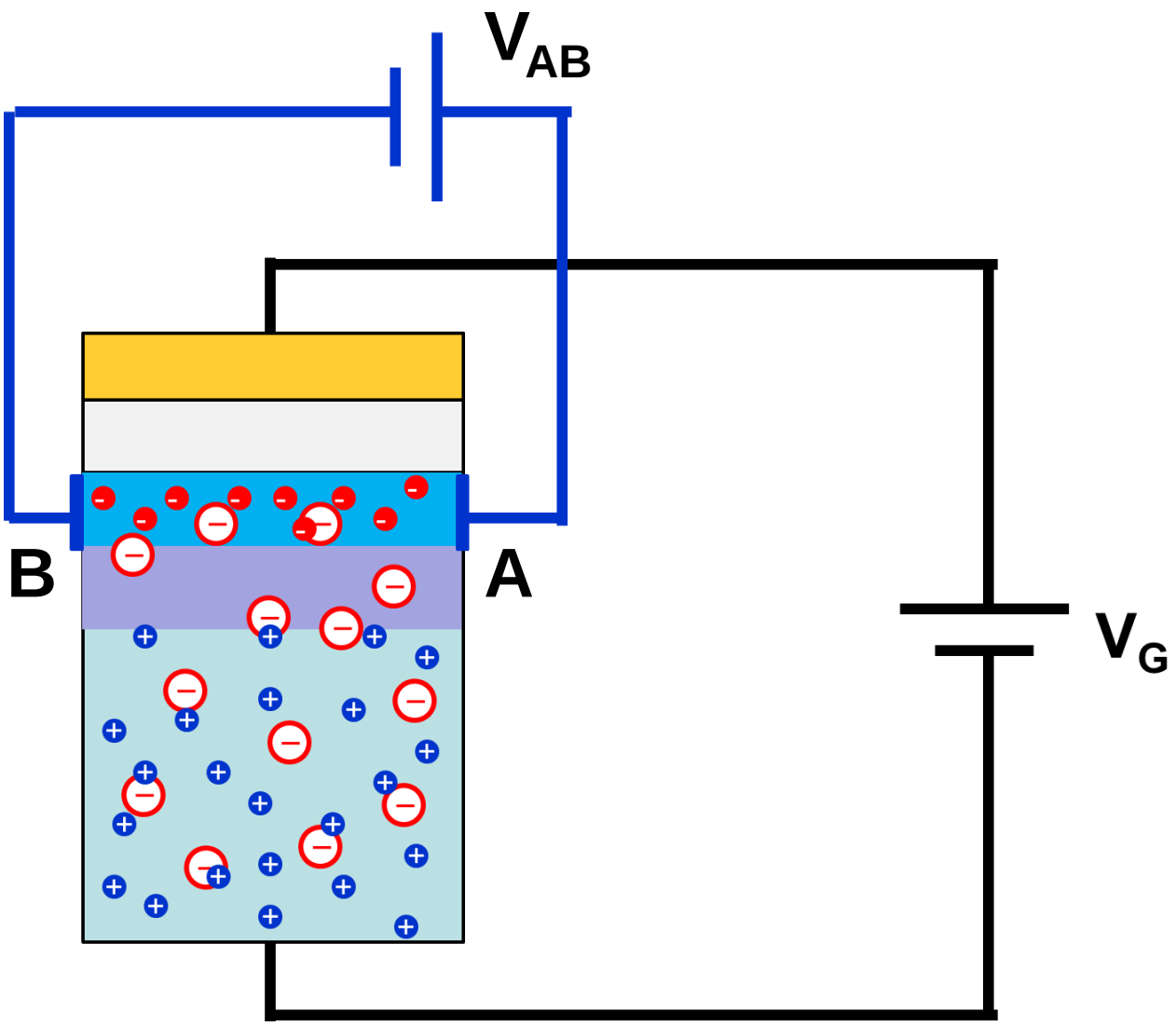
Increased applied voltage



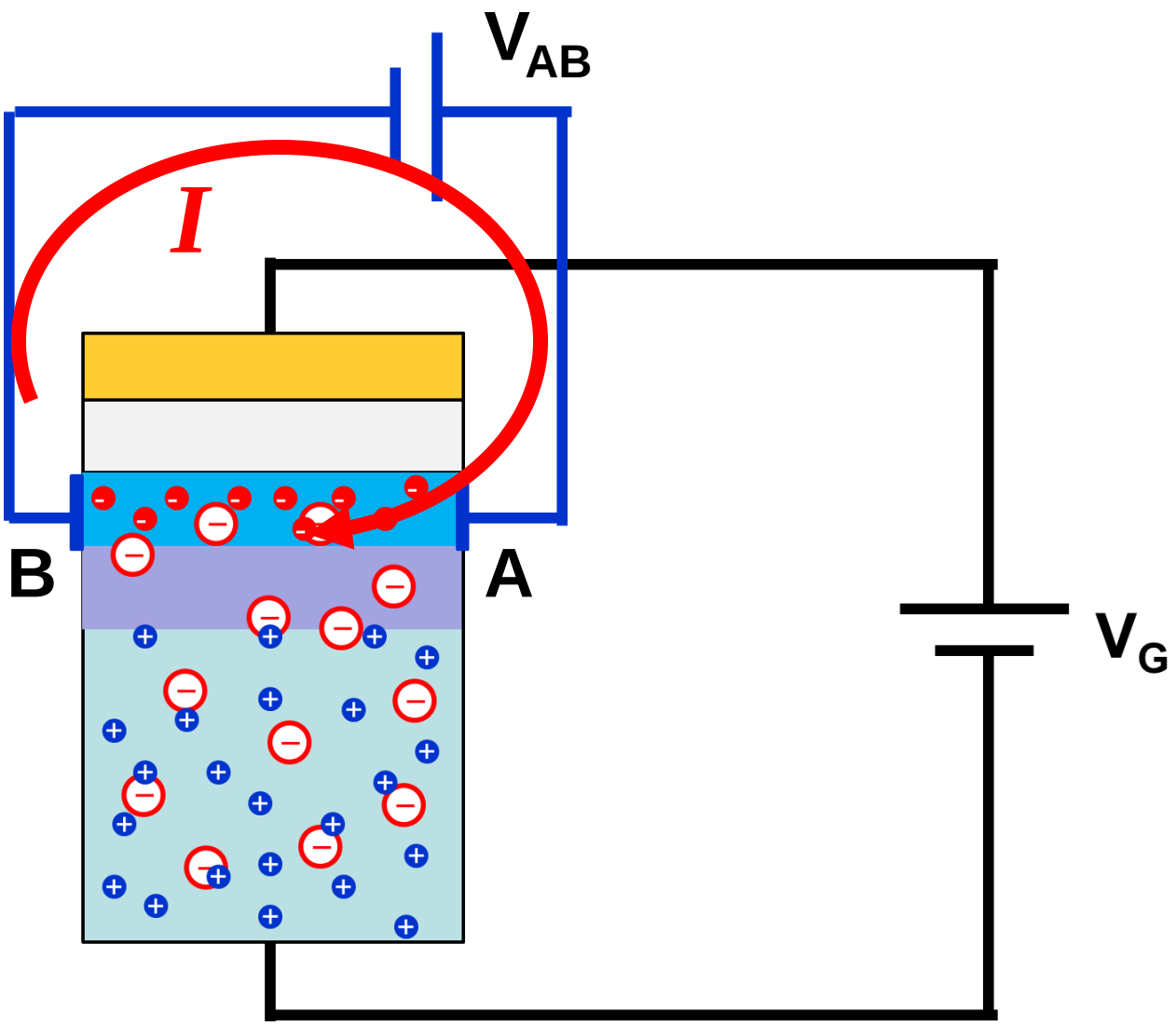
Metal Oxide Semiconductor capacitor



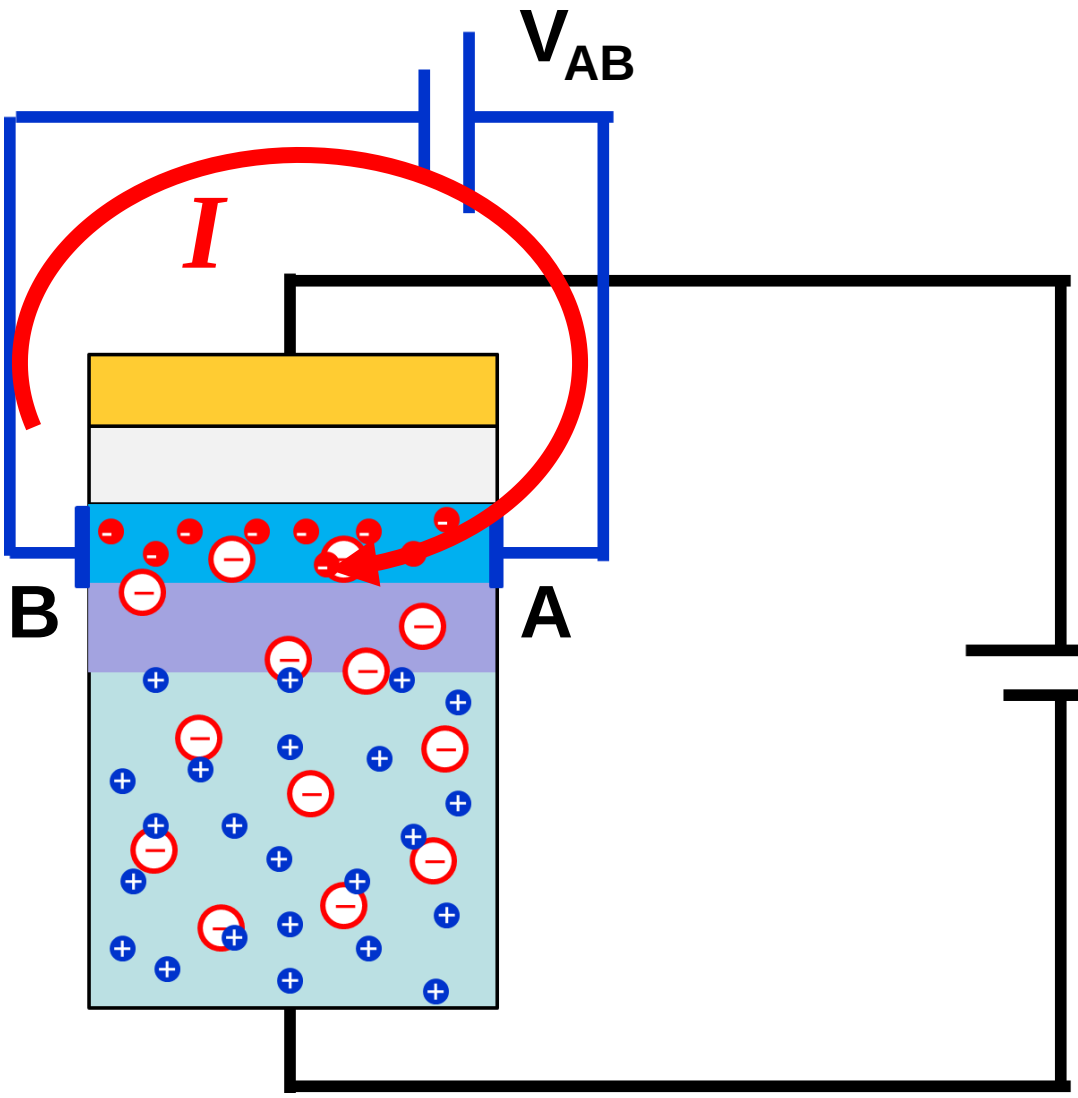
Metal Oxide Semiconductor capacitor



Metal Oxide Semiconductor capacitor

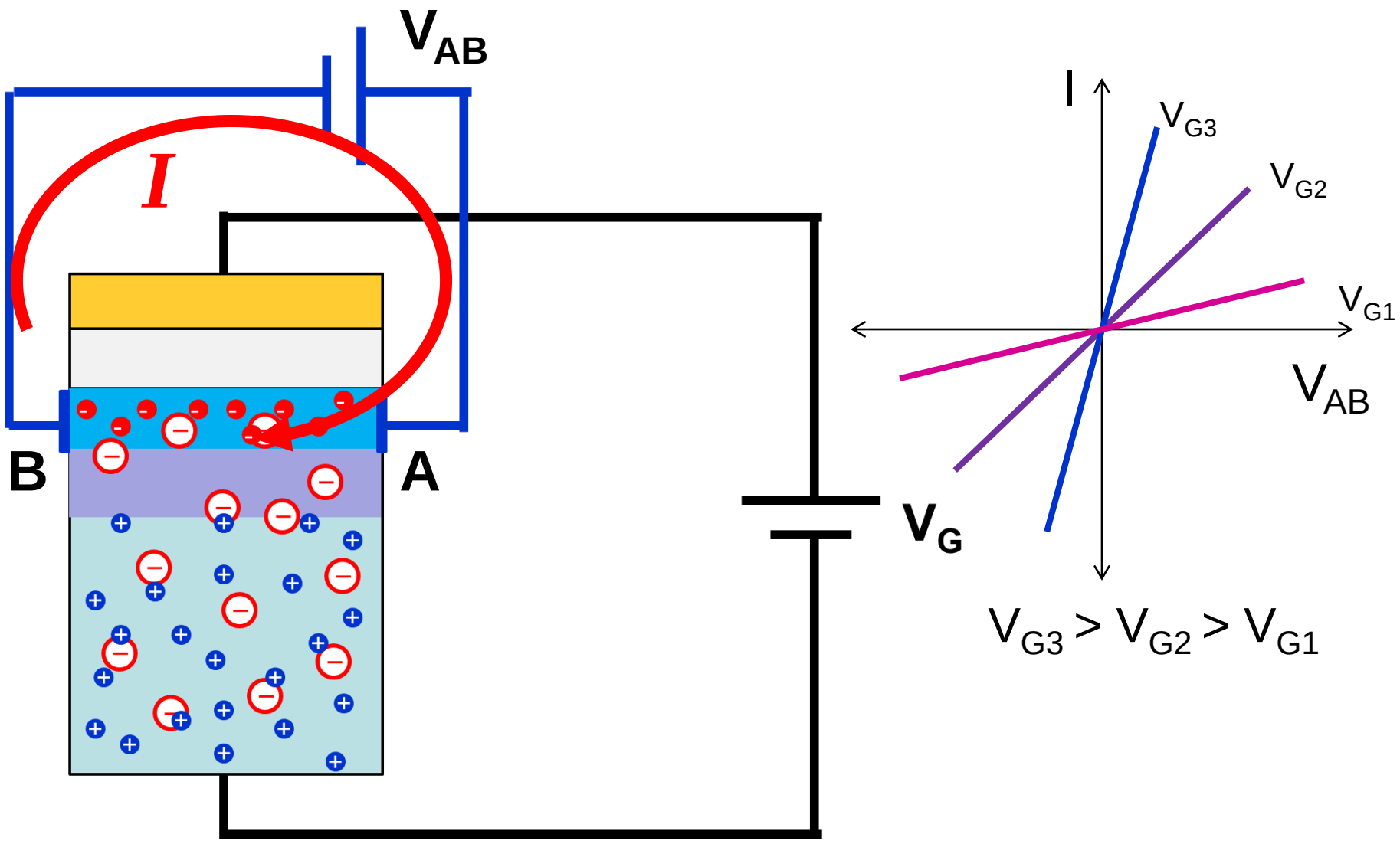


Metal Oxide Semiconductor capacitor

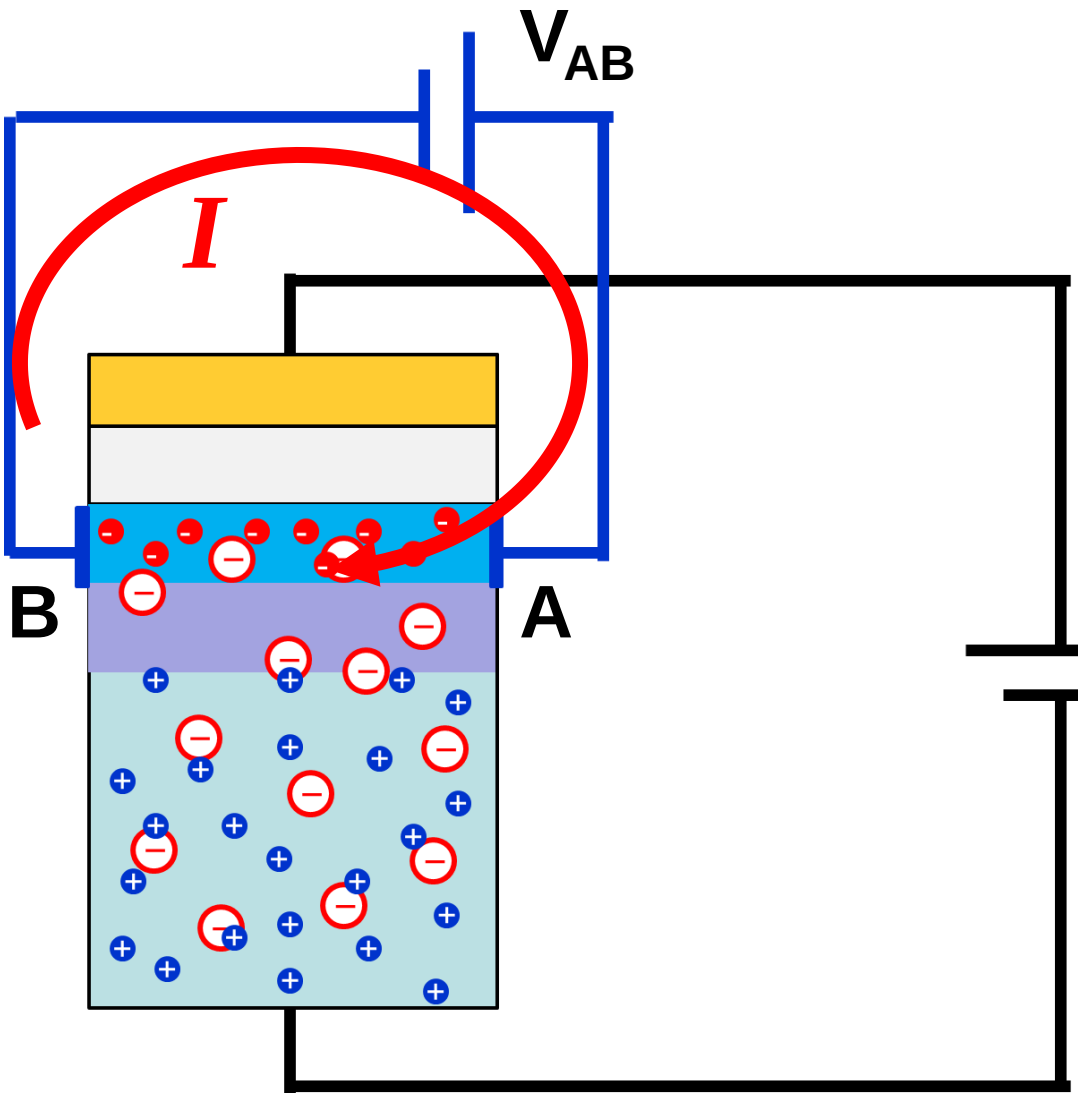


$$V_G \uparrow \quad n \uparrow \quad I \uparrow$$

Metal Oxide Semiconductor capacitor

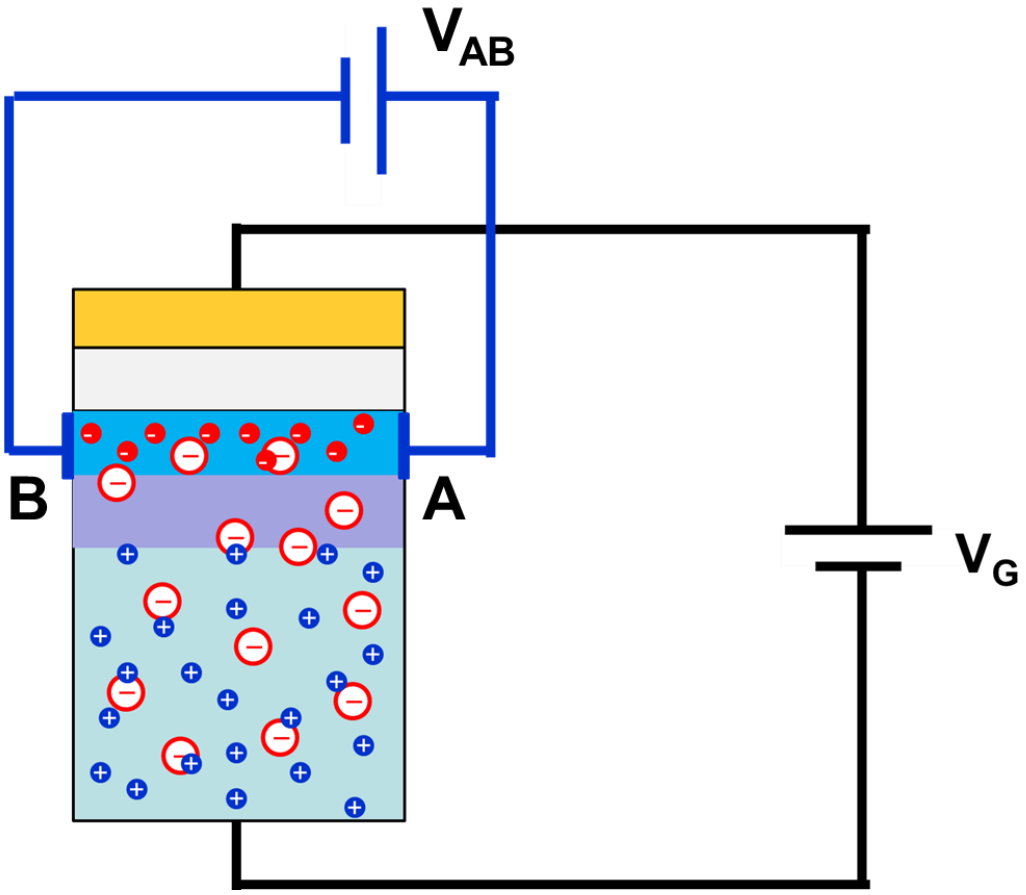


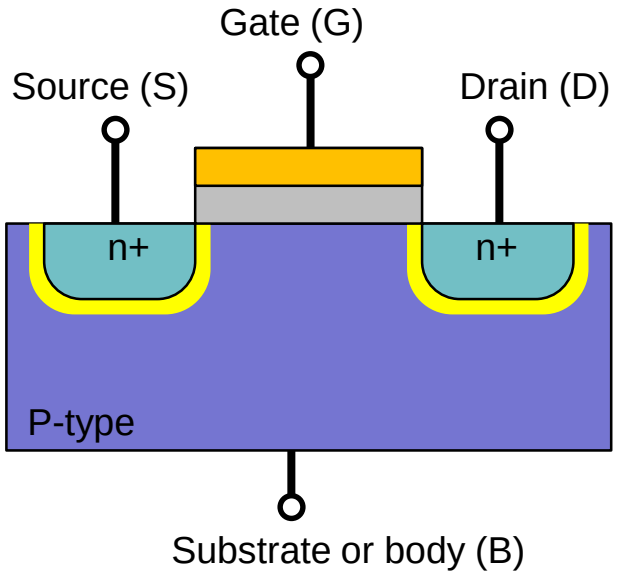
Metal Oxide Semiconductor capacitor



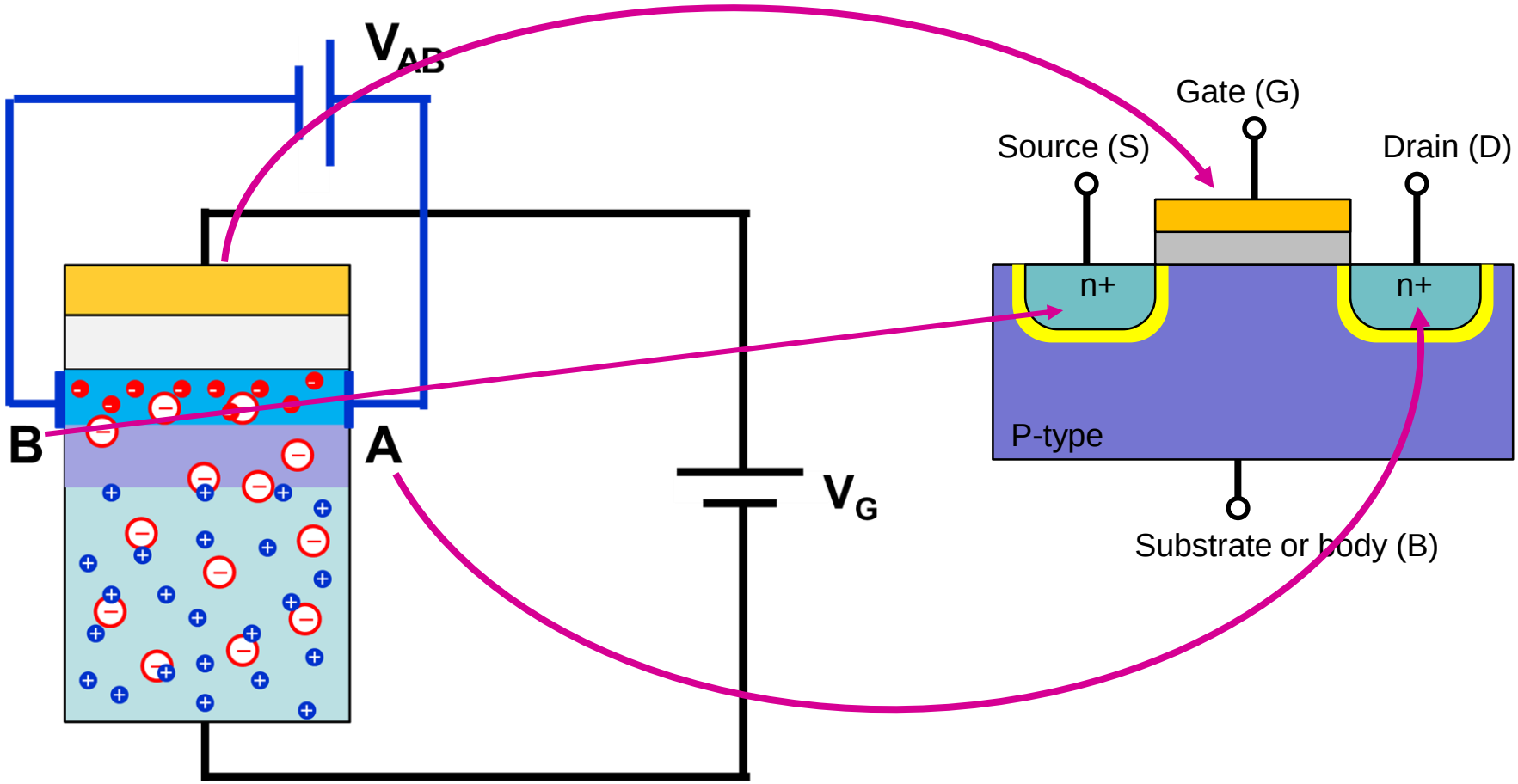
Variable resistance

MOS Field Effect Transistor



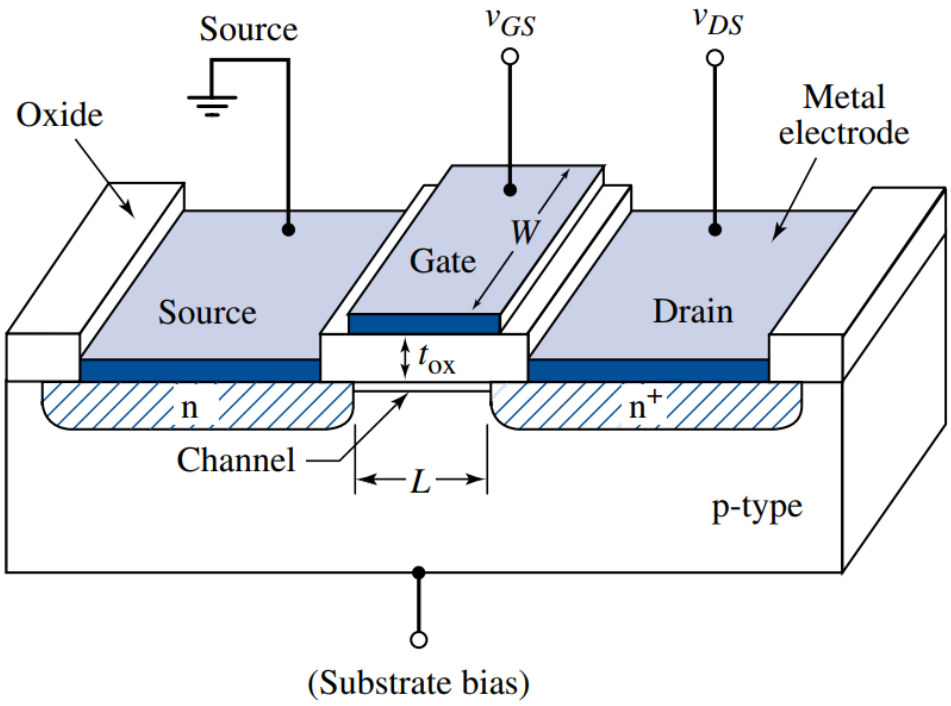


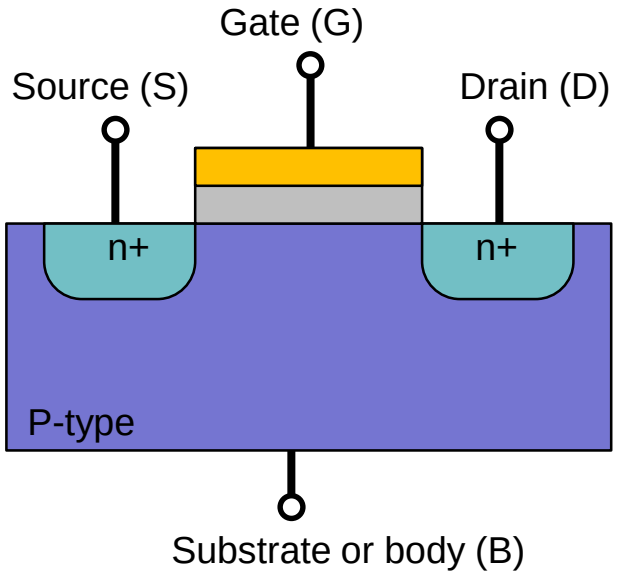
MOS Field Effect Transistor



4 terminal device

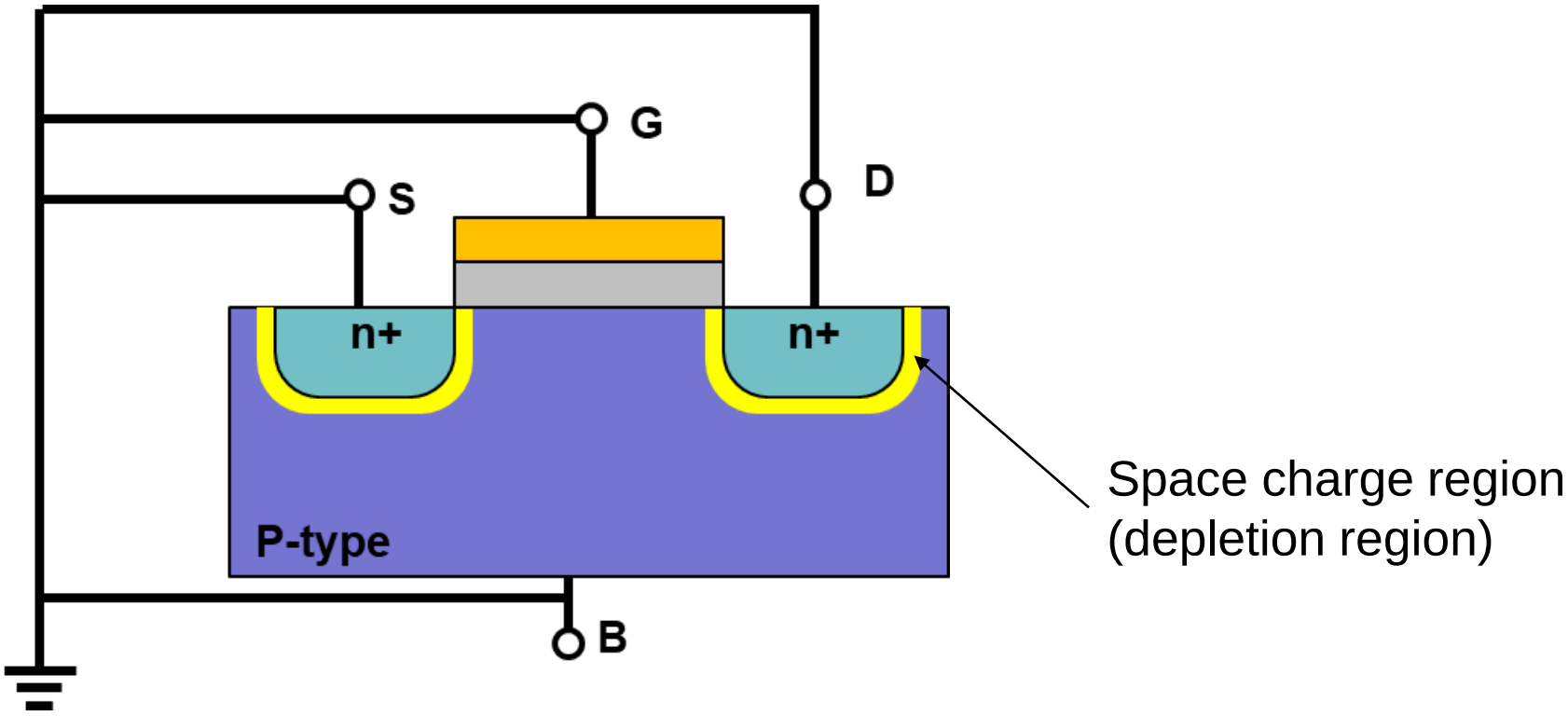
MOS Field Effect Transistor



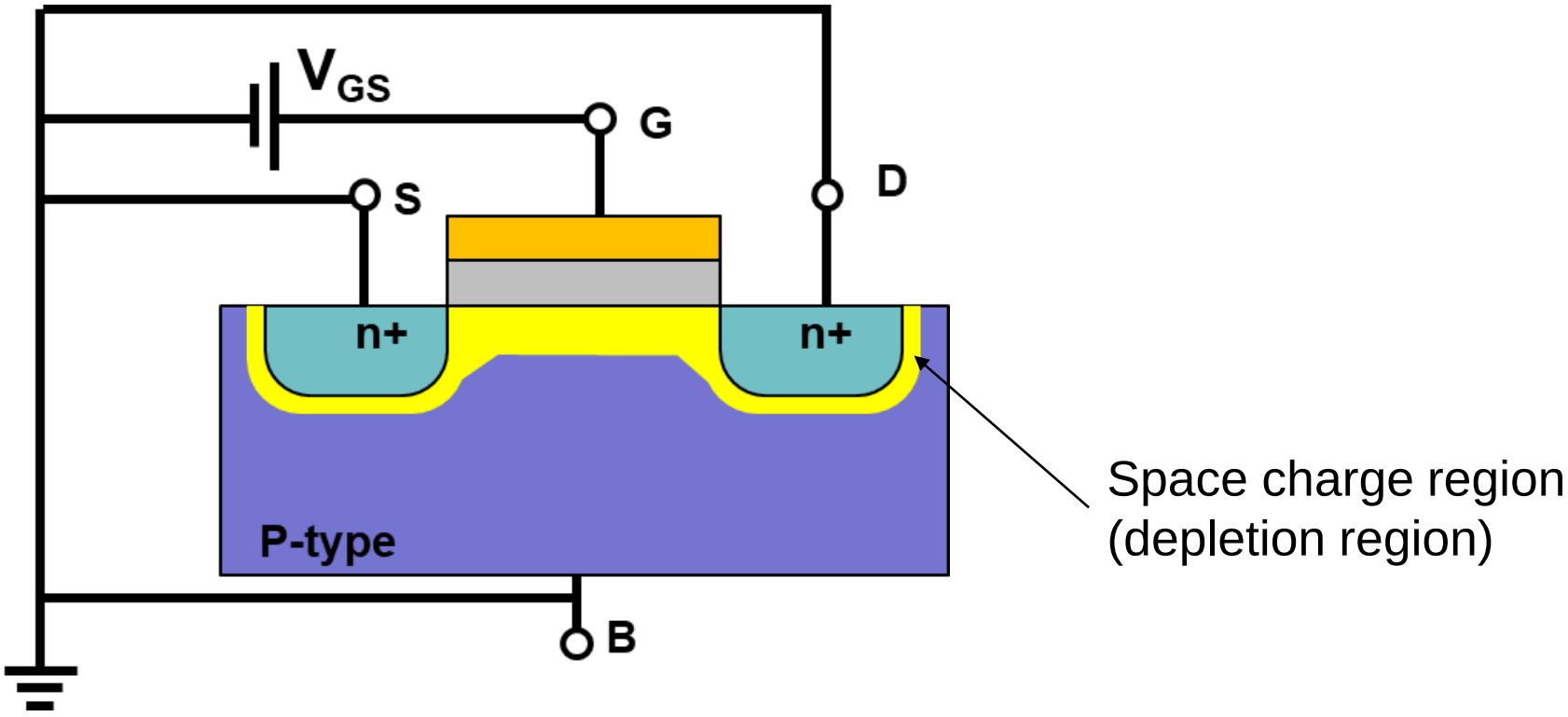


- Channel length, $L \sim 1$ μm
- Oxide length, $t_{ox} \sim 400$ Angstrom

n-MOSFET basic transistor operation

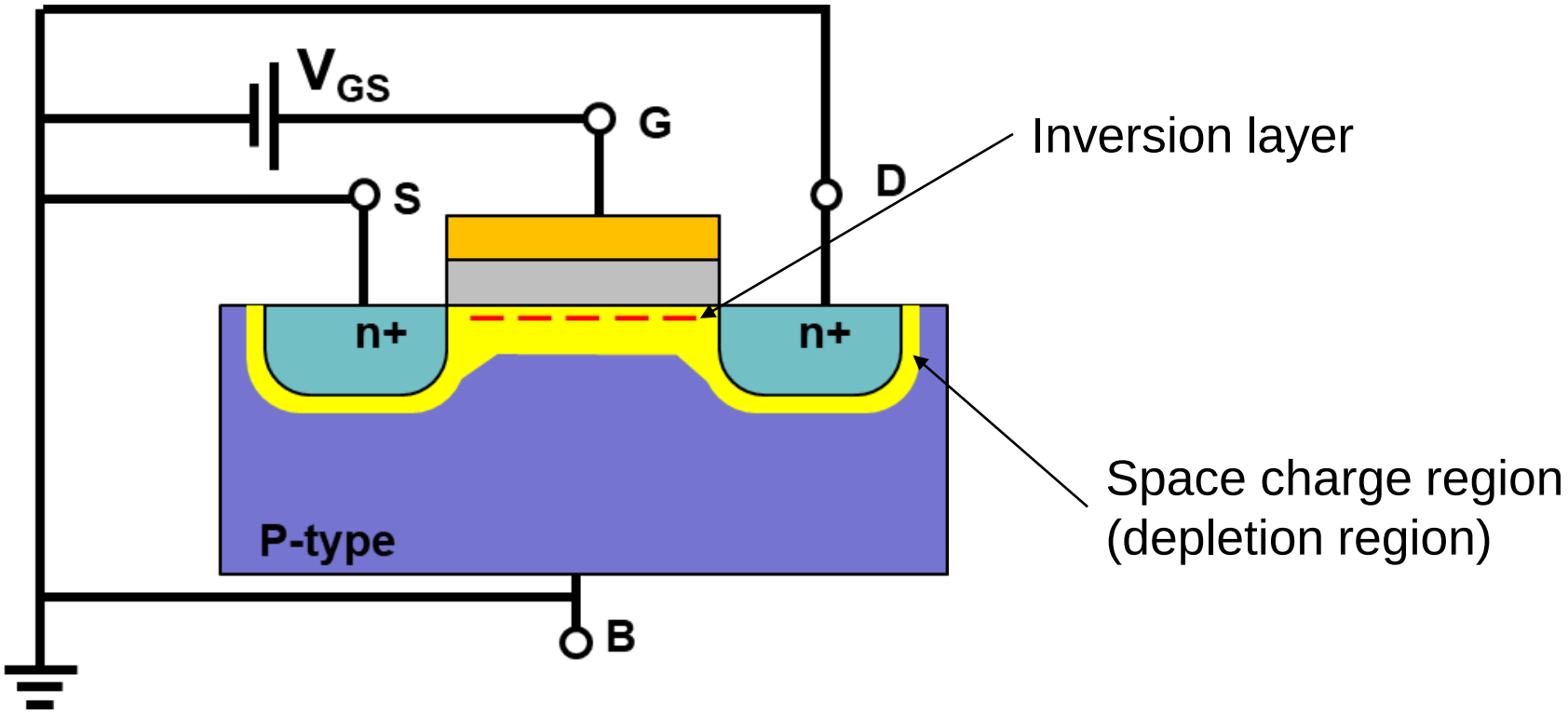


n-MOSFET basic transistor operation



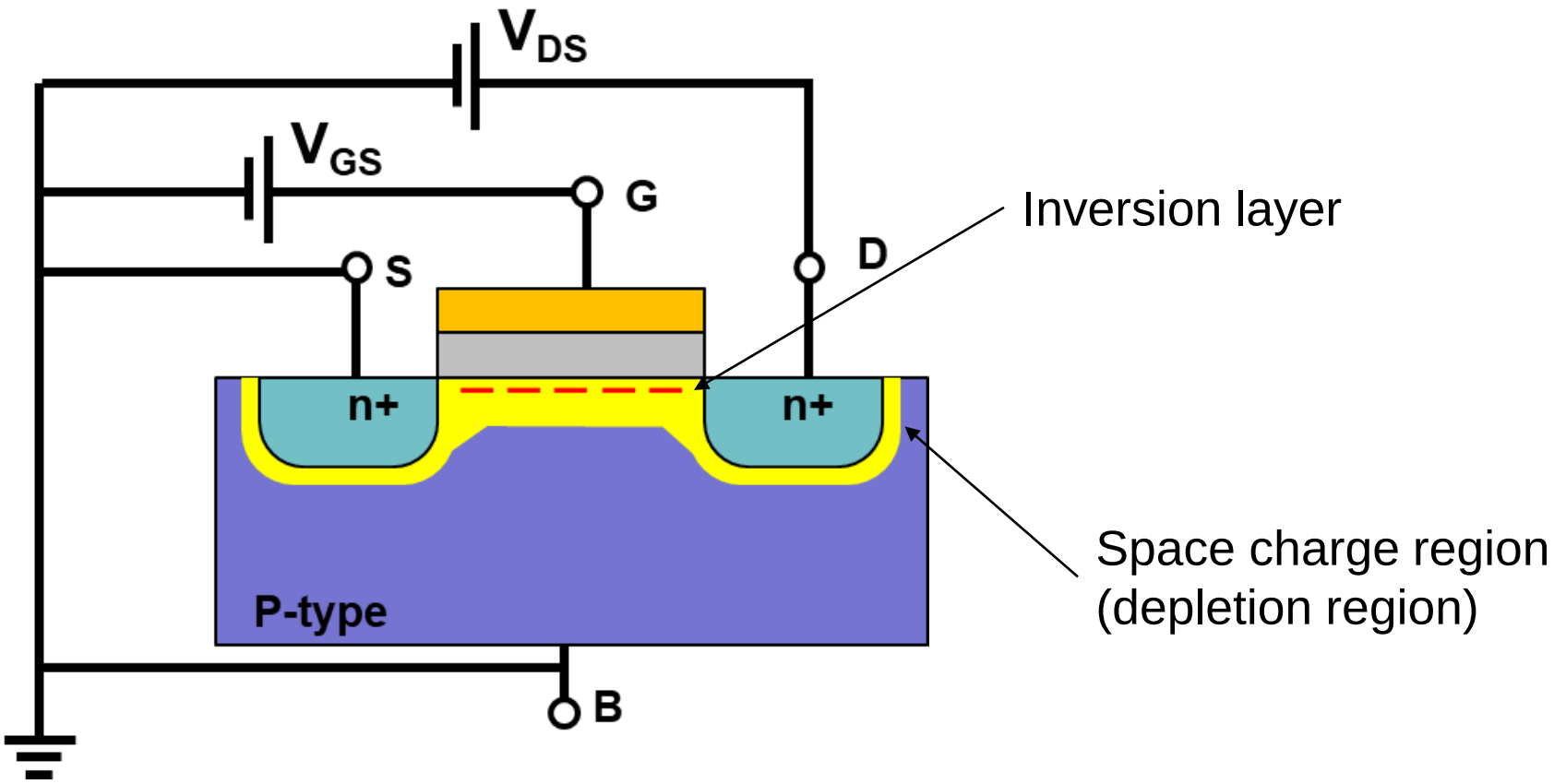
$$V_{GS} < V_{TN}$$

n-MOSFET basic transistor operation

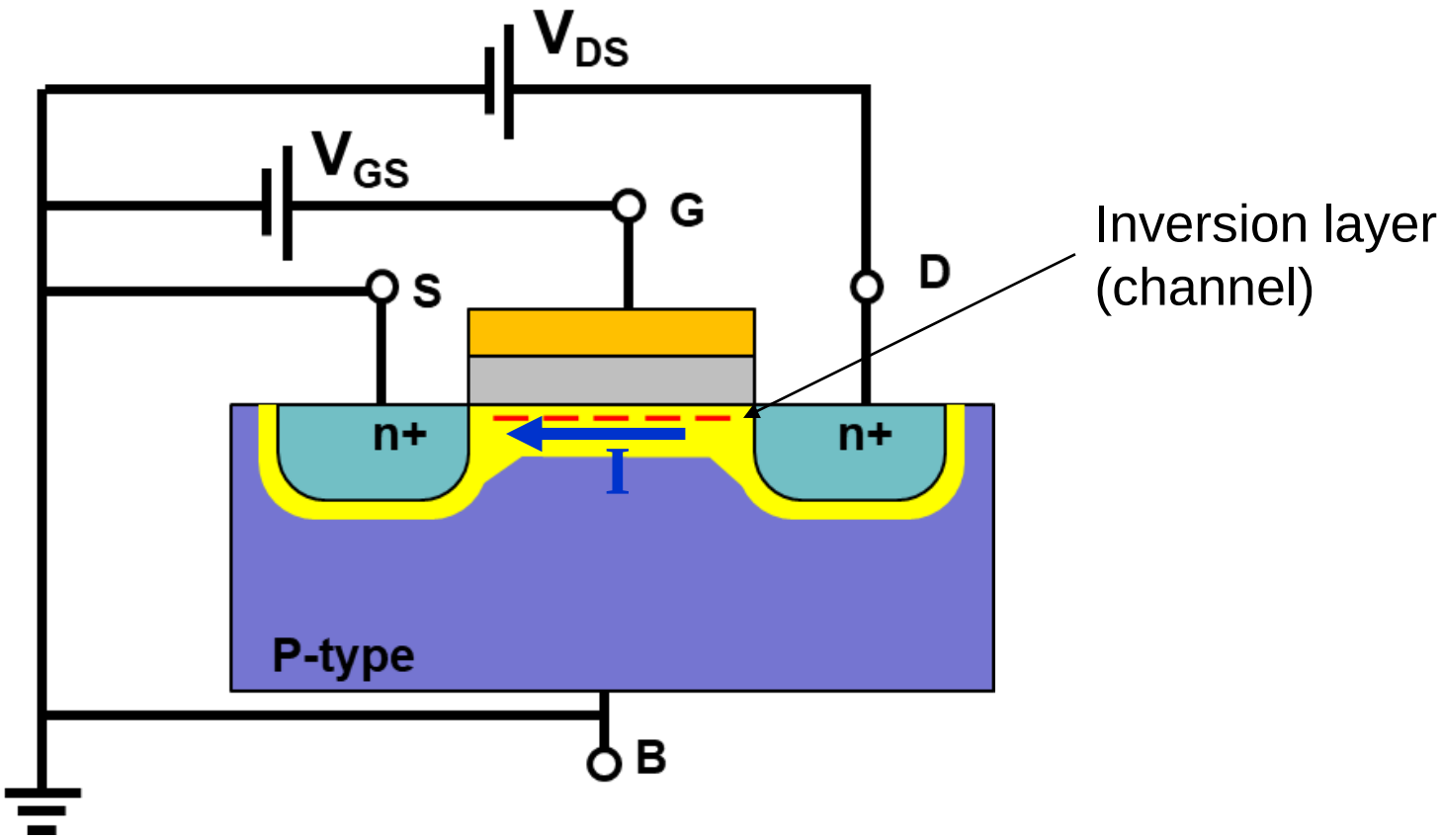


$V_{GS} > V_{TN}$ ← Threshold voltage

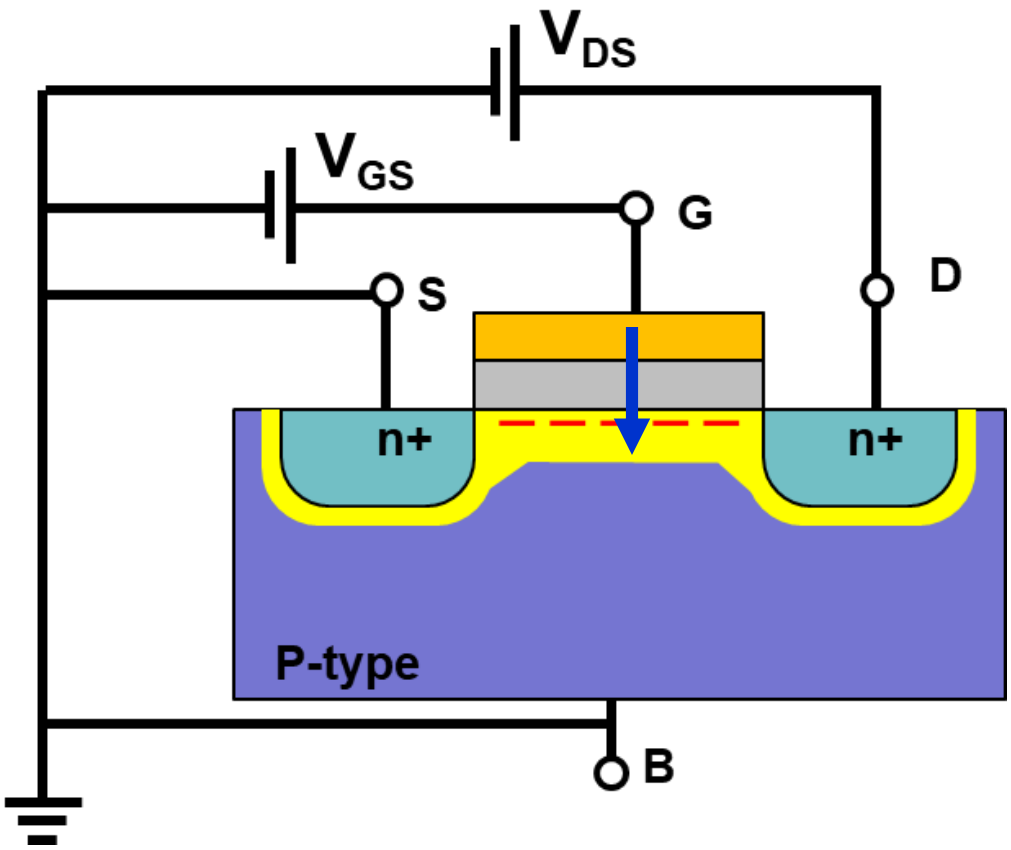
n-MOSFET basic transistor operation



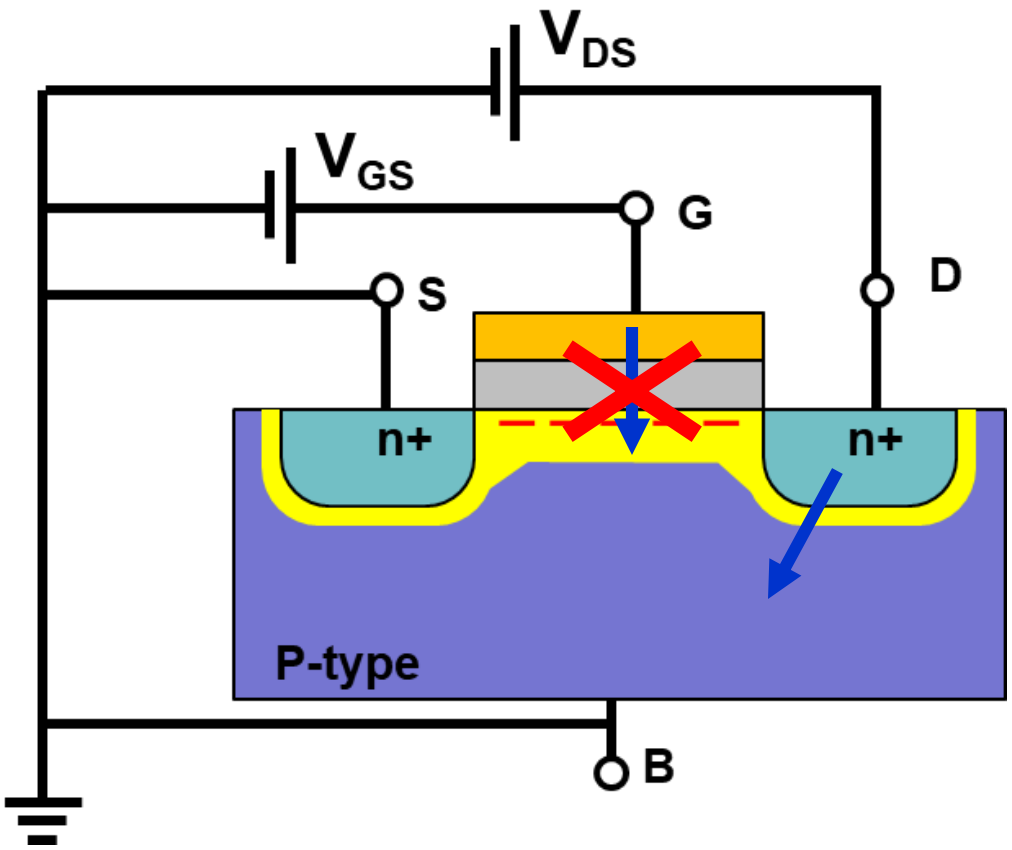
n-MOSFET basic transistor operation



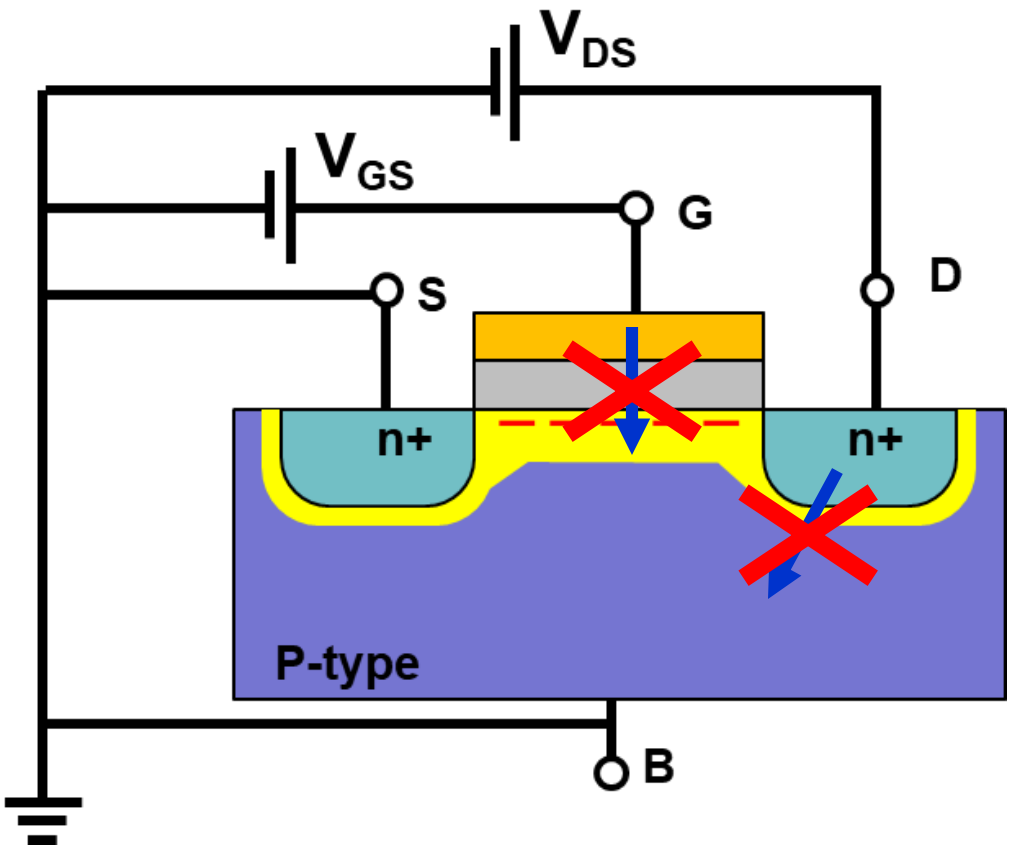
n-MOSFET basic transistor operation



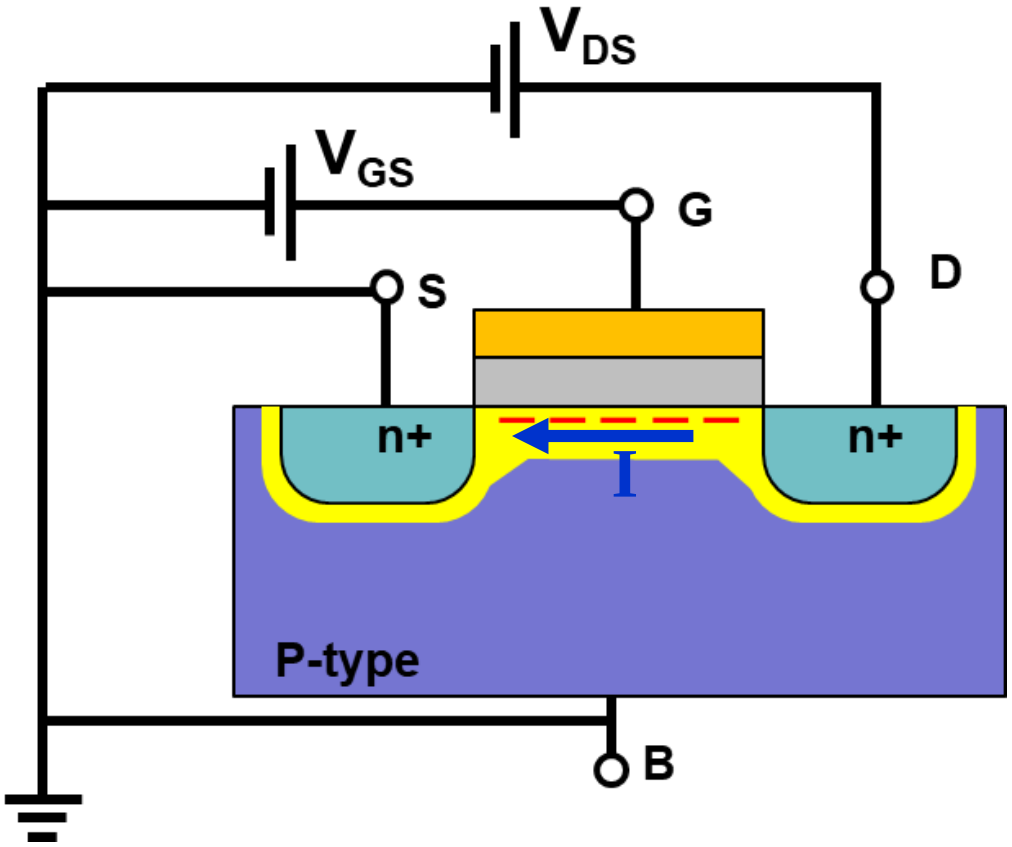
n-MOSFET basic transistor operation



n-MOSFET basic transistor operation



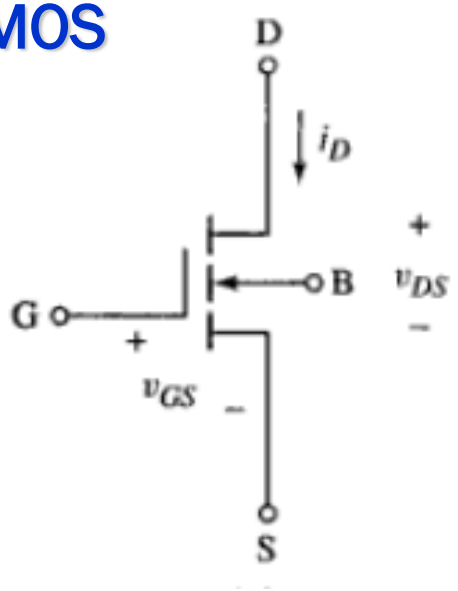
n-MOSFET basic transistor operation

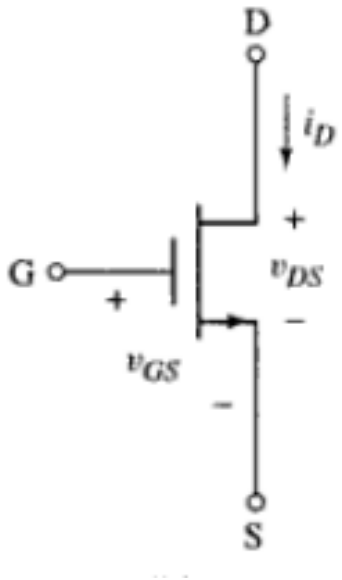


- Only allowed path is through the channel
- Since the channel is formed by electrons, its called an **n-channel MOSFET or NMOS**

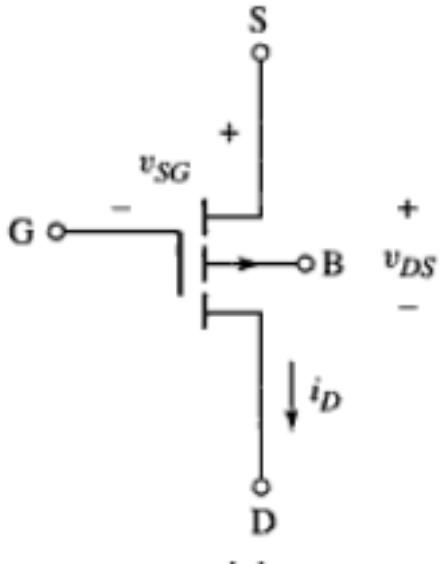
Symbols

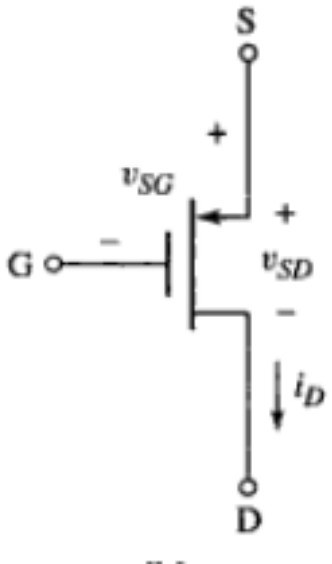
NMOS



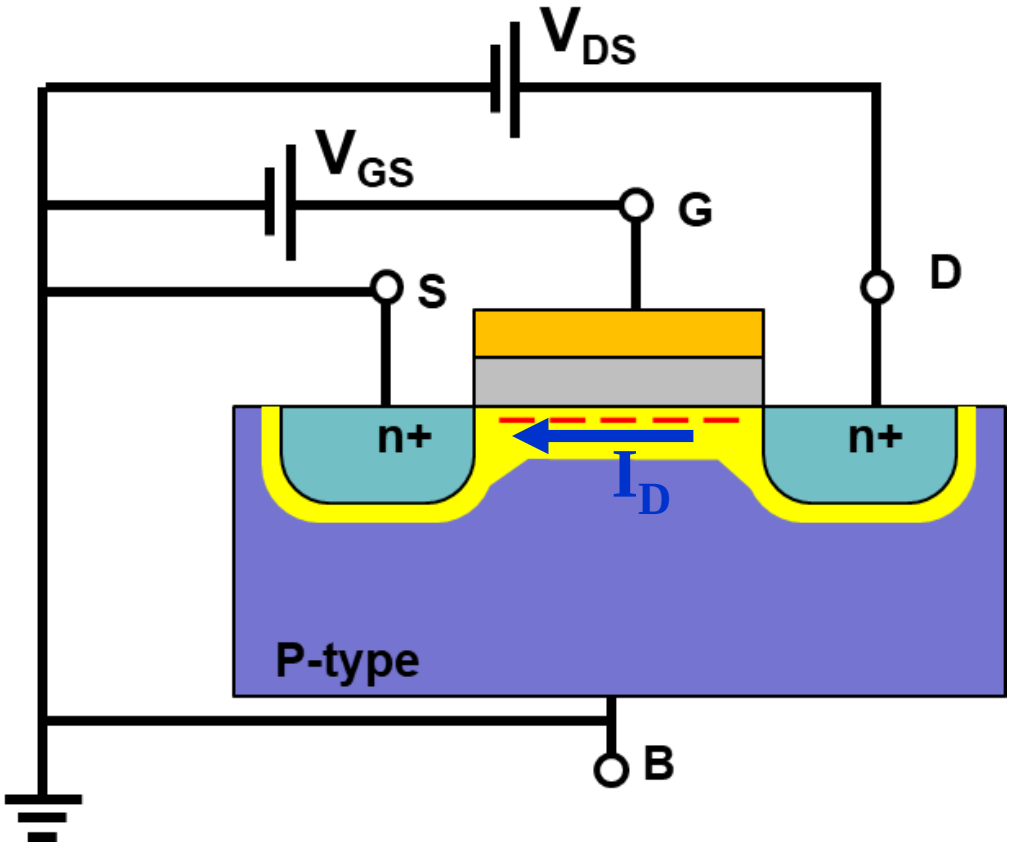


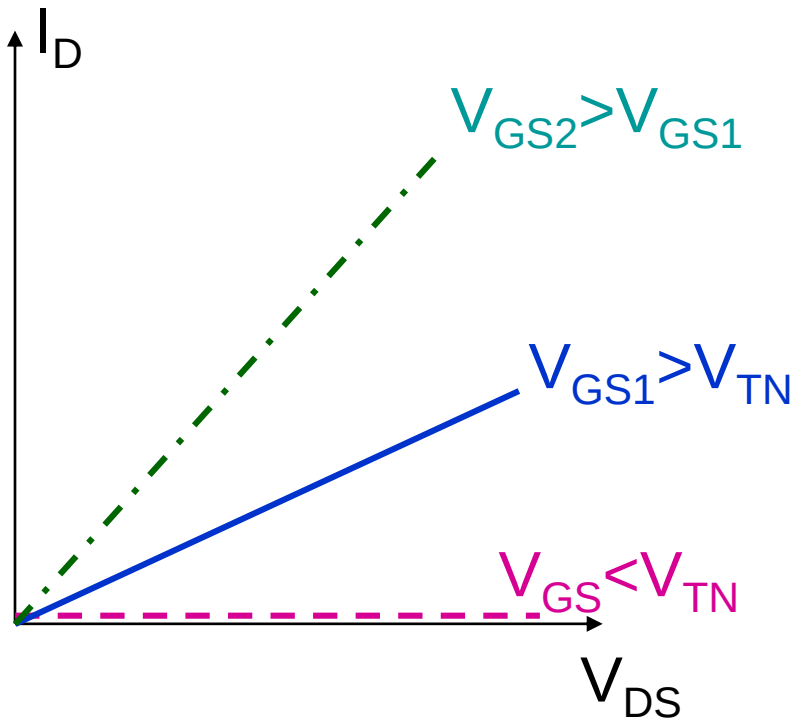
PMOS





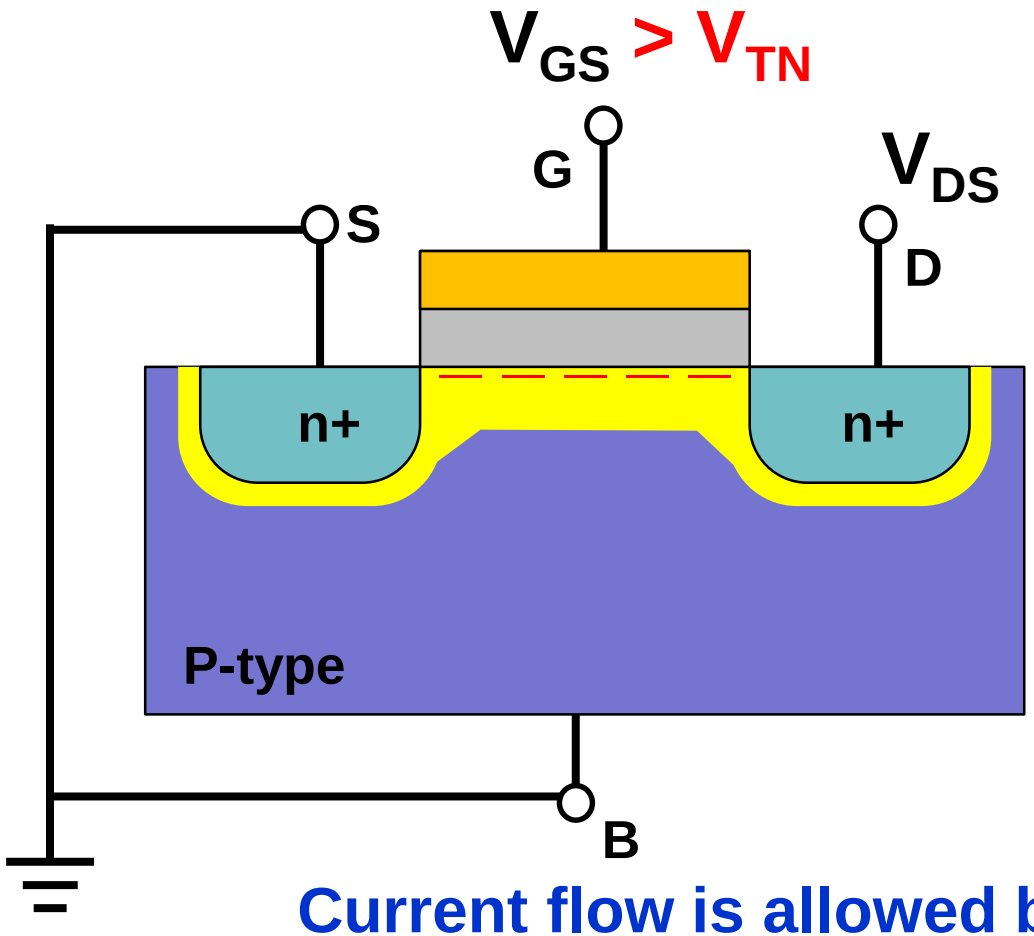
n-MOSFET basic transistor operation





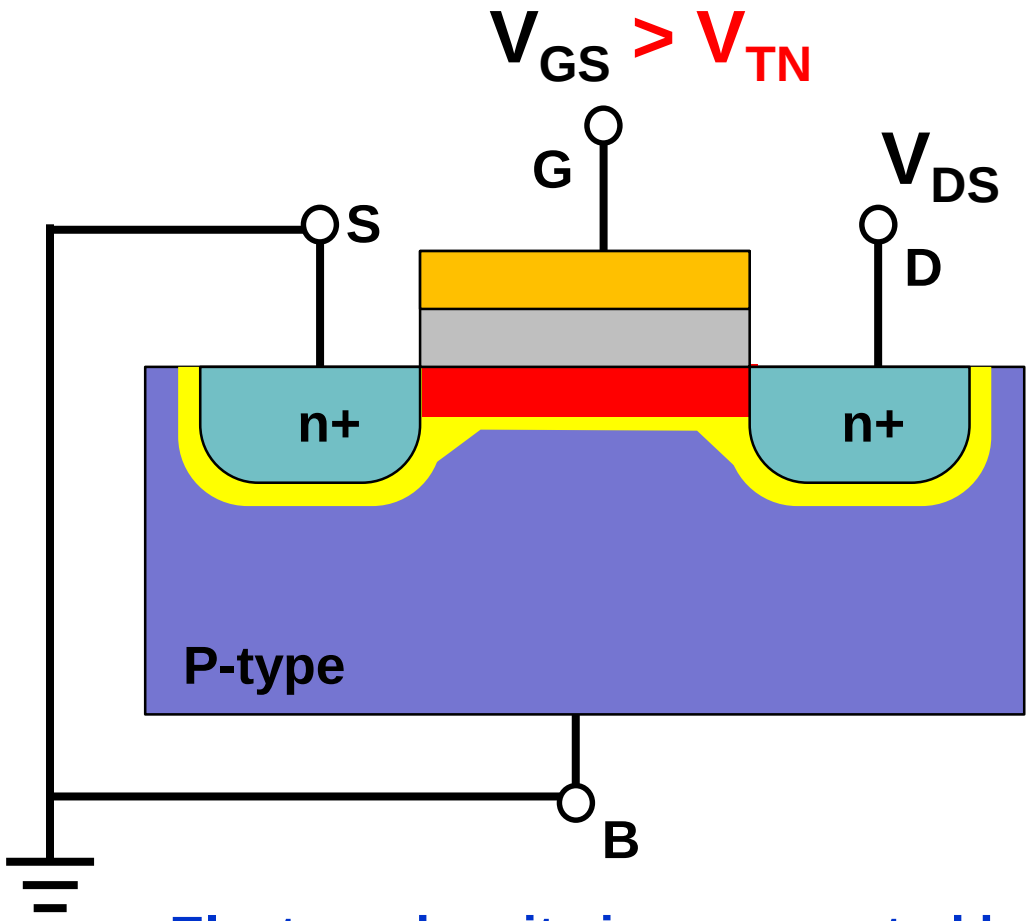
For very small values of V_{DS}

n-MOSFET IV characteristics



Current flow is allowed between drain and source

n-MOSFET IV characteristics

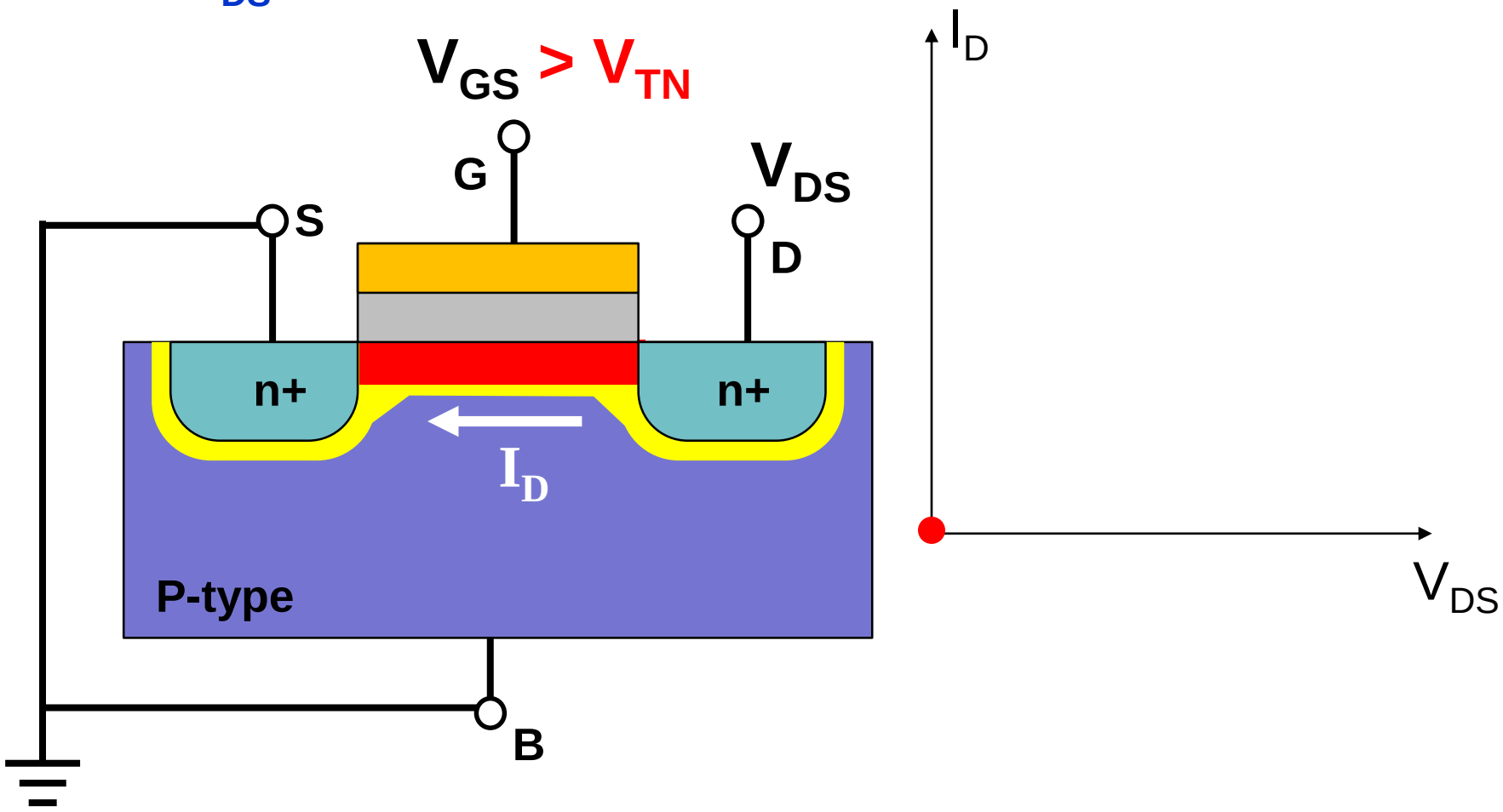


Electron density is represented by the width of the red region

n-MOSFET IV characteristics

Case 1

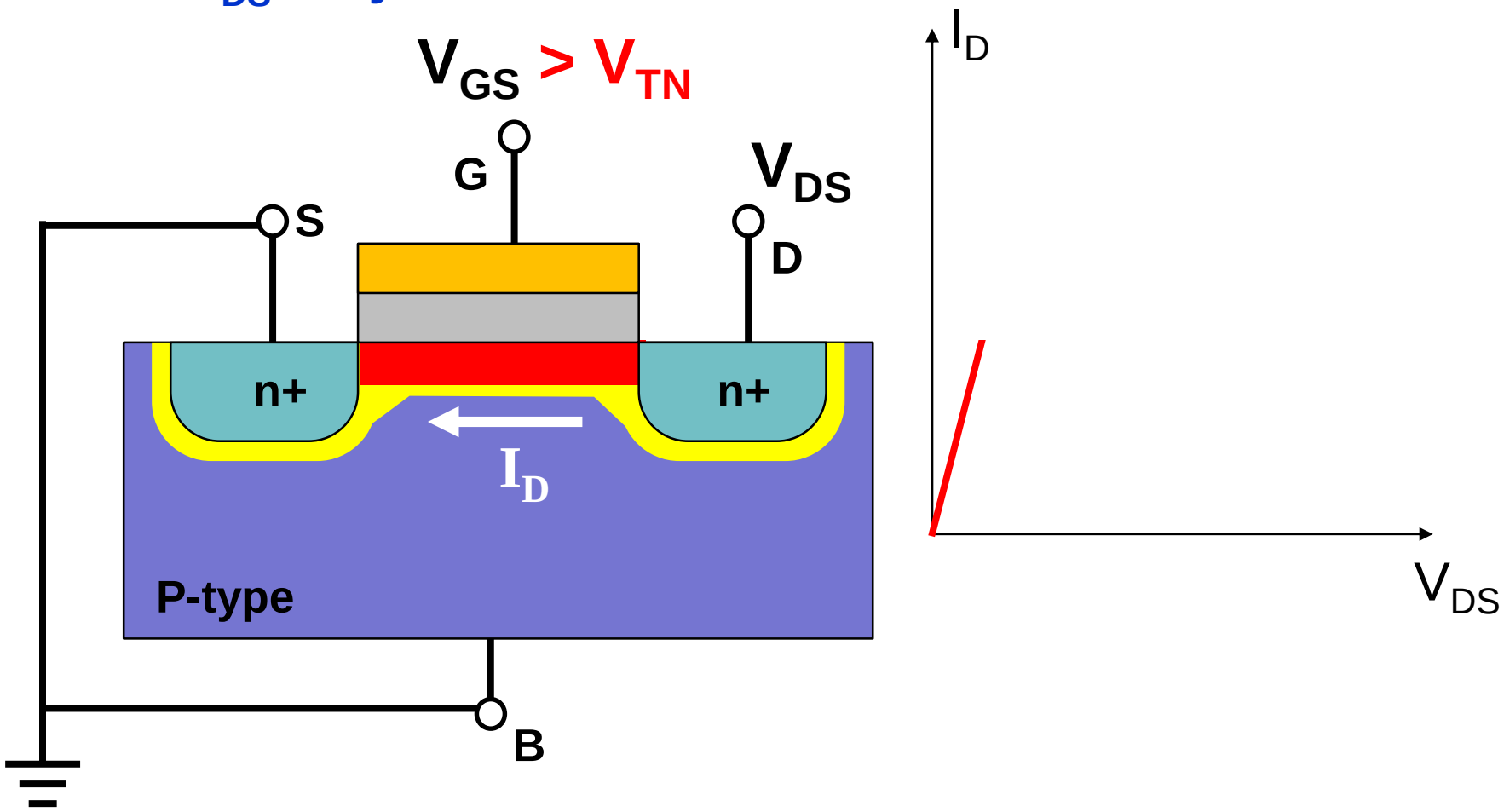
When $V_{DS} = 0$



n-MOSFET IV characteristics

Case 2

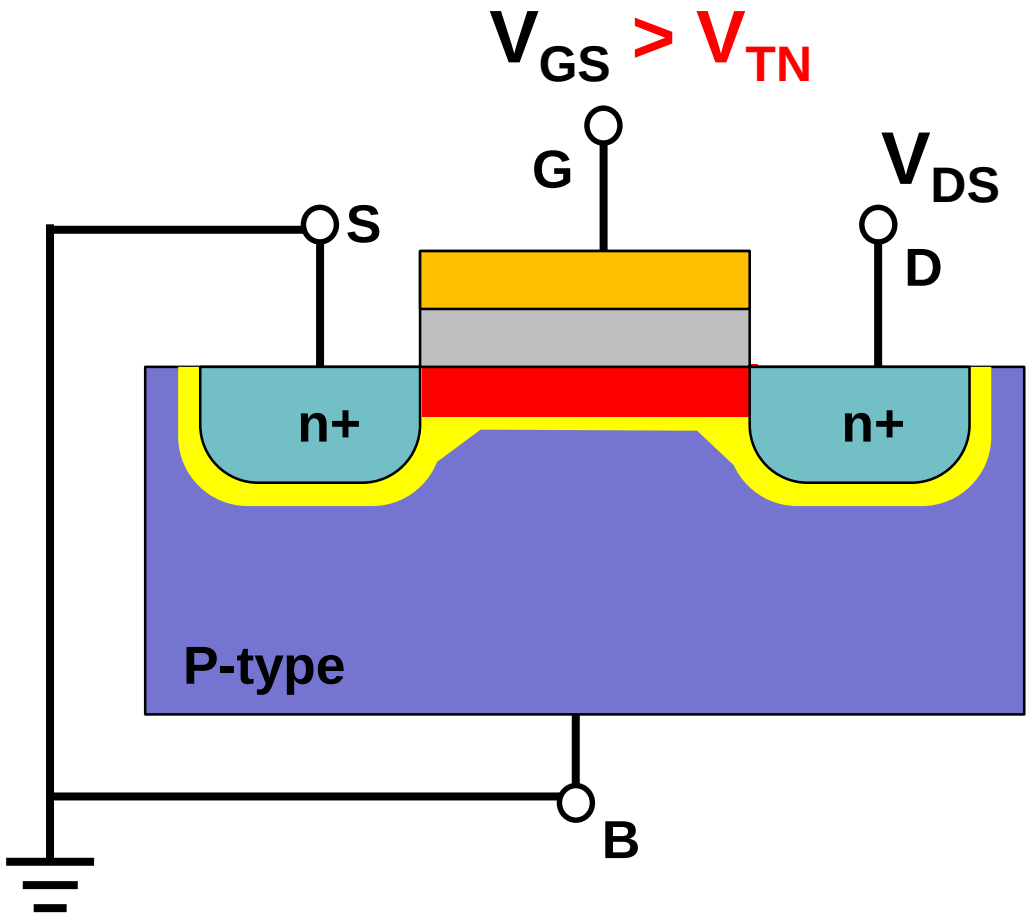
When V_{DS} very close to but more than 0



n-MOSFET IV characteristics

Case 3

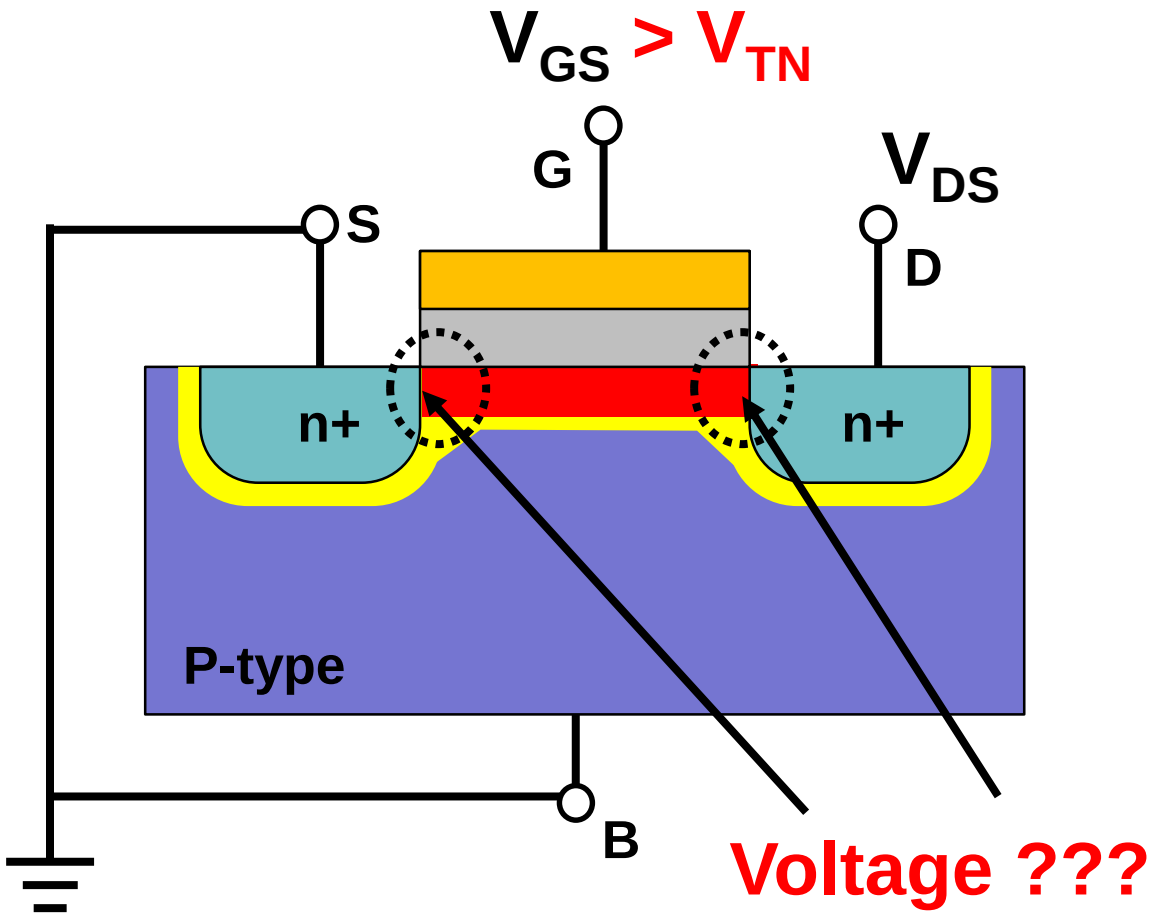
When V_{DS} further increases



n-MOSFET IV characteristics

Case 3

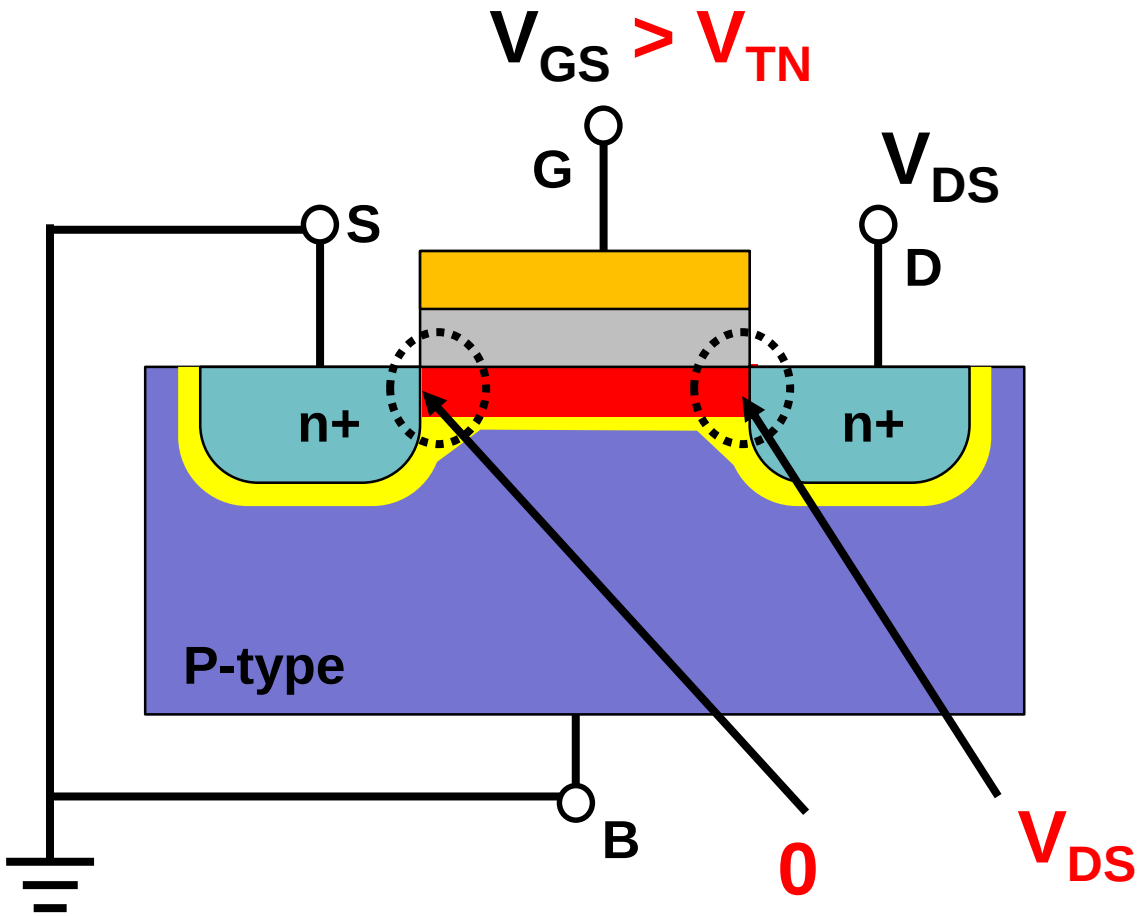
When V_{DS} further increases



n-MOSFET IV characteristics

Case 3

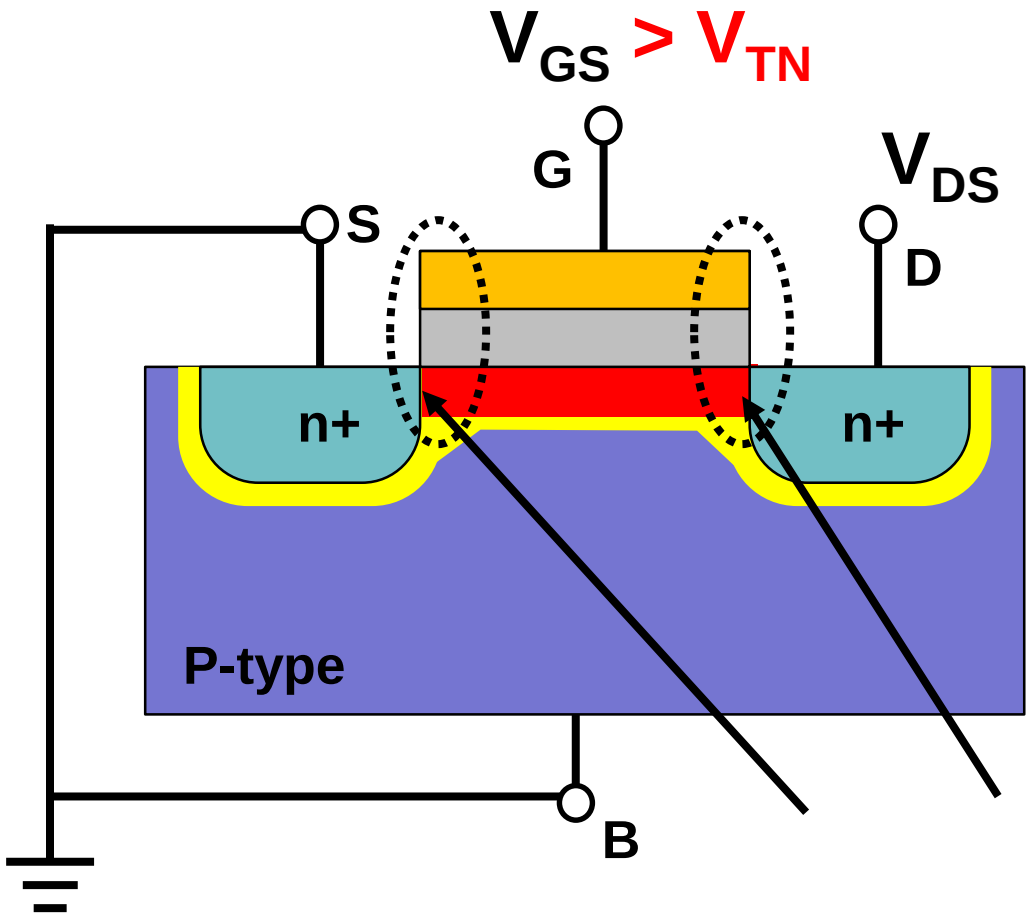
When V_{DS} further increases



n-MOSFET IV characteristics

Case 3

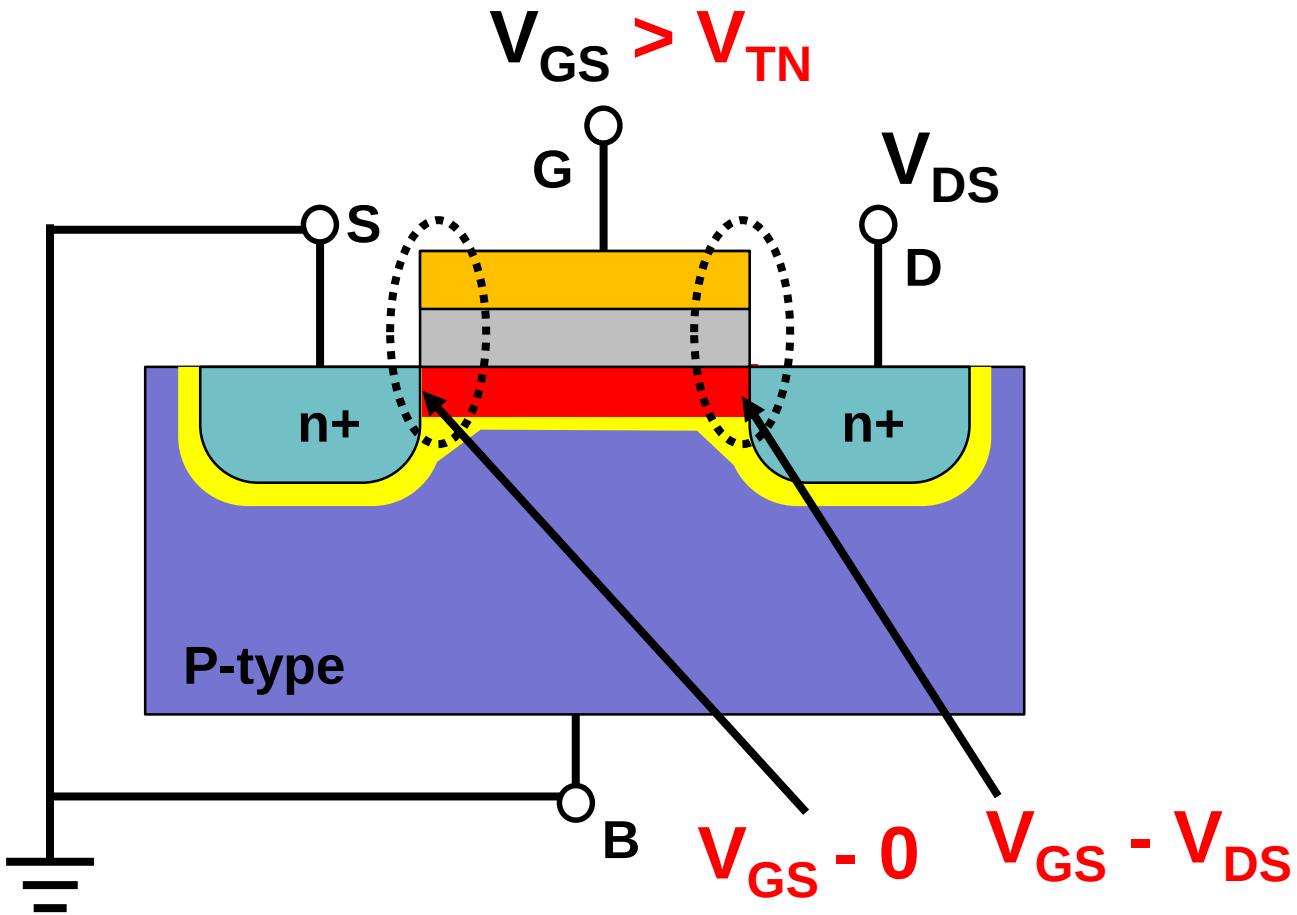
When V_{DS} further increases



n-MOSFET IV characteristics

Case 3

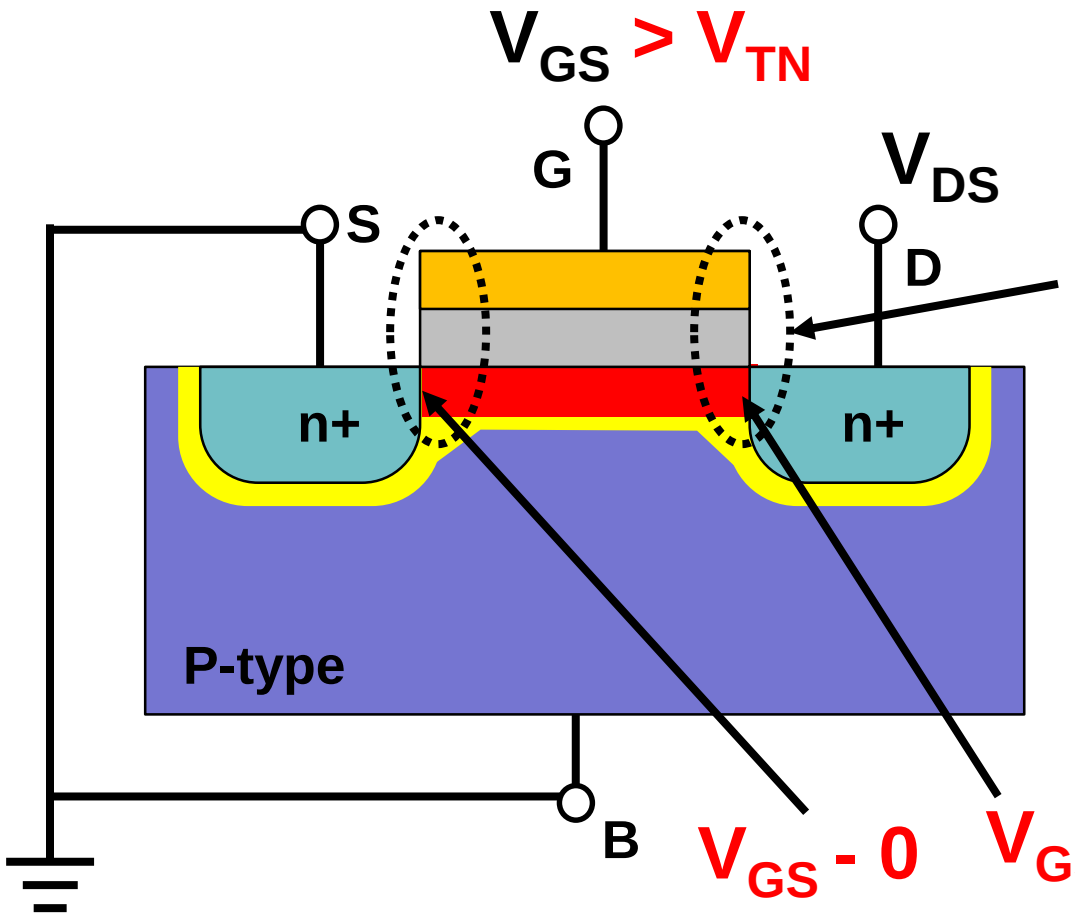
When V_{DS} further increases



n-MOSFET IV characteristics

Case 3

When V_{DS} further increases



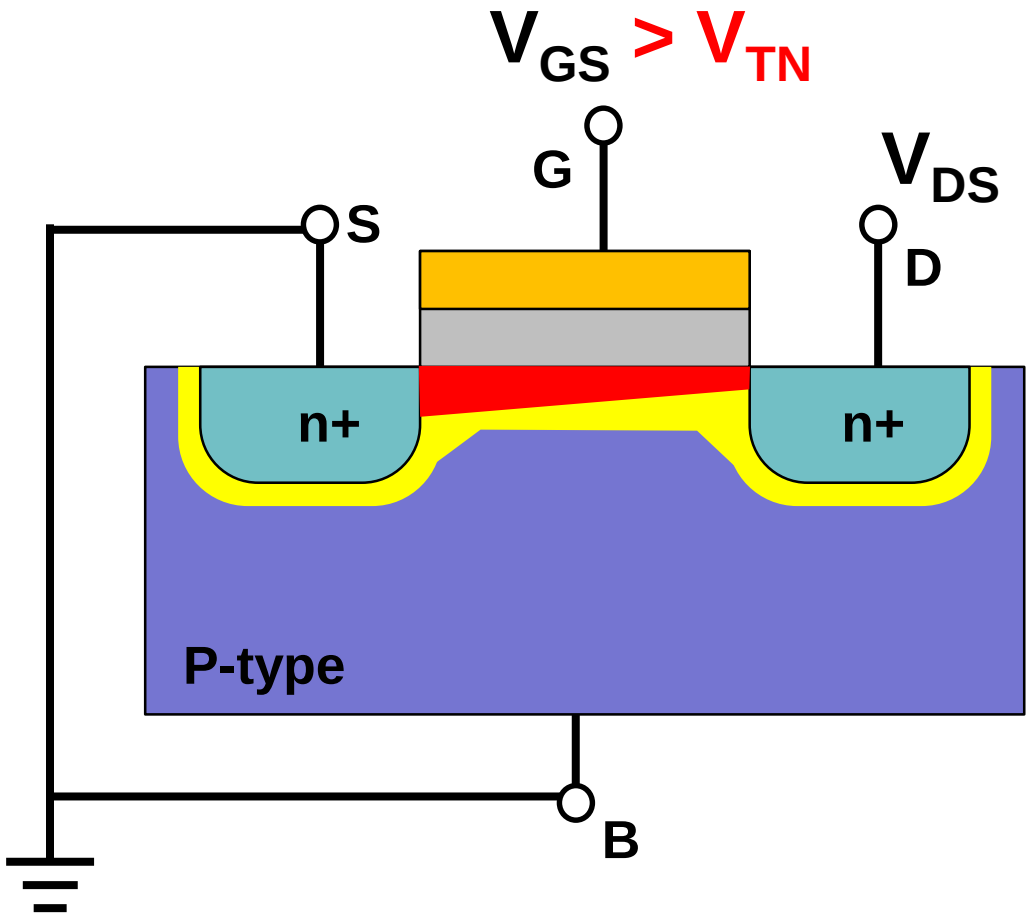
smaller voltage difference

Less electron density

n-MOSFET IV characteristics

Case 3

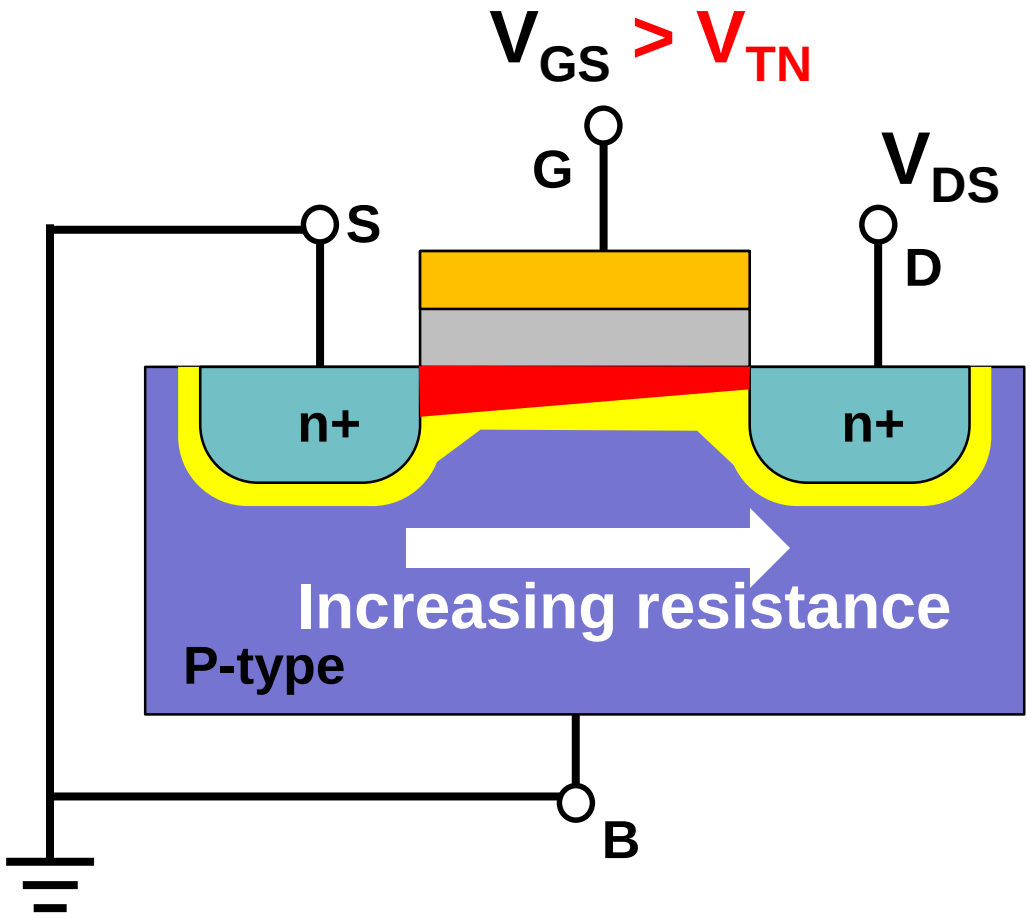
When V_{DS} further increases



n-MOSFET IV characteristics

Case 3

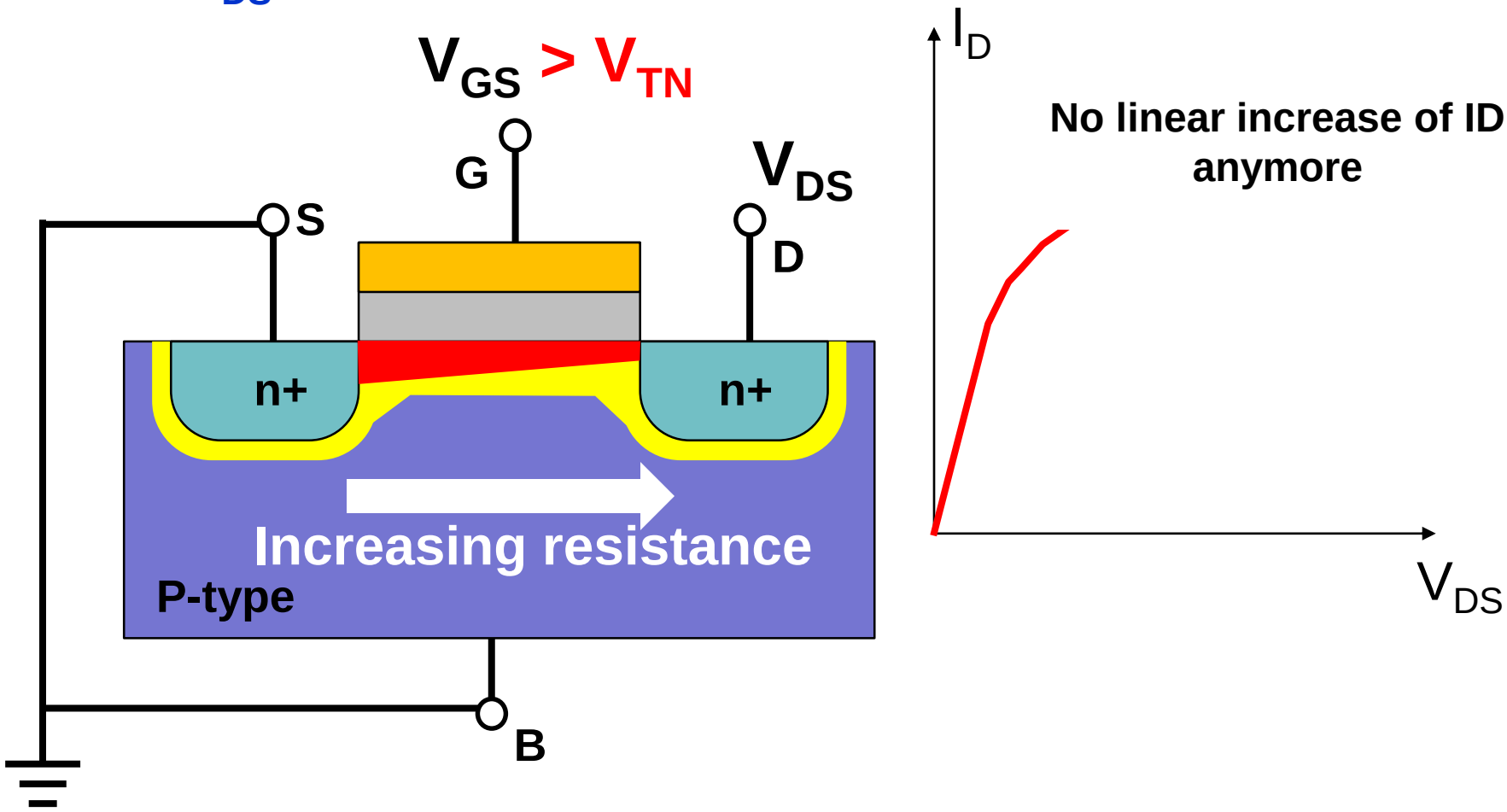
When V_{DS} further increases



n-MOSFET IV characteristics

Case 3

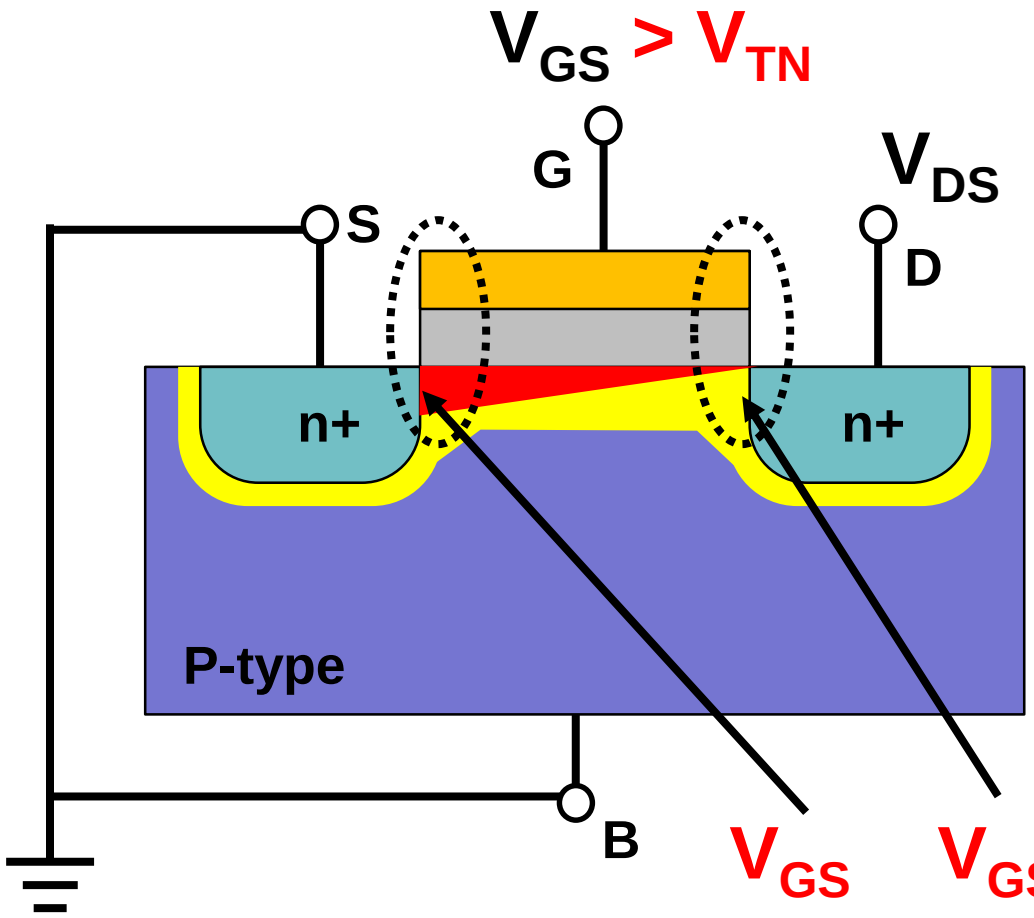
When V_{DS} further increases



n-MOSFET IV characteristics

Case 4

When $V_{DS} = V_{GS}-V_{TN}$



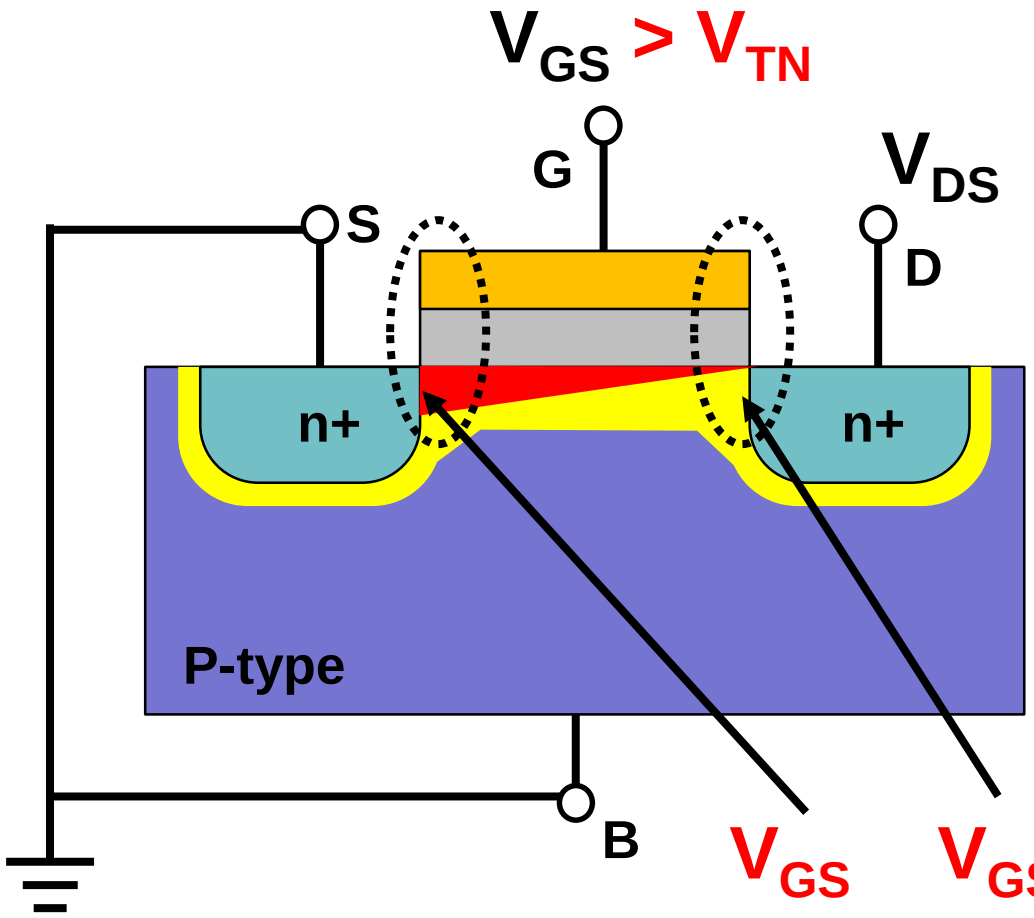
Further increase in V_{DS}

No more inversion layer

n-MOSFET IV characteristics

Case 4

When $V_{DS} = V_{GS}-V_{TN}$

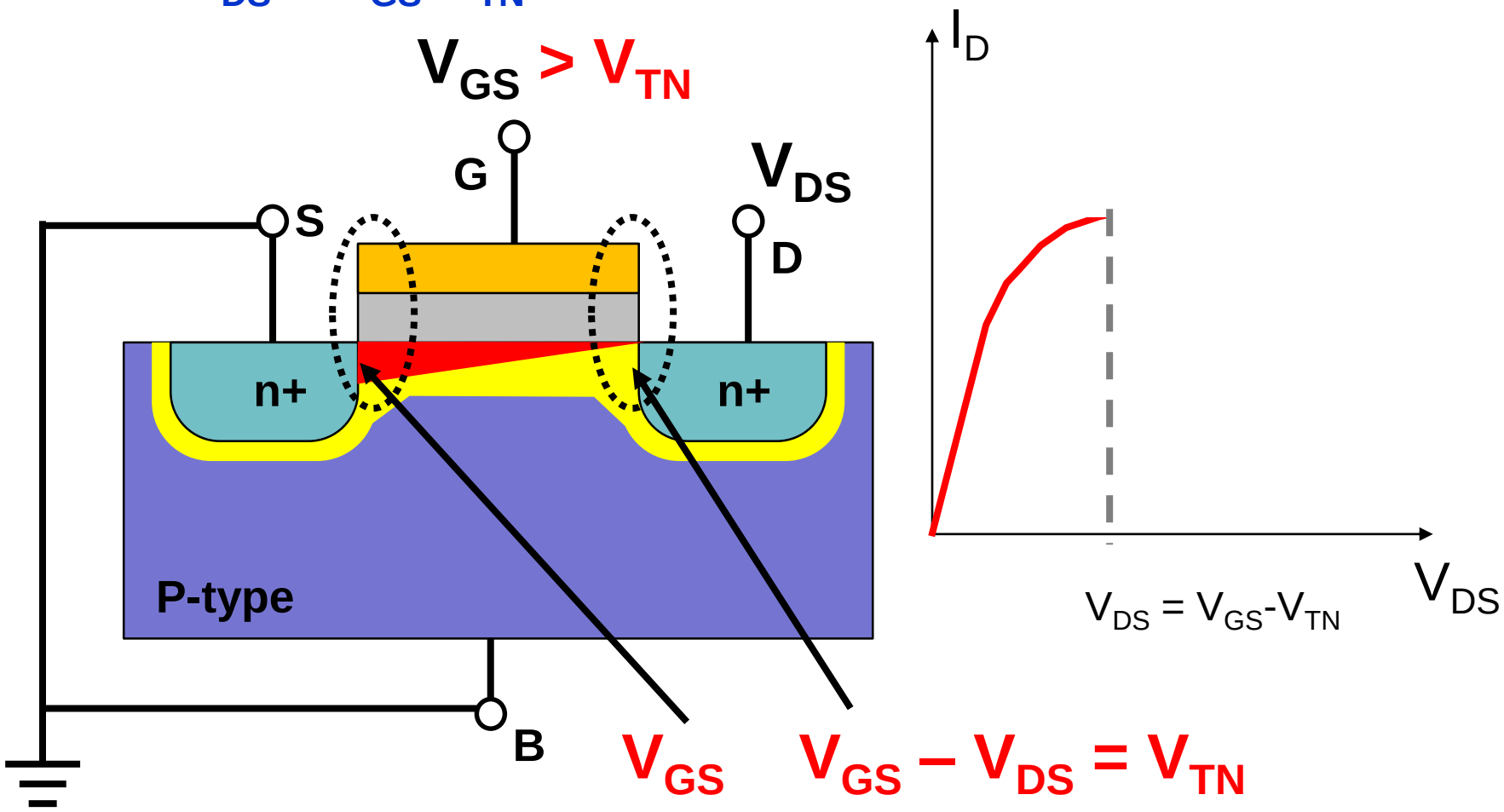


Pinch-off: no more channel

n-MOSFET IV characteristics

Case 4

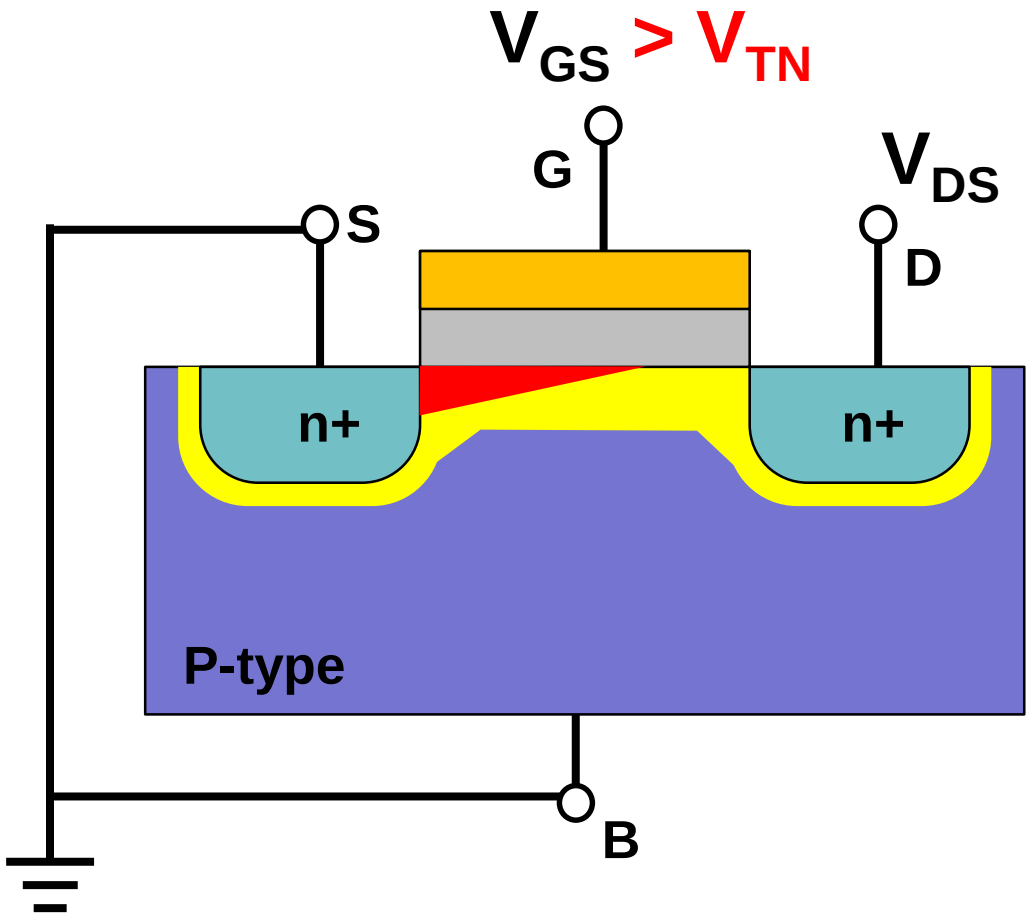
When $V_{DS} = V_{GS}-V_{TN}$



n-MOSFET IV characteristics

Case 5

When $V_{DS} > V_{GS}-V_{TN}$



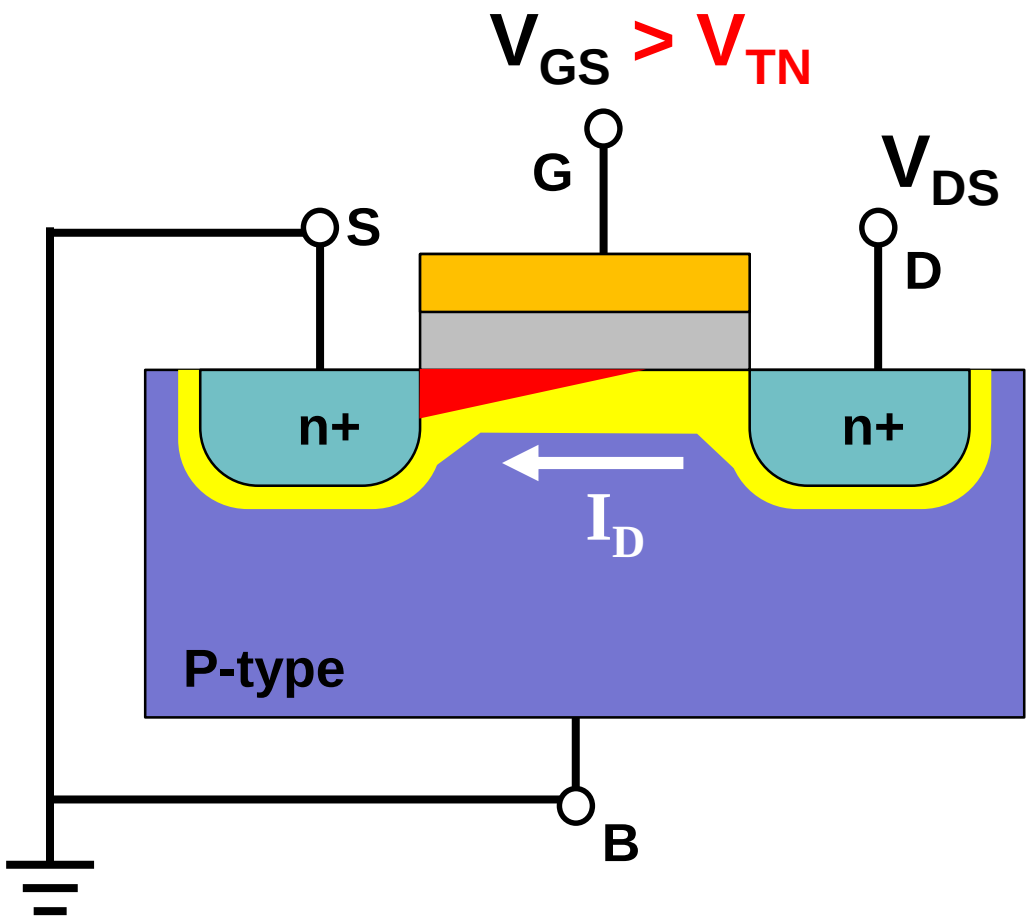
Further increase in V_{DS}

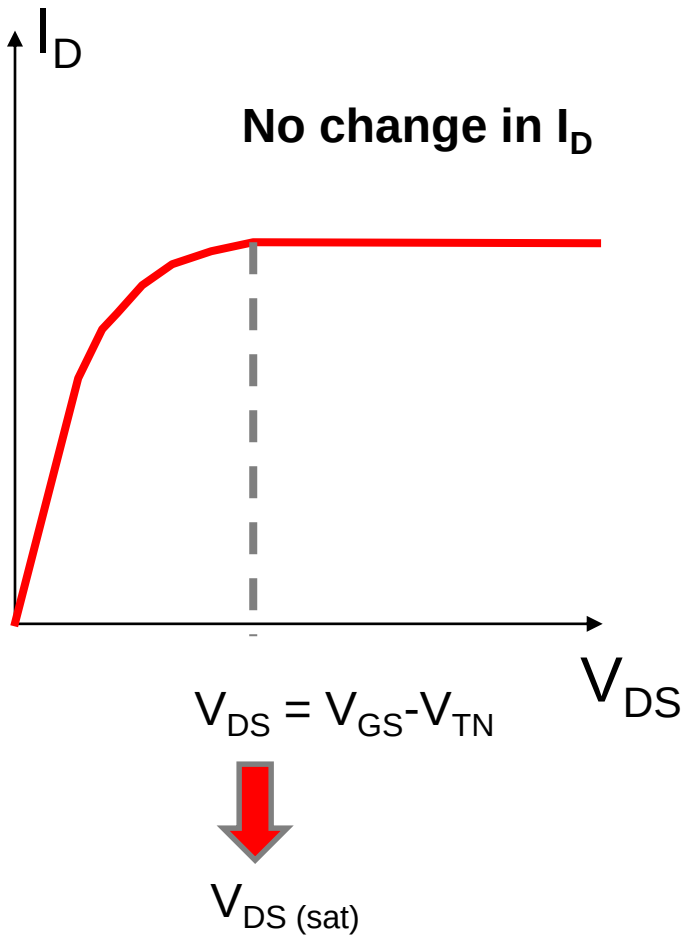
Only reduce the channel width

n-MOSFET IV characteristics

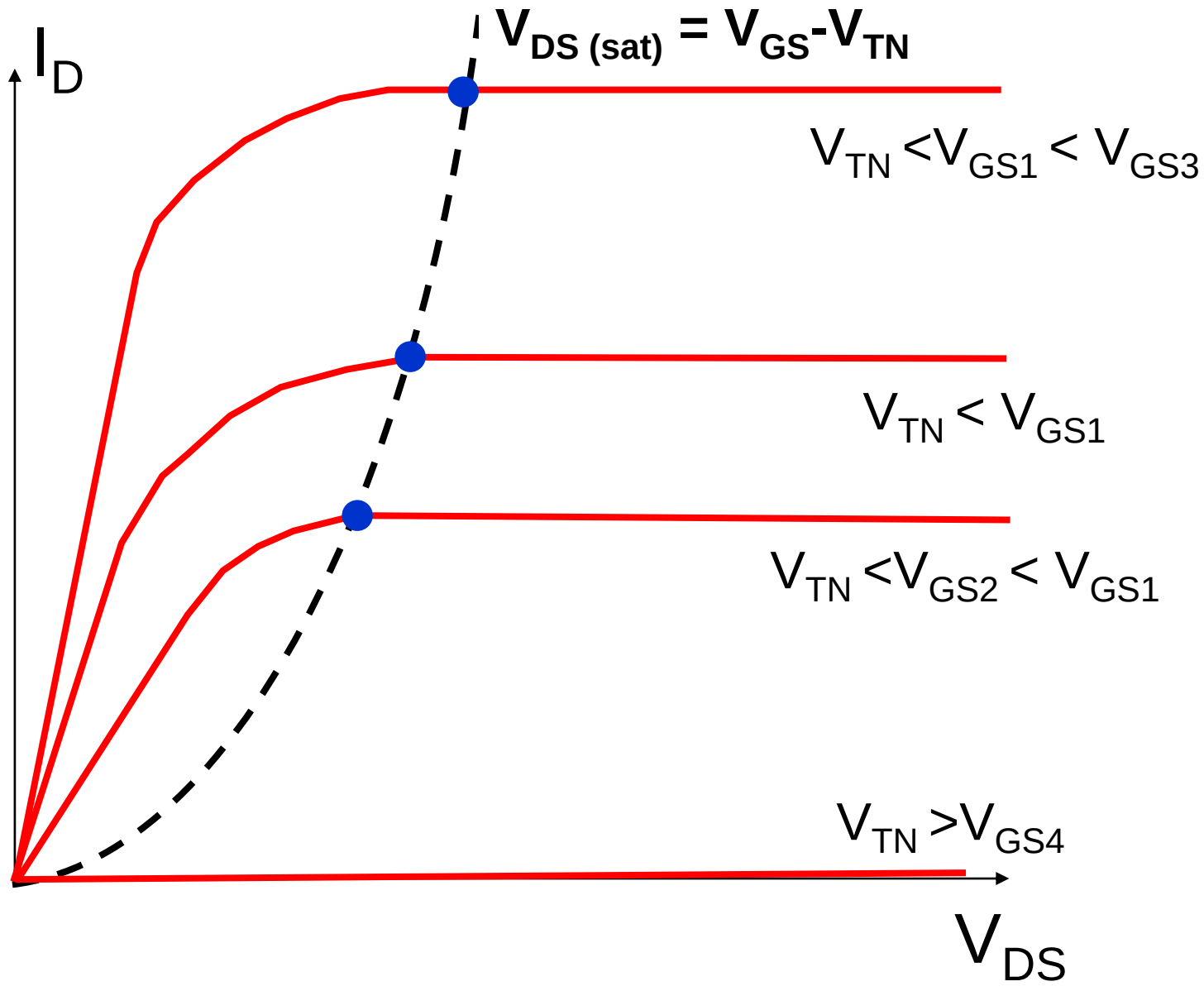
Case 5

When $V_{DS} > V_{GS}-V_{TN}$

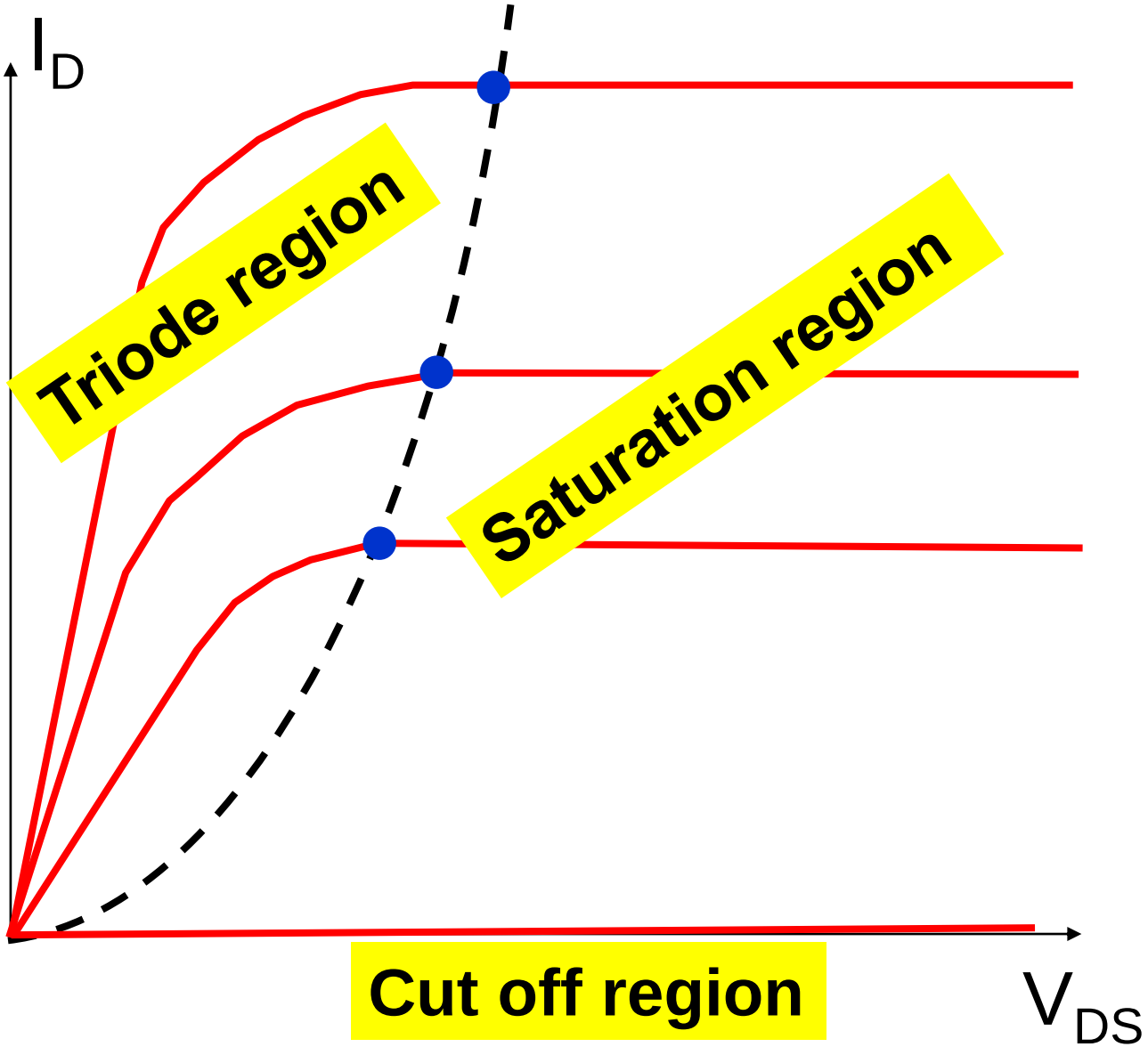




n-MOSFET IV characteristics



n-MOSFET IV characteristics



n-MOSFET IV characteristics

Triode region:

$$I_D = K_n\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$$ **V_{DS} and V_{GS} dependence**

Saturation region:

$$I_D = K_n(V_{GS} - V_{TN})^2$$ **Only V_{GS} dependence**

Cut off region:

$$I_D = 0$$

n-MOSFET IV characteristics

Triode region:

$$I_D = K_n\left[2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2\right]$$

Saturation region:

$$I_D = K_n(V_{GS} - V_{TN})^2$$

Cut off region:

$$I_D = 0$$

Conduction parameter

$$K_n = \frac{W\mu_n C_{ox}}{2L}$$

Unit = mA/V^2