DEPARTMENT OF ELECTRONICS AND ELECTRICAL COMMUNICATION ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

Date: **24 April 2019**, ~~FN~~/AN, Time: 3 Hrs, Full Marks: **100**, No. of Students: **704** (Non-ECE branches); End Spring Semester-2019,
Sub. No.: **EC21101**, Sub. Name: **Basic Electronics**

Instructions

- **All waveform sketches / diagrams must be neatly drawn and clearly labeled.** Answers must be brief and to the point.
- The final answers (numerical values with unit) should be **underlined** or enclosed within box with unit.
- **For every Question No., start your answer from a new page.**
- **Avoid writing answers of the various parts of a single question at different locations in your answer-script.**
- For any value related to any device parameter or circuit parameter, which you may find not given with a problem, assume suitable value for such parameter.
- **No Queries will be entertained. Candidate may make necessary assumptions, if so required.**

Question 1A (1x 10 = 10 marks)

(i) In a Zener diode voltage regulator, the source resistance R_i is used to control the

(a) minimum Zener diode current when load current is maximum
(b) limit the maximum current through the Zener diode
(c) limit the maximum power dissipation at the Zener diode
(d) both (b) and (c)

(ii) The junction and diffusion capacitance of a p-n junction

(a) Limits the high frequency response
(b) Limits the low frequency response
(c) Causes the built-in voltage
(d) Decreases with reverse bias

(iii) The inversion layer/channel in a MOSFET is induced by electric field originating from the

(a) gate
(b) drain
(c) body
(d) source

(iv) In the closed loop configuration of an op-amp circuit, the feedback loop is always tied to the inverting terminal to achieve

(a) output voltage stability
(b) buffering the input
(c) achieving virtual short between the inverting and non-inverting terminal
(d) None of the above

(v) In a BJT, which current relation holds true?

(a) $I_E = I_C$
(b) $I_E > I_C$
(c) $I_E < I_C$
(d) $I_E = \alpha I_C$

(vi) An ideal operational amplifier has

(a) infinite output impedance
(b) zero input impedance
(c) infinite bandwidth
(d) all of the above

(vii) The current direction in a pnp transistor is

(a) From Base to Collector and Emitter
(b) From Emitter to Base and Collector
(c) From Collector to Base and Emitter
(d) None of the above

(viii) In a MOSFET, beyond threshold voltage (for fixed V_{DS})

(a) I_D increases exponentially with V_{GS}
(b) I_D increases linearly with V_{GS}
(c) I_D increases quadratically with V_{GS}
(d) I_D remains independent of V_{GS}

(ix) The "virtual short" concept for op-amp exists for

(a) $A_{od} = \infty$, $R_i = \infty$, $R_o = 100\ \Omega$

(b) $A_{od} = 1000$, $R_i = 50\ k\Omega$, $R_o = \infty$

(c) $A_{od} = 1000$, $R_i = \infty$, $Ro = 0$

(d) $A_{od} = \infty$, $R_i = 50\ k\Omega$, $R_o = 100\ \Omega$

(x) The direction of current in NMOS transistor under saturation region is

(a) Drain to Source

(b) Drain to Gate

(c) Gate to Drain

(d) Source to Drain

Question 1B. True/False/Fill-in the blank (0.5×10= 5 marks)

(i) High-pass filter acts as a differentiator whereas low-pass filter is Integrator.

(ii) DeMorgan's second theorem states about the sum of products.

(iii) An operational amplifier is a transconductance amplifier

(iv) For an ideal n-channel MOSFET, the drain current becomes independent of the drain voltage in the saturation region

(v) MOSFET is a three terminal device.

(vi) Common emitter current gain ranges between 0 and 1

(vii) The breakdown voltage in pn junction decreases with increase in doping level.

(viii) The ripple voltage in Half-wave rectifier is _____than the full-wave rectifier.

(ix) CMRR stands for _____

(x) If β of a BJT is 80, the value of α is _____.

Question 2.

(a) Explain very briefly the necessity of DC biasing for a BJT amplifier. Which biasing scheme should be preferred and why? **[3 marks]**

(b) For the circuit shown in the right (Fig. 2.1), determine the value of V_{th} and R_{th} for the base terminal. R_1=33 kΩ, R_2=10 kΩ, R_C = 2.2kΩ, R_E=1 kΩ. **[2 marks]**

(c) For the circuit shown in Fig. 2.1, determine I_{BEQ}, I_{CEQ} and V_{CEQ}. Assume that V_{BE} (on) = 0.7 V and $\beta = 100$ **[3 marks]**

(d) If β varies by ±20%, determine the percentage change in I_{BEQ}, I_{CEQ} and V_{CEQ}. Plot the load line for output characteristics and show the variation of Q point in the load line. Comment on the biasing stability of the circuit. **[6+2 marks]**

(e) Does increase in R_E increases the stability of the biasing circuit? Explain in one or two sentences. **[2 marks]**

(f) In two or three sentences, discuss base width modulation or Early effect. **[2 marks]**

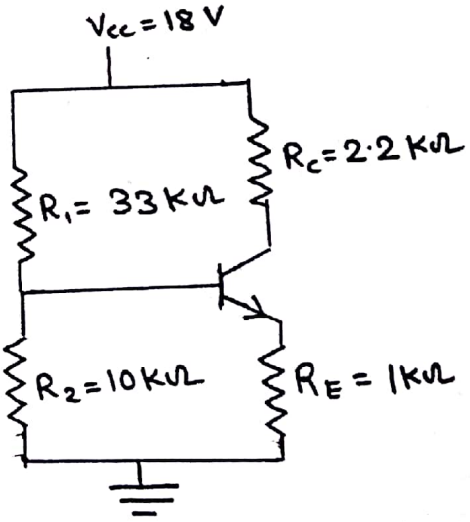

Fig. 2.1

Question 3.

(a) Obtain the small-signal parameters (g_m, r_π) of a BJT based CE amplifier circuit shown in Fig. 3.1. The transistor parameters are β =100. Assume that V_{BE} (on) = 0.7 V, V_T = 26mV, R_1 = 20kΩ, R_2 =10kΩ, R_C = 3kΩ, R_{E1} =1 kΩ, R_{E2} = 1.1kΩ, C_C = C_E = 10μF and V_{cc} =12 V. **[7 marks]**

(b) Draw the hybrid-π equivalent circuit if the Early voltage is very large. Also obtain input resistance, R_i and R_{ib}. **[2+1+1 marks]**

(c) Obtain the gain of amplifier circuit when C_E is not connected. What happens to the gain when C_E is connected. **[5+4 marks]**

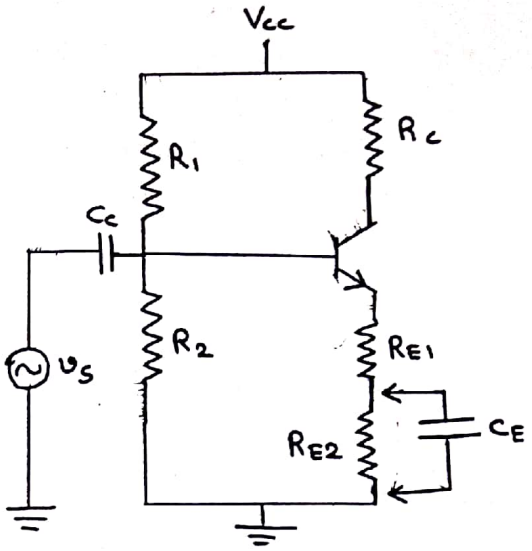

Fig. 3.1

Question 4

(a) Briefly describe the basic operation of an ideal n-channel MOSFET transistor. Draw the I_D-V_{DS} characteristic curves for different values of V_{GS}. Identify the three regions of operation. **[4 marks]**

(b) When the gate-to-source voltage (V_{GS}) of an n-channel MOSFET with threshold voltage of 0.4 V, working in saturation is 0.9 V, the measured drain current is 1 mA. Assume that the MOSFET is operating in saturation, what will be the drain current for an applied V_{GS} of 1.4 V? **[4 marks]**

(c) For NMOS, V_{TN}= 0.8 V, L=0.8 μm, $k_n' = 120\mu A/V^2$. When the transistor is biased in the saturation region with V_{GS} =1.4 V, the drain current is 0.6 mA. Obtain the channel width W and determine the drain current if the V_{DS} =0.4 V. **[2 marks]**

Question 5

(a) For the circuit shown in the right (Fig. 5.1), find the voltage gain (A_V), input resistance (R_i), output resistance (R_o). Consider the Op-amp to be ideal. **[5 marks]**

(b) Using an ideal op-amp, design a summing amplifier to have the output voltage expression

$v_o = -(2v_1 + 0.5\,v_2)$

where v_1 and v_2 are the two input voltages. Consider all the resistances are in kΩ. **[2 marks]**

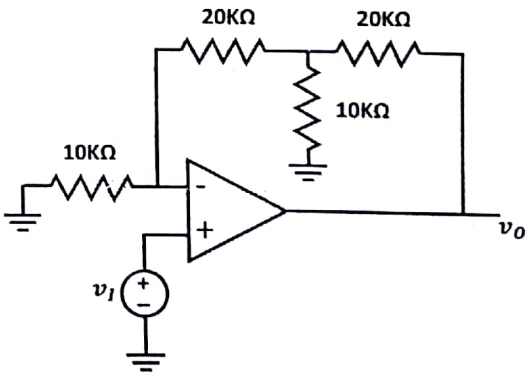

Fig. 5.1

(c) The circuit shown in Fig. 5.2 represents which type of filter? Derive the gain expression. **[3 marks]**

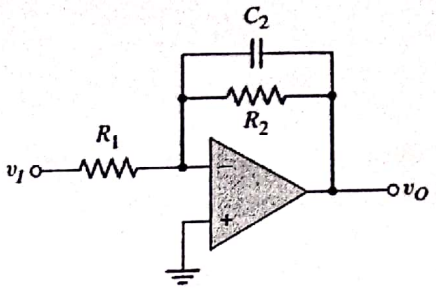

Fig. 5.2

Question 6

(a) Calculate the percentage difference in output voltage of an op-amp for the following two sets of input signals : the first set of signals is $v_{I1} = -50$ μV and $v_{I2} = +50$ μV and the second set is $v_{I1} = 950$ μV and $v_{I2} = 1050$ μV, where v_{I1} and v_{I2} are connected to inverting and non-inverting terminals, respectively. Consider a CMRR of 100. What should be the ideal value of CMRR? **[5+2 marks]**

(b) For the op-amp difference amplifier shown in Fig. 6.1, Let $R_1 = R_3 = 25$ kΩ and $R_2 = R_4$. A load resistance $R_L = 5$ kΩ is connected between v_0 and ground. The circuit has a differential voltage gain of $A_d = 5$. If the load current is i_L=0.5 mA when $v_{I1} = 2$ V, determine v_{I2}. **[8 marks]**

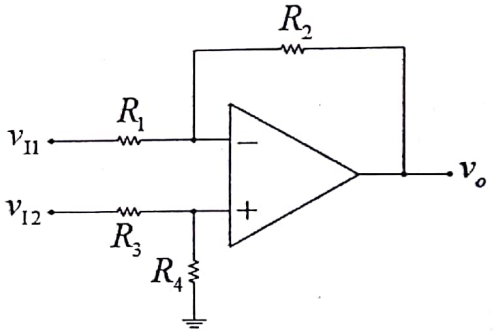

Fig. 6.1

Question 7

(a) Write down the truth table for the logic gate circuit shown in Fig. 7.1. Show that the circuits shown in Figures 7.1 and 7.2 are equivalent. **[2+3 marks]**

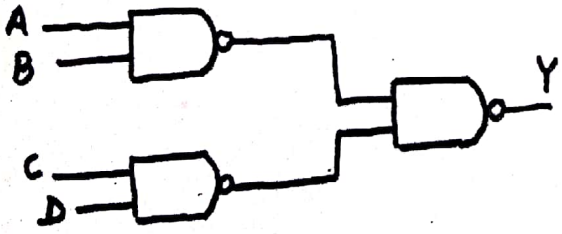

Fig. 7.1

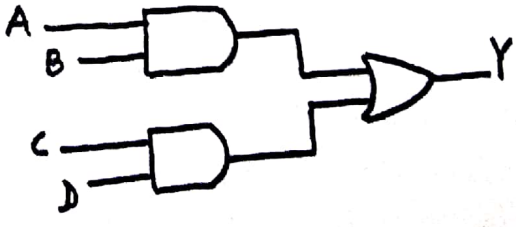

Fig. 7.2

(b) Design OR gate using minimum number of NAND gates. **[5 marks]**

End of Question Paper