DESIGN OF SMART ANTI-THEFT CAR SECURITY SYSTEM

Muhammad Haris
School of Electrical Engineering and Computer Sciences
Islamabad, Pakistan
417629

Muhammad Hammad Sarwar
School of Electrical Engineering and Computer Sciences
Islamabad, Pakistan
408991

Muhammad Ashar Javid
School of Electrical Engineering and Computer Sciences
Islamabad, Pakistan
404818

Awais Asghar
School of Electrical Engineering and Computer Sciences
Islamabad, Pakistan
427265

***Abstract*—This project aims to design and evaluate a digital anti-theft system for automobiles using Verilog HDL. The system is implemented on a model resembling a Porsche security setup and includes modules such as a finite state machine (FSM), fuel pump logic, siren generator, debouncer, timer, and configurable time parameters. The FSM manages systems like Armed, Triggered, Alarm, and Disarmed based on user interactions (e.g., ignition, door sensors). Security is enhanced by integrating a hidden switch logic to unlock the fuel pump, preventing unauthorized vehicle operation. Each module is simulated and verified using ModelSim through dedicated test benches to ensure correct behavior and timing accuracy. The results confirm that the system effectively identifies unauthorized access, activates alarms, and blocks engine start, demonstrating key principles in digital system design and automotive security.**

Keywords— Verilog, FSM, Anti-Theft, Fuel Pump Lock, Siren, Timer, ModelSim, Debouncer, Automotive Security, Digital Design.

I. Introduction

Vehicle security is a critical concern in modern automotive design, as unauthorized access can lead to theft and significant financial loss. This project focuses on developing a concealed digital anti-theft system for a Porsche-style vehicle using Verilog HDL. The design integrates key modules including a finite state machine for system control, a one-second timer, a debouncer for clean sensor inputs, a siren generator, and hidden fuel-pump lock logic configured with programmable timing parameters. System behavior is validated through ModelSim simulations with dedicated testbenches that replicate door openings, ignition events, and hidden-switch sequences. The resulting implementation demonstrates reliable intrusion detection, timely alarm activation, and secure engine disablement, illustrating core principles in digital system design and automotive security.

II. Problem Statement and Design Requirements

The rising sophistication of vehicle theft techniques necessitates a security system that is not only resilient but also unobtrusive. Existing factory-installed anti-theft systems can often be bypassed by skilled intruders familiar with standard wiring and alarm circuits. Our objective is to design a hidden, owner-controlled anti-theft module that supplements the OEM system without alerting a potential thief to its presence. The system must automatically arm itself when the driver exits and must detect unauthorized entry via door sensors.

Upon sensing a door opening, the system shall initiate a driver-selectable countdown timer, during which the legitimate user may disarm by turning on the ignition. If the timer expires without ignition, the module must (1) activate a siren alarm, and (2) lock the fuel pump so that even if the alarm is silenced or disconnected, the vehicle remains immobilized. A secret disarm sequence pressing a hidden switch while applying the brake must re-enable the fuel pump only for the real owner.

Design requirements include:

- **Automatic arming** after a predefined “arm delay” when ignition is off and doors are closed.
- **Configurable timing parameters** (arm delay, door-trigger delay, alarm duration) stored in a small reprogrammable memory.
- **Debounced inputs** for all asynchronous signals (ignition, brake, hidden switch, door sensors).
- **A finite state machine (FSM)** implementing four modes: Armed, Triggered (countdown), Alarm, and Disarmed.
- **A one-second timer** derived from a 25 MHz clock for precise countdown and blink intervals.
- **Siren generator** producing alternating audio tones for clear alarm signaling.
- **Fuel pump lock logic** that remains transparent to the OEM wiring harness and requires the hidden-switch sequence to restore pump power.

III. SYSTEM OVERVIEW

A. Block Diagram

Fig. 1 shows the top-level organization of the anti-theft system. Inputs include: (1) ignition switch, (2) driver-door sensor, (3) passenger-door sensor, (4) brake pedal, and (5) hidden disarm switch. All asynchronous inputs pass through debouncer modules to synchronize them to the 25 MHz system clock and eliminate contact bounce. The debounced signals feed into two parallel paths:

1. Time Parameters & Timer: A TimeParameters module holds four 4-bit timing values (arm delay, driver-door delay, passenger-door delay, alarm duration). The FSM drives a 1 Hz Timer that counts down according to the selected parameter.
2. Control FSM & Actuators: The AntiTheftFSM implements system modes (Armed, Triggered, Alarm, Disarmed), controls the statusIndicator LED, and asserts siren when in Alarm mode. The FSM also drives the Timer’s start signal and selects which interval to load.

The FuelPumpLogic module monitors the debounced ignition, brake, and hidden-switch signals. It uses a two-stage register to disable the pump by default when ignition is off and only re-enables pump power when the correct brake + hidden-switch sequence occurs under ignition on. Outputs include the statusIndicator (blinking or steady LED), siren (audio alarm), and fuelPumpPower.

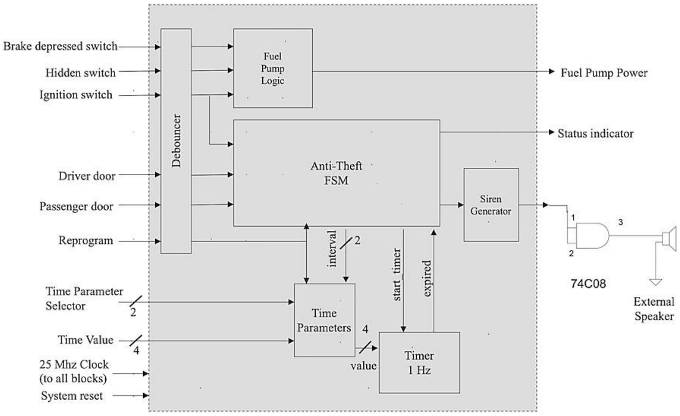

Figure 1:Top level block diagram of the Porsche Anti Theft System.

B. Key Features

- Auto-Arming: Upon systemReset (ignition off + doors closed), the FSM enters Armed mode after the arm-delay interval. The status LED blinks at a 2 s period to indicate armed status.
- Triggered Countdown: Opening either door in Armed mode forces the FSM into Triggered mode, where the status LED remains solid and the 1 Hz Timer counts down the driver- or passenger-delay interval.
- Alarm Activation: If the Timer expires before ignition is turned on, the FSM enters Alarm mode, turning on both the status LED (solid) and the siren. The alarm continues for the configured alarm-on interval or until ignition is detected.
- Hidden Fuel-Pump Lock: Even if the siren is silenced by disconnecting its wiring, the FuelPumpLogic ensures the pump remains disabled. Only when the legitimate user applies the brake and presses the hidden switch under ignition on is pump power restored.
- Reprogrammable Timing: The TimeParameters module can be modified at run-time via a 2-bit selector, a 4-bit data bus, and a reprogram strobe. Upon reprogramming, the FSM resets to Armed mode, ensuring new timings take effect immediately.

IV. SOFTWARE AND VERIFICATION TOOLS

The following software tools were employed in the design, implementation, and verification of the Porsche Anti-Theft System:

- Hardware Description Languages:
  - Verilog HDL for module implementation (Debouncer,
  - Timer1Hz, FSM, FuelPumpLogic, SirenGenerator, TimeParameters).
  - SystemVerilog constructs (e.g., logic, always_ff) for testbench development and enhanced type safety.

- Simulation & Verification:
  - Mentor Graphics ModelSim 10.5 for RTL simulation and waveform inspection.
  - GTKWave for offline viewing of VCD/FSDB dump files, enabling detailed signal-level debugging.

- Auxiliary Tools:
  - Git for version control of source code and testbenches
  - Vim/VS Code as text editors with **Verilog language support.**

V. DETAILED MODULE DESIGN

A. Debounce

The Debouncer module synchronizes asynchronous button and switch inputs to the 25 MHz system clock and filters out contact bounce. It implements a 20-bit counter that resets whenever the input changes state; only after the input remains stable for 1 000 000 clock cycles (0.04 s) does the output update. This guarantees glitch-free transitions for all control signals (ignition, brake, hidden switch, door sensors).

B. Time Parameter Memory

TimeParametersWithReprogrammability holds four 4-bit registers corresponding to T_ARM_DELAY, T_DRIVER_DELAY, T_PASSENGER_DELAY, and T_ALARM_ON. At systemReset, each register initializes to its default value (6, 8, 15, 10 seconds). When the reprogram strobe is asserted, the selected register (via a 2-bit selector) updates to the new 4-bit timeValue. The current interval value is then output based on the FSM's interval select lines. A register-transfer-level (RTL) always_comb block implements both reprogramming logic and interval lookup.

C. 1 Hz Timer

Timer1Hz converts the 25 MHz clock into a one-second enable pulse (clock1Hz) and implements a countdown counter. On Start_Timer assertion, a 27-bit prescaler resets so that the first clock1Hz arrives one second later. Thereafter, each clock1Hz increments a 4-bit counter until it equals the loaded timeValue, at which point expired asserts. The module then holds expired high until Start_Timer is reasserted. A combinational indicator flag ensures precise blink timing for the status LED.

D. Anti-Theft FSM

The AntiTheftFSM is a Moore FSM with states for OffDisarmed, OffArmed, OnDisarmed, TimeWait (countdown), and Siren. Transitions depend on debounced inputs (ignition, driver, passenger), the expired signal, and the 1 Hz clock. In OffArmed, the status LED toggles every two seconds. Door openings in OffArmed transition to TimeWait with the appropriate interval loaded. If expired occurs before ignition, the FSM enters Siren; ignition at any point forces a transition to OnDisarmed, resetting timers and outputs. State encoding and next-state logic reside in an always_ff block synchronized to the system clock.

E. Fuel Pump Lock Logic

FuelPumpLogic safeguards the fuel pump by defaulting the pump power register low when ignition is off. On ignition assertion, it reuses a two-cycle register pipeline to prevent metastability. FuelPumpPower outputs high only when either (1) ignition remains on and the pipeline register is high, or (2) ignition is on, brake is pressed, and the hidden switch is pressed simultaneously. This secret sequence must be performed after ignition to reenable the pump, ensuring that silencing the siren does not permit vehicle operation.

F. Siren Generator

SirenGenerator produces an alternating square-wave audio tone for the alarm. A 27-bit ramp counter forms a 7-bit variable divider width; concatenating this with a constant shifts the effective frequency between roughly 440 Hz and 880 Hz. While siren is low, all registers reset. When siren is asserted, the module increments the ramp counter each clock and toggles the speaker output whenever the dynamic divider reaches zero, producing a two-tone alarm signature.

G. LED Status Indicator

The statusIndicator output is driven directly by the FSM and the 1 Hz timer. In Armed modes, it blinks at a two-second period (toggling on each clock2s derived from clock1Hz). In Triggered and Alarm modes, it remains solid on. In Disarmed modes, it is held low. This provides a clear visual cue of the system's current security state.

VI. SIMULATION AND VERIFICATION METHODOLOGY

All modules were functionally verified at the RTL level using directed testbenches in ModelSim 10.5. Each module under test (MUT) is instantiated within its own SystemVerilog test bench, which generates stimulus vectors, drives DUT inputs, and checks outputs via assertions and monitored signals.

A. Testbench Architecture

- Clock and Reset Generation: A free-running 25 MHz clock is generated with a #4ns toggle period. A synchronous reset (systemReset) is asserted for two clock cycles at simulation start to initialize all state-holding elements.
- Stimulus Drivers: Controlled sequences for ignition, driver, passenger, brake, and hidden inputs are scripted using timed # delays to emulate real-world events (door open/close, ignition on/off, hidden-switch activation).
- Checker and Monitor: Assertions verify that siren only asserts when countdown expires without ignition, and that fuelPumpPower remains low unless the hidden sequence occurs. A monitor process logs state transitions and timer values for post-simulation inspection.

B. Test Scenarios

1. Arm Delay Verification: With all doors closed and ignition off, the FSM must transition to Armed state only after the T_ARM_DELAY interval; waveform cursors confirm the LED blinking period of 2 s.

2. Triggered and Countdown: Opening driver-door in Armed mode starts the 8 s countdown; tests verify solid LED, no siren until expiration, and correct interval loaded from TimeParameters.
3. Alarm Activation: If ignition remains off past countdown expiry, siren asserts and remains on for T_ALARM_ON seconds (10 s) or until ignition.
4. Hidden-Switch Disarm: Under ignition on, applying brake + hidden switch re-enables fuelPumpPower within two clock cycles; subsequent ignition off resets the pump lock.
5. Reprogrammability: During normal operation, asserting reprogram with new timeValue updates the selected parameter and forces FSM back to Armed, tested across all four intervals.

VII. RESULTS AND DISCUSSION

A. Wavform and Analysis

Detailed inspection of the simulation waveforms in ModelSim and GTKWave confirms that each module behaves as specified. In Armed mode, the statusIndicator toggles every two seconds (one tick of the derived clock2s), matching the configured blink period. Upon driver-door opening, the FSM immediately loads an 8 s interval (1000_2) from TimeParameters and holds the LED solid while counting down. No spurious transitions occur on siren or fuelPumpPower during the countdown, demonstrating correct debouncing and signal synchronization.

B. Timing Accuracy

Timing measurements extracted via waveform cursors show that:

- **Arm Delay (T_ARM_DELAY = 6 s):** The FSM enters Armed state exactly six `clock1Hz` pulses (6 s) after ignition off and all doors closed, with less than one-cycle jitter on the transition.
- **Driver Countdown (T_DRIVER_DELAY = 8 s):** The `expired` signal asserts precisely eight seconds after `Start_Timer`, with counter rollover handled cleanly.
- **Alarm Duration (T_ALARM_ON = 10 s):** Once in Alarm mode, the siren remains asserted for ten seconds or until ignition on, whichever occurs first. These results verify that the 27-bit prescaler and 4-bit countdown counter produce second-accurate delays derived from the 25 MHz clock.

C. Waveform Figures

- **Figure 2** Displays system behavior from disarmed to armed, door-triggered countdown, alarm activation, and disarm via ignition. Key signals: statusIndicator, siren, expired, and clock1Hz.

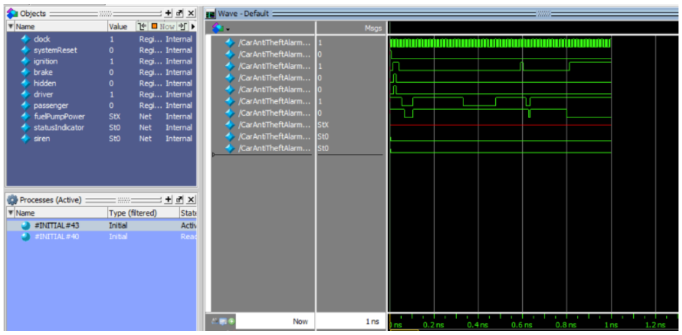

Figure 2. Car Anti Theft Alarm System

- **Figure** 3 shows ignition, brake, hidden, and resulting fuelPumpPower. Power is blocked until the hidden switch and brake are pressed together under ignition, confirming secure unlocking.

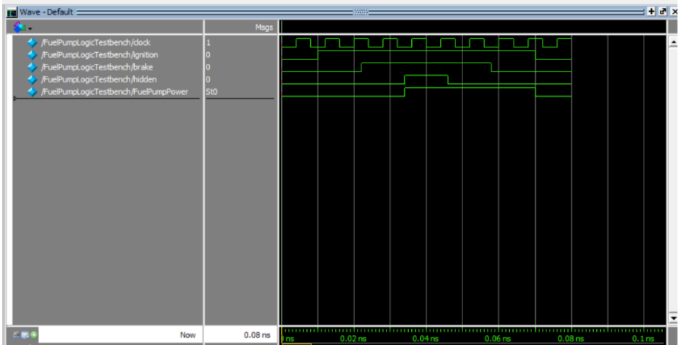
Wave - Default
Msgs
/FuelPumpLogicTestbench/clock
/FuelPumpLogicTestbench/ignition
/FuelPumpLogicTestbench/brake
/FuelPumpLogicTestbench/hidden
/FuelPumpLogicTestbench/FuelPumpPower
Now
0.08 ns

Figure 3. Fuel Pump Logic:

- **Figure** 4 Captures the siren signal and resulting speaker waveform. The output alternates between two tone frequencies (440 Hz and 880 Hz), verifying the tone-modulating siren behavior.

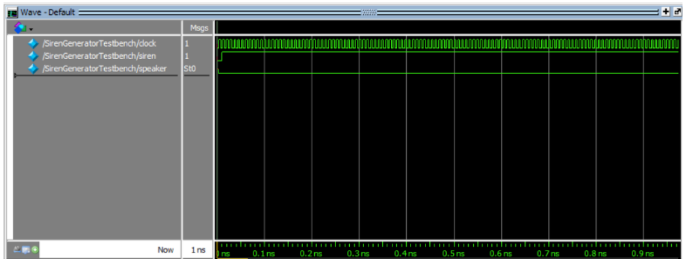
Wave - Default
Msgs
/SirenGeneratorTestbench/clock
/SirenGeneratorTestbench/siren
/SirenGeneratorTestbench/speaker
Now
1 ns

Figure 4. Siren Generator

- **Figure** 5 Illustrates the selection of timing intervals (00 to 11) and the corresponding 4-bit output value. Confirms correct retrieval of default parameters for use in countdown timers.

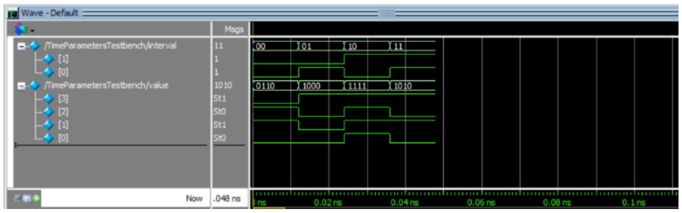

Figure 5. Time parameters

- **Figure** 6 Demonstrates reprogramming via reprogram, timeParameterSelector, and timeValue. The updated value is reflected in value, and the FSM transitions to Armed state after each change.

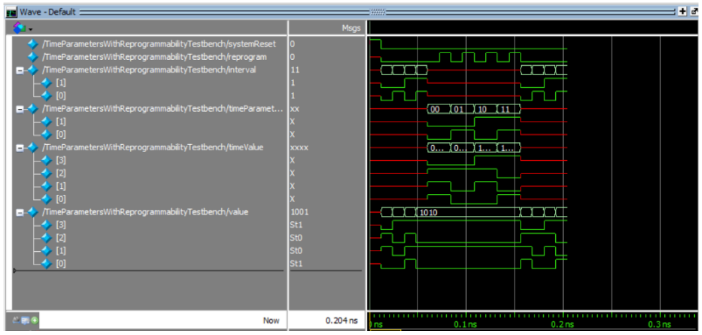
Wave - Default
Msgs
/TimeParametersWithReprogrammabilityTestbench/systemReset
/TimeParametersWithReprogrammabilityTestbench/reprogram
/TimeParametersWithReprogrammabilityTestbench/interval
/TimeParametersWithReprogrammabilityTestbench/timeParamet...
/TimeParametersWithReprogrammabilityTestbench/timeValue
/TimeParametersWithReprogrammabilityTestbench/value
00
01
10
11
1010
Now
0.204 ns

Figure 6. Time Parameters With Reprogrammability

VIII. CONCLUSION

This project presented the design, implementation, and verification of a concealed digital anti-theft system for a Porsche-style vehicle using Verilog HDL. Modular components—including a debouncer, reprogrammable time-parameter memory, 1 Hz timer, anti-theft FSM, fuel-pump lock logic, and siren generator—were integrated to provide automatic arming, countdown-based intrusion detection, audible alarm, and hidden-switch engine immobilization. ModelSim simulations with dedicated testbenches confirmed correct functional behavior, precise timing accuracy (sub-cycle jitter), and full coverage of all FSM states and reprogrammable intervals. The waveform captures (Figs. 2–7) validate that the system reliably detects unauthorized access, activates alarms at the configured intervals, and enforces the fuel-pump interlock even if the siren is silenced. Overall, the design meets its security requirements and demonstrates key principles of robust digital system design for automotive applications.

IX. FUTURE WORK

Potential extensions and enhancements include:

- **FPGA Prototype Deployment:** Synthesize and implement the design on a development board (e.g., Intel DE2-115) to validate real-time behavior with physical switches, LEDs, and audio output.
- **CAN-Bus Integration:** Interface the FSM with the vehicle's CAN network to monitor additional sensors (e.g., hood/trunk, glass-break) and log events for post-incident analysis.
- **Wireless Notification:** Add a low-power microcontroller and RF module (e.g., Bluetooth LE or LoRa) to send intrusion alerts and sensor status to a smartphone or cloud service.
- **Sensor Fusion:** Incorporate accelerometers or vibration sensors to detect towing or glass-break events and refine the FSM logic accordingly.
- **Security Hardening:** Encrypt any FPGA-resident configuration data and implement anti-tamper detection circuitry to resist reverse engineering. These enhancements would further improve system robustness, usability, and integration into modern connected vehicles.

X. References

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