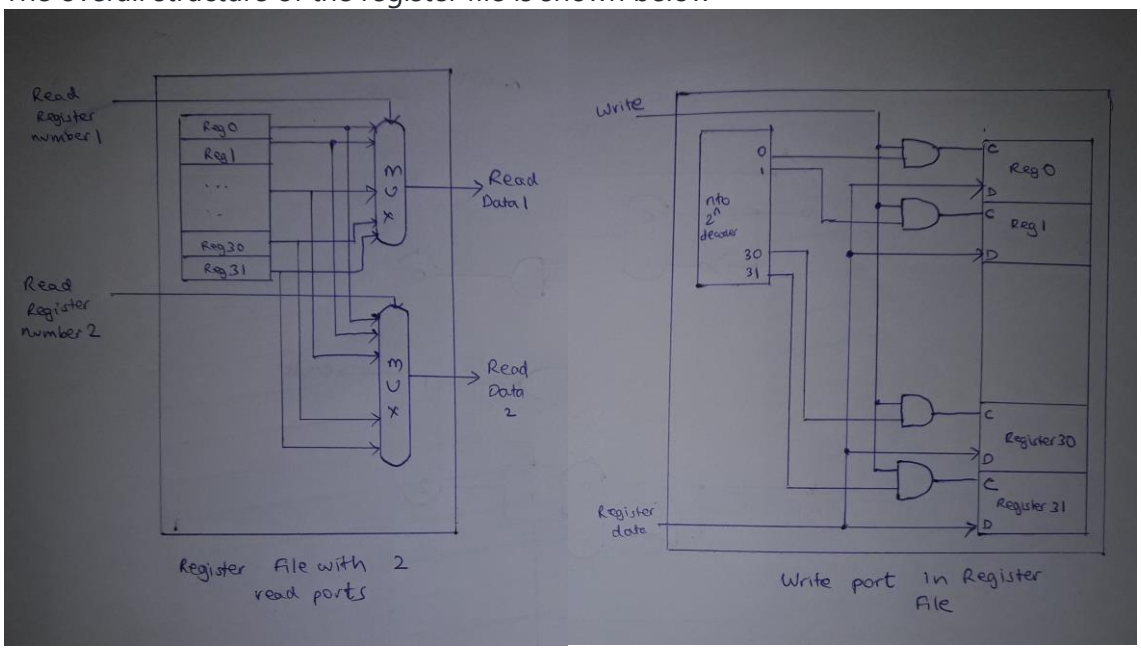
32 bit Register File

The register file is an extremely small, extremely fast memory at the heart of your CPU. They vary per architecture, but you will create one with the following specifications:

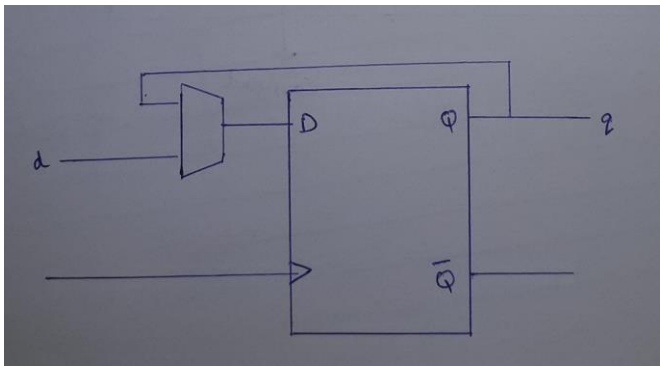
- Width: 32 bits
- Depth: 32 words
- Write Port: Synchronous, Positive Edge Triggered
- Read Port 1: Asynchronous
- Read Port 2: Asynchronous

The overall structure of the register file is shown below



The core is the 32-bit registers: 31 normal registers and a constant zero. The read ports are a pair of giant multiplexers connected to the register outputs. The write port connects to the input of all registers, and a decoder optionally enables one register to be written.

Circuit diagram for structural equivalent for each of the registers is:



Files included:

t_regfile.v – TestBench File

register.v – Includes the implementation of 1bit D FlipFlop and 32 bit D FlipFlop register0 having value set to 0, and the mux

regfile.v – Includes the top-level file for the register.

decoders.v – Includes the implementation of 32 bit decoder with enable.

If the enable is 0, output won't come, If the enable is 1, output will come.