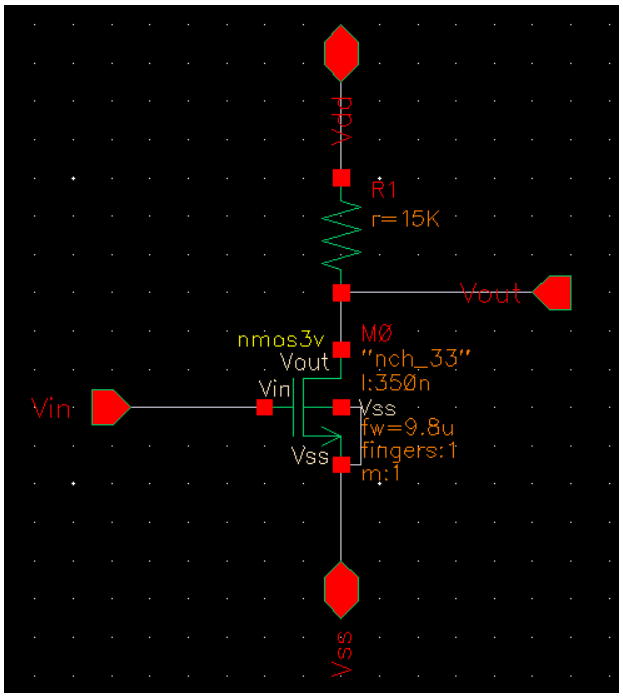
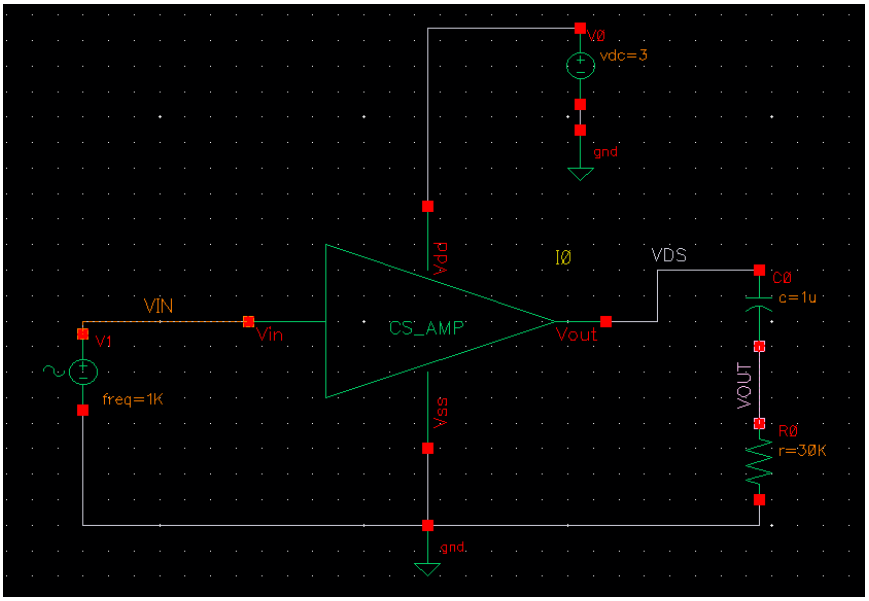
Lab Task:

Task#1: Transient analysis of CS amplifier.

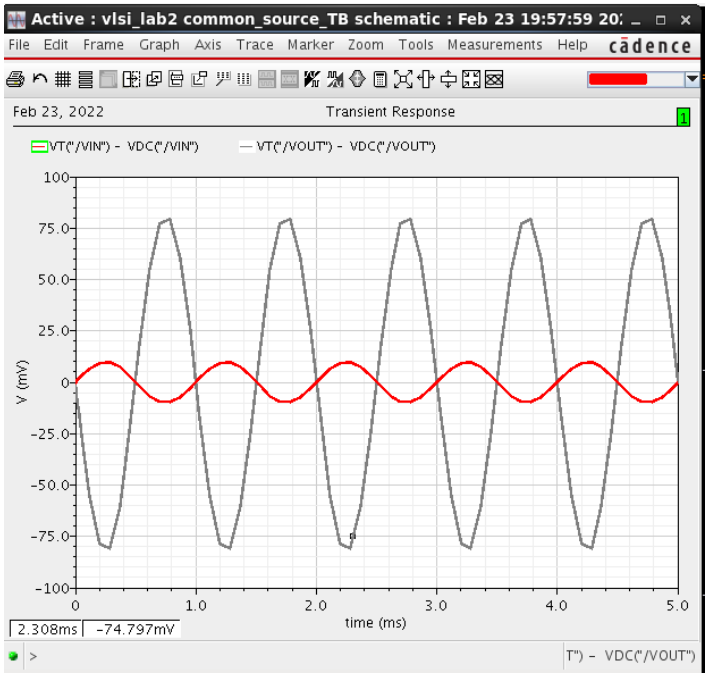
Internals of the symbol:



Testbench circuit:

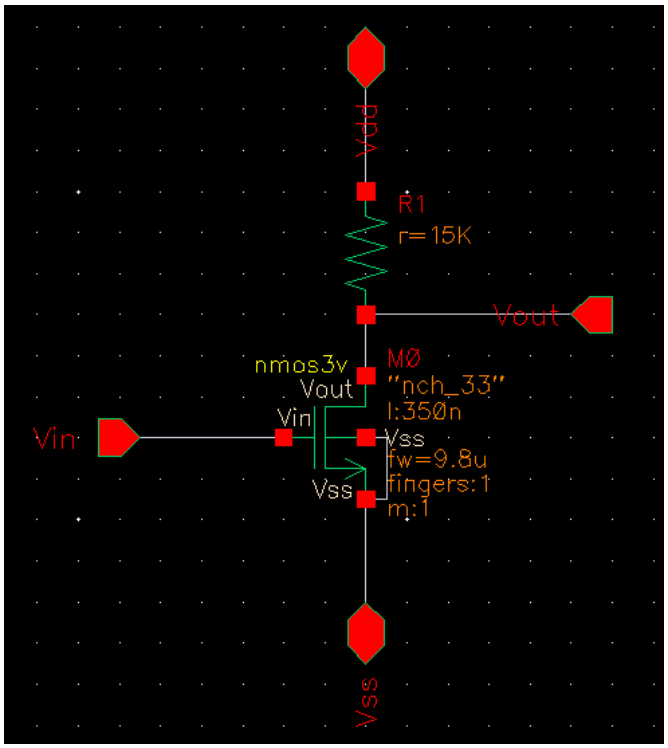


Input Vs Output:

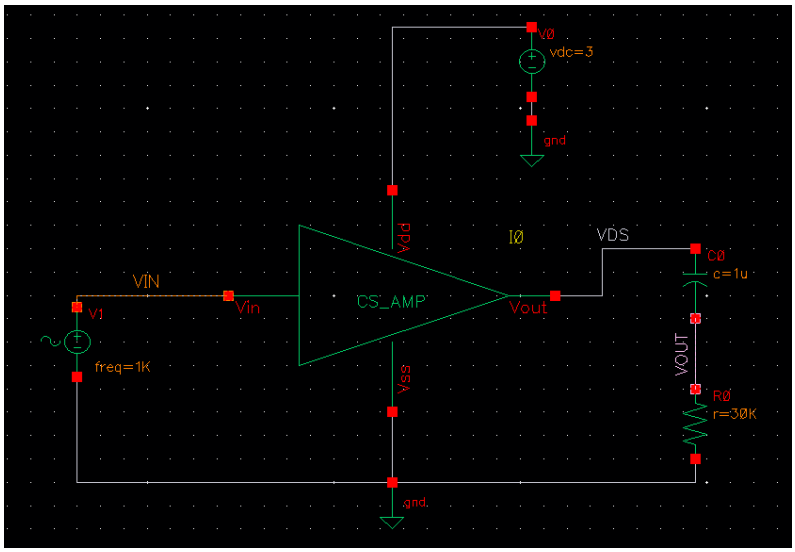


Task#2: Ac analysis of CS amplifier.

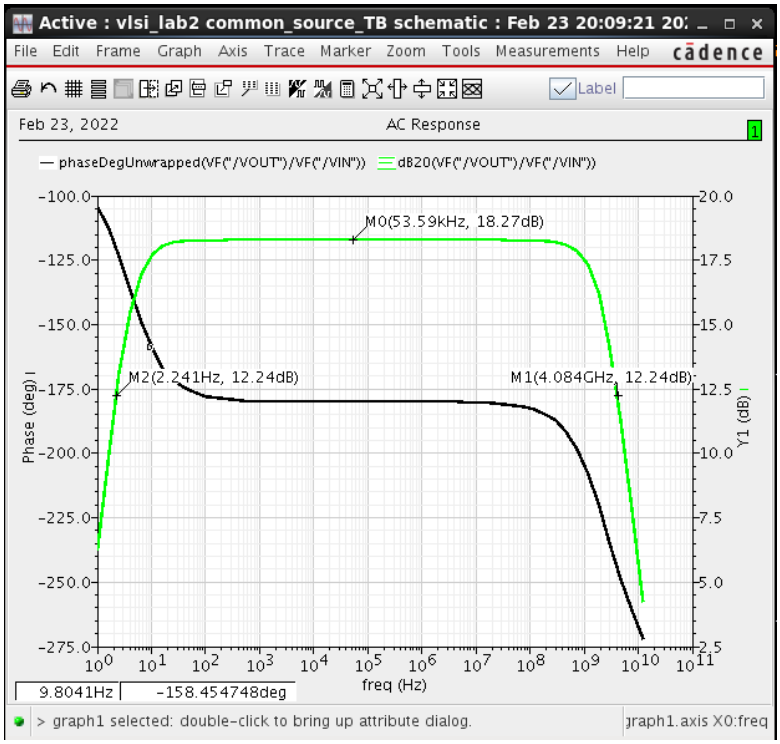
Internals of the symbol:



Testbench circuit:



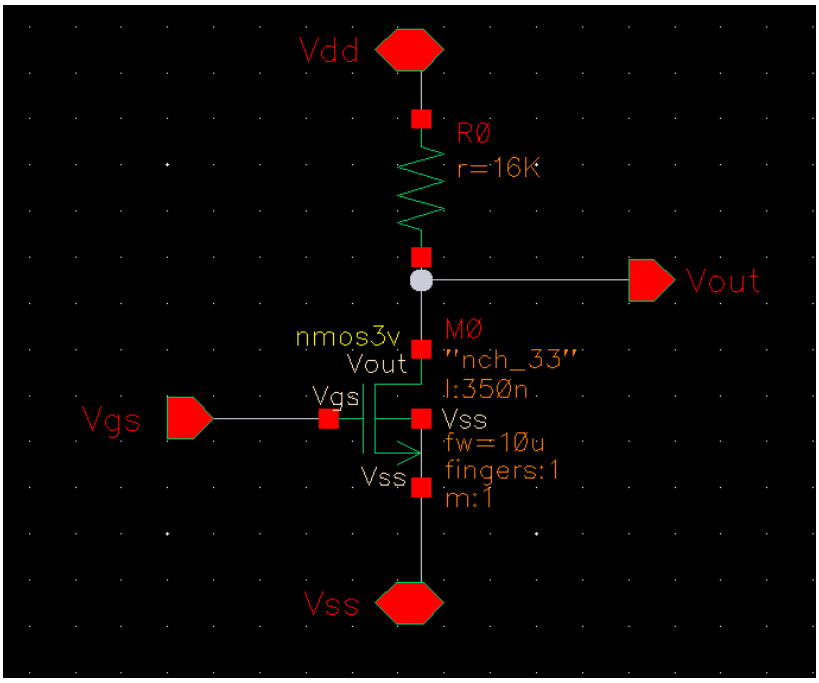
Gain and phase for a frequency range of 1Hz - 12 GHz:



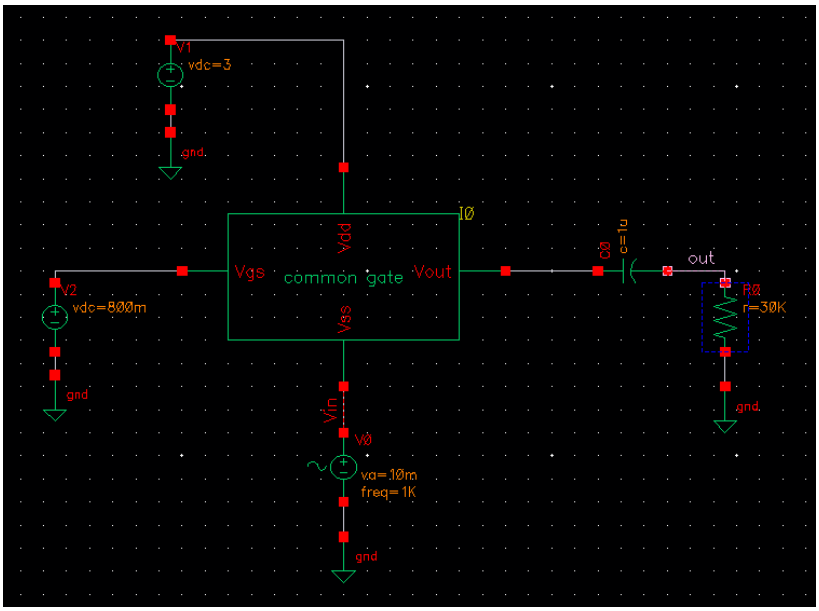
Lab Assignments:

Task#1: Transient & Ac analysis of CG amplifier.

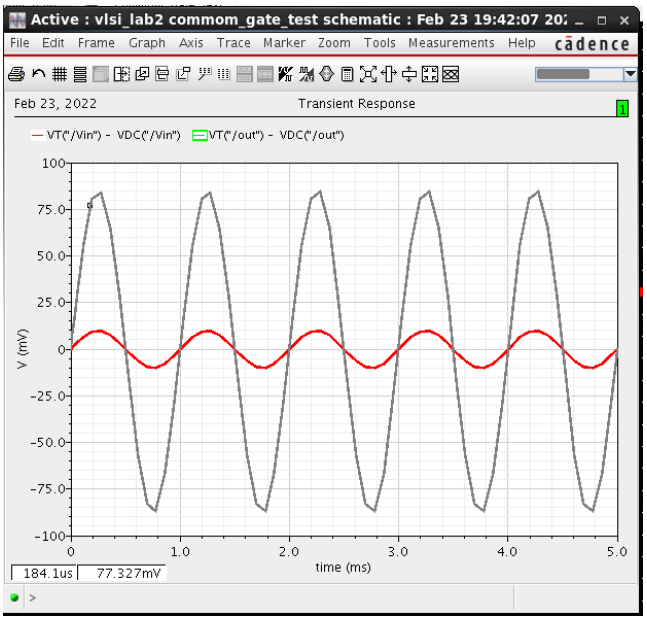
Internals of the symbol:



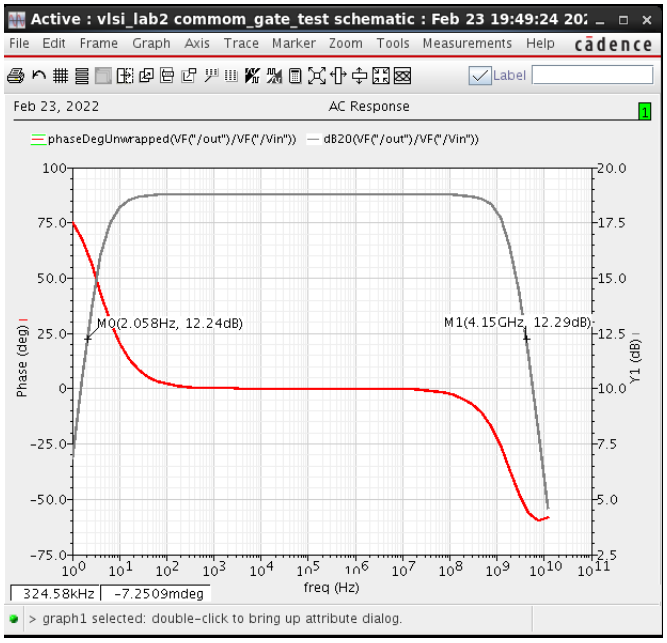
Testbench circuit:



Input Vs Output:

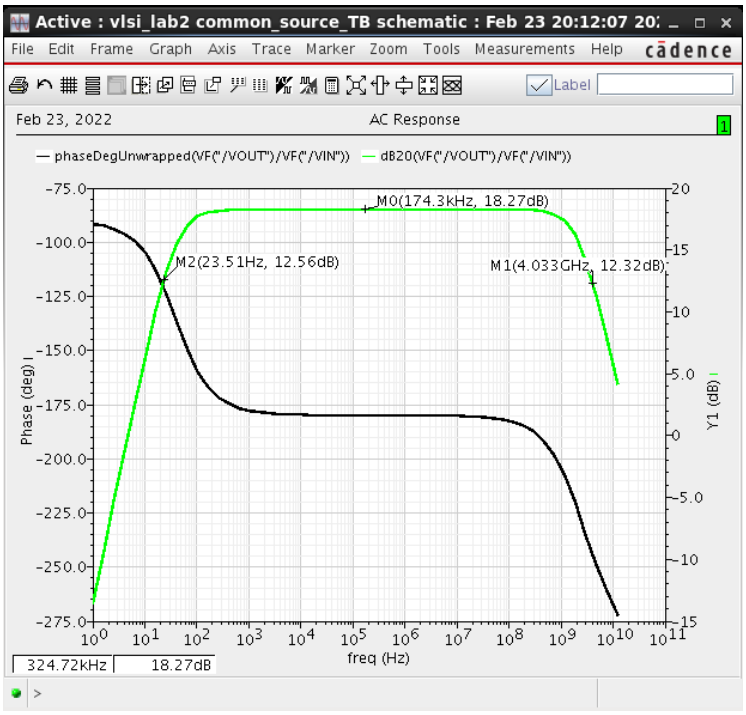


Gain and phase for a frequency range of 1Hz - 12 GHz:

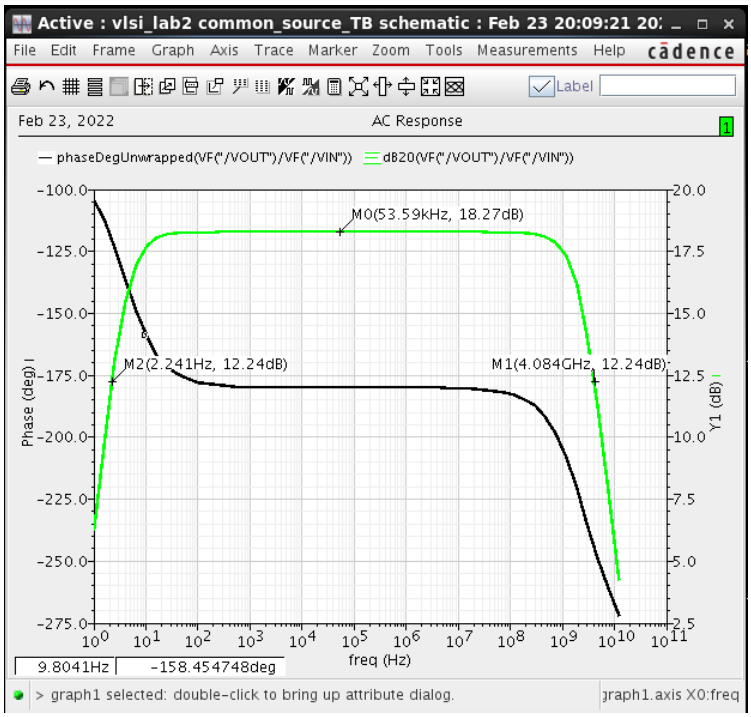


Task#2: Effect of different load capacitance on CS amplifier.

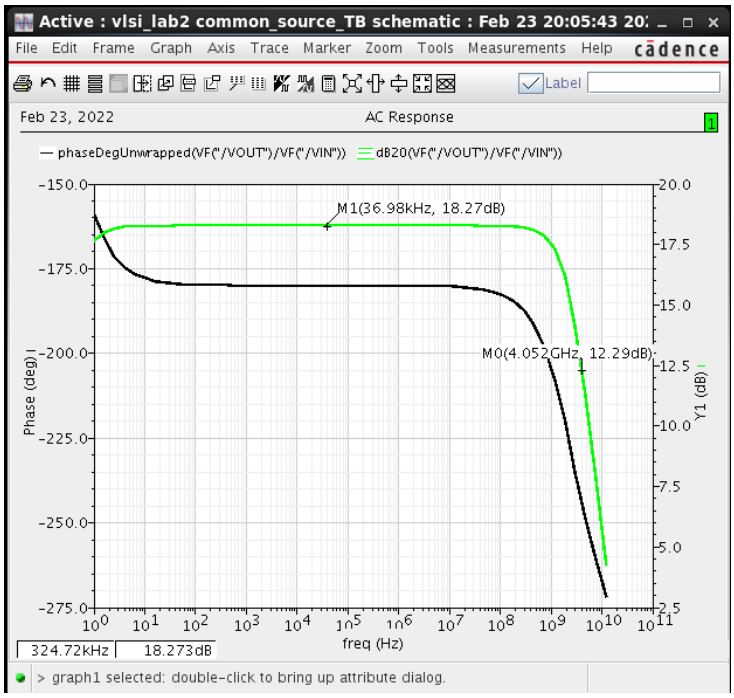
1) 100 nF


Active : vlsi_lab2 common_source_TB schematic : Feb 23 20:12:07 20
File Edit Frame Graph Axis Trace Marker Zoom Tools Measurements Help
cadence
Label
Feb 23, 2022
AC Response
1
phaseDegUnwrapped(VF("/VOUT")/VF("/VIN"))
dB20(VF("/VOUT")/VF("/VIN"))
M0(174.3kHz, 18.27dB)
M2(23.51Hz, 12.56dB)
M1(4.033GHz, 12.32dB)
Phase (deg)
Y1 (dB)
freq (Hz)
324.72kHz
18.27dB

2) 1 µF


Active : vlsi_lab2 common_source_TB schematic : Feb 23 20:09:21 20
File Edit Frame Graph Axis Trace Marker Zoom Tools Measurements Help
cadence
Label
Feb 23, 2022
AC Response
1
phaseDegUnwrapped(VF("/VOUT")/VF("/VIN"))
dB20(VF("/VOUT")/VF("/VIN"))
M0(53.59kHz, 18.27dB)
M2(2.241Hz, 12.24dB)
M1(4.084GHz, 12.24dB)
Phase (deg)
Y1 (dB)
freq (Hz)
9.8041Hz
-158.454748deg
> graph1 selected: double-click to bring up attribute dialog.
graph1.axis X0:freq

3) 10 µF



Observation: It is observed that the mid-band gain remained the same in all three cases but the bandwidth increased with effective movement in the lower cutoff frequency towards 0 Hz as we increased the capacitance.