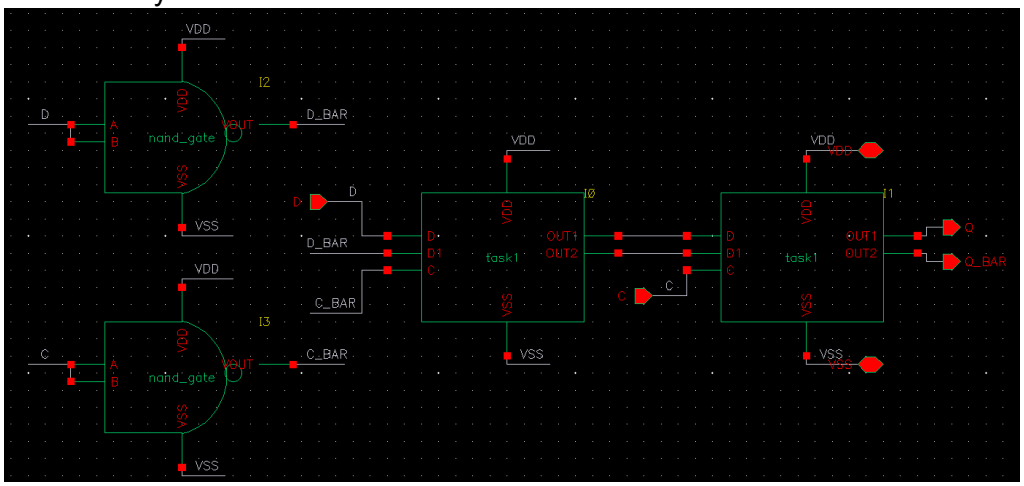
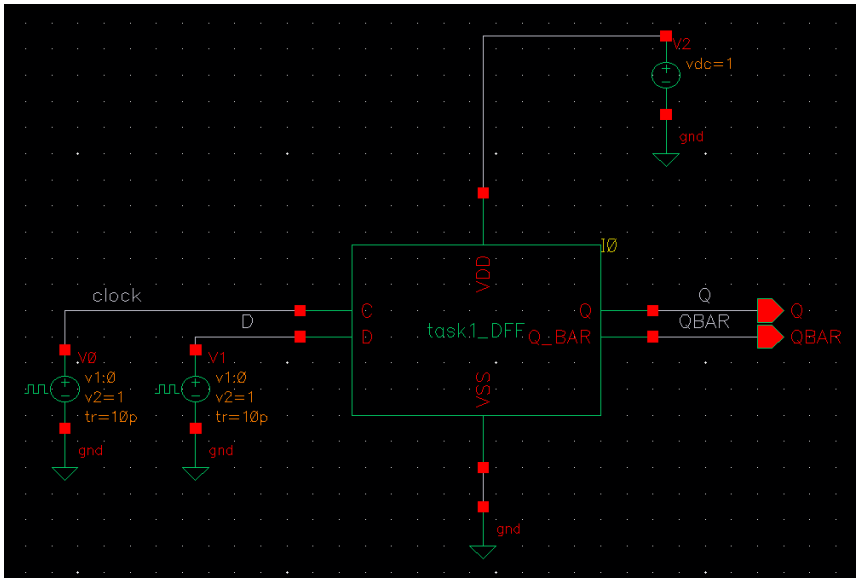
Analog Flow:

Apart from spice simulation and characterization of CMOS circuits, I also designed the schematic and layout of a D-type flip flop using Cadence Virtuoso as shown below.

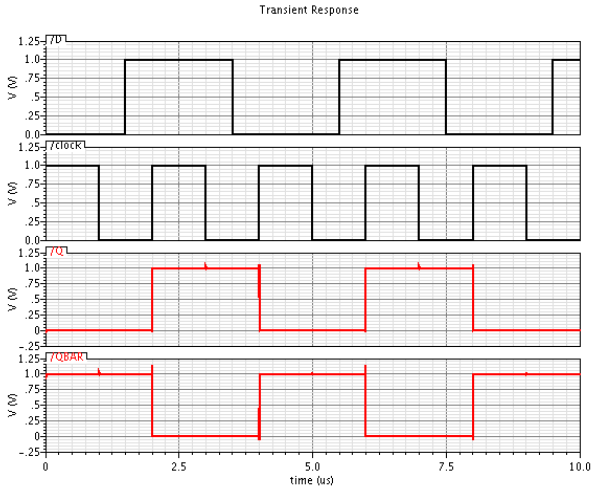
- Internals of the symbol:



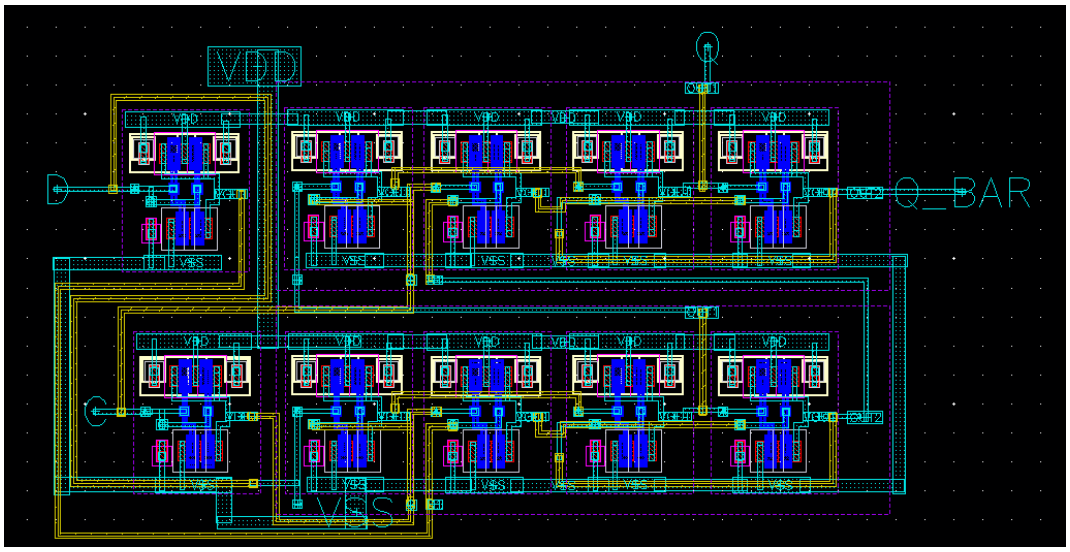
- Test Circuit:



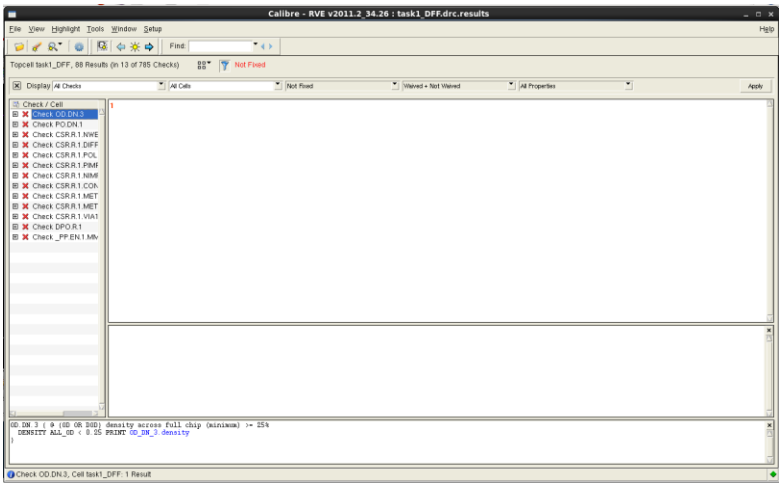
- Plot:



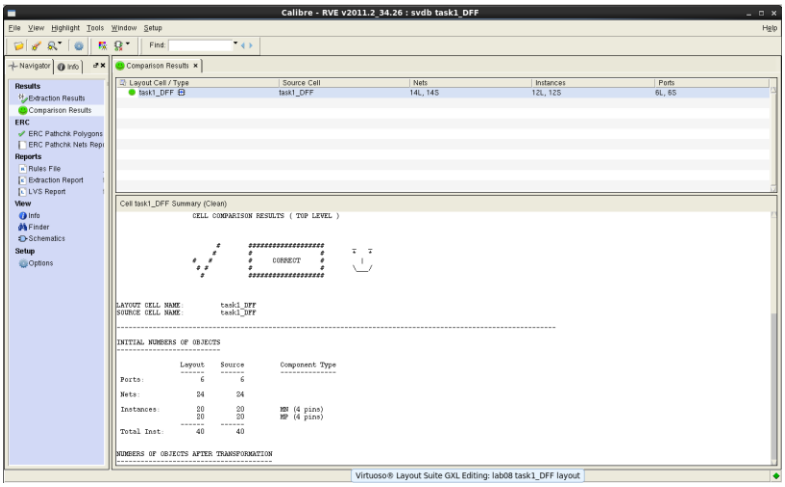
- Layout:



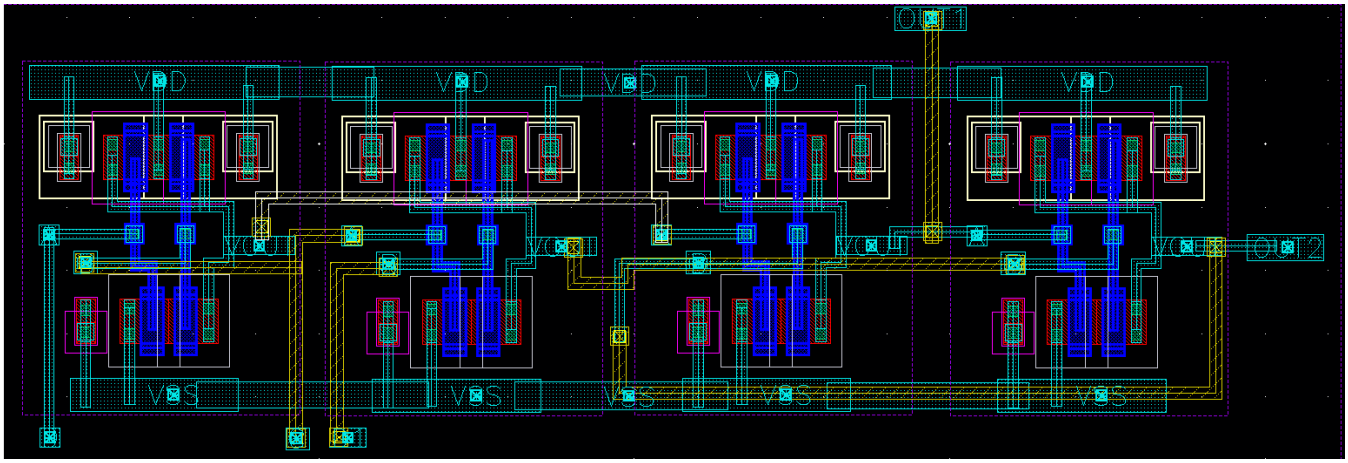
- DRC Results:



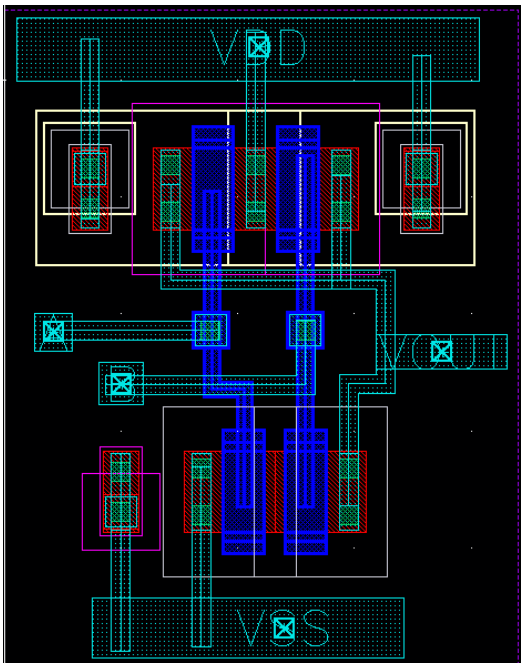
- LVS Results:



- Layout of an Individual latch:



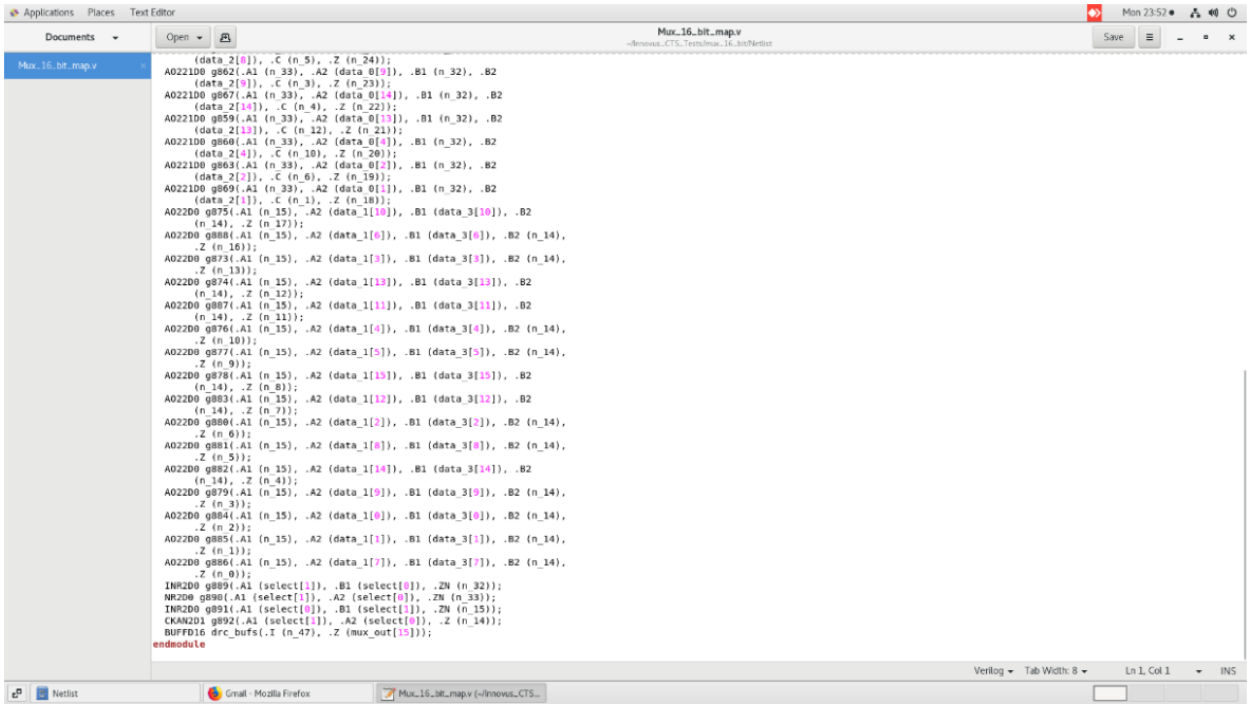
- Layout of an individual NAND Gate:



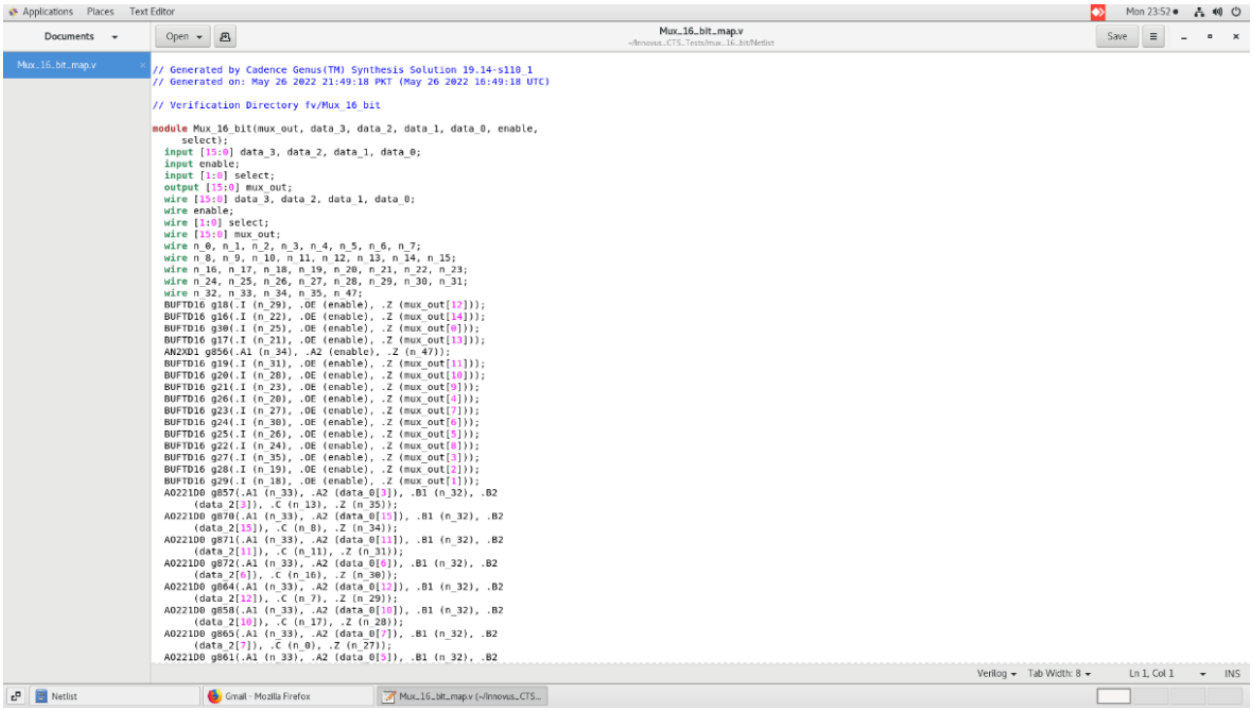
Digital Flow:

Physical layout of a 16*1 mux using the netlist synthesized from the Verilog code.

- Netlist



```
      (data_2[8]), .C (n_5), .Z (n_24));
A0221D0 g862(.A1 (n_33), .A2 (data_0[9]), .B1 (n_32), .B2
      (data_2[9]), .C (n_3), .Z (n_23));
A0221D0 g867(.A1 (n_33), .A2 (data_0[14]), .B1 (n_32), .B2
      (data_2[14]), .C (n_4), .Z (n_22));
A0221D0 g859(.A1 (n_33), .A2 (data_0[13]), .B1 (n_32), .B2
      (data_2[13]), .C (n_12), .Z (n_21));
A0221D0 g860(.A1 (n_33), .A2 (data_0[4]), .B1 (n_32), .B2
      (data_2[4]), .C (n_10), .Z (n_20));
A0221D0 g863(.A1 (n_33), .A2 (data_0[2]), .B1 (n_32), .B2
      (data_2[2]), .C (n_6), .Z (n_19));
A0221D0 g869(.A1 (n_33), .A2 (data_0[1]), .B1 (n_32), .B2
      (data_2[1]), .C (n_1), .Z (n_18));
A022D0 g875(.A1 (n_15), .A2 (data_1[10]), .B1 (data_3[10]), .B2
      (n_14), .Z (n_17));
A022D0 g888(.A1 (n_15), .A2 (data_1[6]), .B1 (data_3[6]), .B2 (n_14),
     .Z (n_16));
A022D0 g873(.A1 (n_15), .A2 (data_1[3]), .B1 (data_3[3]), .B2 (n_14),
     .Z (n_13));
A022D0 g874(.A1 (n_15), .A2 (data_1[13]), .B1 (data_3[13]), .B2
      (n_14), .Z (n_12));
A022D0 g887(.A1 (n_15), .A2 (data_1[11]), .B1 (data_3[11]), .B2
      (n_14), .Z (n_11));
A022D0 g876(.A1 (n_15), .A2 (data_1[4]), .B1 (data_3[4]), .B2 (n_14),
     .Z (n_10));
A022D0 g877(.A1 (n_15), .A2 (data_1[5]), .B1 (data_3[5]), .B2 (n_14),
     .Z (n_9));
A022D0 g878(.A1 (n_15), .A2 (data_1[15]), .B1 (data_3[15]), .B2
      (n_14), .Z (n_8));
A022D0 g883(.A1 (n_15), .A2 (data_1[12]), .B1 (data_3[12]), .B2
      (n_14), .Z (n_7));
A022D0 g880(.A1 (n_15), .A2 (data_1[2]), .B1 (data_3[2]), .B2 (n_14),
     .Z (n_6));
A022D0 g881(.A1 (n_15), .A2 (data_1[8]), .B1 (data_3[8]), .B2 (n_14),
     .Z (n_5));
A022D0 g882(.A1 (n_15), .A2 (data_1[14]), .B1 (data_3[14]), .B2
      (n_14), .Z (n_4));
A022D0 g879(.A1 (n_15), .A2 (data_1[9]), .B1 (data_3[9]), .B2 (n_14),
     .Z (n_3));
A022D0 g884(.A1 (n_15), .A2 (data_1[0]), .B1 (data_3[0]), .B2 (n_14),
     .Z (n_2));
A022D0 g885(.A1 (n_15), .A2 (data_1[1]), .B1 (data_3[1]), .B2 (n_14),
     .Z (n_1));
A022D0 g886(.A1 (n_15), .A2 (data_1[7]), .B1 (data_3[7]), .B2 (n_14),
     .Z (n_0));
INR2D0 g889(.A1 (select[1]), .B1 (select[0]), .ZN (n_32));
NR2D0 g890(.A1 (select[1]), .A2 (select[0]), .ZN (n_33));
INR2D0 g891(.A1 (select[0]), .B1 (select[1]), .ZN (n_15));
CKAN2D1 g892(.A1 (select[1]), .A2 (select[0]), .Z (n_14));
BUFFD16 drc_bufs(.I (n_47), .Z (mux_out[15]));
endmodule
```

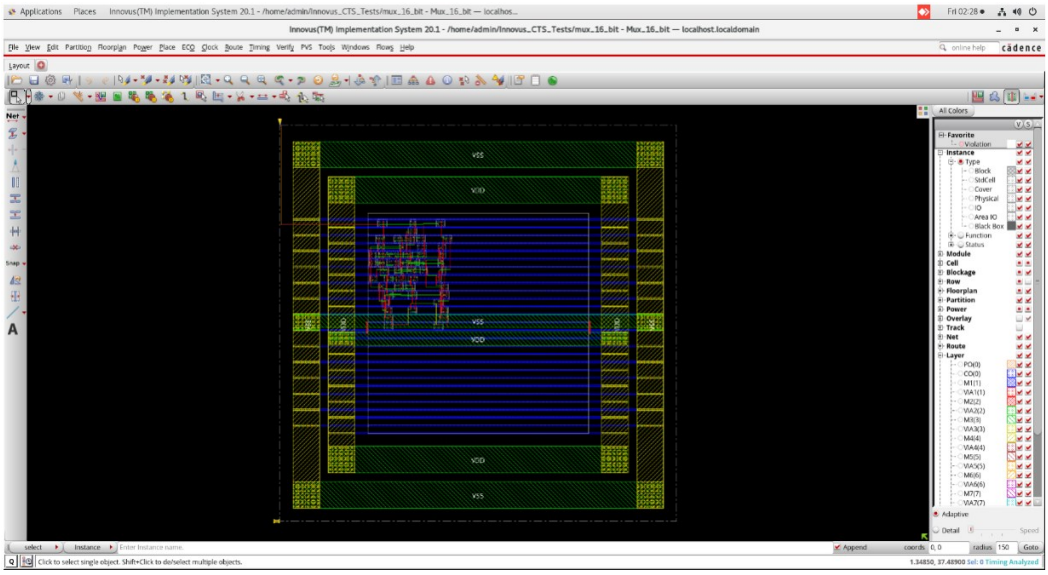


```
// Generated by Cadence Genus(TM) Synthesis Solution 19.14-s110_1
// Generated on: May 26 2022 21:49:18 PKT (May 26 2022 16:49:18 UTC)

// Verification Directory fv/Mux_16_bit

module Mux_16_bit(mux_out, data_3, data_2, data_1, data_0, enable,
     select);
  input [15:0] data_3, data_2, data_1, data_0;
  input enable;
  input [1:0] select;
  output [15:0] mux_out;
  wire [15:0] data_3, data_2, data_1, data_0;
  wire enable;
  wire [1:0] select;
  wire [15:0] mux_out;
  wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
  wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
  wire n_16, n_17, n_18, n_19, n_20, n_21, n_22, n_23;
  wire n_24, n_25, n_26, n_27, n_28, n_29, n_30, n_31;
  wire n_32, n_33, n_34, n_35, n_47;
  BUFTD16 g18(.I (n_29), .OE (enable), .Z (mux_out[12]));
  BUFTD16 g16(.I (n_22), .OE (enable), .Z (mux_out[14]));
  BUFTD16 g30(.I (n_25), .OE (enable), .Z (mux_out[0]));
  BUFTD16 g17(.I (n_21), .OE (enable), .Z (mux_out[13]));
  AN2XD1 g856(.A1 (n_34), .A2 (enable), .Z (n_47));
  BUFTD16 g19(.I (n_31), .OE (enable), .Z (mux_out[11]));
  BUFTD16 g20(.I (n_28), .OE (enable), .Z (mux_out[10]));
  BUFTD16 g21(.I (n_23), .OE (enable), .Z (mux_out[9]));
  BUFTD16 g26(.I (n_20), .OE (enable), .Z (mux_out[4]));
  BUFTD16 g23(.I (n_27), .OE (enable), .Z (mux_out[7]));
  BUFTD16 g24(.I (n_30), .OE (enable), .Z (mux_out[6]));
  BUFTD16 g25(.I (n_26), .OE (enable), .Z (mux_out[5]));
  BUFTD16 g22(.I (n_24), .OE (enable), .Z (mux_out[8]));
  BUFTD16 g27(.I (n_35), .OE (enable), .Z (mux_out[3]));
  BUFTD16 g28(.I (n_19), .OE (enable), .Z (mux_out[2]));
  BUFTD16 g29(.I (n_18), .OE (enable), .Z (mux_out[1]));
  A0221D0 g857(.A1 (n_33), .A2 (data_0[3]), .B1 (n_32), .B2
       (data_2[3]), .C (n_13), .Z (n_35));
  A0221D0 g870(.A1 (n_33), .A2 (data_0[15]), .B1 (n_32), .B2
       (data_2[15]), .C (n_8), .Z (n_34));
  A0221D0 g871(.A1 (n_33), .A2 (data_0[11]), .B1 (n_32), .B2
       (data_2[11]), .C (n_11), .Z (n_31));
  A0221D0 g872(.A1 (n_33), .A2 (data_0[6]), .B1 (n_32), .B2
       (data_2[6]), .C (n_16), .Z (n_30));
  A0221D0 g864(.A1 (n_33), .A2 (data_0[12]), .B1 (n_32), .B2
       (data_2[12]), .C (n_7), .Z (n_29));
  A0221D0 g858(.A1 (n_33), .A2 (data_0[10]), .B1 (n_32), .B2
       (data_2[10]), .C (n_17), .Z (n_28));
  A0221D0 g865(.A1 (n_33), .A2 (data_0[7]), .B1 (n_32), .B2
       (data_2[7]), .C (n_0), .Z (n_27));
  A0221D0 g861(.A1 (n_33), .A2 (data_0[5]), .B1 (n_32), .B2
```

- Layout


Innovus(TM) Implementation System 20.1 - /home/admin/Innovus_CTS_Tests/mux_16_bit - Mux_16_bit — localhost.localdomain
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
cadence
Layout
Net
All Colors
Favorite
Violation
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black-box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
PO(0)
CO(0)
M1(1)
VIA1(1)
M2(2)
VIA2(2)
M3(3)
VIA3(3)
M4(4)
VIA4(4)
M5(5)
VIA5(5)
M6(6)
VIA6(6)
M7(7)
VIA7(7)
Adaptive
Detail
Speed
VSS
VDD
VSS
VDD
VSS
select
Instance
Enter Instance name.
Append
coords 0, 0
radius 150
Goto
Click to select single object. Shift+Click to de/select multiple objects.
1.34850, 37.48900 Sel: 0 Timing Analyzed