Name:

EECE 7352: Computer Architecture
Quiz 1

Q1. (5 points) Assume a hypothetical program that spends 40% of its time in multiplication operations and 30% of time in performing I/O operations. These are operations are disjoint set of operations. This hypothetical program takes 60 seconds to execute. You are given two optimization options, which one will you prefer if you can choose only one?

(a) A multiplication operation is sped up by 20% using the proposed optimization. Assume that each multiplication instruction takes equal amount of time.
(b) Each I/O operation takes exactly 1 second. Using the proposed optimization, the latency of an I/O operation reduces to 0.5 second.

Q2. (5 points) Suppose that a chip's microarchitecture was modified in such a way that the clock rate of this chip was increased by a factor of 20. Recall that clock rate is inverse of clock time (or cycle time). As a result of an increase in the clock rate, the (average) cycles per instruction (CPI) for a given program increased by 50%. Our goal is to reduce the overall runtime of the program (i.e., improve its performance). Calculate the minimum fraction of instructions in the original program that the compiler must eliminate in order to improve the performance (i.e, obtain some speedup over the original chip when the clock rate was not increased).