Name:

EECE 7352: Computer Architecture
Quiz 2

Q1. (4 points) Assume traditional 5-stage pipeline that we have learned and discussed in class. How many cycles will the following code segment take to execute? You can assume that (1) bypassing is enabled, and (2) register file is written in the first half and read in the second half.

```
ADD R1, R2, R3
ST  R1, #0(R3)
SUB R3, R1, R2
LD  R1, #0(R3)
```

Q2. (1 point) Assume traditional 5-stage pipeline that we have learned and discussed in class. How many cycles will the following code segment take to execute? You should assume that (1) bypassing is *not* enabled, and (2) register file is written in the first half and read in the second half.

```
ADD R1, R2, R3
LD  R3, #0(R1)
SUB R4, R3, R1
MUL R2, R6, R7
```

Q3. (1 point) Assume traditional 5-stage pipeline that we have learned and discussed in class. How many cycles will the following code segment take to execute? You should assume that (1) bypassing is *not* enabled, and (2) register file is written in the first half and read in the second half.

```
ADD R1, R2, R3
MUL R2, R6, R7
LD  R3, #0(R1)
SUB R4, R3, R1
```

Q4. (2 points) Assume traditional 5-stage pipeline that we have learned and discussed in class. How many cycles will the following code segment take to execute? You can assume that (1) bypassing is enabled, and (2) register file is written in the first half and read in the second half.

```
ADD R1, R2, R3
LD  R3, #0(R1)
SUB R4, R3, R1
MUL R2, R6, R7
```

Q5. (2 points) Assume traditional 5-stage pipeline that we have learned and discussed in class. How many cycles will the following code segment take to execute? You can assume that (1) bypassing is enabled, and (2) register file is written in the first half and read in the second half.

```
ADD R1, R2, R3
MUL R2, R6, R7
LD  R3, #0(R1)
SUB R4, R3, R1
```