EECE 7352: Computer Architecture
Quiz 5

Q1. (2 point) Fully-associative caches have higher access latency compared to the direct mapped cache of the same cache size (and block size). True or False?

Q2. (2 points) True or False? A 2-way set-associative cache has more number of sets than 4-way set-associative cache of the same size (and block size). Assume 1MB cache size, 8 Byte cache block size, and 32-bit address space.

Q3. [6 points] Assume a 16-bit address space and byte-addressable memory. Consider a two-way set associative cache with a total of 256 sets, write-back policy, and perfect LRU replacement implementation. The entire cache has an overhead of a total of 3328 bits of storage (this is not the cache size). Overhead for a cache block and cache set may include: tag bits, valid bits (e.g., one bit for indicating the valid/not-valid status for each block in a set), sufficient bits to implement LRU policy (i.e., maintaining the perfect LRU order among the blocks in the set), and potential dirty bits depending on the write-policy (e.g., one bit for maintaining dirty status if write-back policy is in place). What is the block size of this cache?

Hint: 3328 = (2^8) x 13