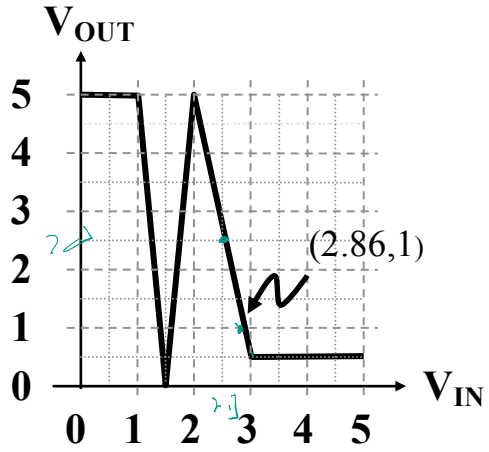
6.004 Tutorial Problems
L05 – The Digital Abstraction

Note: A small subset of essential problems are marked with a red star (★). We especially encourage you to try these out before recitation.

Problem 1. ★

Ms. Anna Logge, founder at a local MIT startup, has developed a device to be used as an inverter. Anna is considering the choice of parameters by which her logic family will represent logic values and needs your help.

The figure on the right shows the voltage transfer curve of a proposed inverter for a new logic family (you can find spare copies below).

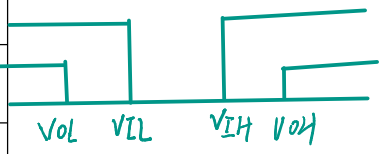


Several possible schemes for mapping logic values to voltages are being considered, as summarized in the incomplete table below. ***Noise Immunity*** **(the last row) is defined as the smaller of the two noise margins**.

Complete the table by filling in missing entries. Choose each value to maximize the noise margins of the corresponding scheme. **If the numbers in a scheme can't be completed such that the device functions as an inverter with positive noise margins, fill the entries for that column with *X*s.**

LNI's Possible Logic Mappings:

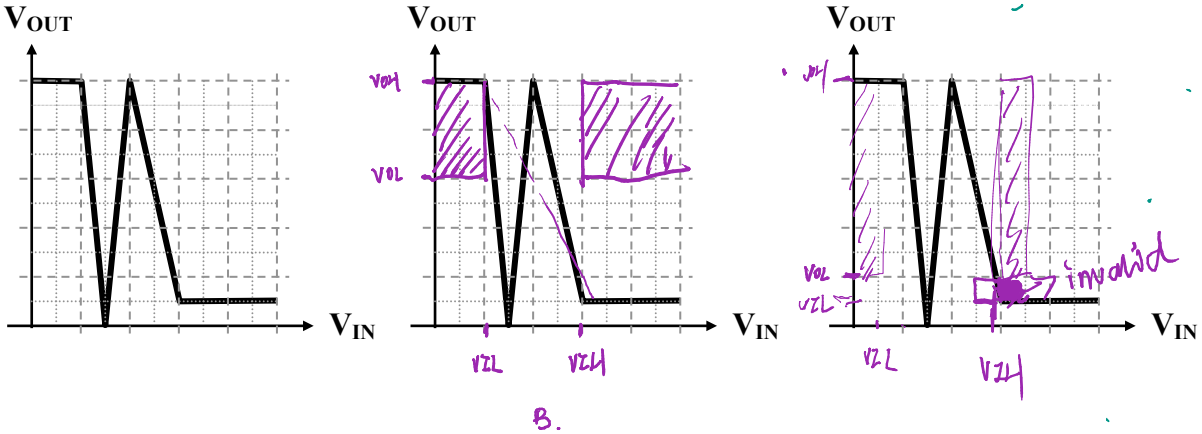
	Scheme A	Scheme B	Scheme C
V_{OL}	X	0.5	1
V_{IL}	2	1	0.5
V_{IH}	X	3	X
V_{OH}	X	✓	X
Noise Immunity	X	0.5	X



C 1 0.5 2.86 ✓

B 0.5 1 3 ✓

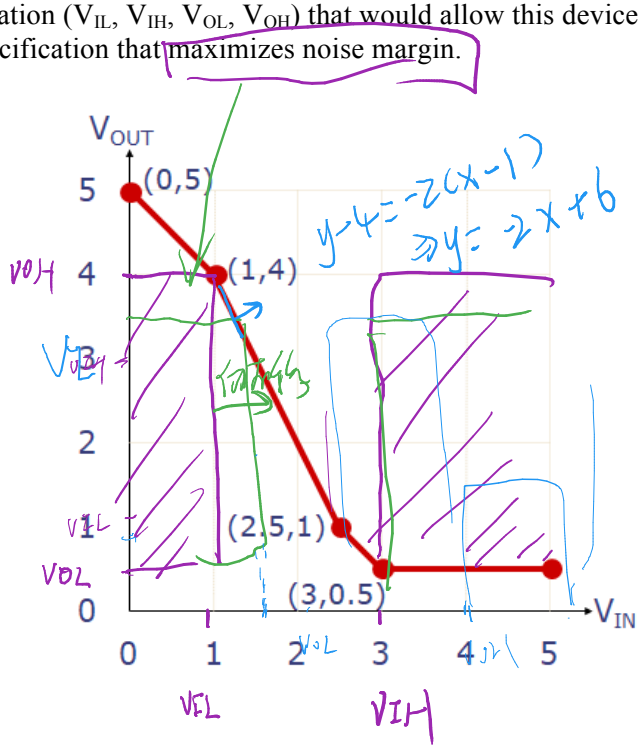
A 2 ✓



B.

Problem 2.

Suppose that you measured the voltage transfer curve of the device shown below. Can we find a signaling specification (V_{IL}, V_{IH}, V_{OL}, V_{OH}) that would allow this device to be a digital inverter? If so, give the specification that maximizes noise margin.



当两边NM相等时，NM取最大值

$V_{OH} - V_{IH} = V_{IL} - V_{OL}$

$\Rightarrow y - 3 = x - 0.5$

$\Rightarrow x = \frac{7}{6}$

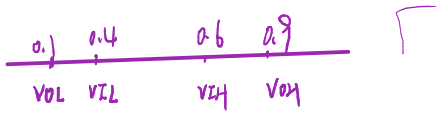
$y = \frac{11}{3}$

$\Rightarrow \begin{cases} V_{IL} = \frac{7}{6} \\ V_{OH} = \frac{11}{3} \end{cases}$

Problem 3. ★

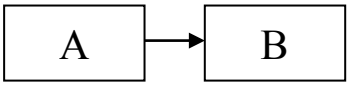
Suppose we define all signaling thresholds in our digital system to be relative to the supply voltage, V_{DD}:

- $V_{OL} = 0.1V_{DD}$
- $V_{IL} = 0.4V_{DD}$
- $V_{IH} = 0.6V_{DD}$
- $V_{OH} = 0.9V_{DD}$



We want to connect two types of digital devices, A and B, that use different supply voltages, $V_{DD,A}$ and $V_{DD,B}$. **We are given that $V_{DD,A}$ = 1V**.

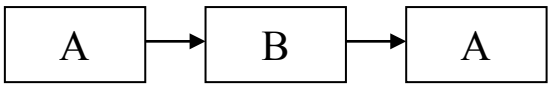
(1) In the circuit below, under what range of supply voltages $V_{DD,B}$ will the system work correctly?



$V_{OLA} \le V_{ILB}$

$V_{OHA} \ge V_{IHB}$ $\Rightarrow 0.25 \le V_{DD} \le 1.5$

(2) In the circuit below, under what range of supply voltages $V_{DD,B}$ will the system work correctly?



$V_{OLB} \le V_{ILA}$

$V_{OHB} \ge V_{IHB}$ $\Rightarrow \frac{2}{3} \le V_{DD} \le 1.5$

(3) For the same circuit as in part 2, under what range of supply voltages $V_{DD,B}$ will the system have noise margins of at least 0.1V?

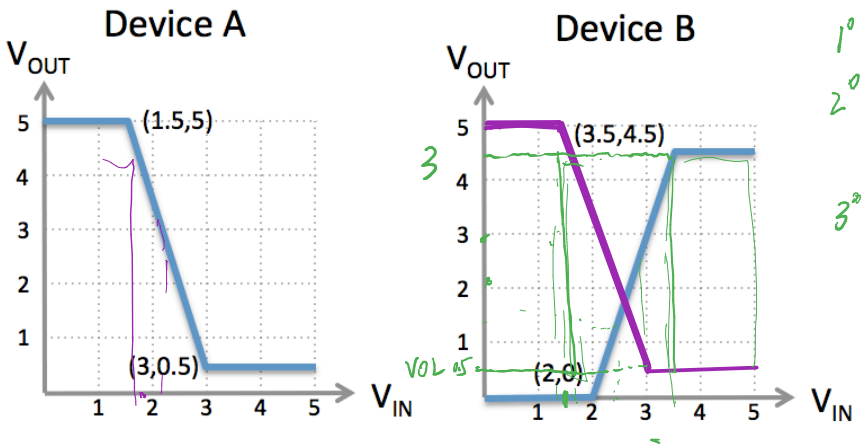
$0.2 \le V_{INB} \le V_{ILB} \Rightarrow V_{DD} \ge 0.5$

$0.8 \le V_{INB} \ge V_{IHB} \Rightarrow V_{DD} \le 0.75$

$\therefore 0.5 \le V_{DD} \le 0.75$

Problem 4. ★

The following are voltage transfer characteristics of single-input, single-output devices to be used in a new logic family:



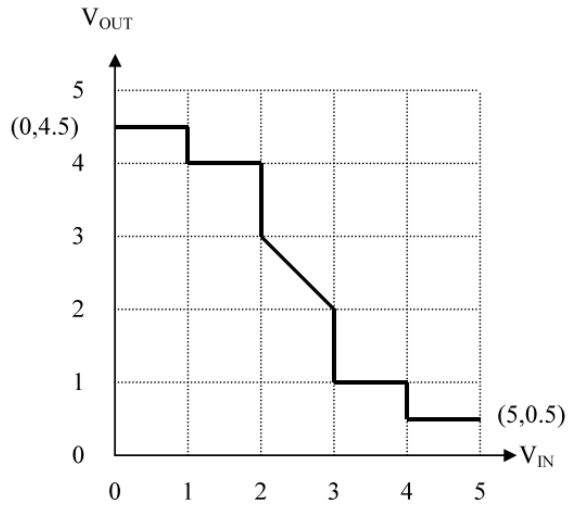
Your job is to choose a single set of signaling thresholds V_{OL}, V_{IL}, V_{OH}, and V_{IH} to be used with both devices to give the best noise margins you can. Recall that the VTC can touch the edge of the forbidden regions but not pass through those regions. Fill in your answers below, together with the resulting noise margins. You'll get partial credit for anything that works with nonzero noise margins; for full credit, maximize the noise immunity (i.e., the smaller of the two noise margins).

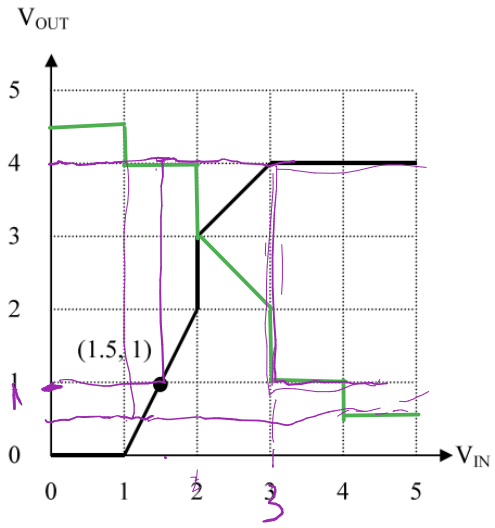
V_{OL} = _____ **V_{IL} =** _____ **V_{IH} =** _____ **V_{OH} =** _____

Low Noise Margin = _____ **High Noise Margin =** _____

Problem 5.

The following are voltage transfer characteristics of devices to be used in a new logic family as an inverter and buffer, respectively:



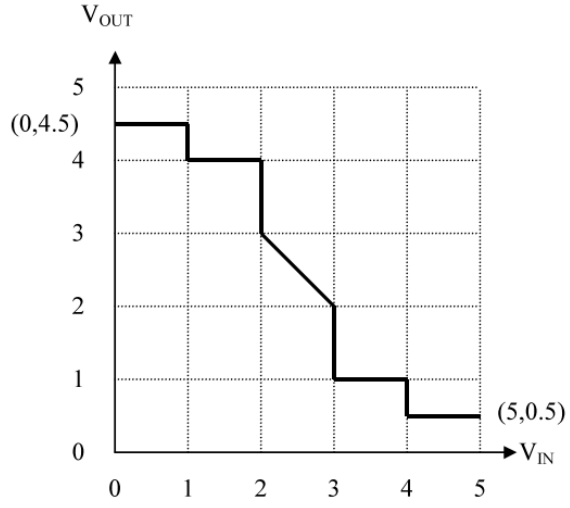


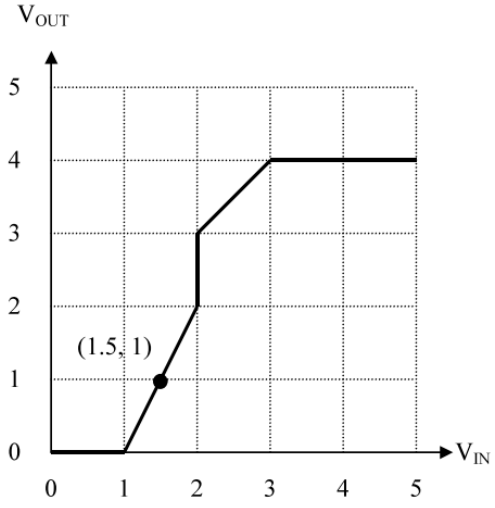
Your job is to choose a single set of signaling thresholds V_{OL}, V_{IL}, V_{OH}, and V_{IH} to be used with both devices to give the best noise margins you can. Recall that the VTC can touch the edge of the forbidden regions but not pass through those regions. Fill in your answers below, together with the resulting noise margins. You'll get partial credit for anything that works with nonzero noise margins; for full credit, maximize each of the noise margins.

V_{OL} = 1 **V_{IL} =** 1.5 **V_{IH} =** 3 **V_{OH} =** 4

Low Noise Margin = 0.5 **High Noise Margin =** 1

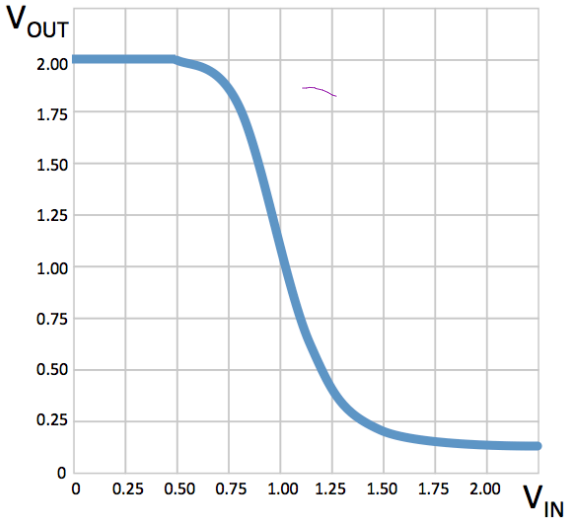
Scratch copy of the VTC diagrams:





Problem 6. ★

The voltage transfer curve for an inverter is shown to the right. The manufacturer decided to crowdsource the digital signaling specifications for their inverter and has received some suggestions for V_{OL}, V_{IL}, V_{IH}, and V_{OH}, presented in tabular form below.



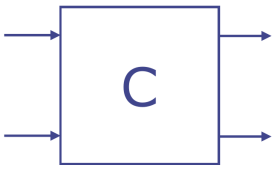
For each suggested specification, determine if the inverter would be a legitimate combinational device with non-zero positive noise margins. If it is a legitimate combinational device, give the noise immunity of the inverter (the smaller of the low and high noise margins) when operating under that specification. If the inverter wouldn't be a legitimate combinational device, please write NOT LEGIT in the rightmost column.

Fill in rightmost column for each suggested specification.

Suggestion	V_{OL}	V_{IL}	V_{IH}	V_{OH}	*Noise immunity, or NOT LEGIT*
#1	0.00	0.50	1.50	2.00	NOT LEGIT
#2	0.25	0.75	1.25	1.75	NOT LEGIT
#3	0.50	0.75	1.25	1.50	0.25
#4	0.75	0.50	1.75	1.50	NOT LEGIT

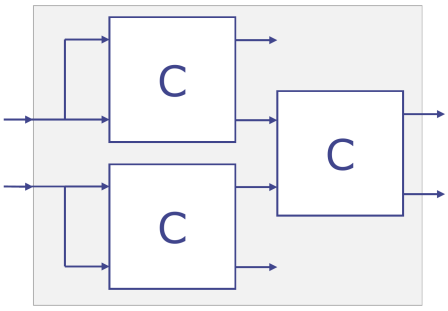
Problem 7. ★

The circuit C shown below is a 2-input, 2-output combinational device.

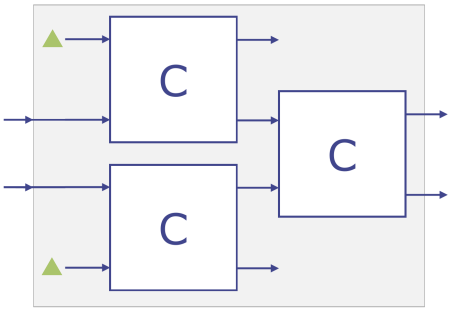


Each of the three circuits below contains multiple copies of circuit C. **Note**: the ▲ symbol indicates a "floating" input.

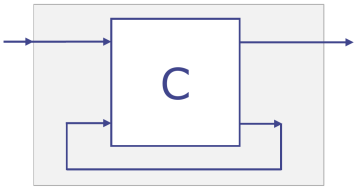
Circuit 1



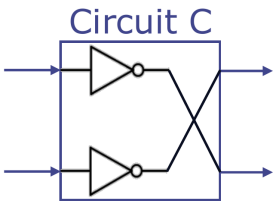
Circuit 2



Circuit 3



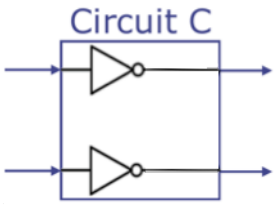
(A) Below is one possible implementation of C:



Given this implementation, determine which of the above circuits are combinational.

Circuit 1 ____ **Circuit 2** ____ **Circuit 3** ____

(B) Below is an alternative implementation of C:



Given this alternative implementation, determine which of the above circuits are combinational.

Circuit 1 ____ **Circuit 2** ____ **Circuit 3** ____