Schematic & Layout Deliberations

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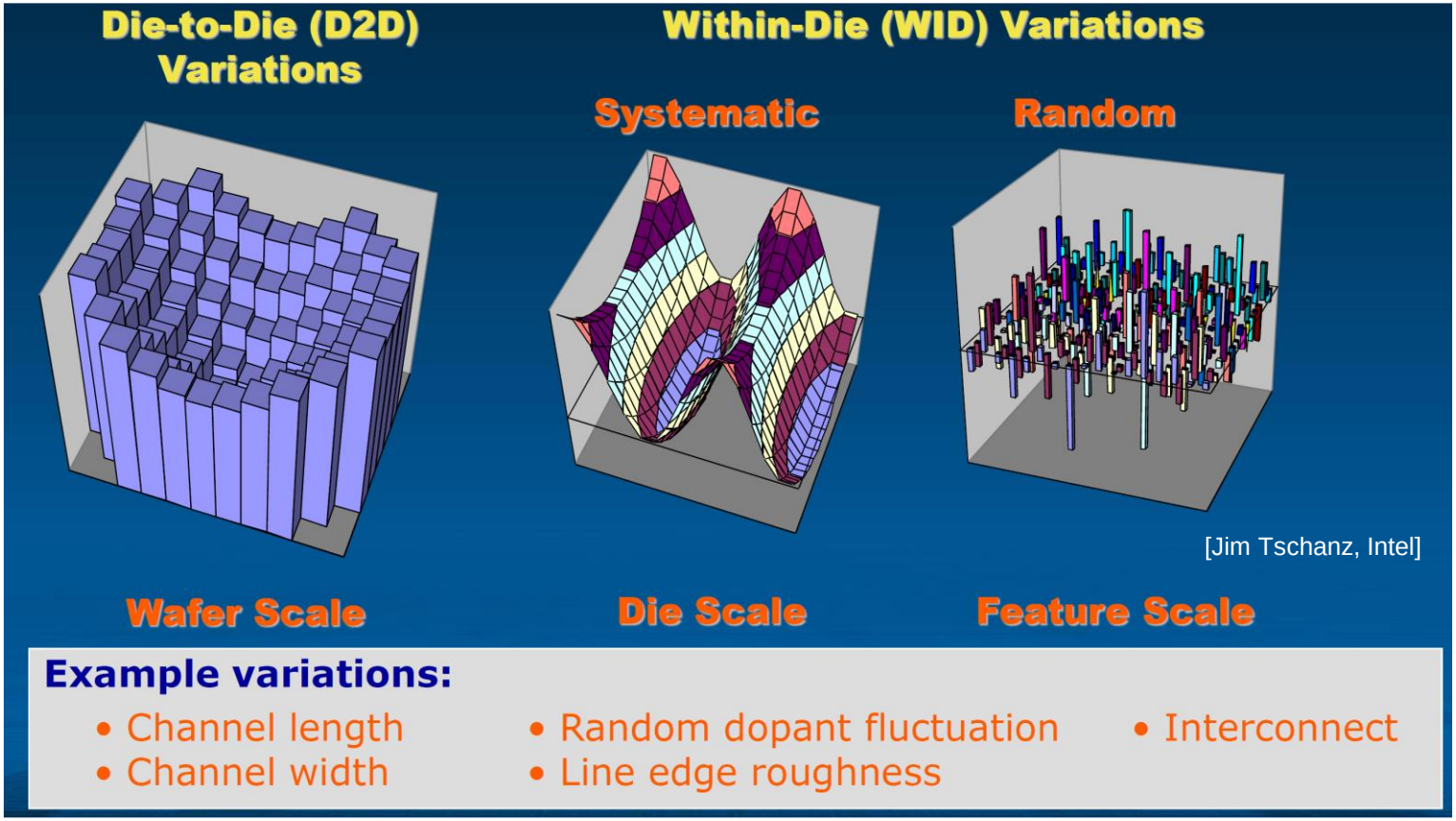
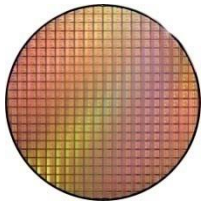
Parameter Variations in Integrated Circuits



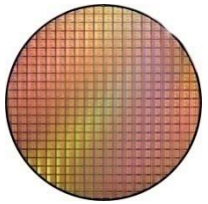
Affects all transistors (of the same type) in the same way

Causes differences between individual transistors (e.g., V_t)

Wafer-Level Variations



Wafer made yesterday
All NMOS are “slow”
All PMOS are “nominal”
All R are nominal
All C are “fast”



Wafer made today
All NMOS are “fast”
All PMOS are “fast”
All R are nominal
All C are “slow”

Examples:

Parameter	“Slow”	“Nominal”	“Fast”
V_t	0.4V	0.3V	0.2V
μC_{ox} (NMOS)	240 mA/V^2	300 mA/V^2	360 mA/V^2
μC_{ox} (PMOS)	80 mA/V^2	100 mA/V^2	120 mA/V^2
R_{poly}	60Ω/□	50Ω/□	40Ω/□
R_{nwell}	1.4 kΩ/□	1 kΩ/□	0.6 kΩ/□
C_{MIM}	1.15 fF/mm^2	1 fF/mm^2	0.85 fF/mm^2

2.1 NMOS

$V_{GS} \leq 1{,}65$ V @ 125°C

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Threshold Voltage Short Channel Device	VTN10x013	V	0.43	0.50	0.55	A.a1	WxL = 10 x 0.13 µm²
Threshold Voltage Long Channel Device	VTN10x10	V	0.16	0.20	0.24	A.a1	WxL = 10 x 10 µm²
Threshold Voltage Small Channel Device	VTN015x013	V	0.4	0.54	0.68	A.a1	WxL = 0.15 x 0.13 µm²
Saturation Current Short Channel Device	IDSN013	µA/µm	380	480	600	A.b1	WxL = 10 x 0.13 µm²
Off-Current Short Channel Device	IOFFN013	LOG10 (A/µm)		-10	-9	A.c1	WxL = 10 x 0.13 µm²
Drain Induced Barrier Lowering 0.1/1.2V	DIBLN013	mV/V	20	50	80	A.d1	WxL = 10 x 0.13 µm²
Sub Threshold Slope	SSN013	mV/dec	76	82	88	A.e	WxL = 10 x 0.13 µm²

2.12 MIM Capacitor

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Specific Area Capacitance	CMIMA	fF/µm²	1.35	1.5	1.65	A.k	
Specific Capacitance MIM Perimeter	CMIMP	aF/µm		*40*		A.l	
Breakdown Voltage	BVMIM	V	15	23		A.y	
Voltage Coefficients	VCMIM1 VCMIM2	ppm/V ppm/V²		*-26* *5*		A.ah	
Temperature Coefficient	TCMIM1 TCMIM2	ppm/K ppm/K²		*3.6* *0.002*		A.ad	
Matching Coefficient	KCMIM	nm					

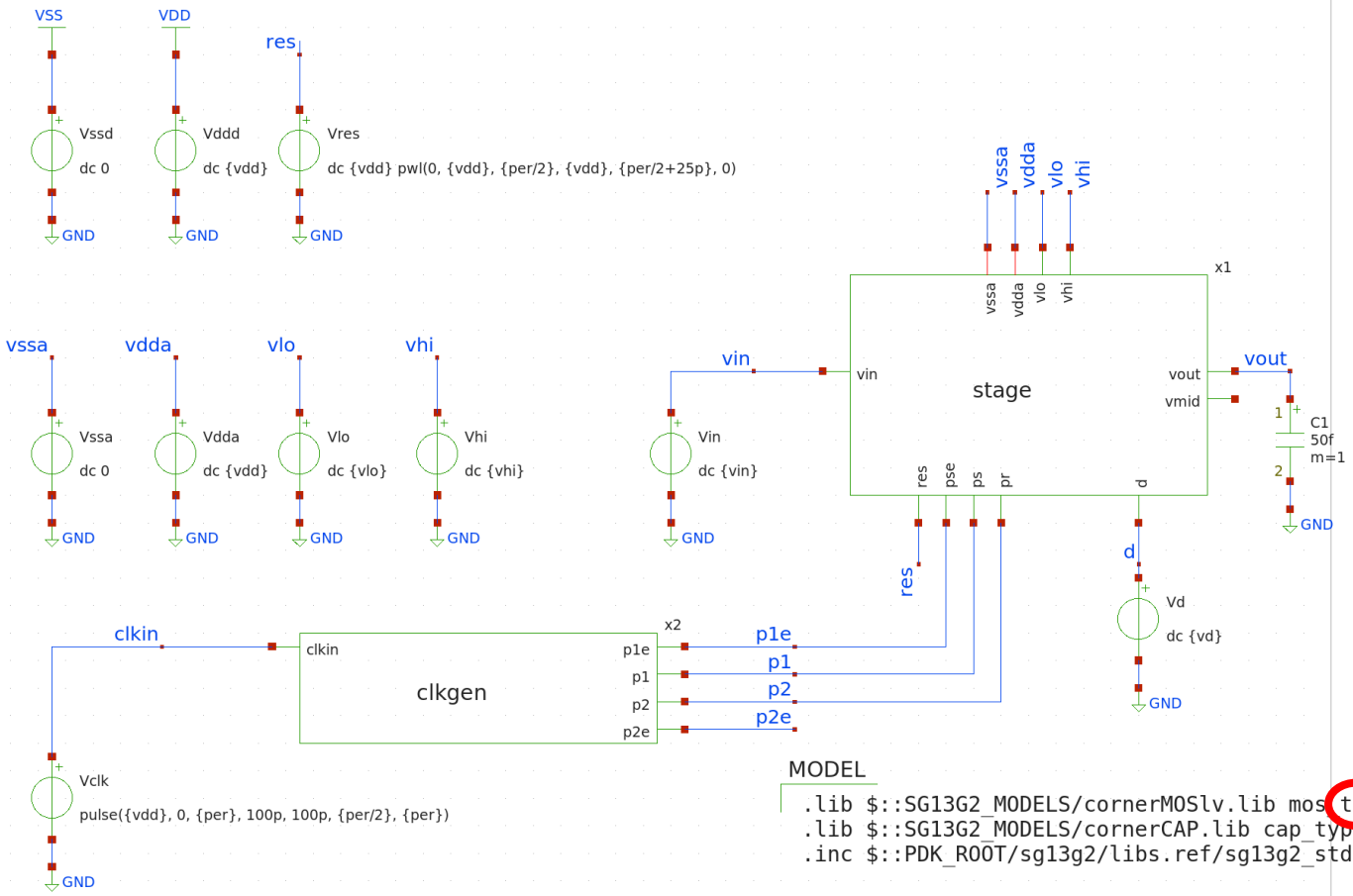
https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_process_spec.pdf

Characterization Across "Corners"

Corner T = −20 °C	TT	FF	FS	SF	SS
V_{out} (mV)	244.4	248.6	229.7	264.7	249.3
I_{DD} (nA)	256	475	243	227	104
DC Gain (dB)	49.8	52	50	50.4	47.4
UGF (MHz)	0.67	1.58	0.63	0.59	0.22
PM (degrees)	69.2	64.6	69	69.9	76.9
PSRR+ (dB)	54.4	56.7	54.7	55.2	52
PSRR- (dB)	56.9	58.9	57.1	57.4	54.7
1% Ts+/Ts- (ns)	685/438	272/182	566/337	854/336	2632/880
Corner T = 27 °C	**TT**	**FF**	**FS**	**SF**	**SS**
V_{out} (mV)	249.9	244.5	249.3	249.9	250
I_{DD} (nA)	488	579	505	479	485
DC Gain (dB)	51.3	51.7	52.1	50.4	51
UGF (MHz)	1.09	1.68	1.13	1.08	0.88
PM (degrees)	69.2	64.3	69.5	69	73.1
PSRR+ (dB)	56.1	56.7	56.9	55.2	55.7
PSRR- (dB)	58.2	58.5	59.8	58.9	58.3
1% Ts+/Ts- (ns)	520/319	240/207	506/322	519/321	719/490
Corner T = 80 °C	**TT**	**FF**	**FS**	**SF**	**SS**
V_{out} (mV)	255.8	249.1	233.9	277.1	259.8
I_{DD} (nA)	1177	2417	1338	1061	621
DC Gain (dB)	52.6	53	53	52.1	51.5
UGF (MHz)	2.2	5.68	2.5	1.98	0.97
PM (degrees)	74.3	77.3	75.8	73.3	73.4
PSRR+ (dB)	57.4	57.7	57.9	56.7	56.3
PSRR- (dB)	59.4	59.7	59.8	58.9	58.4
1% Ts+/Ts- (ns)	356/235	130/123	230/239	233/210	838/436

- Complexity explodes very quickly
  - E.g., 5 (process) x 3 (temperature) x 3 (supply voltage) = 45 tests!

Stage Testbench



NGSPICE

```
.param temp=27 per=20n vdd=1.2
.param vin=0.6 vlo=0.3 vhi=0.9 vd={vdd}
.option method=gear reltol=1e-4

.control
set wr_singlescale
set wr_vecnames
set color0 = white
tran 100p 60n
plot p2e vout
***
wrdata tb_stage_corners_tt.txt p2e vout
***
.endc
```

tt, ss, ff

MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
.lib $::SG13G2_MODELS/cornerCAP.lib cap_typ
.inc $::PDK_ROOT/sg13g2/libs.ref/sg13g2_stdcell/spice/sg13g2_stdcell.spice
```

XSCHEM

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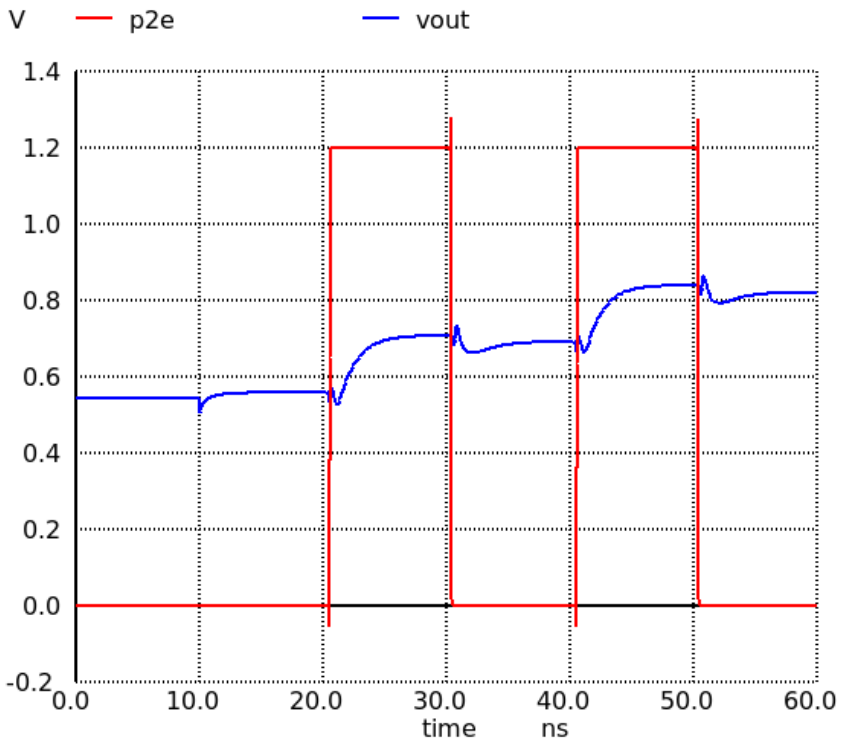
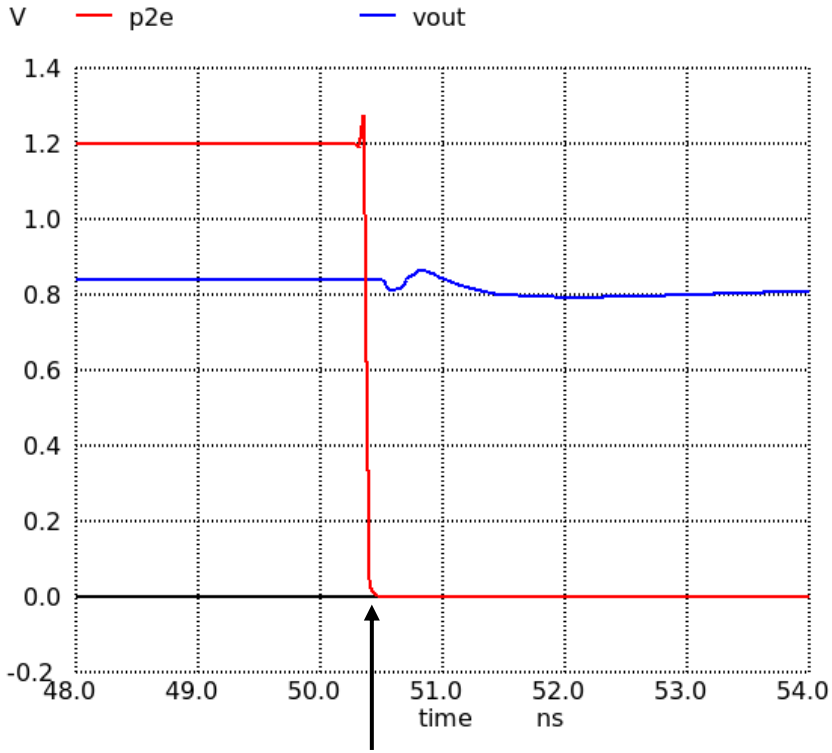
/foss/designs/tb_stage_corners.sch

2024-04-03 03:06:35



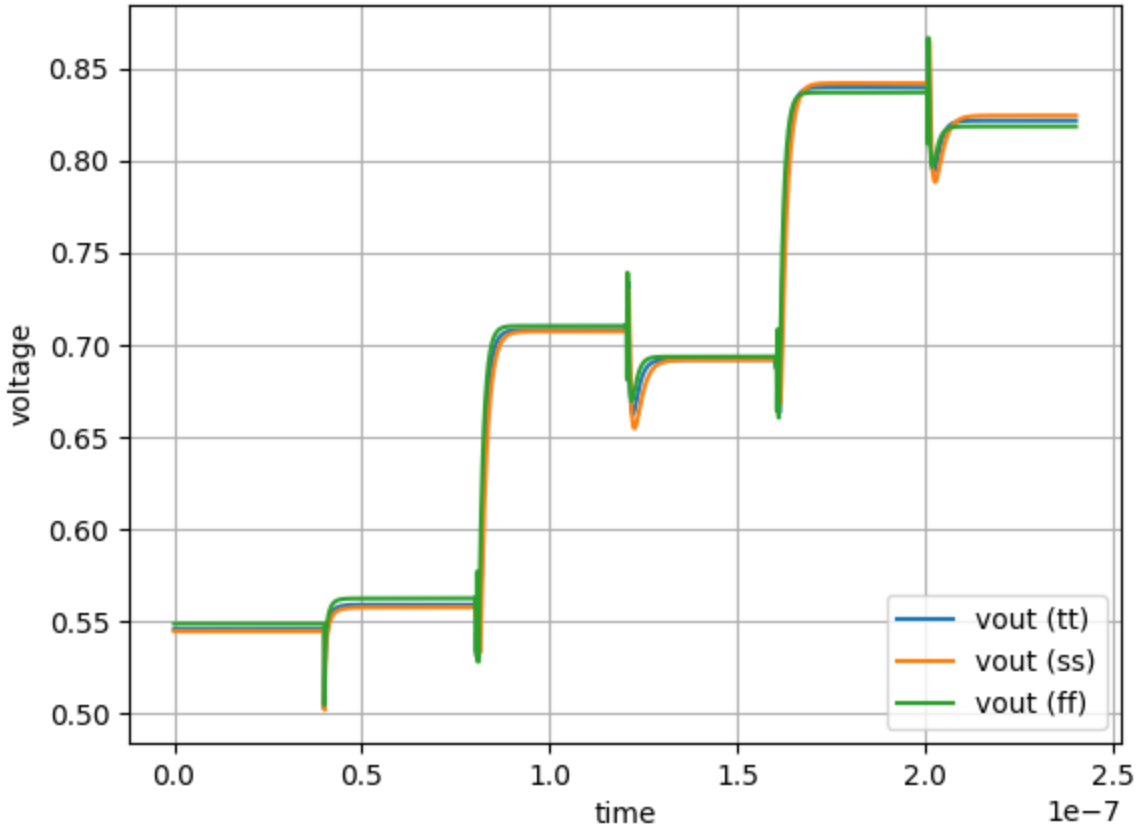


Next stage samples here

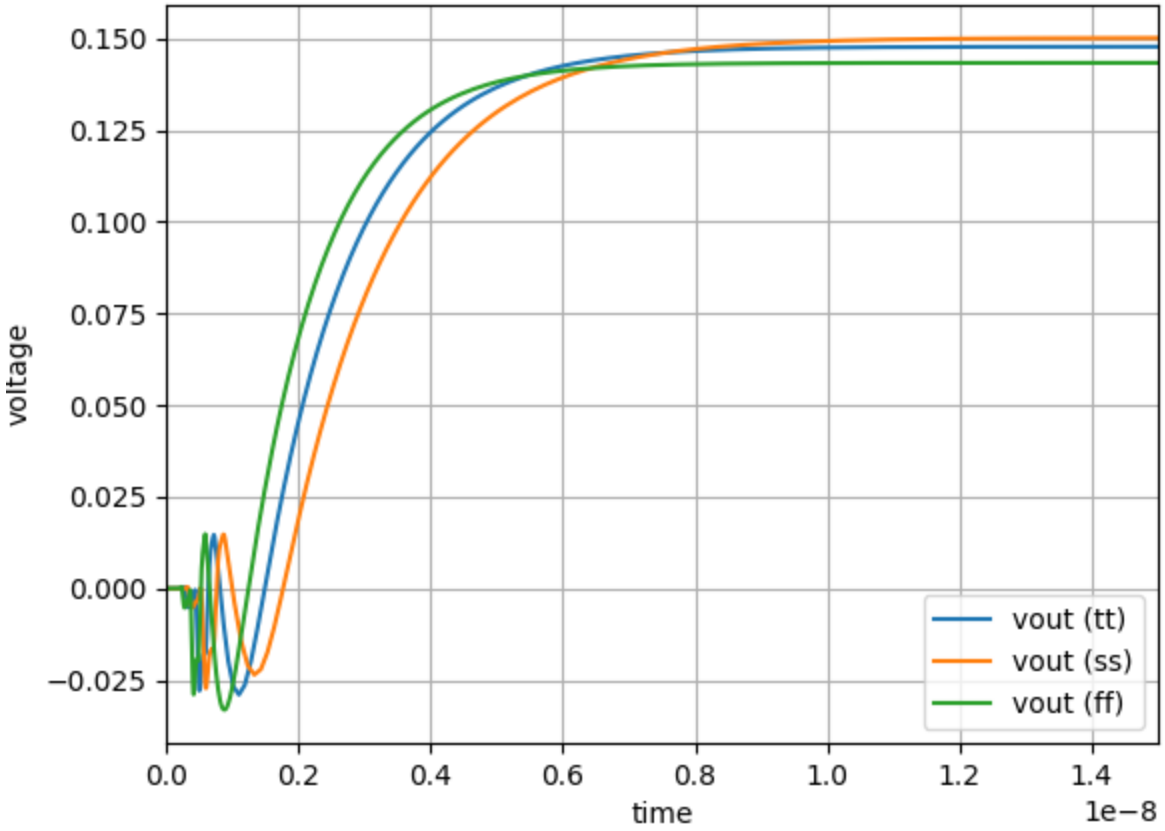
- How close to the “final value” are we at the sampling instant?
  - This is called the dynamic settling error (measured in percent)
- How does the dynamic settling error across corners?
- Need to slow down clock frequency to measure final value (e.g., 4x)

Output with per = 80ns

https://github.com/bmurmann/EE628/blob/main/5_Design/3_Real_circuits/tb_stage_corners.ipynb

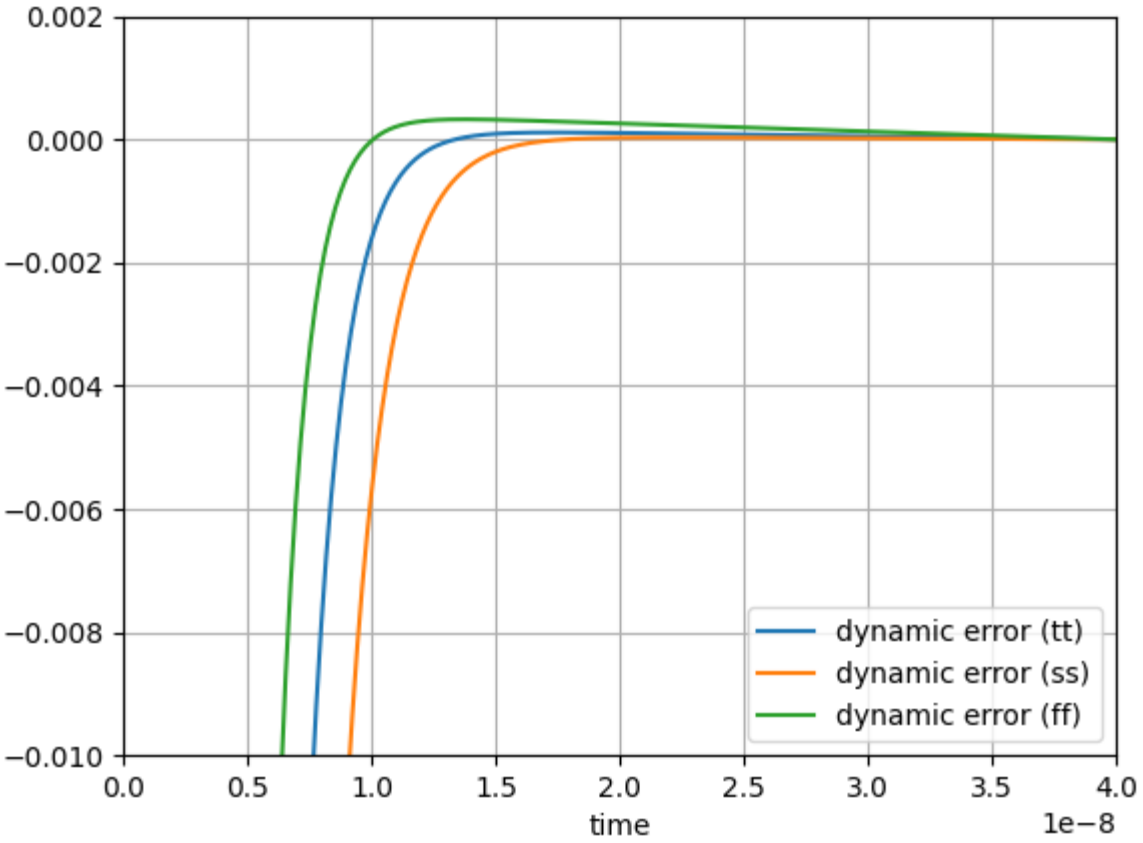


Zooming Into 2nd Redistribution Phase



Dynamic Error

Error = (value(t) – final) / final



Dynamic Error on Log Scale

0.1%-settling time ~ 8, 11, 13 ns (ff, tt, ss)

Max clock frequency for slow corner ~ 1/(2*13ns) = 38.5 MHz