

Introduction to Layout

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Course Schedule

Feb 21	W	Lec 12: Switches	
Feb 26	M	Lec 13: Transistorized Integrator	
Feb 28	W	Lec 14: Introduction to layout	
Mar 04	M	Lec 15: Layout	
Mar 06	W	Lec 16: Layout	
Mar 11	M	Lec 17: Layout	
Mar 13	W	Lec 18: Team presentations	
Mar 18	M	Spring break	
Mar 20	W	Spring break	

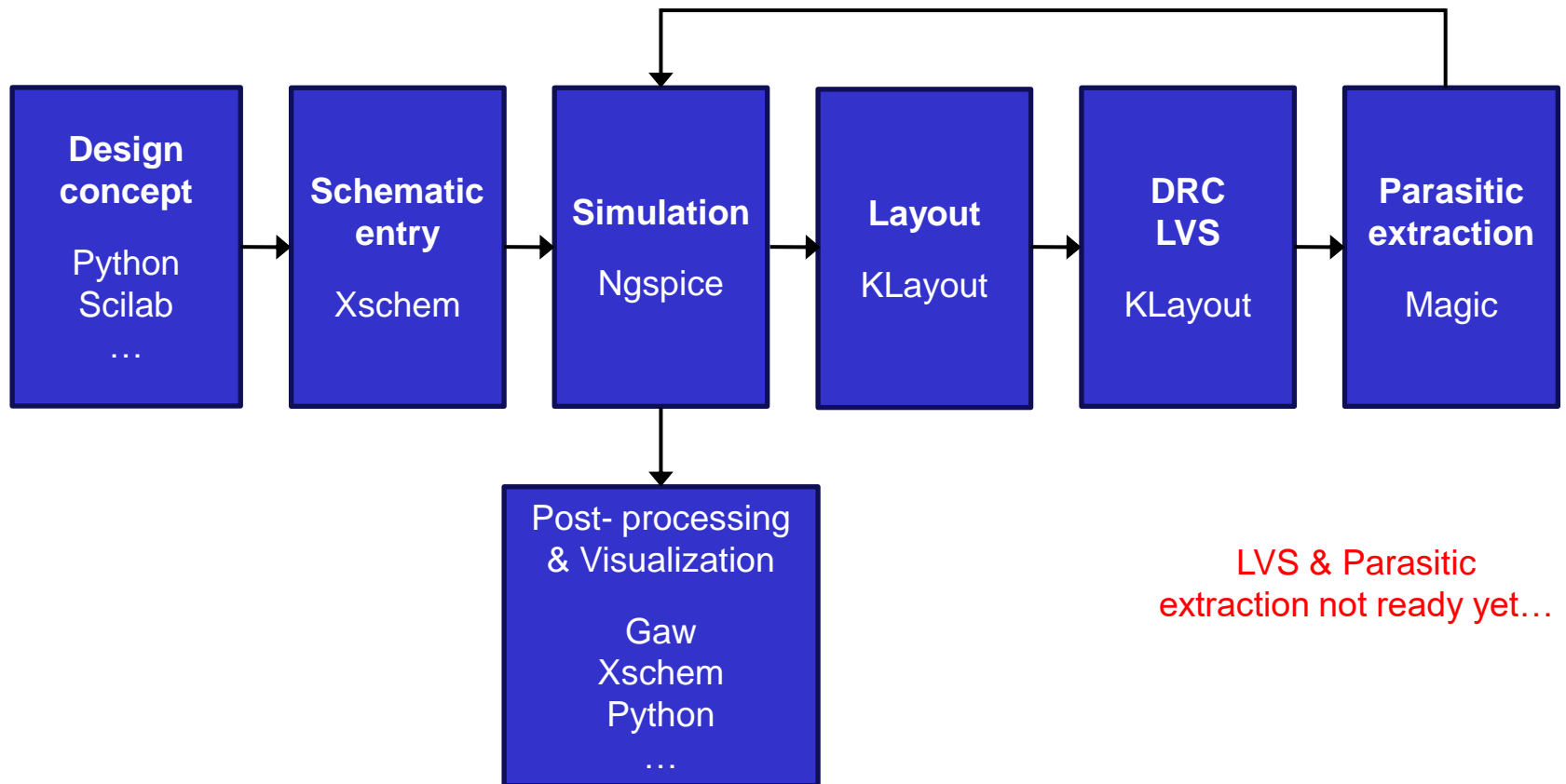


- Presentation time ~ 10 minutes per team

Suggested Outline for Team Presentations

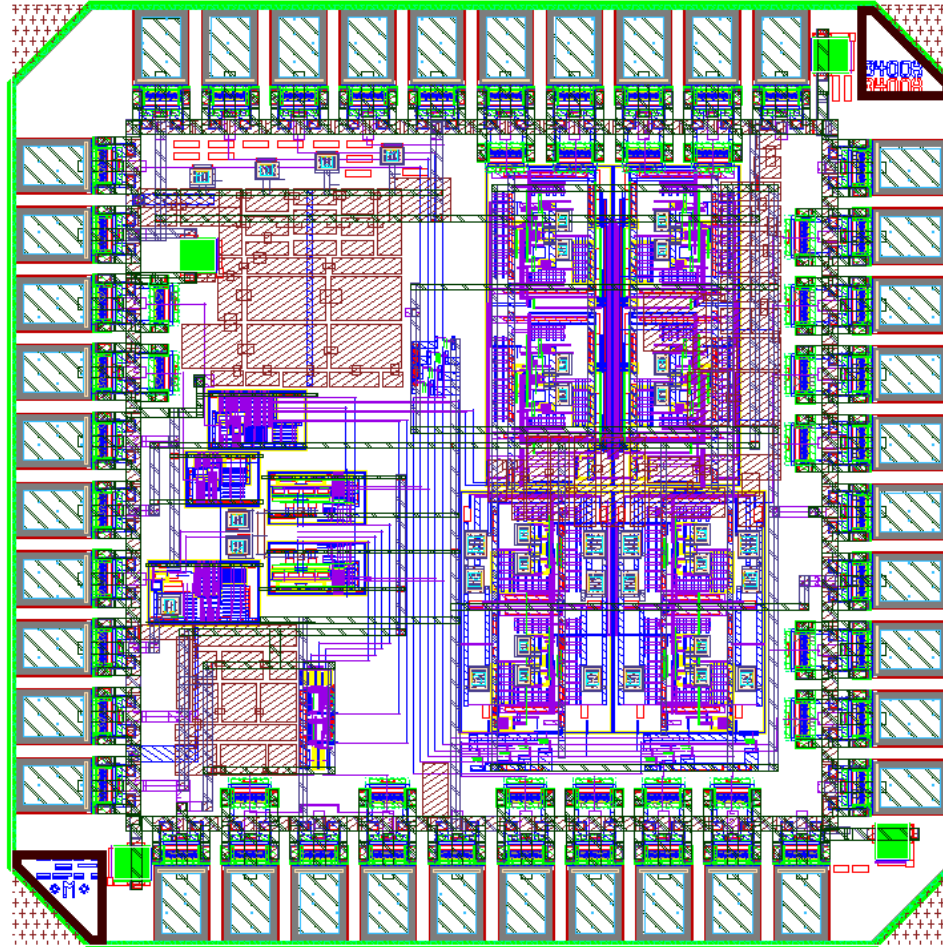
- Explain your design goal
 - Template project (with spec changes?) or another topic?
- Give an executive summary on what your team has done so far
 - Which assignment steps did you complete?
 - Which circuits have you successfully designed/simulated?
 - What remains to be done in terms of schematic design?
- Show a tentative diagram of your top-level schematic
- Describe the task breakdown among team members
 - Who will complete which schematic block?
 - Who will complete which layout design?
- Anything else you'd like to highlight...

Tool Flow



LVS & Parasitic
extraction not ready yet...

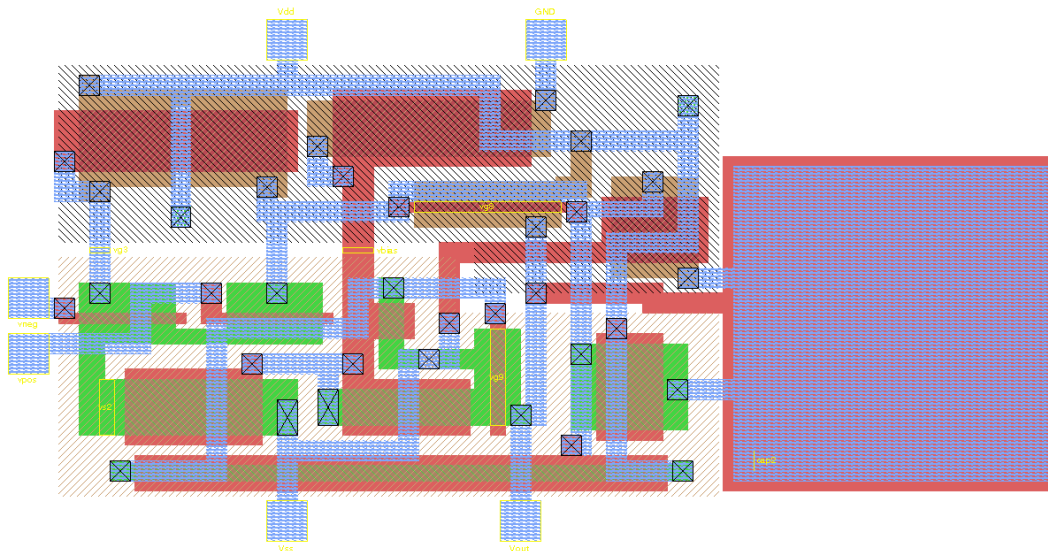
Our Final Output Will Look Like This...



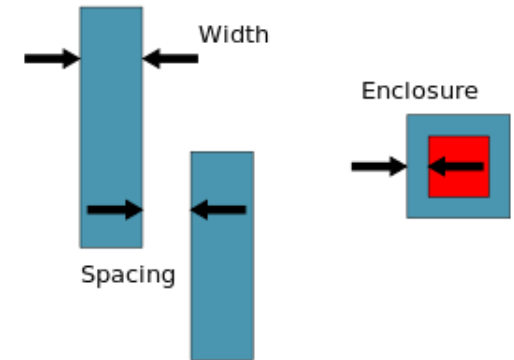
RF Front-End Receiver for ISM-900M

https://www.ee.columbia.edu/~kinget/EE6350_S16/01_DCRRX_Hao_Tuo/Layout.html

Need to Learn Layout and Become Familiar with Design Rules



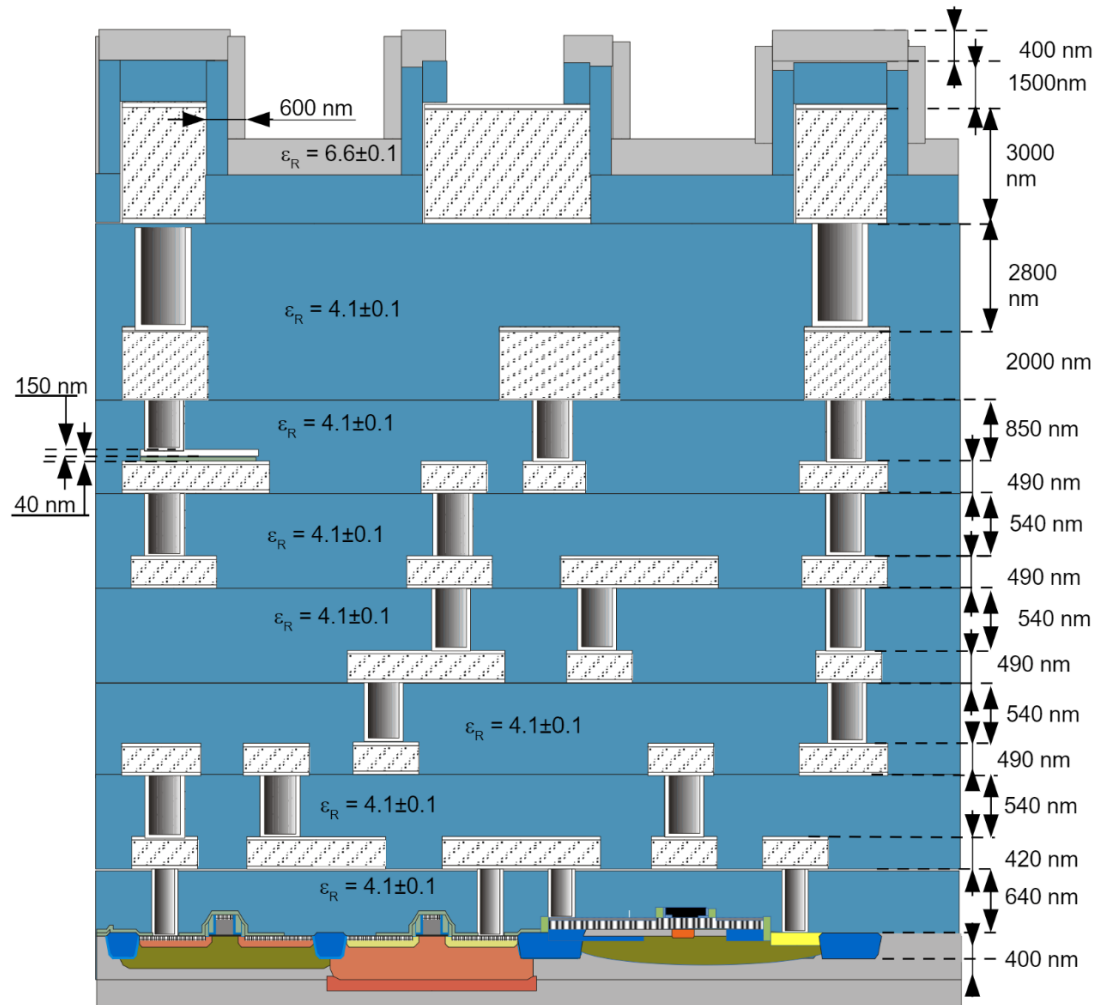
The three basic DRC checks



https://en.wikipedia.org/wiki/Integrated_circuit_layout

https://en.wikipedia.org/wiki/Design_rule_checking

Cross Section (IHP SG13G2 Process)



Designer can only
manipulate x & y
dimensions, z
dimensions are fixed

https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_process_spec.pdf

2 Layer table

This chapter is a documentation of IHP layers definition which is valid in all technologies.

Remark: Only the layers described in the following table are allowed to be used in layout designs. Do not use layers exclusively reserved for internal usage.

Layer name	Purpose	GDS Number	GDS Datatype	Description
L0	drawing	0	0	Reserved for internal use
Activ	drawing	1	0	Defines active regions in substrate, where transistors, diodes and/or capacitors will be fabricated
Activ	label	1	1	Lable in activ layer
Activ	pin	1	2	Pin in active layer
Activ	net	1	3	
Activ	boundary	1	4	
Activ	lvs	1	19	
Activ	mask	1	20	added to Active:drawing at mask generation
Activ	filler	1	22	Activ filler layer
Activ	nofill	1	23	Filler exclusion definition layer
Activ	OPC	1	26	Activ outer OPC definition layer
Activ	iOPC	1	27	Activ inner OPC definition layer
Activ	noqrc	1	28	No parasitics extraction
L2	drawing	2	0	Reserved for internal use
BiWind	drawing	3	0	Defines active npn collector region
BiWind	OPC	3	26	BiWind OPC definition layer
GatPoly	drawing	5	0	Defines polysilicon gates and interconnect, GatPoly = GatPoly OR PolyRes see section

⋮

https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_layout_rules.pdf

Example: Rules for Gate Poly Layer

3.8 GatPoly

Rule	Description	Value
Gat.a	Min. GatPoly width	0.13
Gat.a1	Min. GatPoly width for channel length of 1.2 V NFET	0.13
Gat.a2	Min. GatPoly width for channel length of 1.2 V PFET	0.13
Gat.a3	Min. GatPoly width for channel length of 3.3 V NFET	0.45
Gat.a4	Min. GatPoly width for channel length of 3.3 V PFET	0.4
Gat.b	Min. GatPoly space or notch	0.18
Gat.b1	Min. space between unrelated 3.3 V GatPoly over Activ regions	0.25
Gat.c	Min. GatPoly and GatPoly:filler extension over Activ (end cap)	0.18
Gat.d	Min. GatPoly space to Activ	0.07
Gat.e	Min. GatPoly area (μm^2)	0.09
Gat.f	45-degree and 90-degree angles for GatPoly on Activ area are not allowed	
Gat.g	Min. GatPoly width for 45-degree bent gates (on field oxide) if the bend GatPoly length is $> 0.39 \mu\text{m}$	0.16

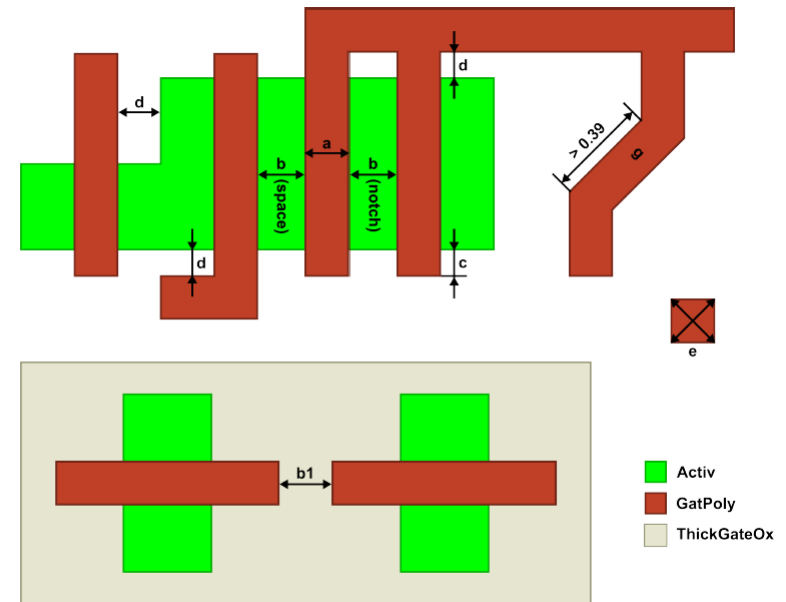
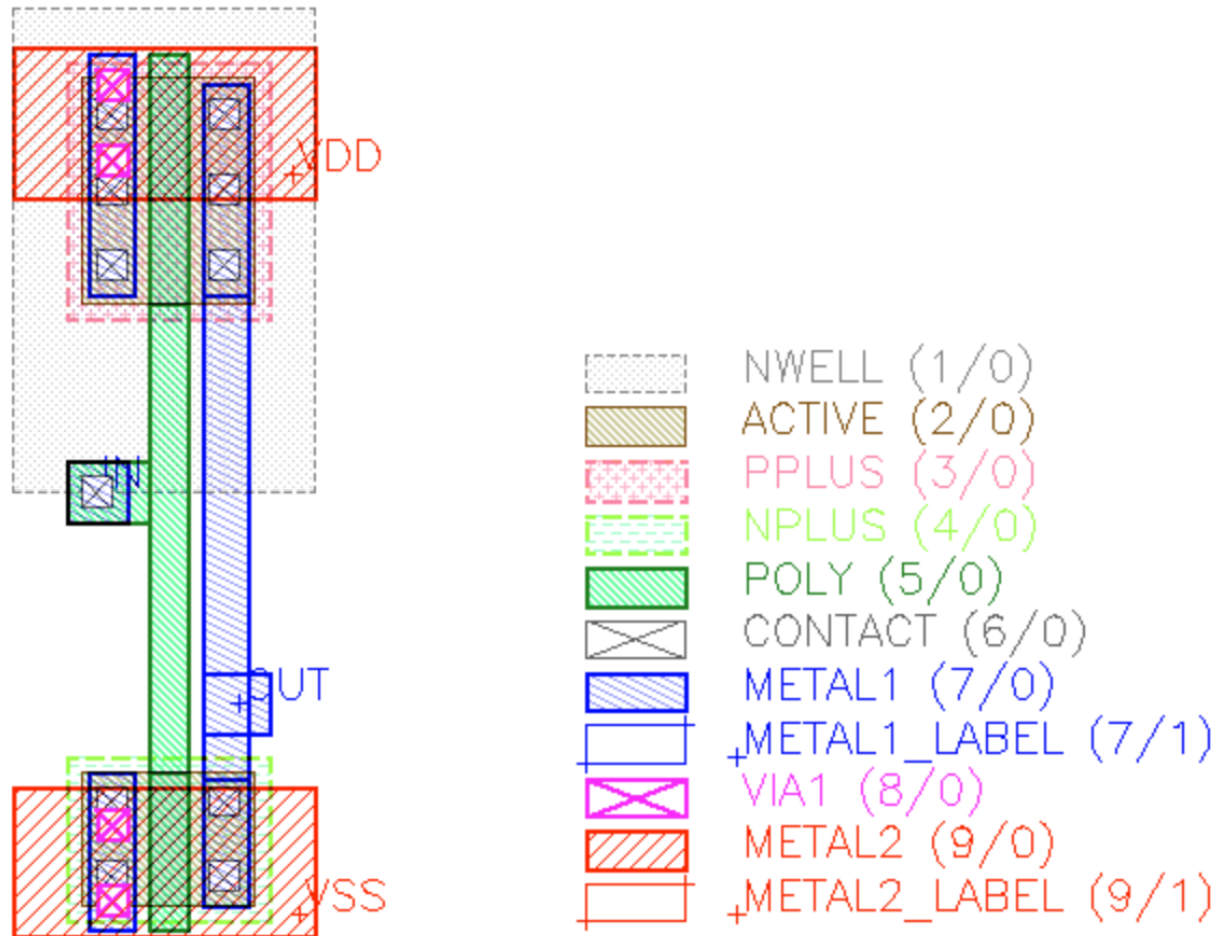


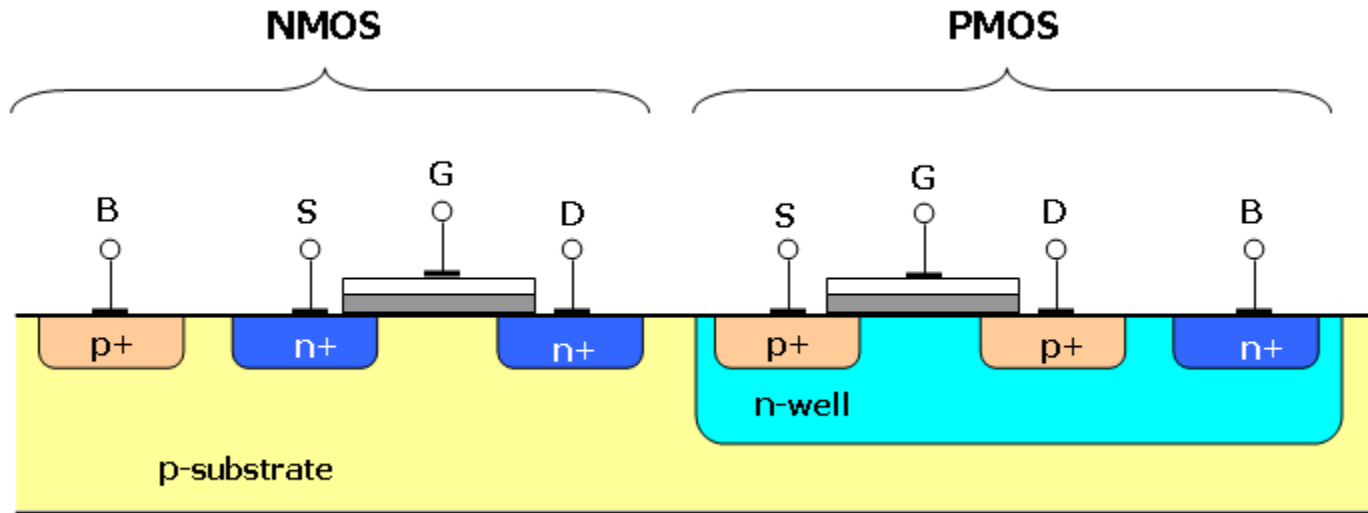
Figure 3.3: GatPoly dimensions

Layout of an Inverter



https://www.klayout.de/doc-qt5/manual/lvs_intro.html

Cross Section



<https://en.wikipedia.org/wiki/CMOS>

- Important: Need plenty of well and substrate contacts (“B”)

Launching KLayout (with IHP tech setup)

9. Create a subdirectory for your layout work.

```
cd /foss/designs  
mkdir layout  
cd layout
```



10. To start Klayout with the proper technology setup, first set the KLAYOUT_HOME environment variable, then launch using the -e option (edit mode). You'll need to set the environment variable each time you start the container (this will be fixed in a future release).

```
export KLAYOUT_HOME=$PDKPATH/libs.tech/klayout  
klayout -e &
```



https://github.com/bmurmannelEE628/blob/main/3_Tools/win.md