


# Schematic & Layout Deliberations


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# KLayout Grid

 **Zion** 03/27/2024 2:48 PM

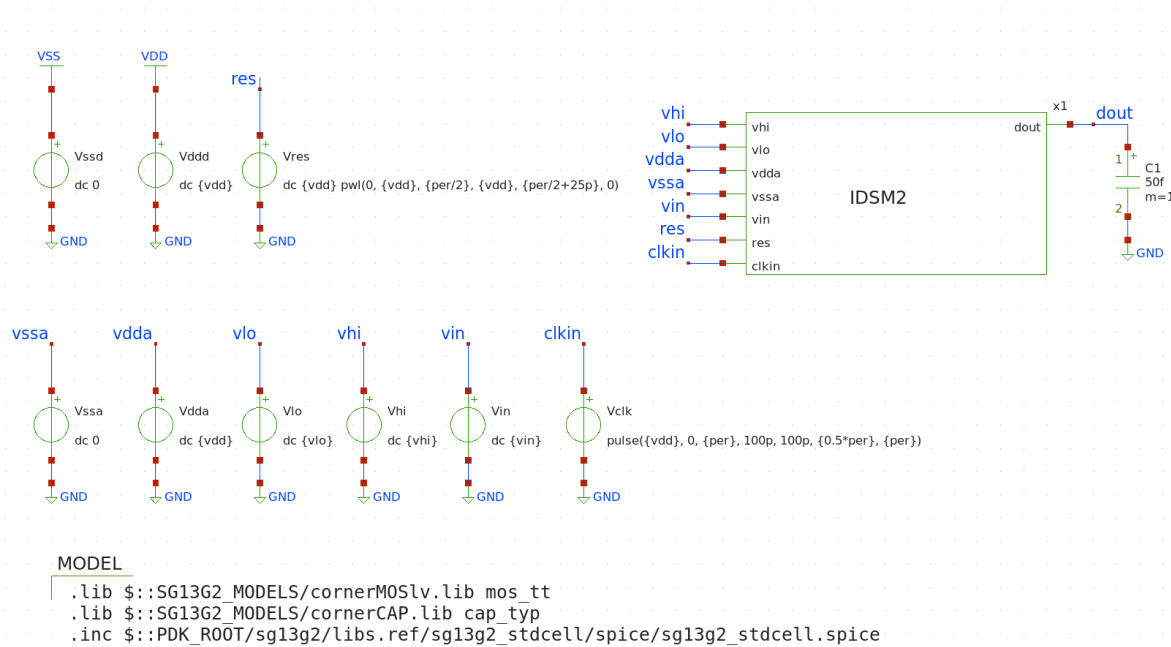
If you change the grid in file>setup>grid to 0.005 (or larger) but keep the GDU as 0.001 it will keep your design to the right grid snapping and size without messing with DRC



 1  1

# Top-Level Testbench

## Simulating 11 input voltages:



### NGSPICE

```
.param temp=27 per=20n N=110
.param vlo=0.3 vhi=0.9 vdd=1.2 vin=0.6
.option method=gear reltol=1e-5
.ic v(x1.x3.out1p)=0
.tran 100p {per*N} uic
.meas tran iavg_ana AVG i(Vdda)
.meas tran iavg_dig AVG i(Vddd)

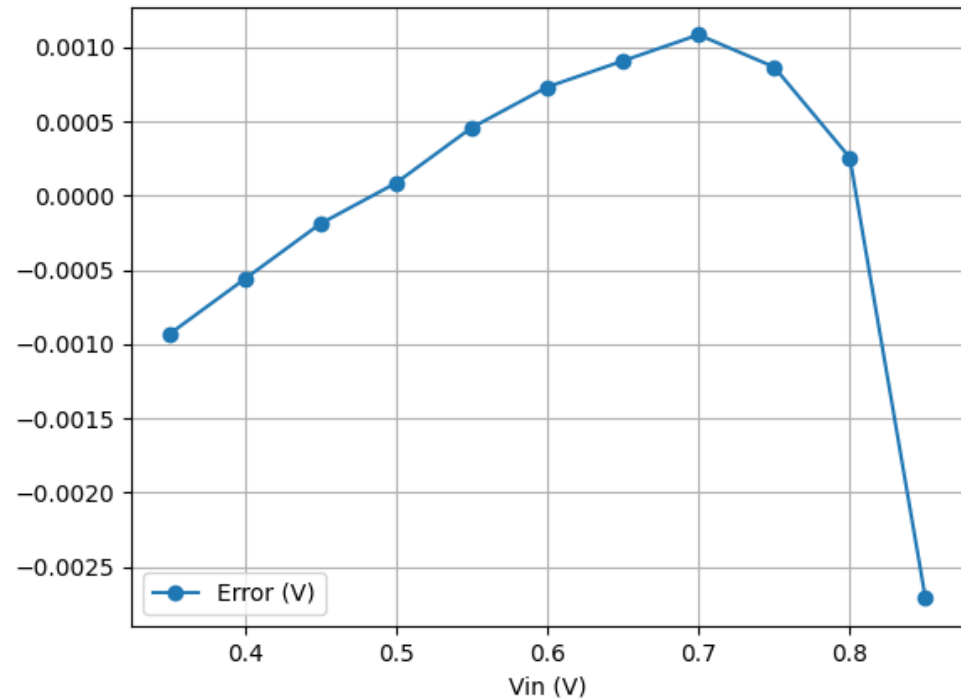
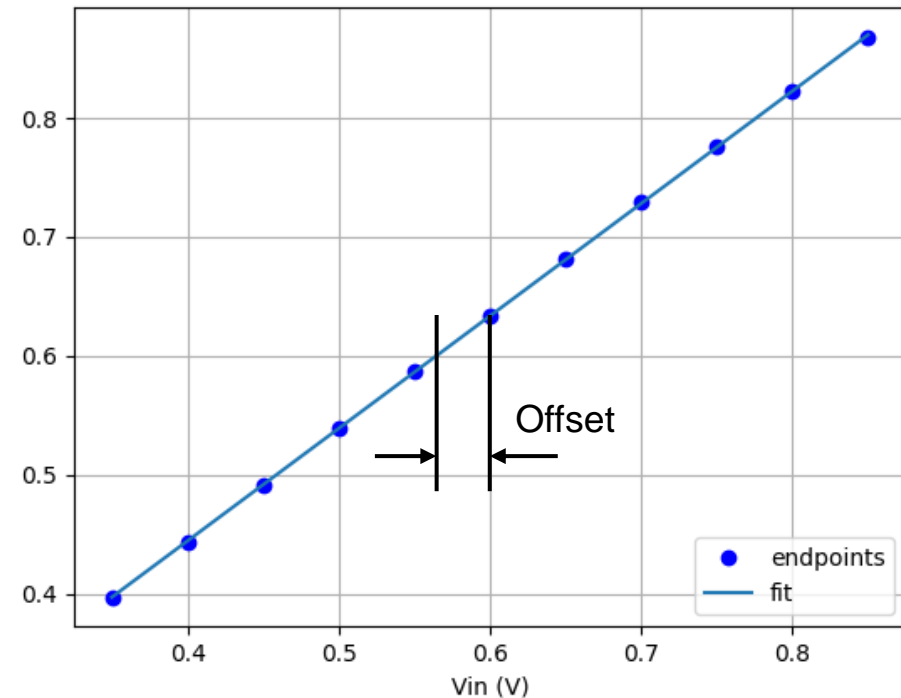
.control
set wr_singlescale
set wr_vecnames
option numdgt = 3
let index = 1
foreach vin_val 0.35 0.4 0.45 0.5 0.55 0.6 0.65 0.7 0.75 0.8 0.85
    alterparam vin = $vin_val
    reset
    run
    set file = {tb_idsm2}_{index}.txt
    wrdata $file x1.vout1 x1.vout2 dout x1.p1 x1.p2
    destroy $curplot
    let index = index + 1
end
.endc
```



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/foss/designs/tb\_IDSM2.sch

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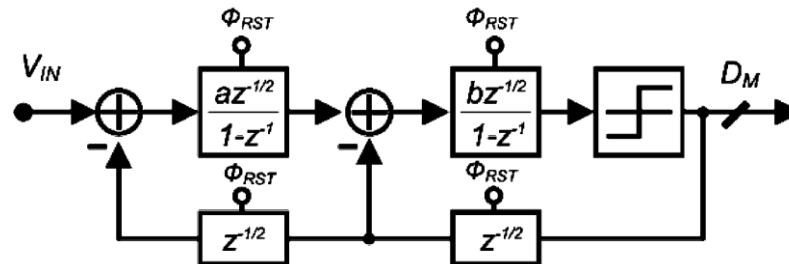
# Linear Fit After Decimation



→ The modulator is still “reasonably linear” with inputs between 0.35...0.85V (0.5V full-scale range)

[https://github.com/bmurrmann/EE628/blob/main/5 Design/3 Real circuits/tb IDSM2.ipynb](https://github.com/bmurrmann/EE628/blob/main/5%20Design/3%20Real%20circuits/tb%20IDSM2.ipynb)

## Input-Referred Noise of IDMS2 (From lecture 11)

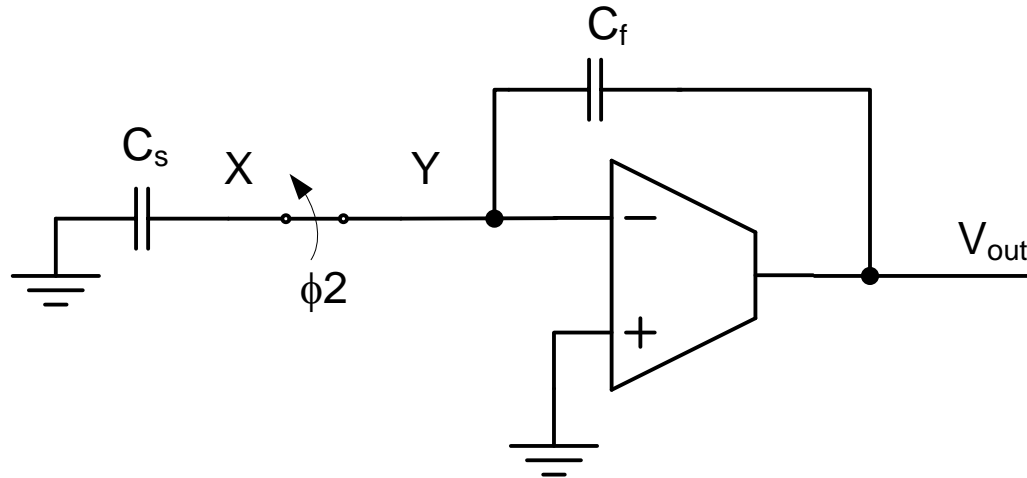


- Noise from second integrator is negligible (attenuated by first integrator)
- Decimation filter averages noise from  $M$  samples
- There is a penalty factor of  $4/3$  due to nonuniform impulse response of the decimation filter

$$\overline{v_n^2} = \overline{v_s^2} \sum_{i=1}^M w_i^2 < \overline{v_s^2} \frac{4}{3M}. \quad (12)$$

↑  
Input-referred noise of first integrator

# Input-Referred Noise of an SC Integrator



[Schreier, TCAS1, 2005]

- At the end of  $\phi2$ , find noise charge left behind at node Y

$$\overline{v_s^2} = \underbrace{\frac{kT}{C_s} + \frac{kT}{C_s} \frac{1}{1 + \frac{1}{x}} + \alpha\gamma \frac{kT}{C_s} \frac{1}{1 + x}}_{\phi2}$$

$$x = 2g_m R_{on}$$

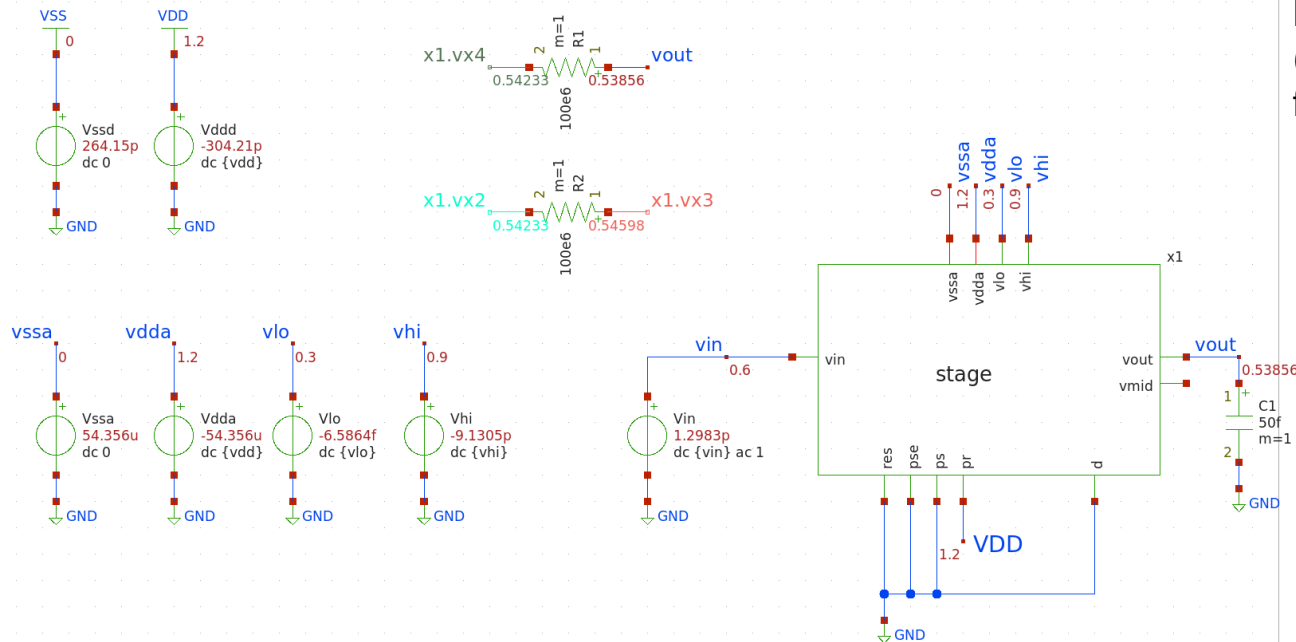
(switch resistance)

$$\overline{v_s^2} \approx \frac{kT}{C_s} + \alpha\gamma \frac{kT}{C_s} \approx \frac{3kT}{C_s}$$

Can simulate the noise contributed during  $\phi2$

# Noise Testbench

## Bias point helpers



### MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
.lib $::SG13G2_MODELS/cornerCAP.lib cap_typ
.inc $::PDK_ROOT/sg13g2/libs.ref/sg13g2_stdcell/spice/sg13g2_stdcell.spice
```

Bring out some internal nodes  
(avoid changing the circuit block  
for simulation purposes)

### NGSPICE

```
.param temp=27 vdd=1.2
.param vin=0.6 vlo=0.3 vhi=0.9
global x1.vx2 x1.vx3 x1.vx4

.control
save all
op
write tb_stage_noise.raw

noise v(x1.vx1, x1.vx2) Vin dec 100 1 1000gig
display
print v(onoise_total)
set color0 = white
setplot noise1
plot onoise_spectrum
plot sqrt(integ(onoise_spectrum^2))
.endc
```

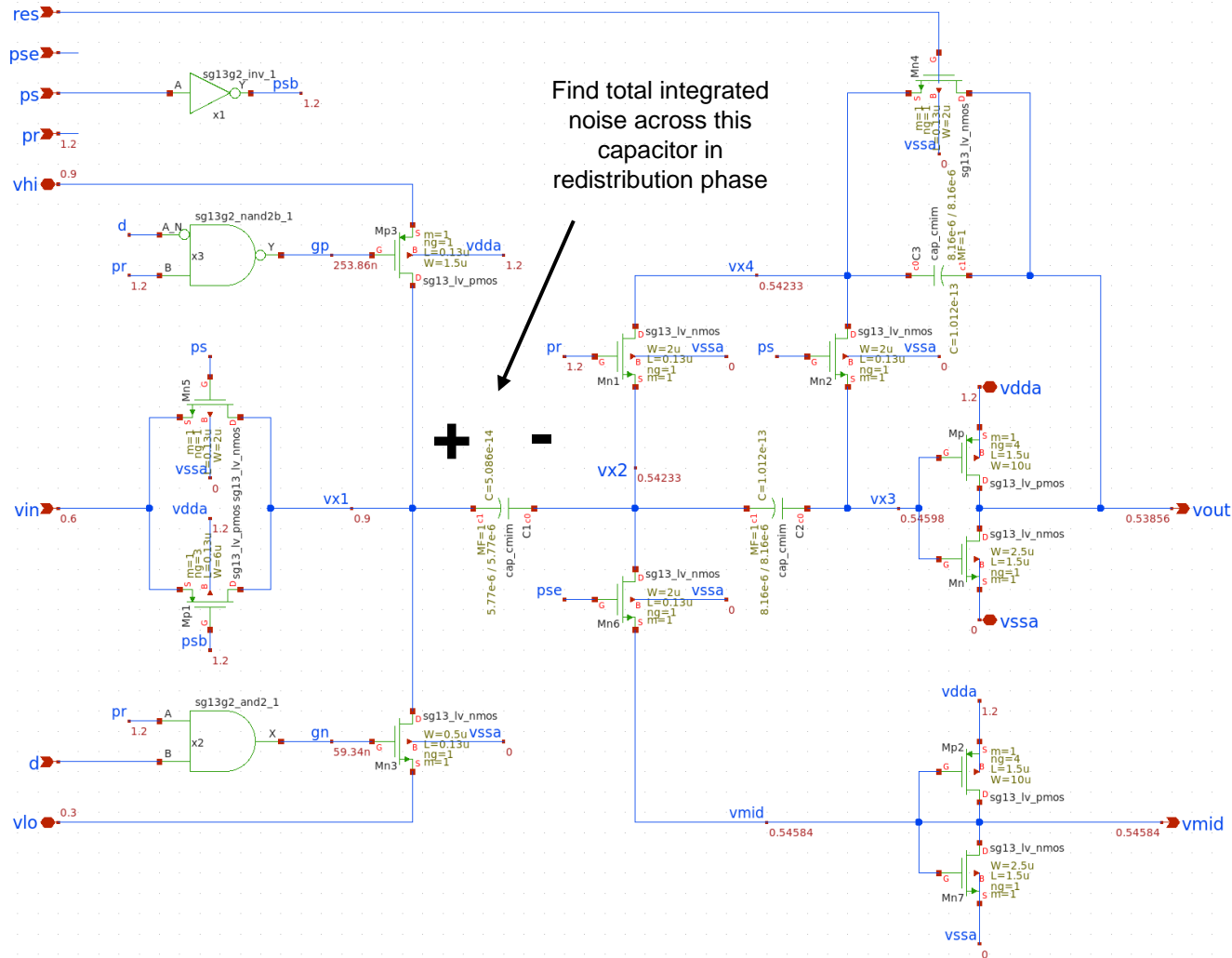
➔ Backannotate

**XSCHEM**

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/foss/designs/tb\_stage\_noise.sch

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# Stage Schematic



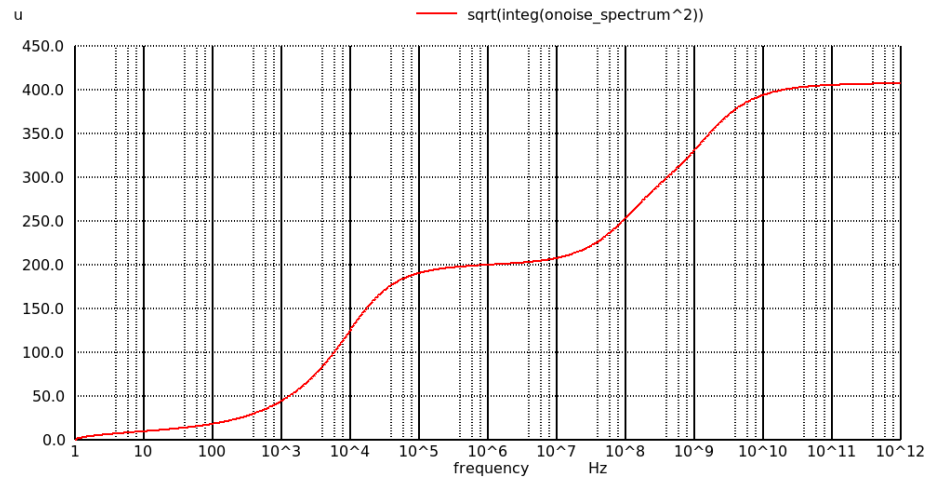
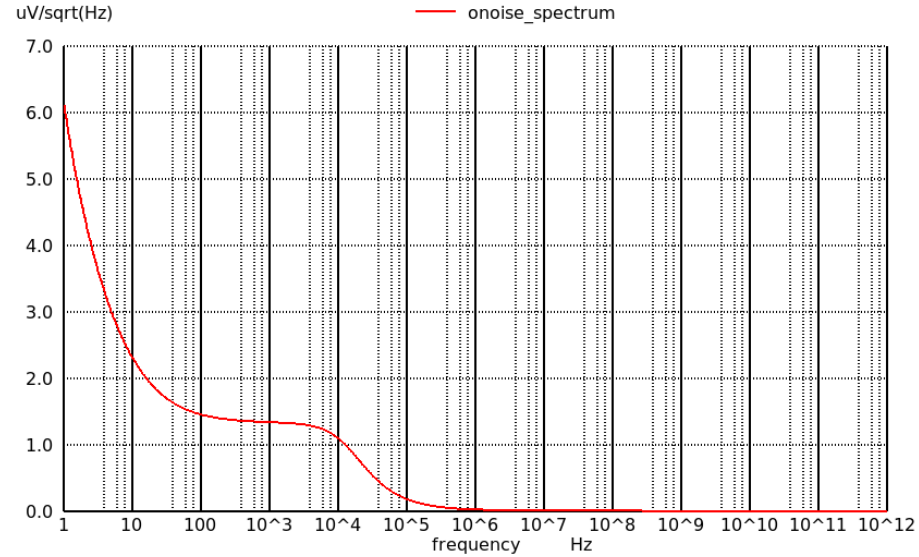
**XSCHEM**

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x1. /foss/designs/stage.sch

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# Simulation Result



408uV

## Dynamic Range Calculation

$$\overline{v_s^2} \approx \frac{kT}{C_s} + N_{redist}$$

$$\overline{v_s^2} \approx (280\mu V)^2 + (408\mu V)^2 = (495\mu V)^2$$

$$\overline{v_n^2} \approx (495\mu V)^2 \frac{4}{3M} = (54.5\mu V)^2 \quad M = 110 \quad (\text{number of samples})$$

$$DR \approx 10 \log \left( \frac{\frac{1}{2} \left( \frac{500mV}{2} \right)^2}{(54.5\mu V)^2} \right) = 70.2dB$$

- Measured values in Chae's design are DR~75 dB, SNR~66dB
- Uses somewhat larger full-scale range
- Our design is good enough to be useful....