Schematic Review

Boris Murmann

bmurmann@hawaii.edu

Issue with IHP PyCells

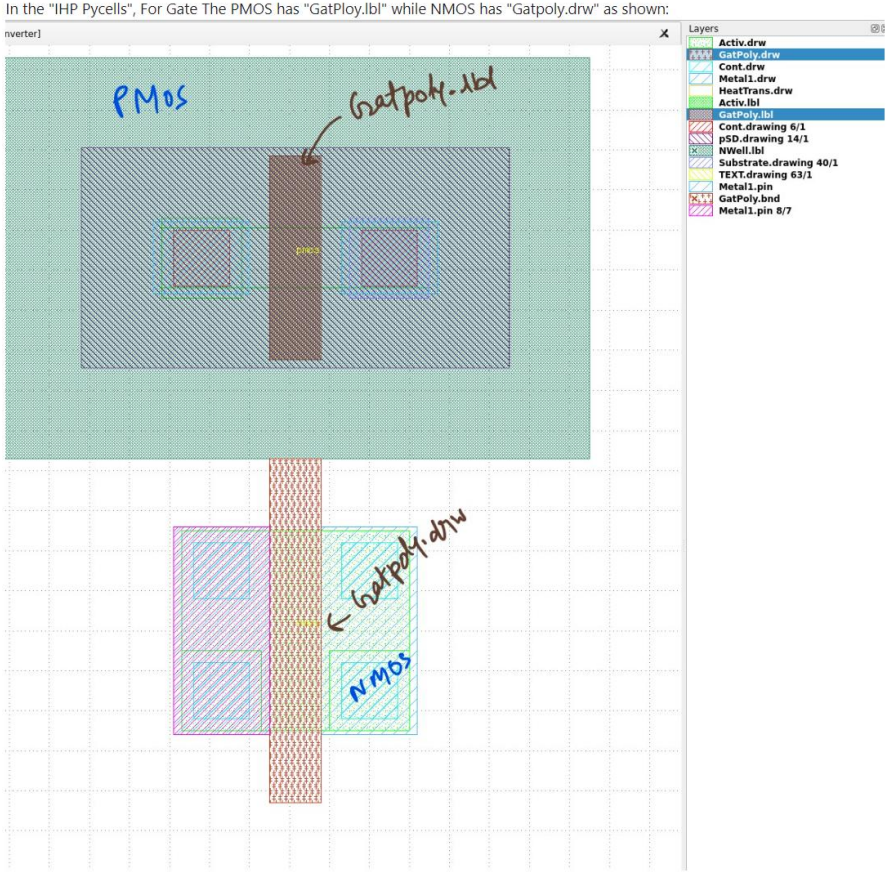
KLayout: PMOS and NMOS have different GatPoly Layers #54

New issue

Open vkrahul77 opened this issue 4 days ago · 1 comment

vkrahul77 commented 4 days ago

In the "IHP Pycells", For Gate The PMOS has "GatPloy.lbl" while NMOS has "Gatpoly.drw" as shown:



Also, I've noticed a discrepancy in dimension input between NMOS and PMOS transistors within the tool. Specifically, while "1u" notation is accepted for PMOS, it's not permitted for NMOS. Instead, we're required to use scientific notation such as "1e-6".

Assignees
No one assigned

Labels
bug

Projects
None yet

Milestone
No milestone

Development
No branches or pull requests

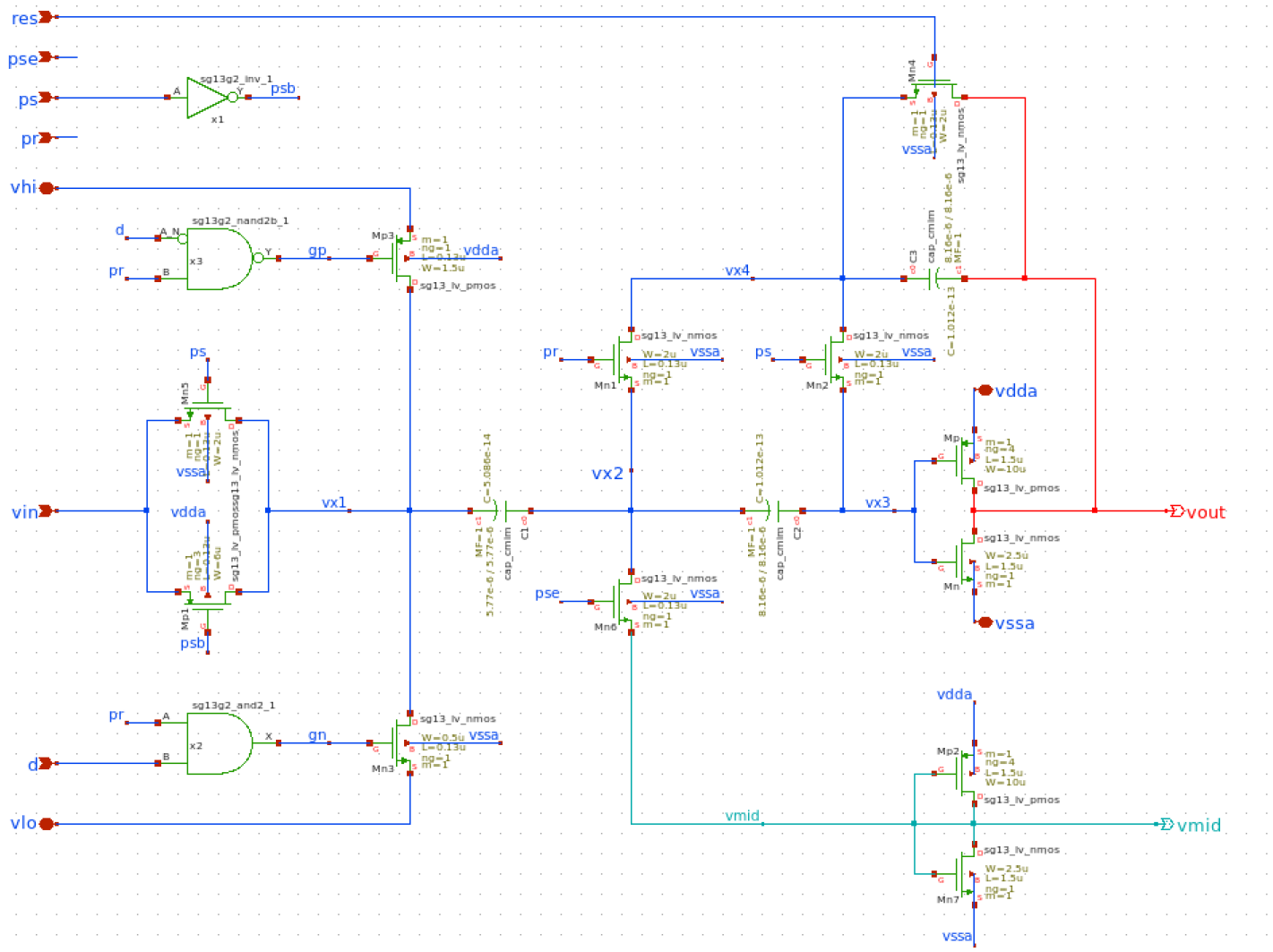
Notifications Customize
Subscribe
You're not receiving notifications from this thread.

2 participants

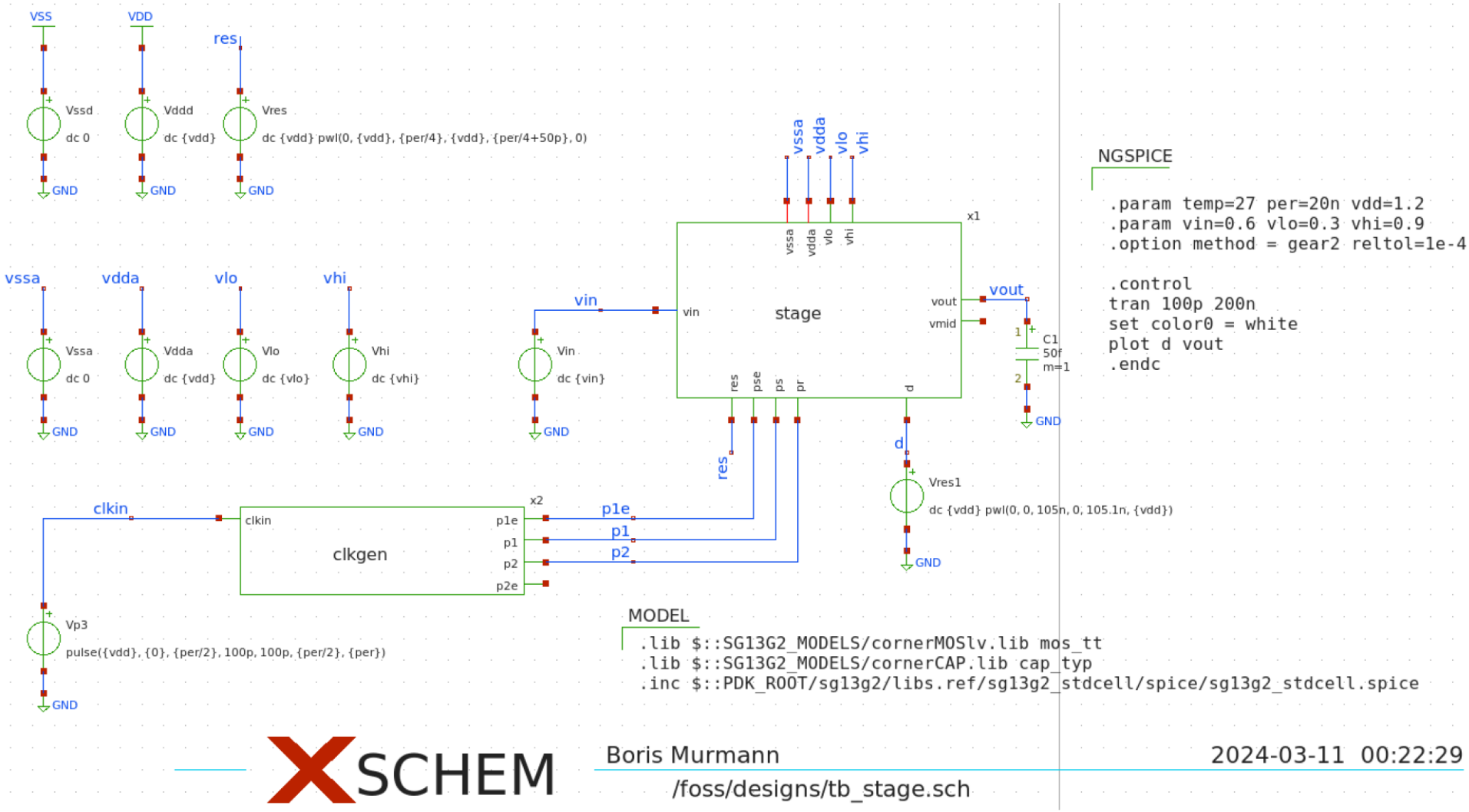
Tentative Schedule

- Corrected PyCells (ASAP?)
- Beta version of LVS (~end of March)
- Beta version of PEX (?)
- Complete all layouts, LVS & DRC clean (~May 1)
- Final checks (with PEX?)
- GDS deadline (~May 20)

Stage

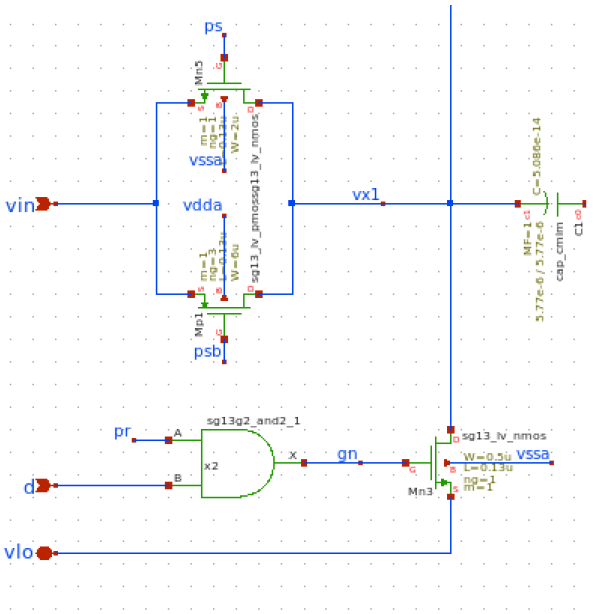

res
pse
ps
pr
vhi
vlo
vin
d
vx1
vx2
vx3
vx4
vmid
vout
vdda
vssa
psb
gp
gn
sg13g2_inv_1
sg13g2_nand2b_1
sg13g2_and2_1
sg13_lv_nmos
sg13_lv_pmos
cap_cmim
Boris Murmann
2024-03-10 20:56:55
x1. /foss/designs/stage.sch

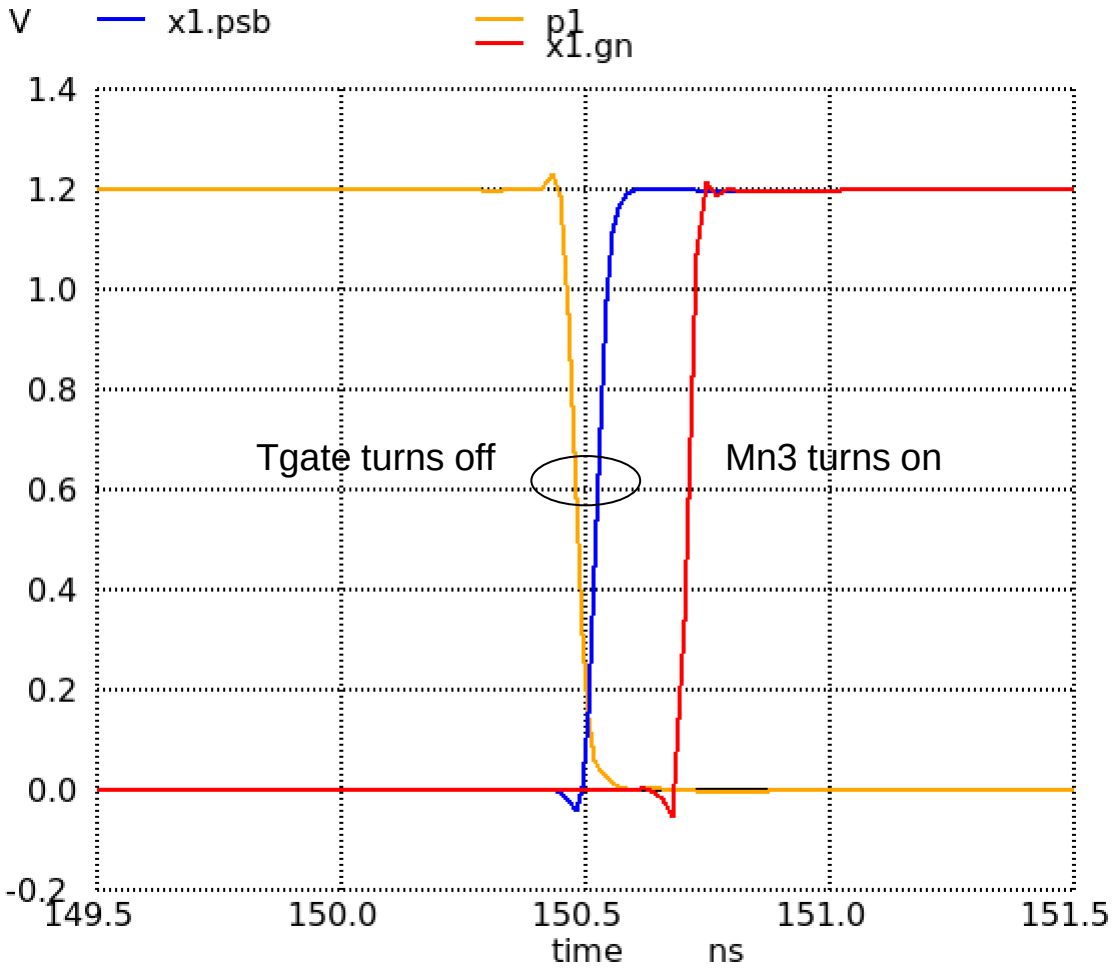
Stage Testbench



Timing Check

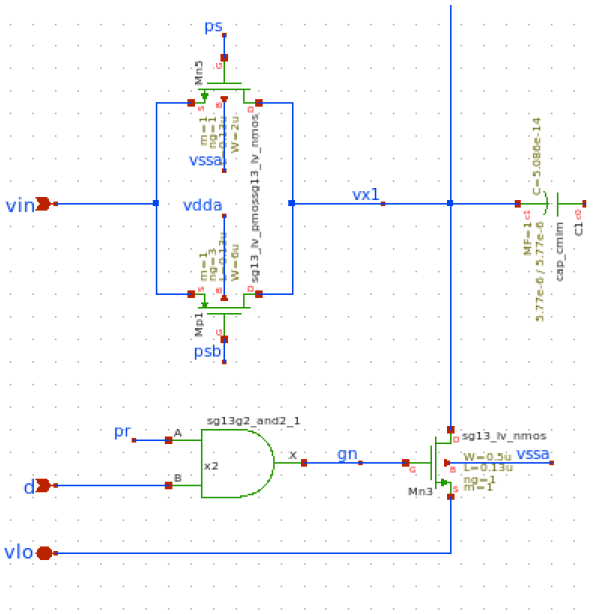
(p1)

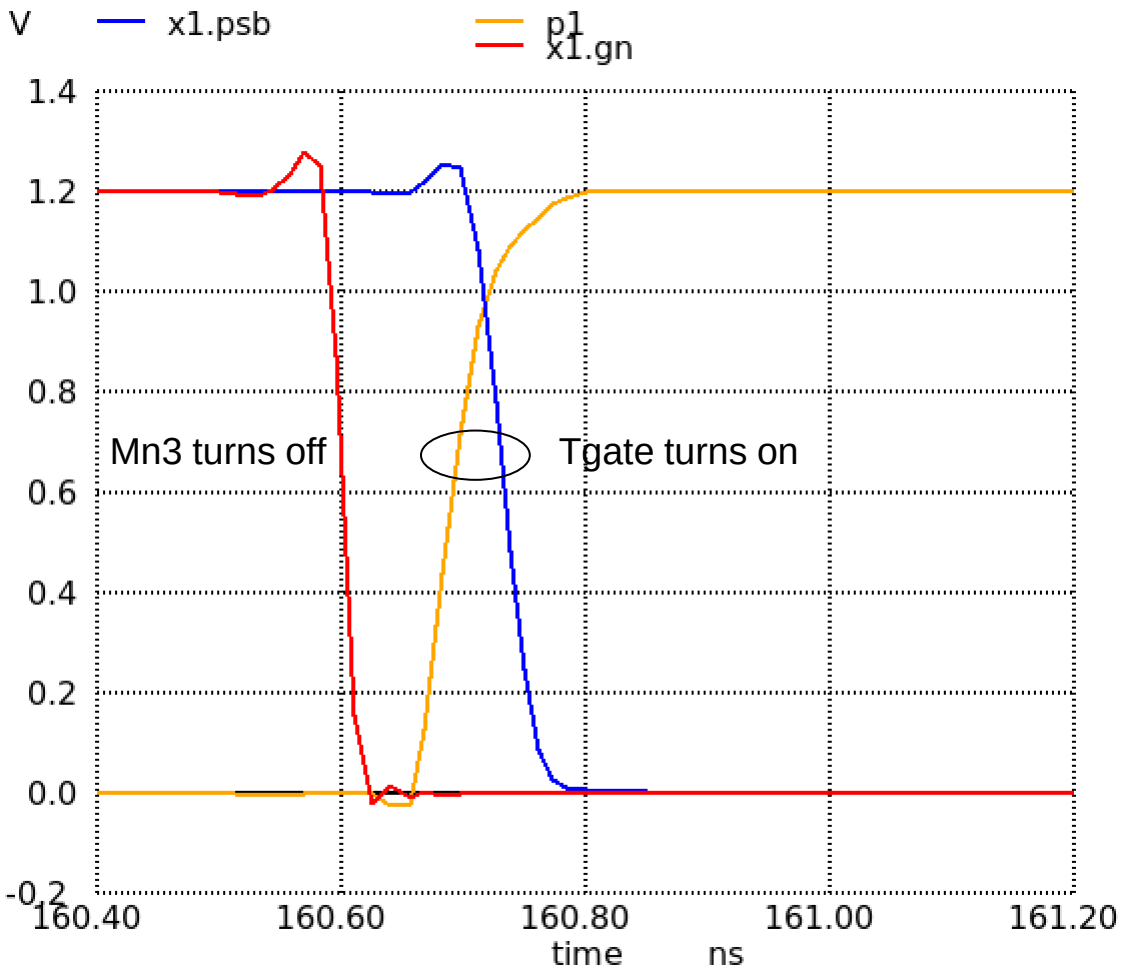




Timing Check

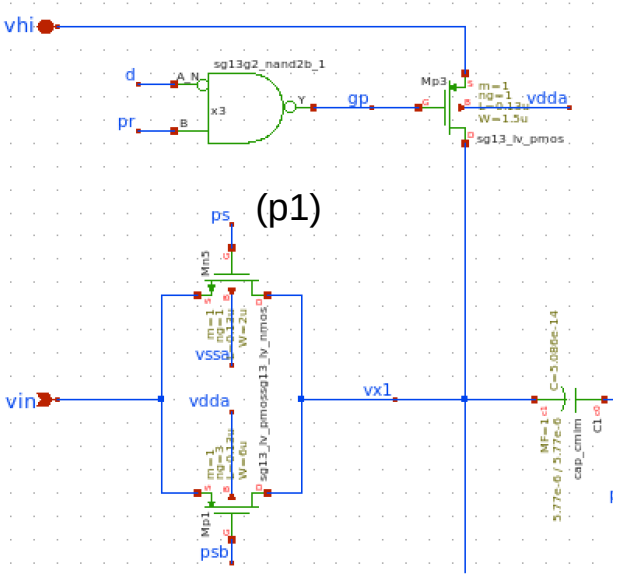
(p1)

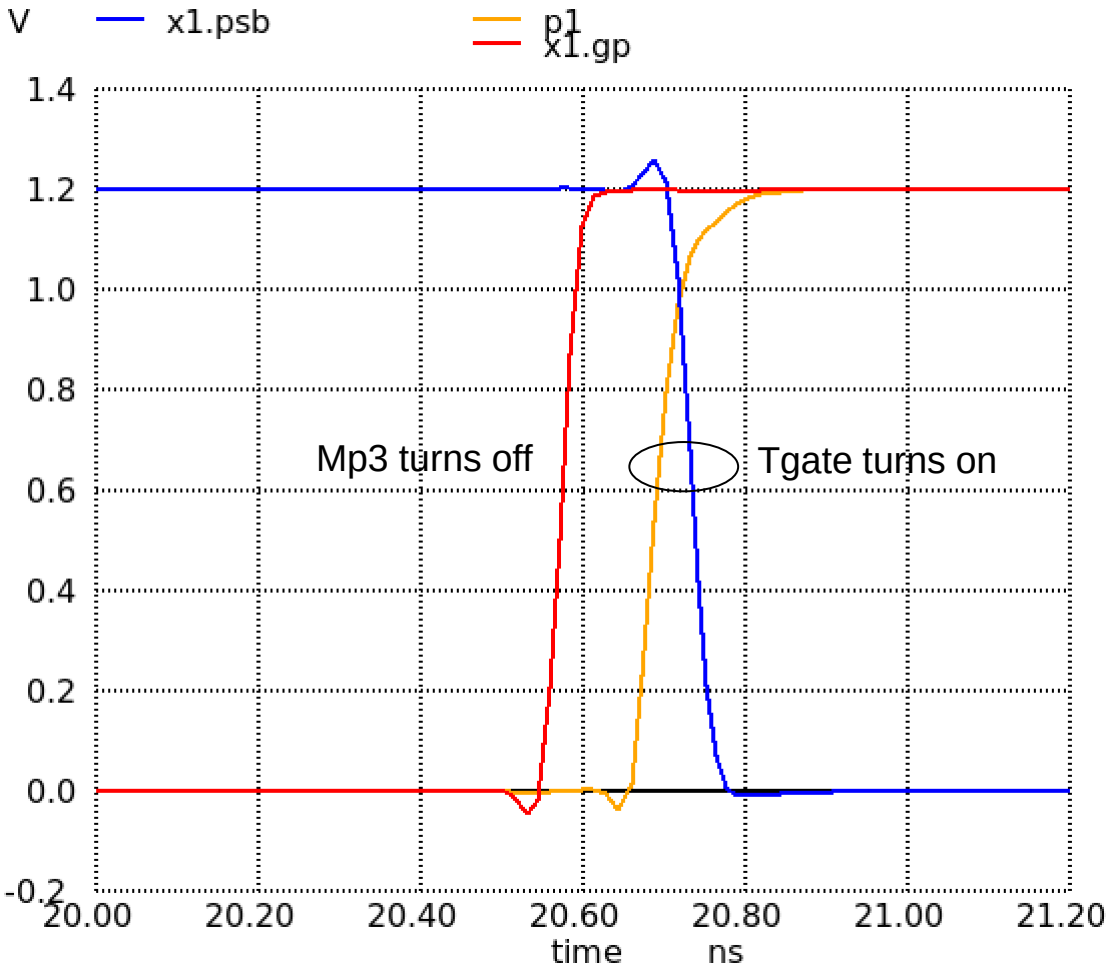




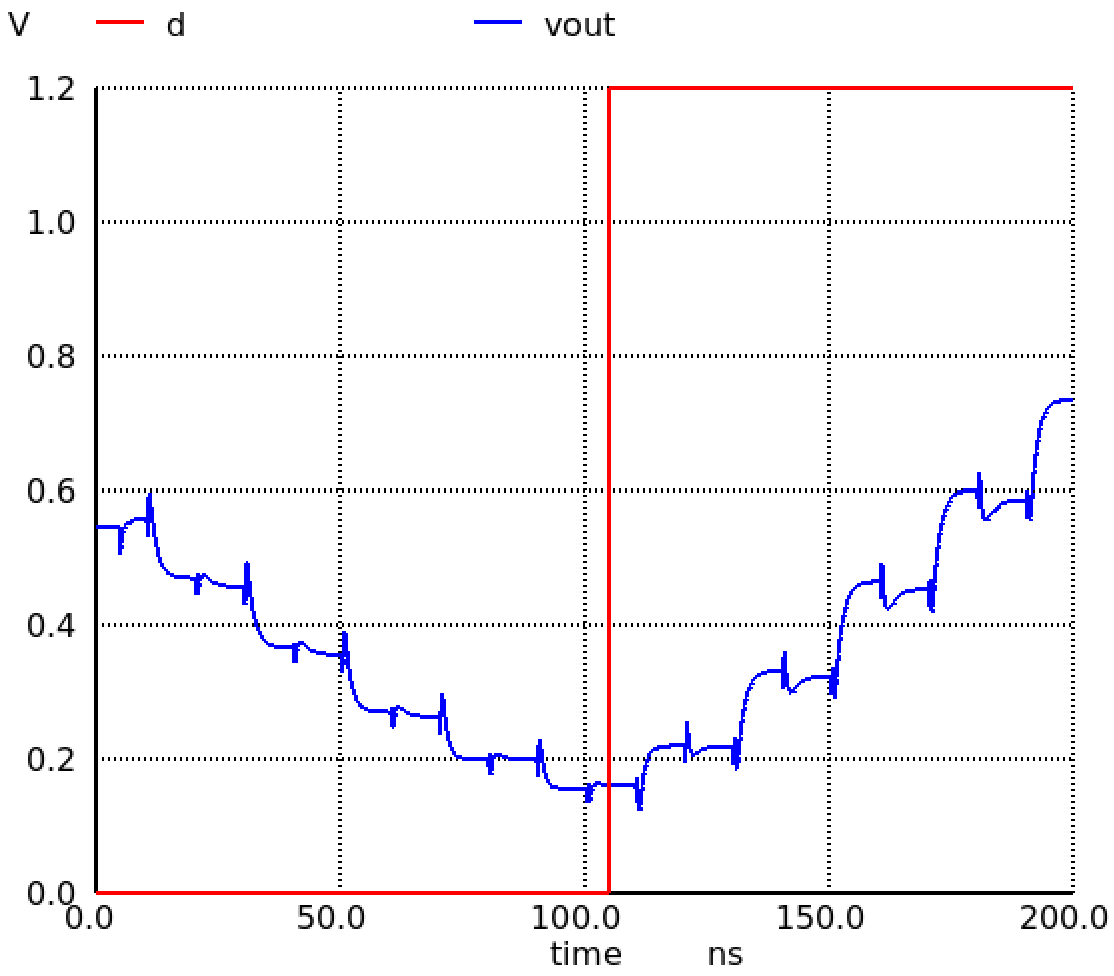
About 100 ps non-overlap; may want to increase number of delay inverters in clkgen

Timing Check

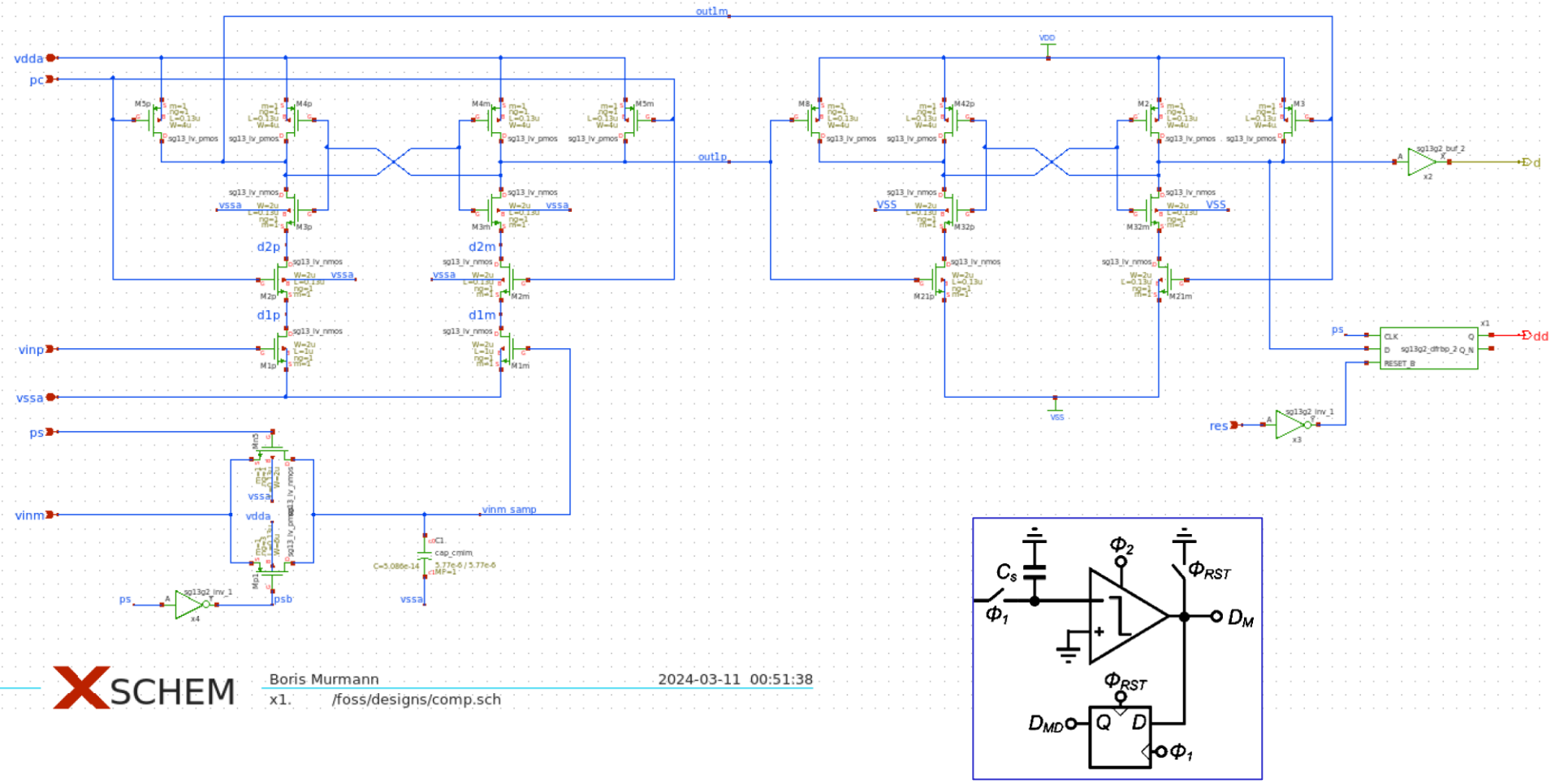




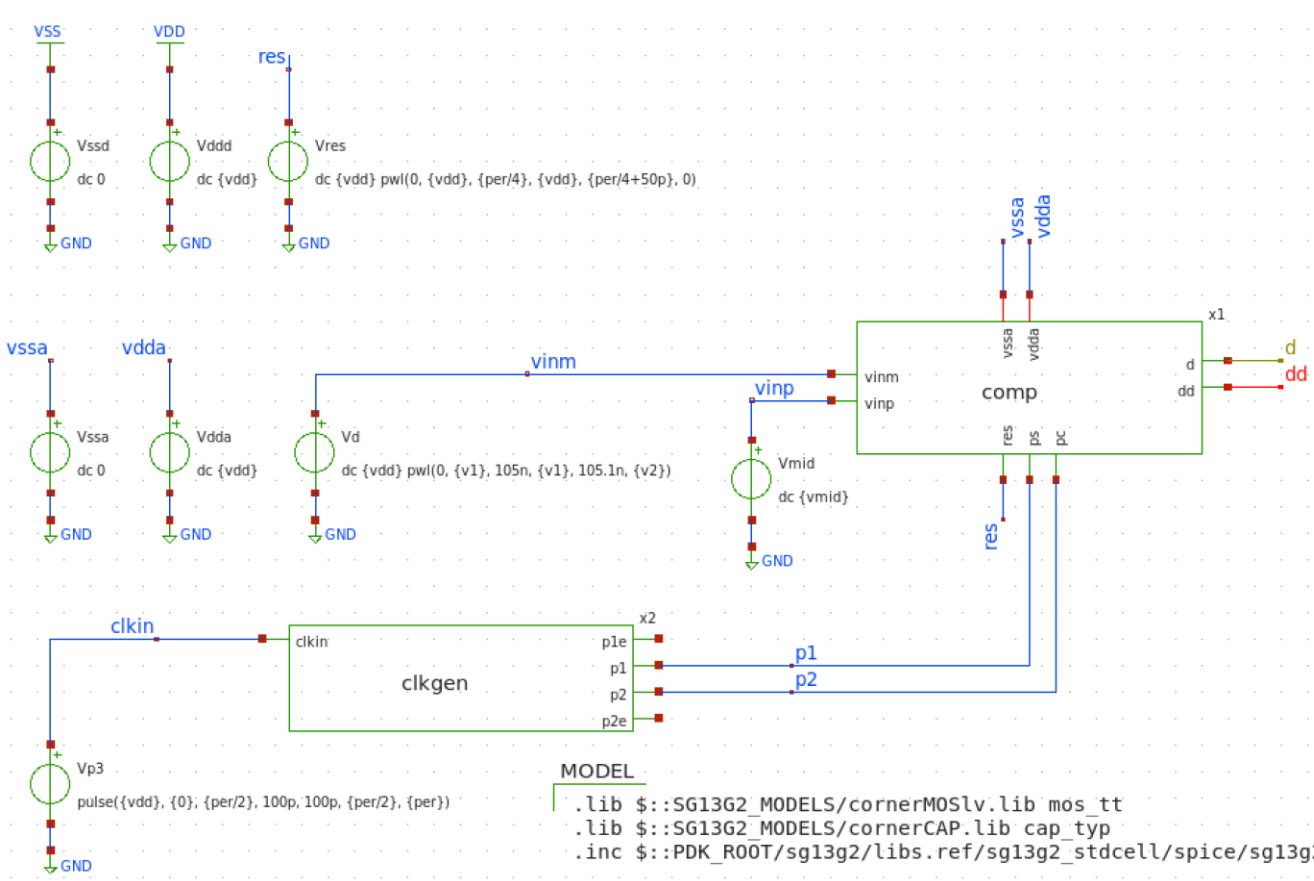
Toggle Data Input



Comparator with Interface Circuitry



Comparator Testbench



NGSPICE

```
.param temp=27 per=20n vdd=1.2
.param vmid=0.6 v1={vmid-100m} v2={vmid+100m}
.option method = gear2 reltol=1e-4
.ic v(out1p)=0

.control
tran 100p 200n
set color0 = white
plot vinm x1.vinm_samp d dd
.endc
```

MODEL

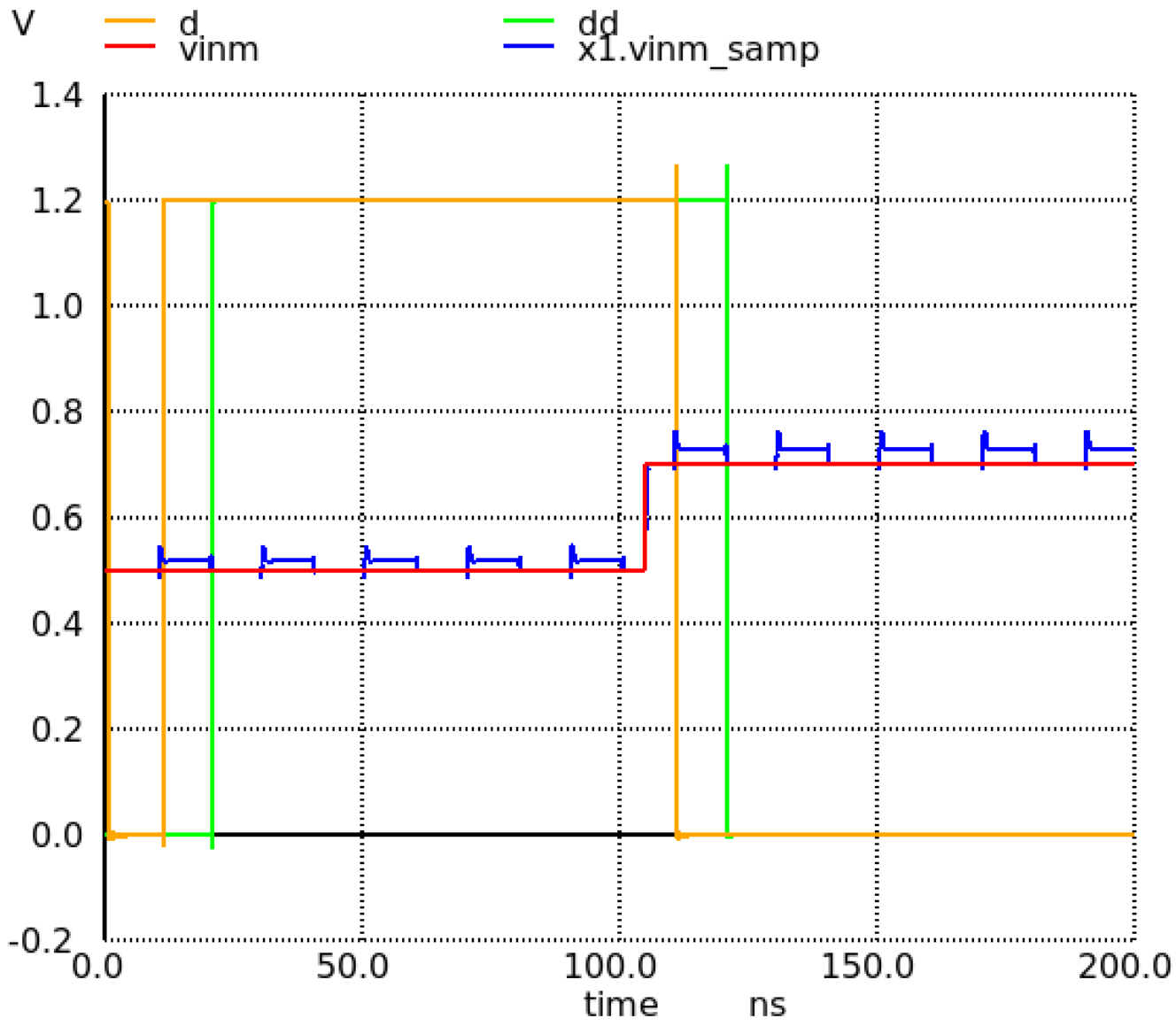
```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
.lib $::SG13G2_MODELS/cornerCAP.lib cap_typ
.inc $::PDK_ROOT/sg13g2/libs.ref/sg13g2_stdcell/spice/sg13g2_stdcell.spice
```

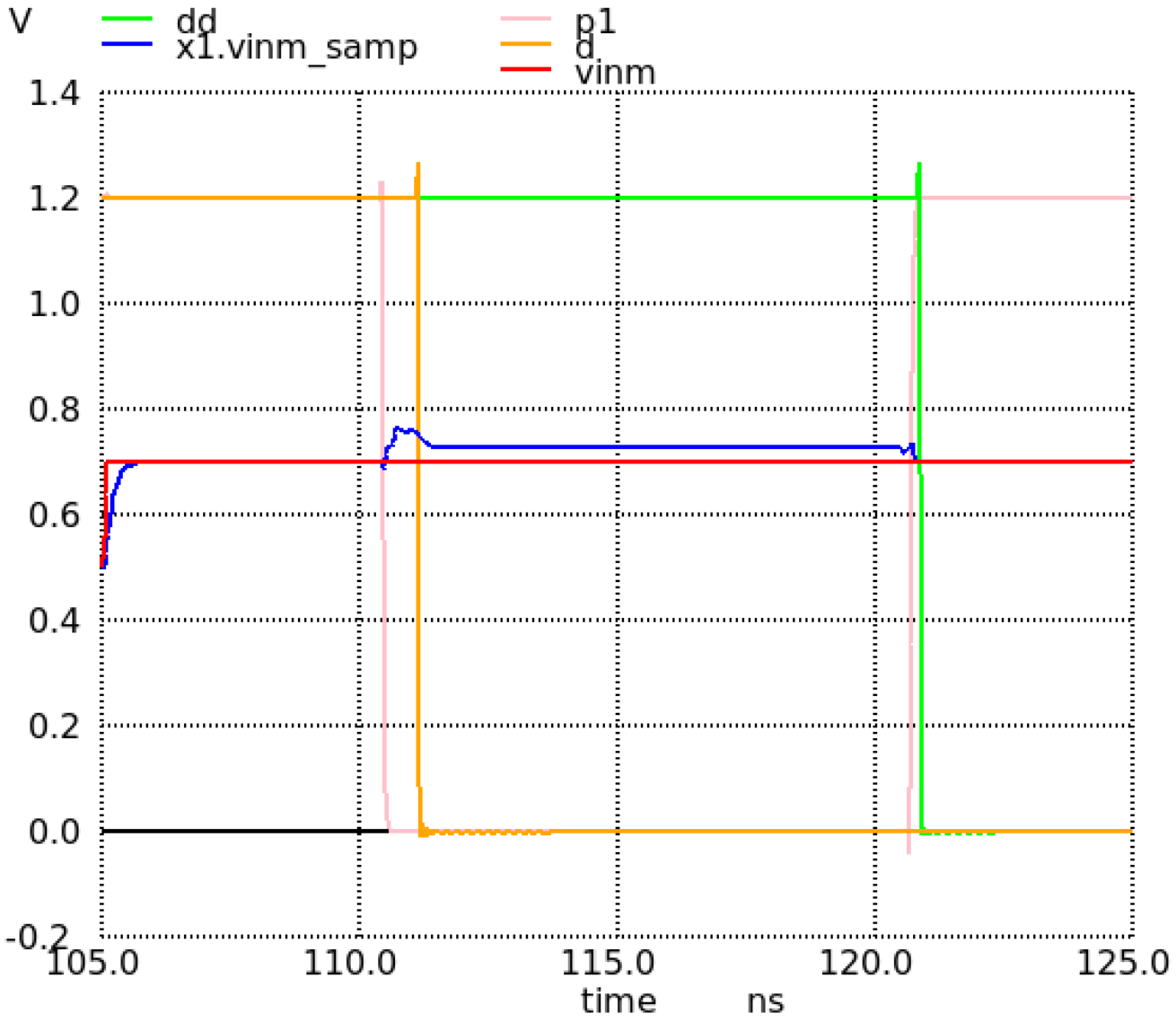
XSCHEM

Boris Murmann

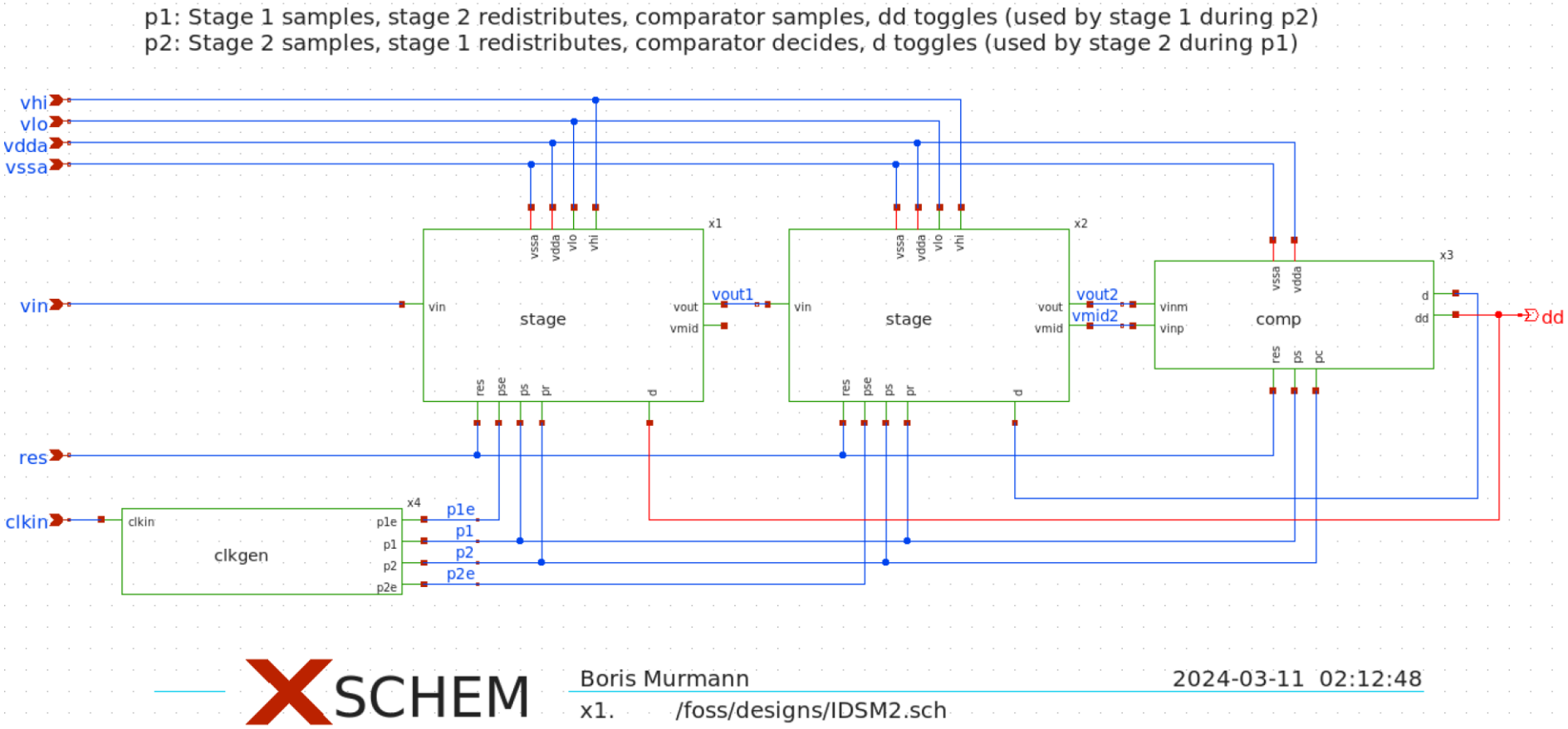
/foss/designs/tb_comp.sch

2024-03-11 00:55:09


V
d
vinm
dd
x1.vinm_samp
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
0.0
50.0
100.0
150.0
200.0
time
ns

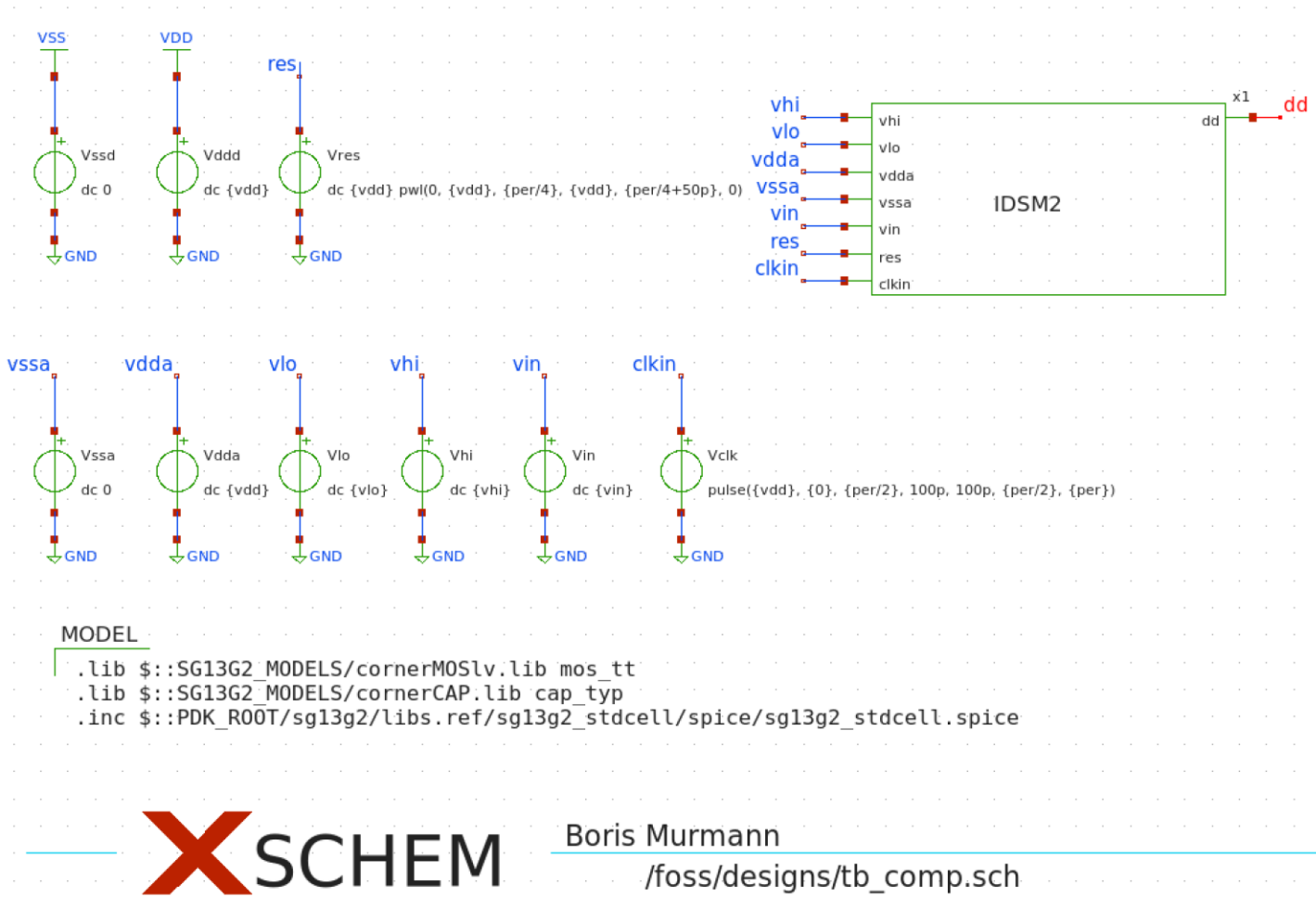

V
dd
x1.vinm_samp
p1
d
vinm
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
105.0
110.0
115.0
120.0
125.0
time
ns

IDSM2



Important: The top-level schematic of your circuit should contain only elements that can be built on chip (Do not include any spice elements

IDSM2 Testbench



MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
.lib $::SG13G2_MODELS/cornerCAP.lib cap_typ
.inc $::PDK_ROOT/sg13g2/libs.ref/sg13g2_stdcell/spice/sg13g2_stdcell.spice
```

NGSPICE

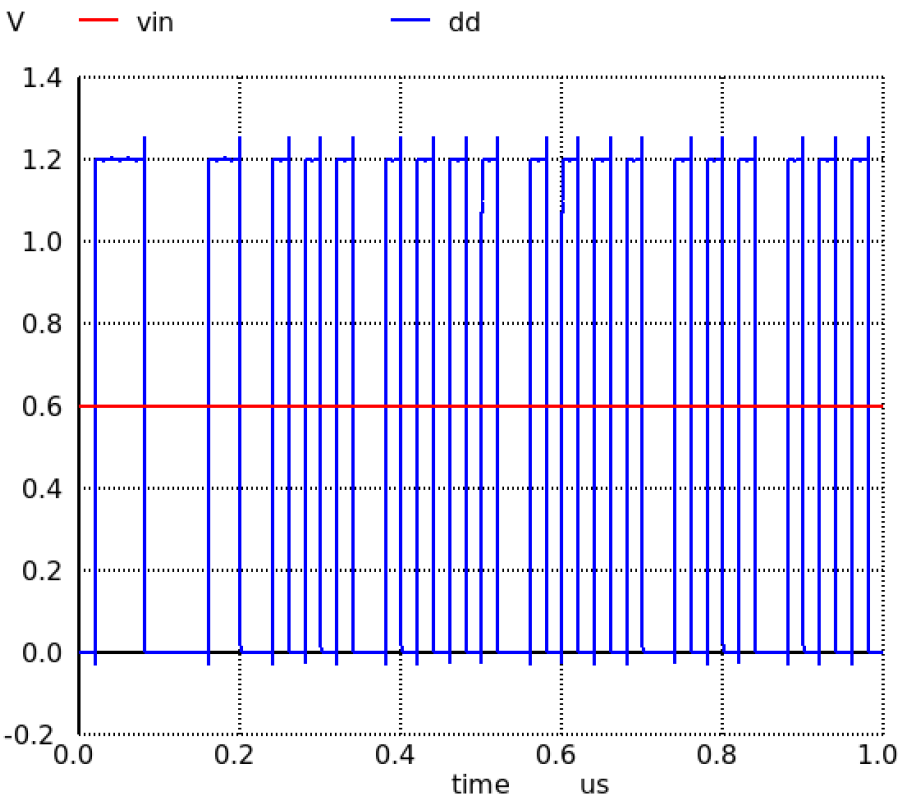
```
.param temp=27 per=20n vdd=1.2
.param vlo=0.3 vhi=0.9 vin=0.6
.option method = gear2 reltol=1e-5
.ic v(x1.x3.out1p)=0
.meas tran iavg_ana AVG i(Vdda)
.meas tran iavg_dig AVG i(Vddd)

.control
tran 100p 1u
set color0 = white
plot vin dd
.endc
```

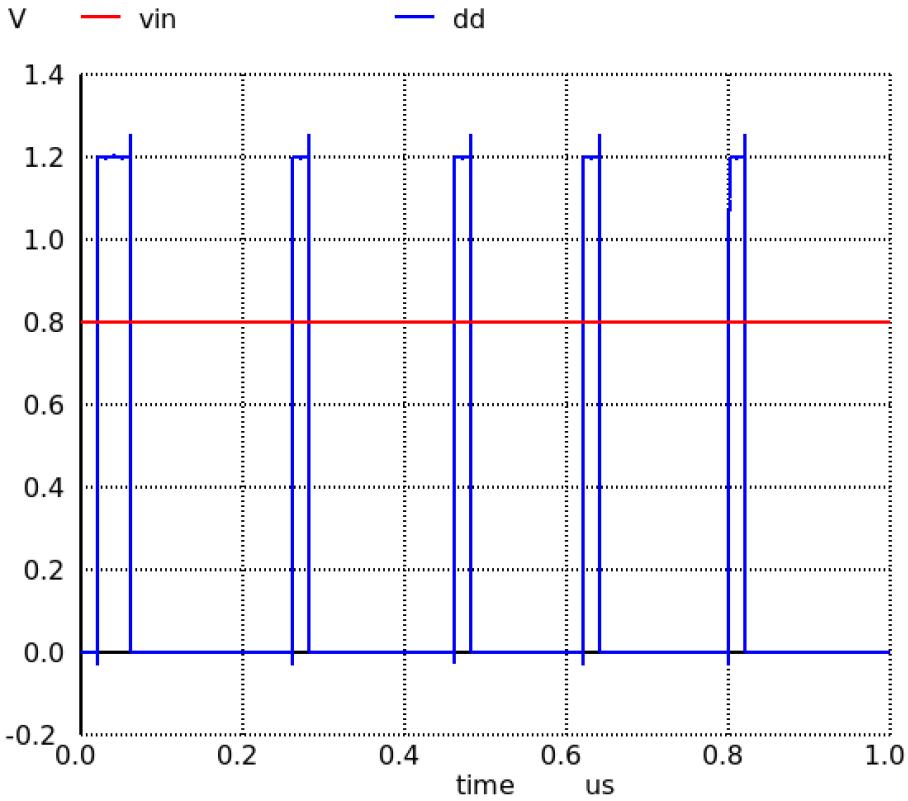
XSCHEM

Boris Murmann

/foss/designs/tb_comp.sch

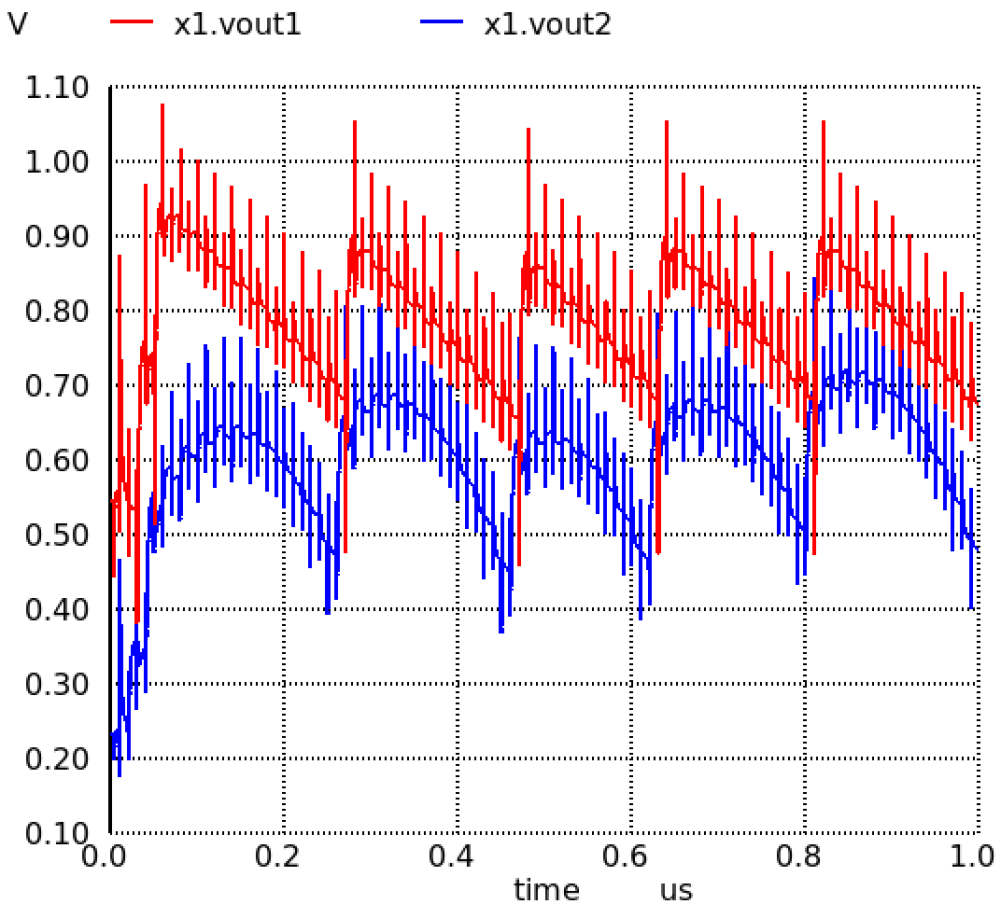
2024-03-11 02:52:25





Basic performance test to runt: Simulate with three DC inputs, post-process bit steam with decimation filter, and verify that the three digital output samples lie on a straight line

Integrator Outputs



Always verify that integrators don’t saturate

Power Consumption

```
  Measurements for Transient Analysis

iavg_ana            =  -1.112856e-04 from=  0.000000e+00 to=  1.000000e-06
iavg_dig            =  -1.913604e-05 from=  0.000000e+00 to=  1.000000e-06
```

$$P = 1.2V(111\mu A + 19\mu A) = 156\mu W$$

- The reference design by Chae et al. consumes only 40 μW
- Optimization opportunities
  - Scale down stage 2
  - Share Vmid generator between stages (Chae likely does not count power of Vmid generation)
  - …