Incremental Delta-Sigma Modulators

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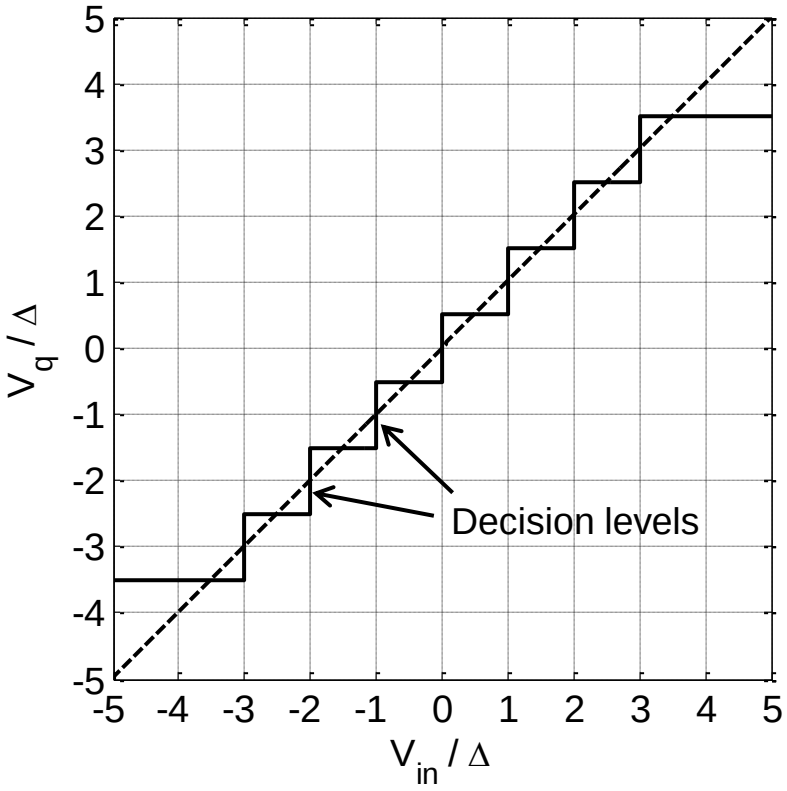
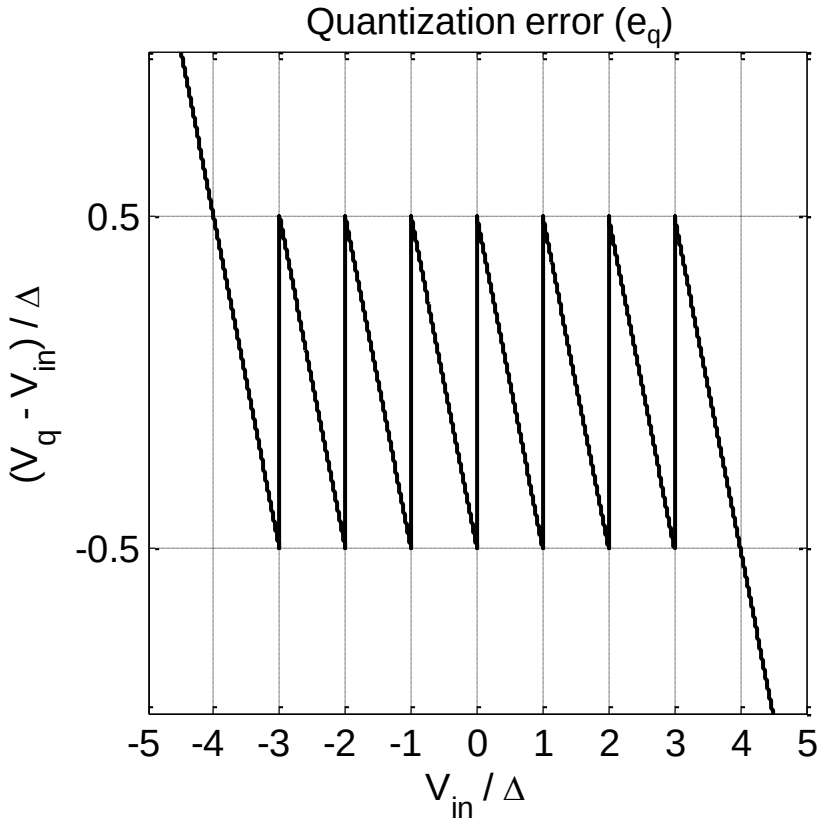
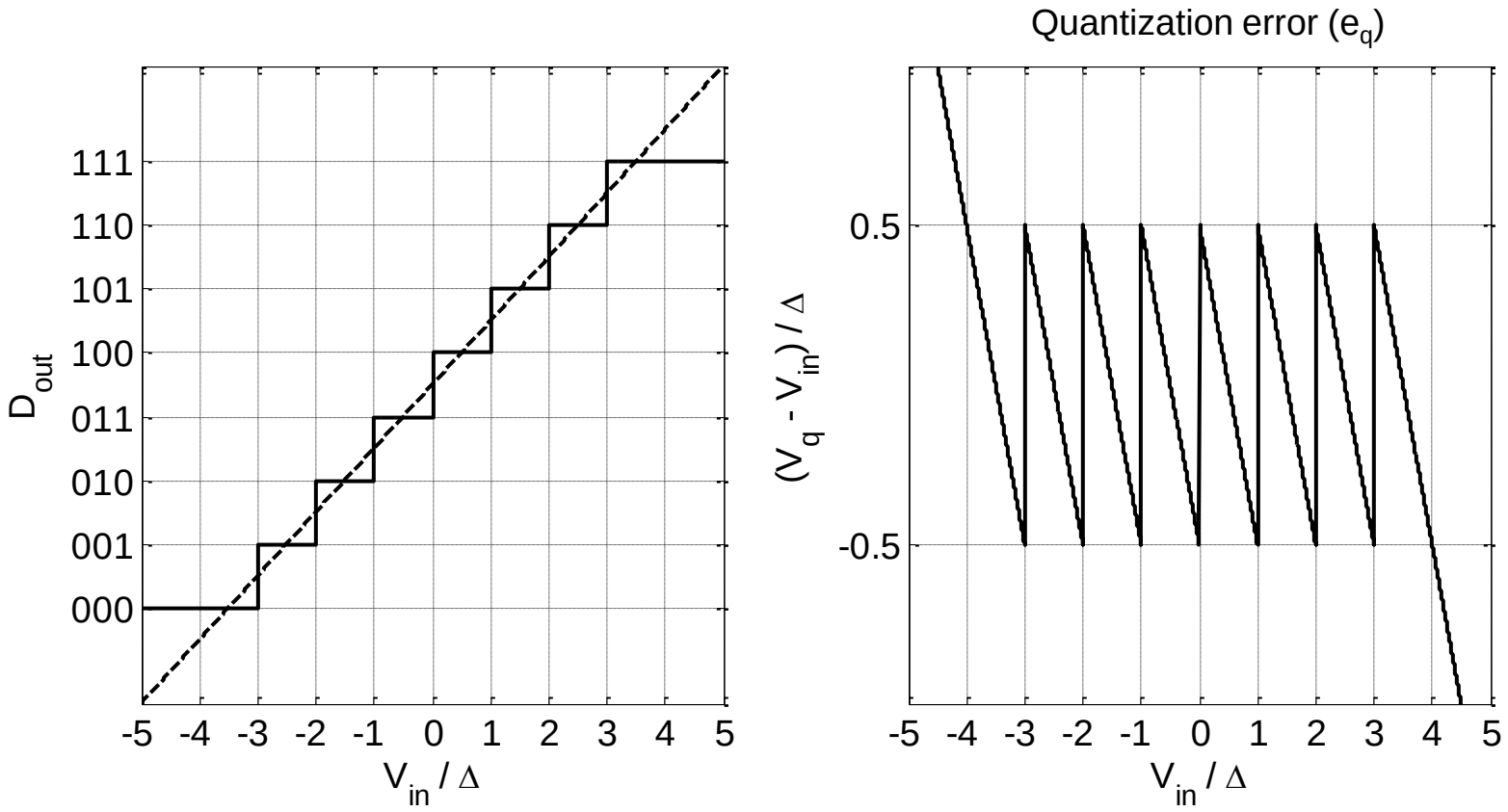
Basics of Quantization





- Example of a 3-bit quantizer (2^3 output levels)
- Quantization step size (or “LSB size”) is Δ
- Full-scale range defined by region with quantization error magnitude < $\Delta/2$

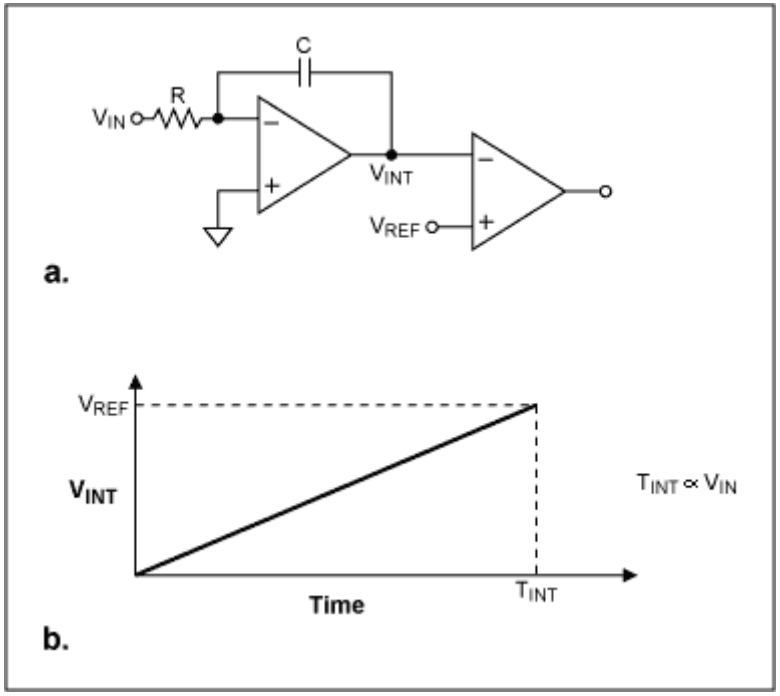
Output Encoding



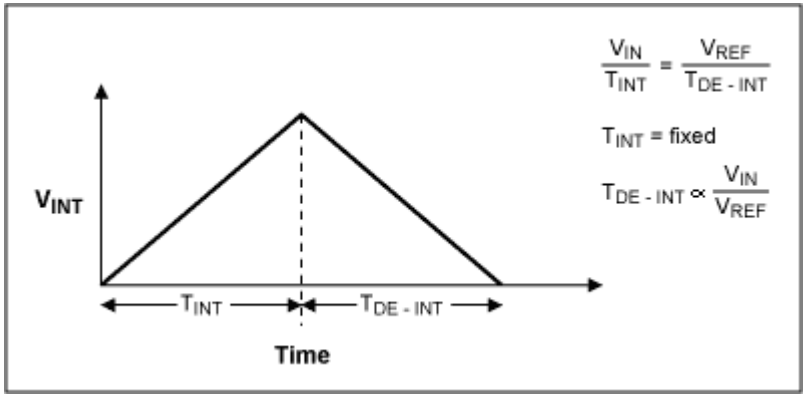
- The output of a real quantizer is mapped into a digital code
  - Many options exist, shown is a basic binary encoding

Single- and Dual-Slope ADCs

Single slope

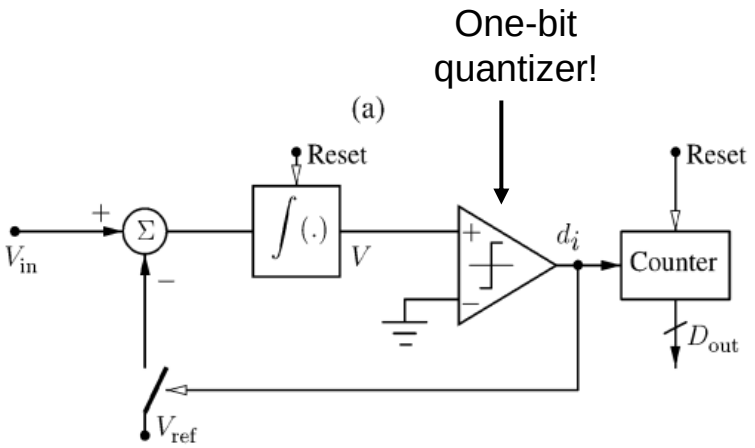


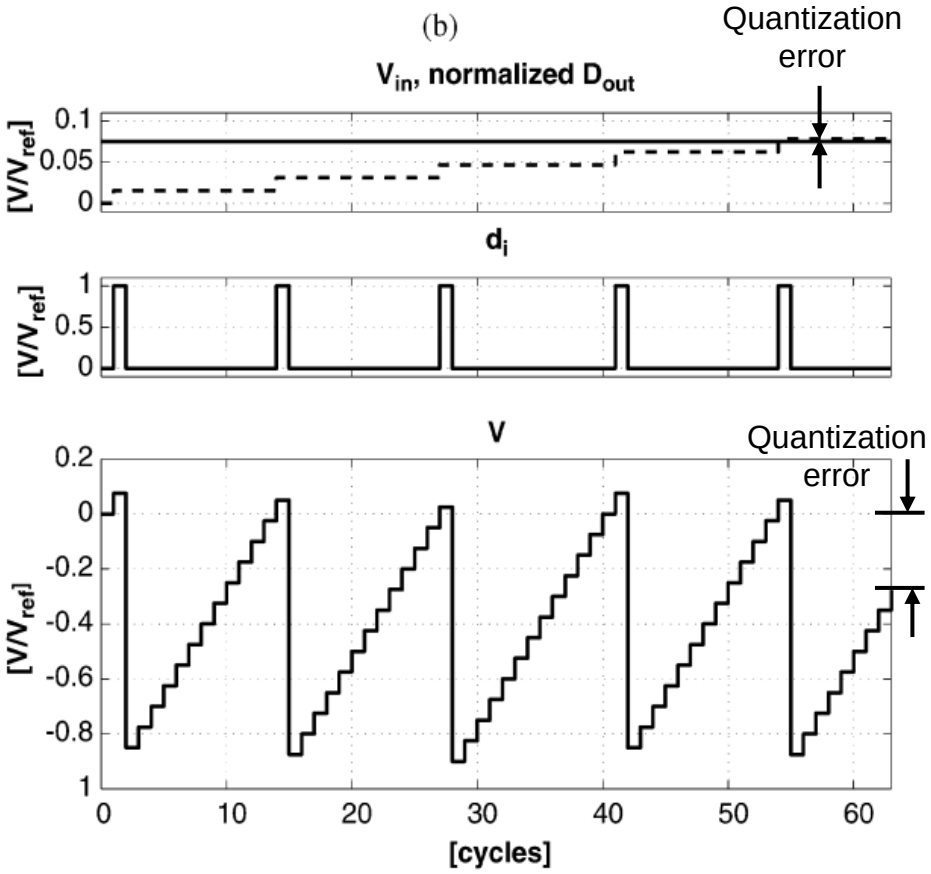
Dual slope



Quantization error comes from discretization of steps or threshold crossing

First Order Incremental Delta Sigma Converter

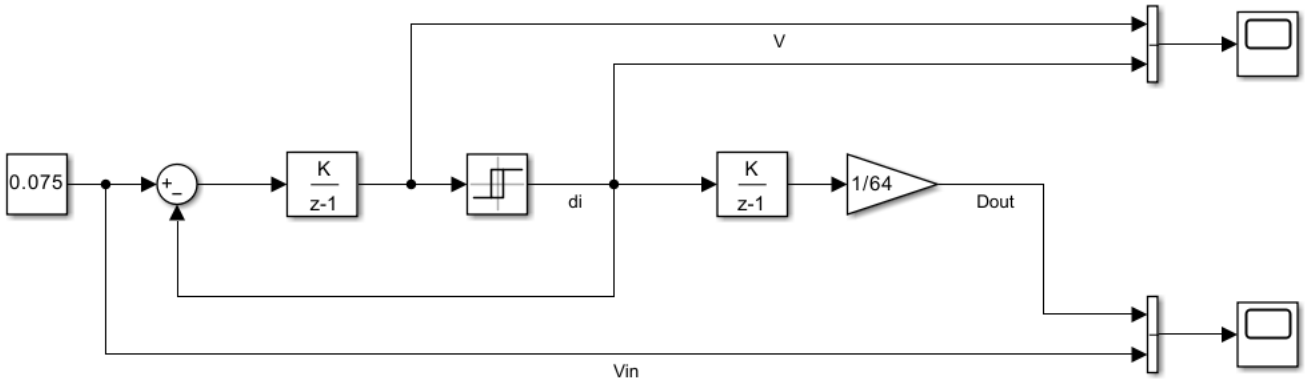


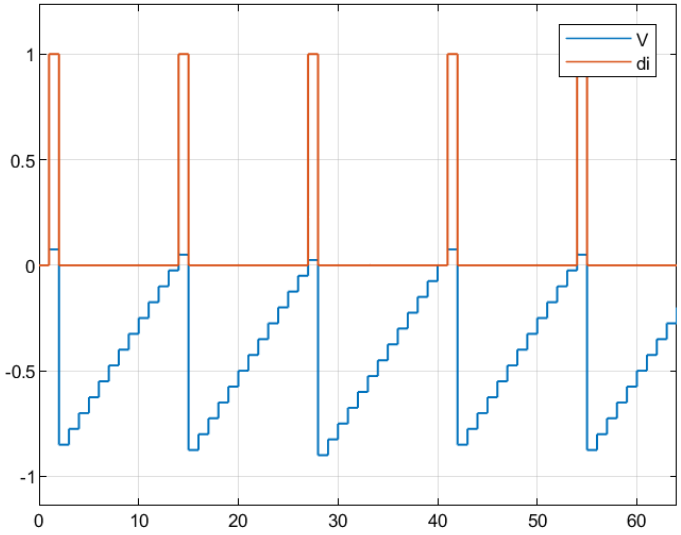


- Similar to dual-slope, but V_{in} integration and V_{ref} de-integration occur together
- Number of de-integration pulses (d_i) is proportional to V_{in} → use a counter
- Ideally V should be zero at the end of conversion, but it can be anywhere between $-V_{ref}$ and V_{in} → quantization error

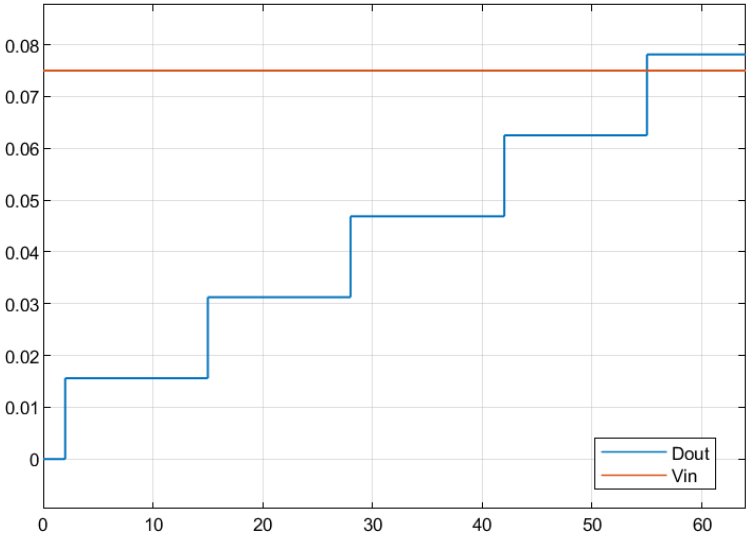
J. Markus, J. Silva and G. C. Temes, "Theory and applications of incremental Delta Sigma converters," in IEEE Transactions on Circuits and Systems I, April 2004. https://ieeexplore.ieee.org/document/1284742

Simulink Model





Time step



Time step

Analysis

$$V = \sum (V_{in} - d_i V_{ref}) \qquad \sum d_i = D_{out}$$

(counter)

$$V = nV_{in} - D_{out}V_{ref} = \epsilon$$

$$\frac{D_{out}}{n} = \frac{V_{in}}{V_{ref}} - \frac{1}{n}\frac{\epsilon}{V_{ref}}$$

- Error is dived by the number of clock cycles per conversion (n)
- Can we do better, e.g., n^2?

Second-Order Approach

$$V = \sum\sum (V_{in} - d_i V_{ref})$$

$$\sum\sum d_i = D_{out}$$

(cascaded counters)

$$V = \frac{n(n+1)}{2} V_{in} - D_{out} V_{ref} = \epsilon$$

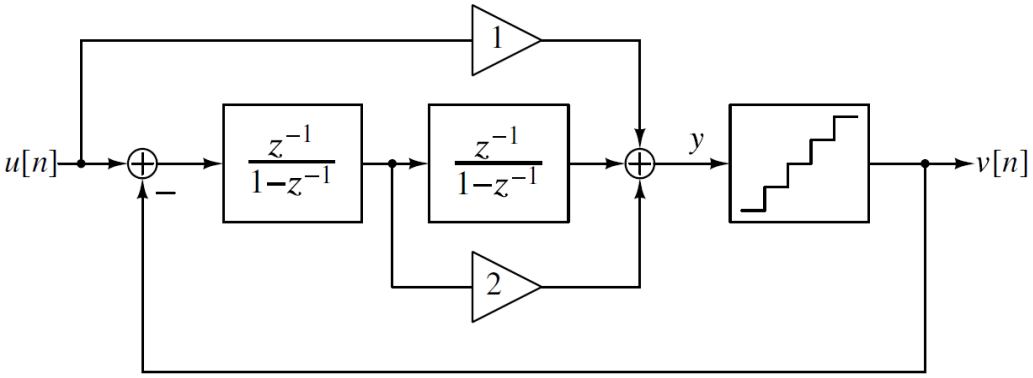
$$\sum_i^n i = \frac{n(n+1)}{2}$$

$$\frac{D_{out}}{\frac{n(n+1)}{2}} \approx \frac{V_{in}}{V_{ref}} - \frac{2}{n^2}\frac{\epsilon}{V_{ref}}$$

- Much better! Need fewer clock cycles to get accurate reading

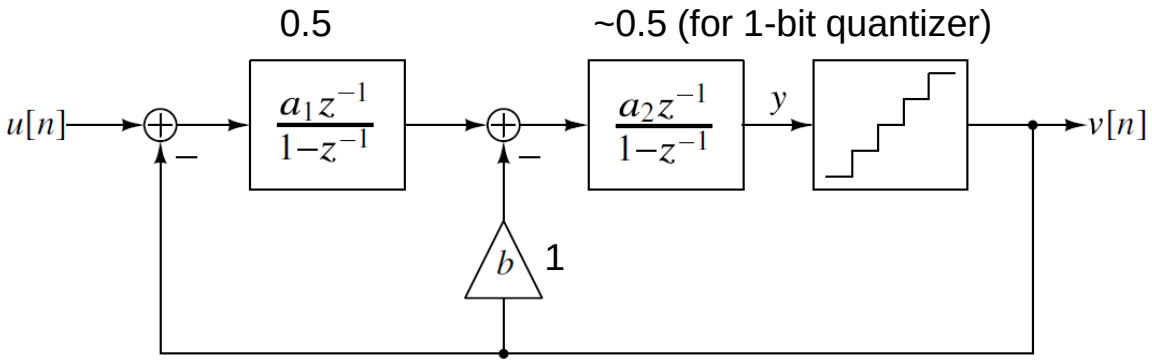
How to Implement?

CIFF architecture



Silva–Steensgaard modulator

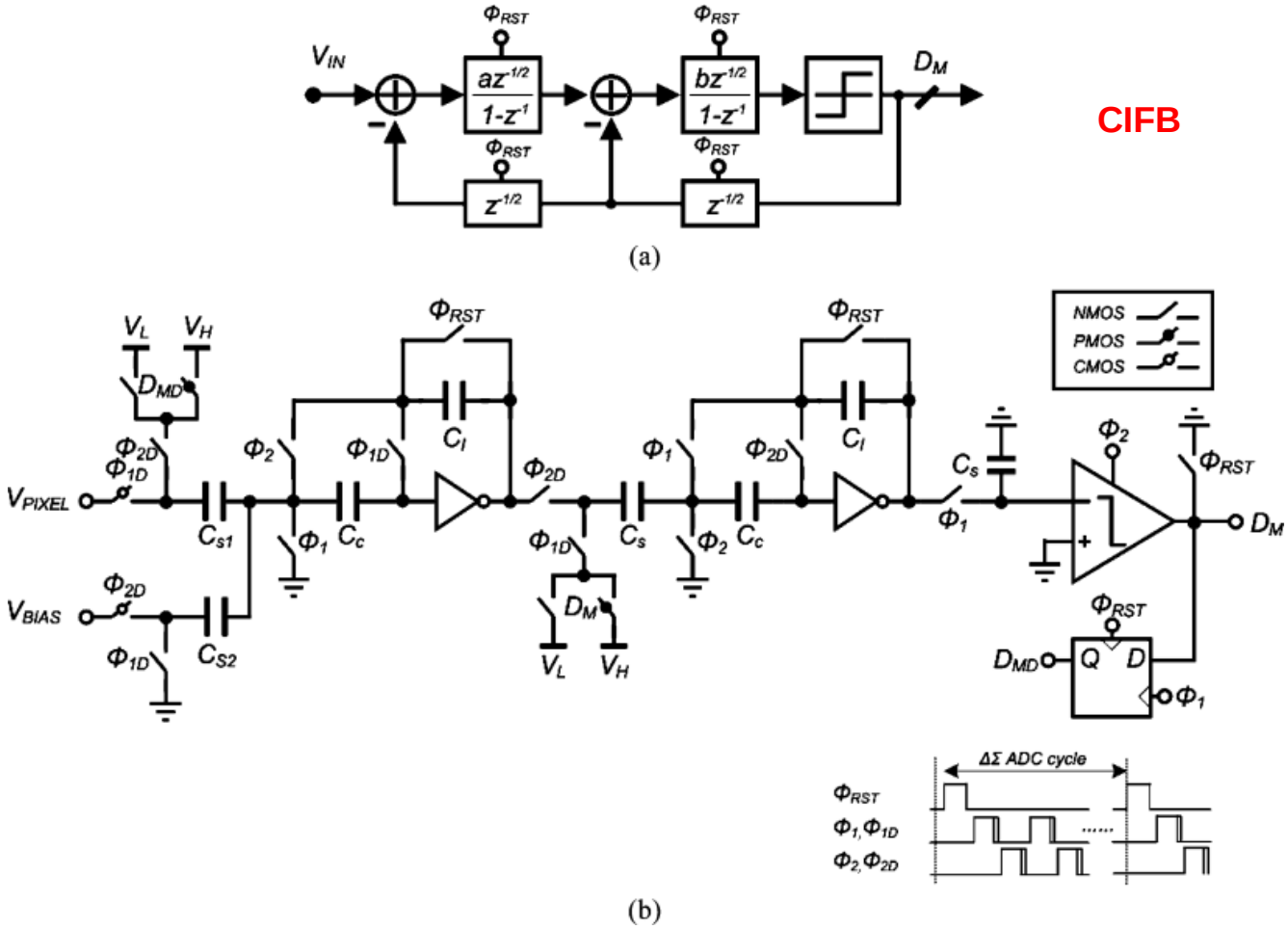
CIFB architecture



Boser-Wooley modulator

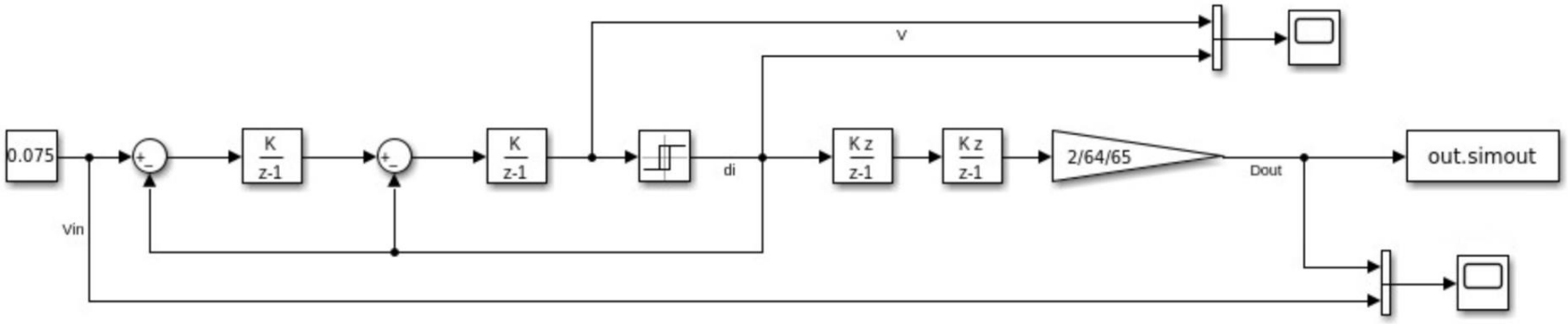
- Cannot just use two plain integrators in a loop (stability)

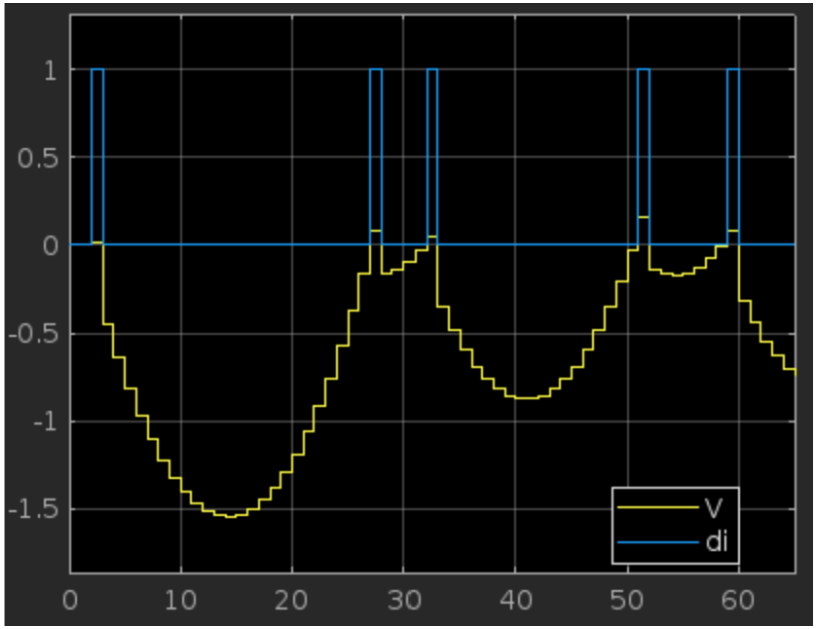
Template Project

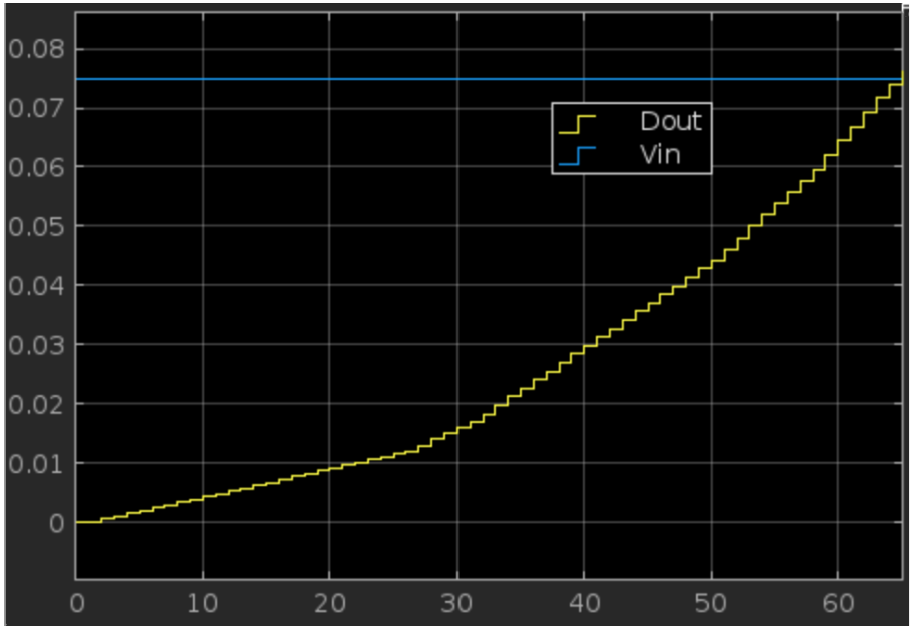


Y. Chae et al., "A 2.1 M Pixels, 120 Frame/s CMOS Image Sensor With Column-Parallel ADC Architecture," in IEEE Journal of Solid-State Circuits, Jan. 2011. https://ieeexplore.ieee.org/document/5641589

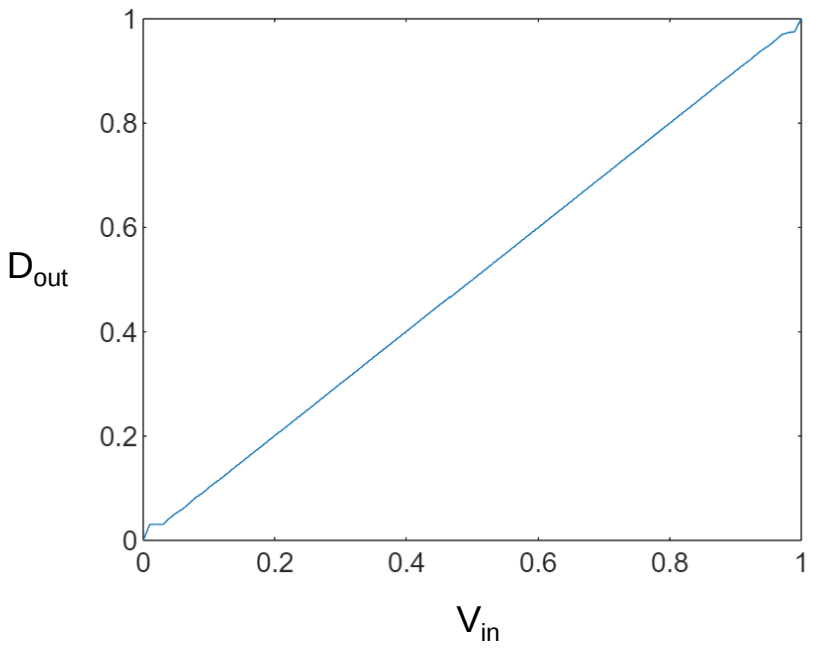
Simulink Model

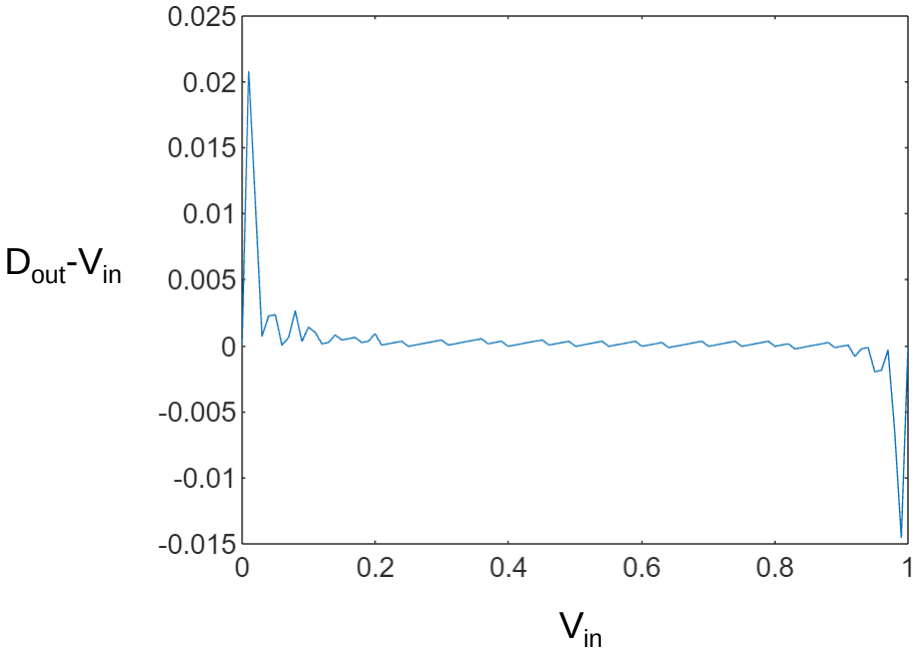




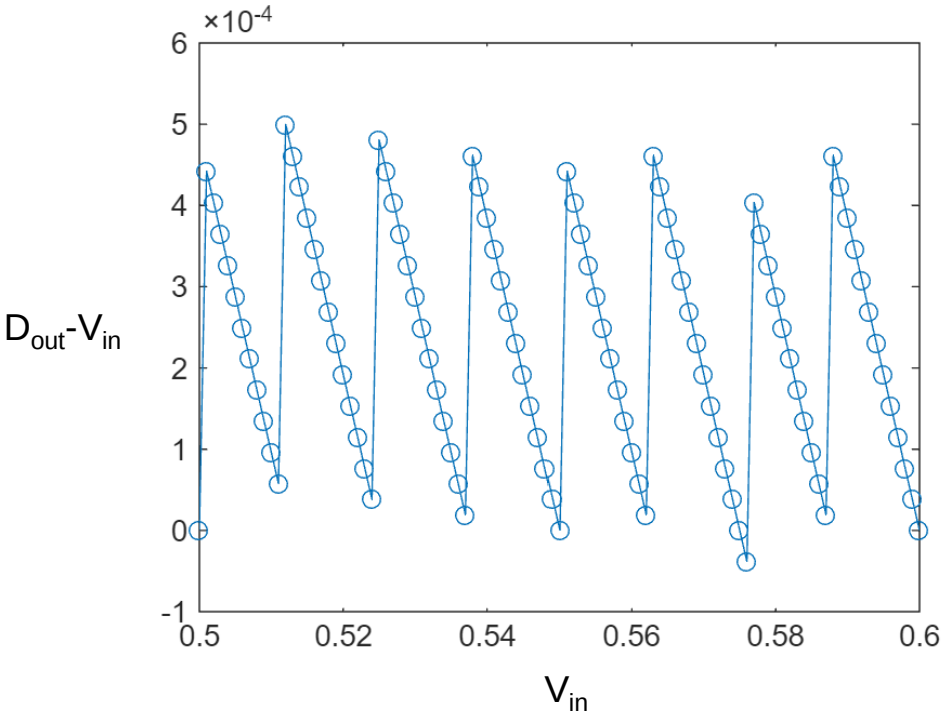


Transfer Function and Quantization Error



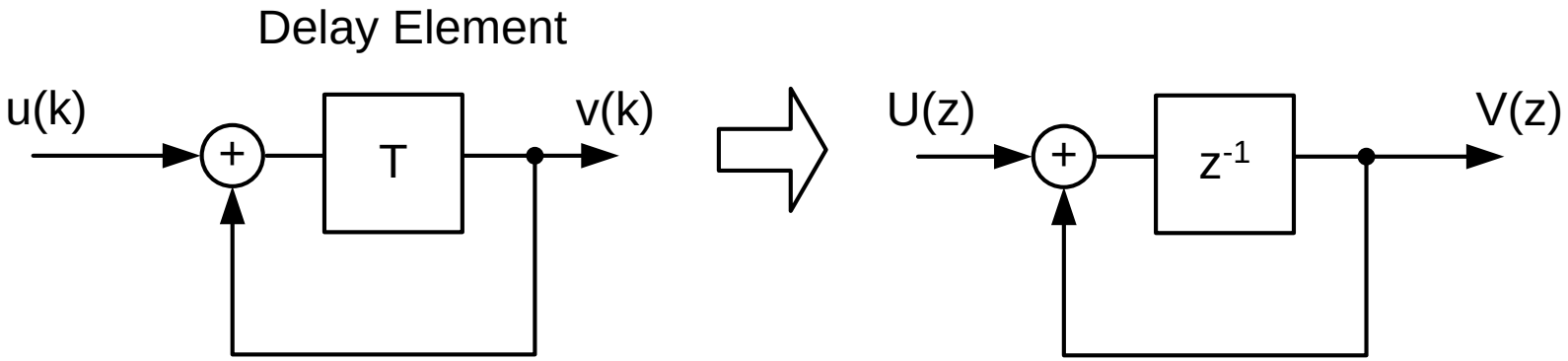


Zooming In



Expected bound ~$2/n^2$ ~ $4.9 \cdot 10^{-4}$ → pretty close!

Ideal Discrete Time Integrator

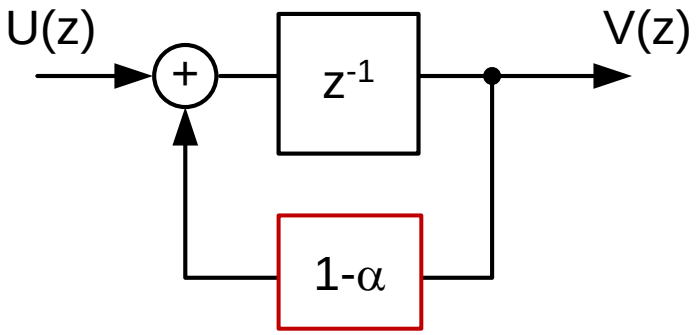


$$v(k) = u(k-1) + v(k-1) \qquad V(z) = z^{-1}U(z) + z^{-1}V(z)$$

$$\frac{V(z)}{U(z)} = \frac{z^{-1}}{1 - z^{-1}} = \frac{1}{z-1} \qquad z = e^{j\omega T}$$

- Infinite gain at DC (ω=0, z=1)
- Finite gain in the analog circuit realization will be a problem…

Leaky Discrete Time Integrator



$$V(z) = z^{-1}U(z) + (1-\alpha)z^{-1}V(z)$$

$$\frac{V(z)}{U(z)} = \frac{z^{-1}}{1-(1-\alpha)z^{-1}}$$

- DC gain is 1/α
- Detailed analysis shows that we need 1/α > n (number of cycles)
  - Can try this out using our simulation model!
  - Replace ideal integrator with above model