Inverter-Based Integrator

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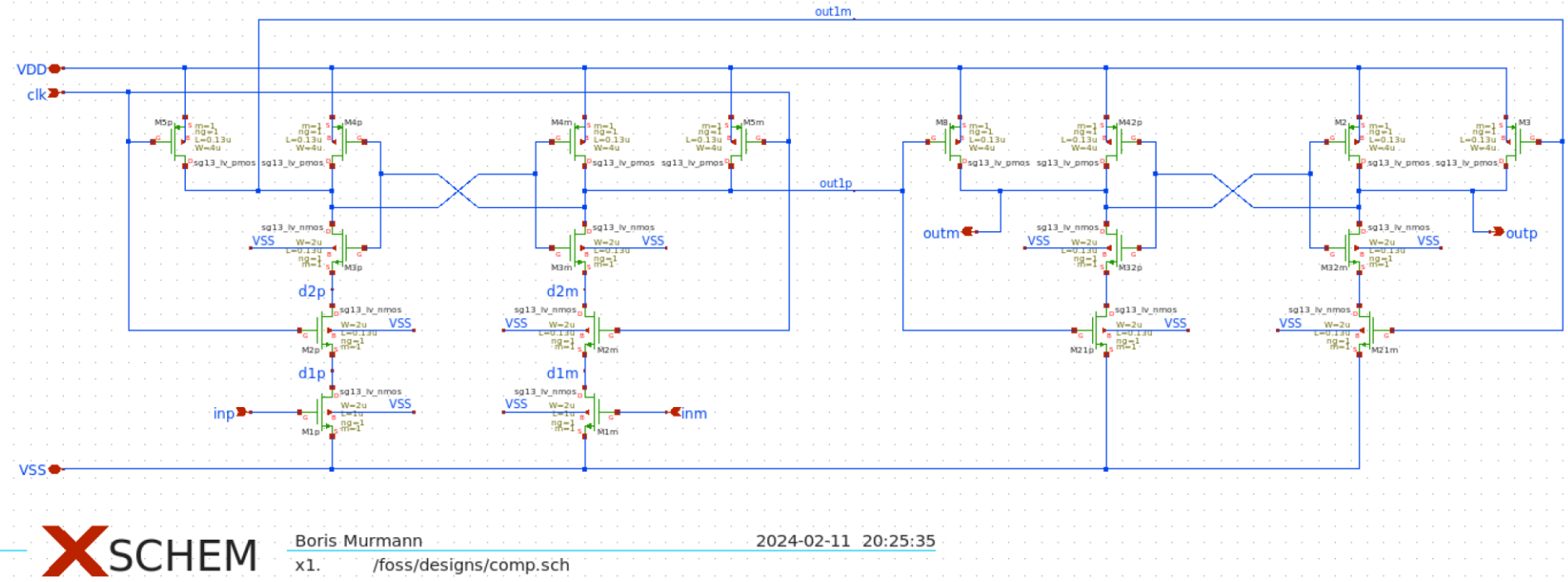
Comparator with Storage Latch



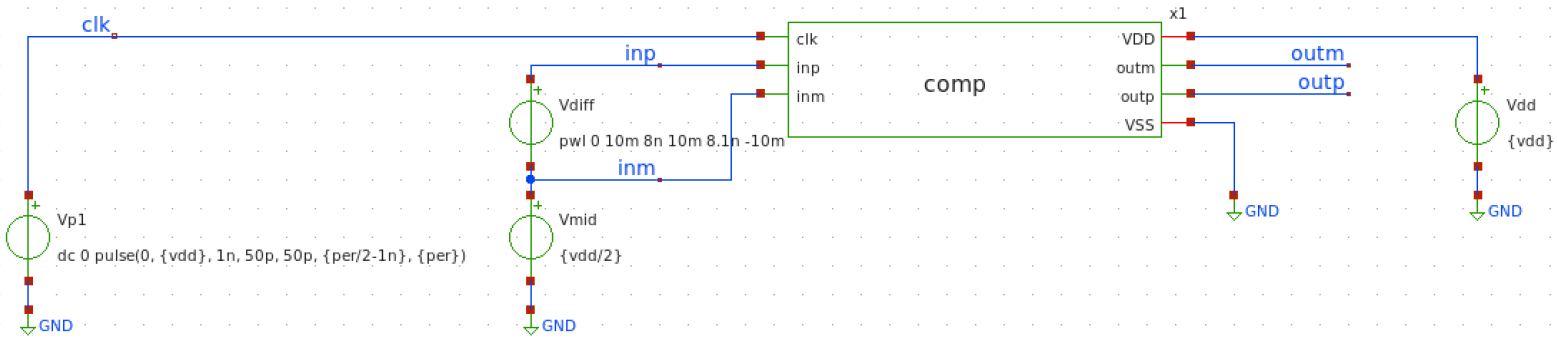
NGSPICE

```
.param temp=27 vdd=1.2 per=10n vdiff=10m
.option method=gear reltol=1e-5
.ic v(outp)=0

.control
save all
tran 10p 20n
plot clk x1.out1m x1.out1p
plot outm outp
.endc
```

MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
```



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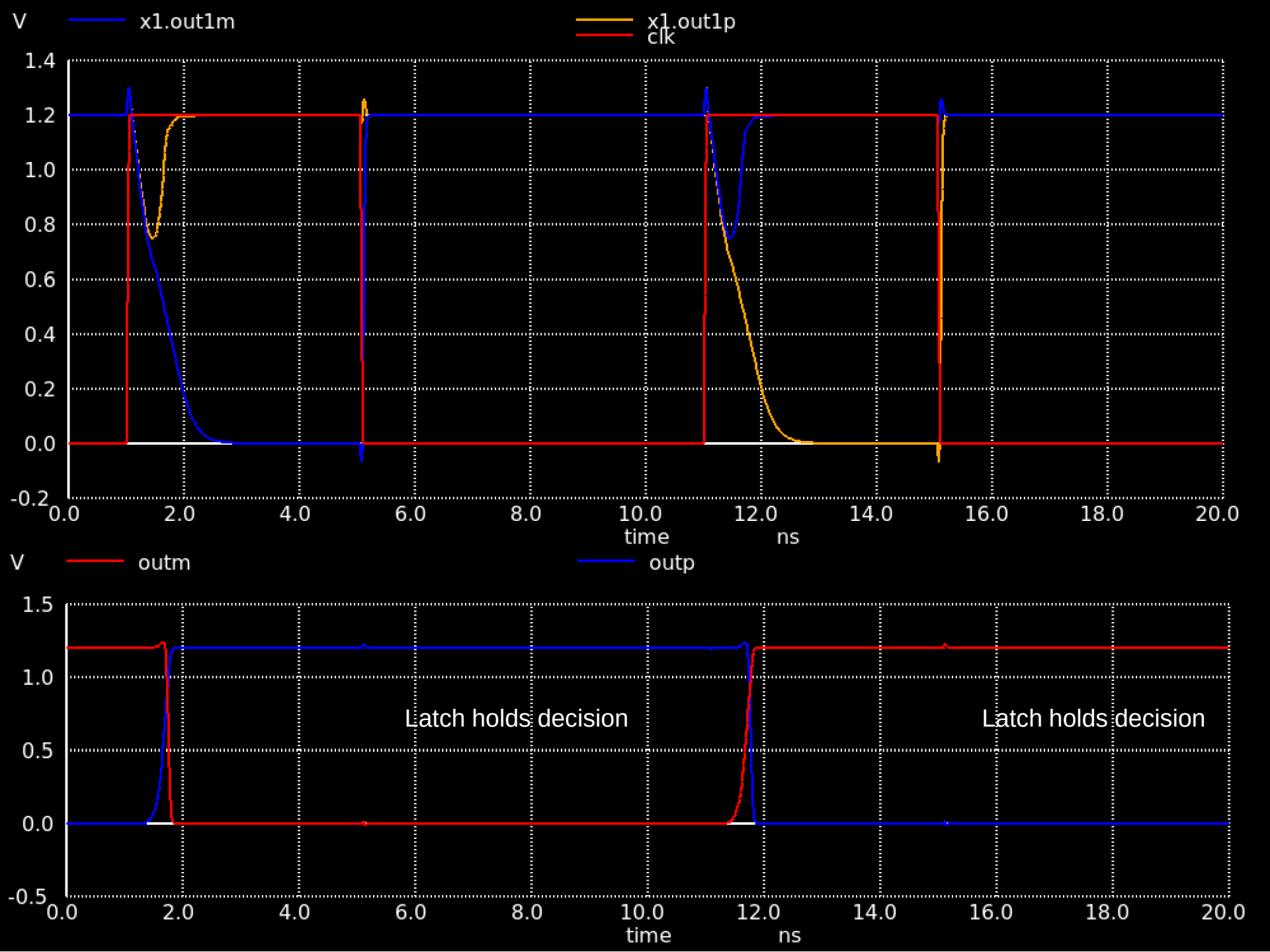
/foss/designs/tb_comp.sch

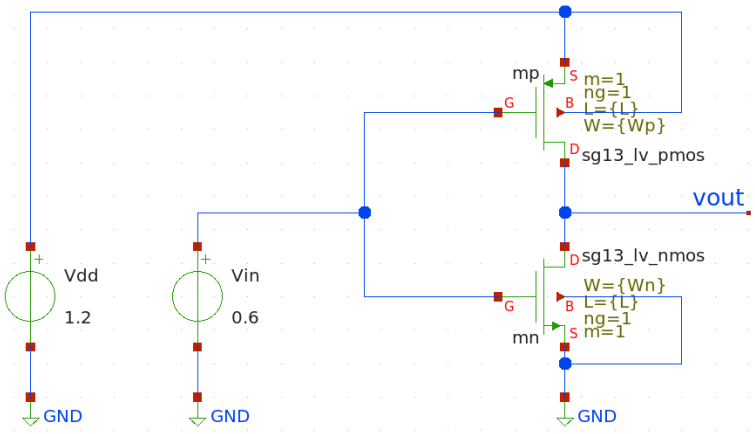

V
x1.out1m
x1.out1p
clk
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
-0.2
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
ns
V
outm
outp
1.5
1.0
0.5
0.0
-0.5
Latch holds decision
Latch holds decision
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
time
ns

Next Steps

- Build integrator with inverter
  - Make sure circuit is practical (using VMID instead of GND, etc.)
  - Use reasonably large L for good initial gain

- Verify operation and see how much “effective gain” we can achieve
  - Compare response to idealized circuit without gain enhancement. Adjust VCVS gain until responses are equal → effective gain
  - Note that the improvement may be somewhat less than expected due to the inverter input capacitance
  - See Chae’s paper for details

Inverter Gain in Our Technology



COMMANDS

```
.param temp=27
.param Wn=4u Wp={2*Wn} L=0.13u

.control
dc Vin 0.2 1 1m
alterparam L=1.5u
reset
dc Vin 0.2 1 1m
plot dc1.vout dc2.vout
plot deriv(dc1.vout) deriv(dc2.vout)
.endc
```

MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
```

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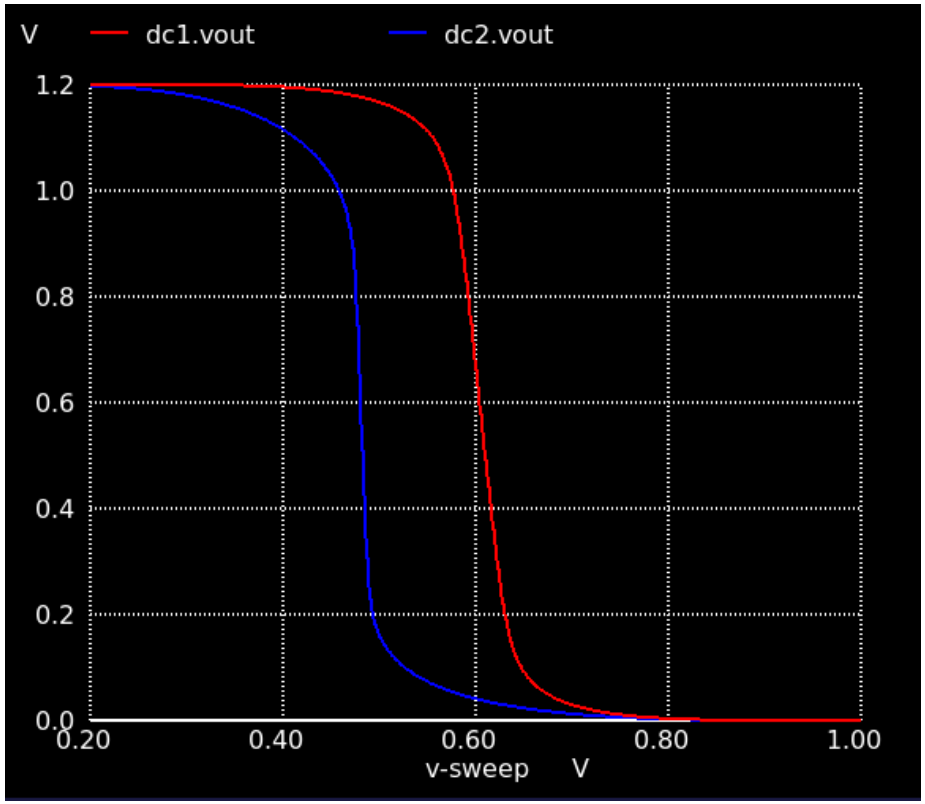
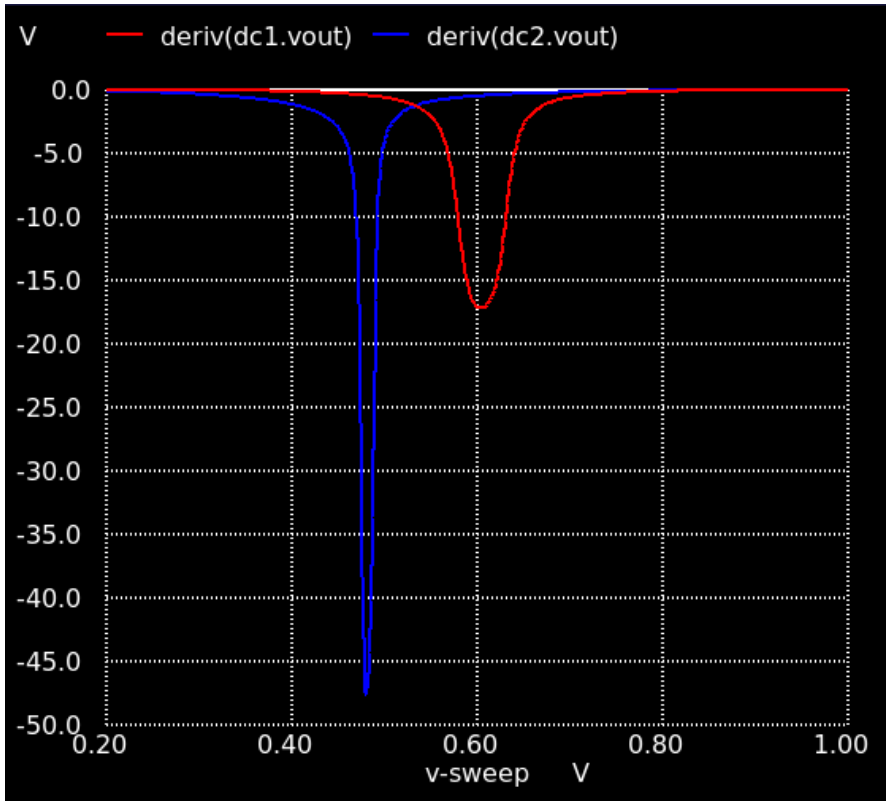
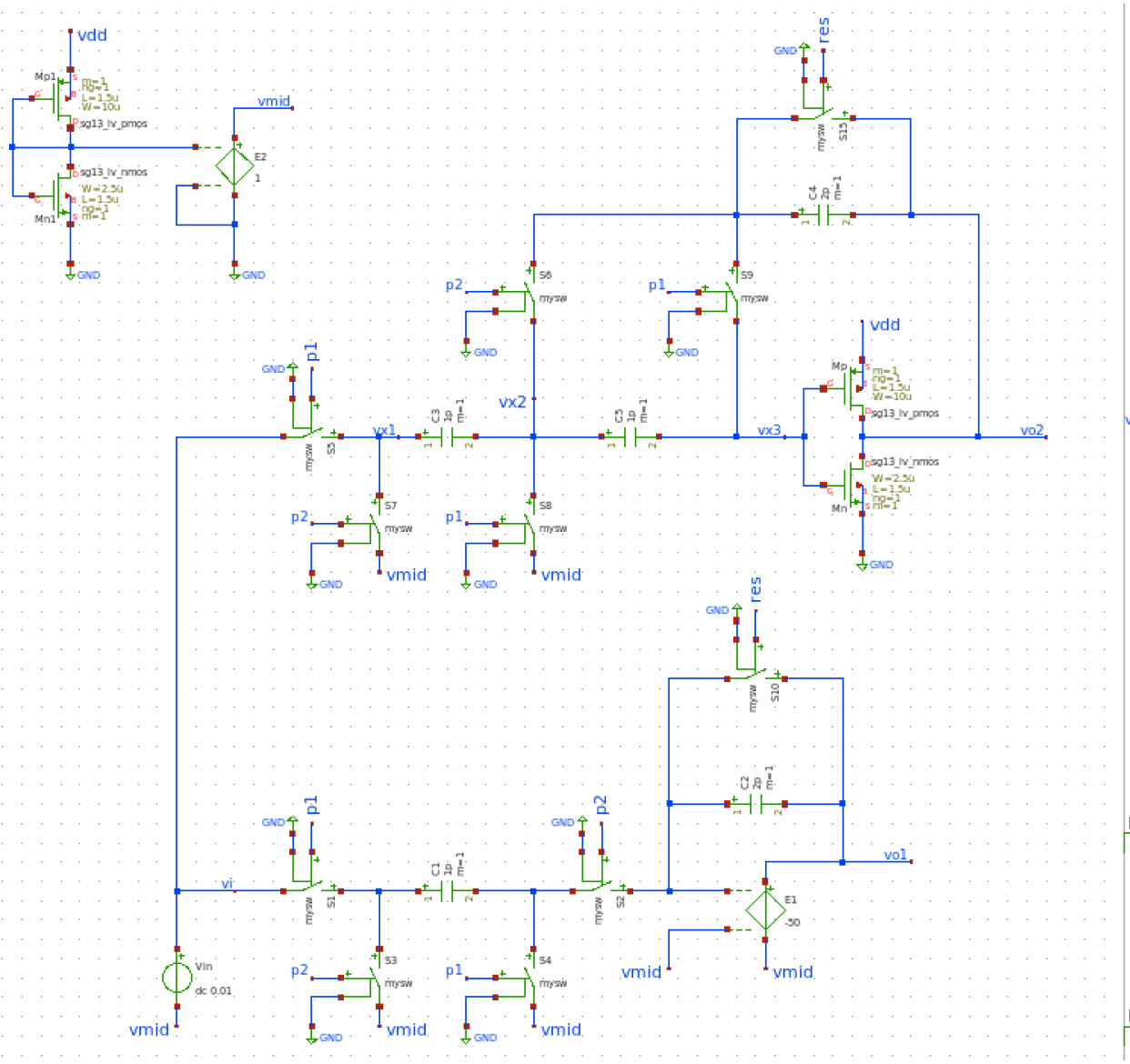
/foss/designs/tb_inv_gain.sch

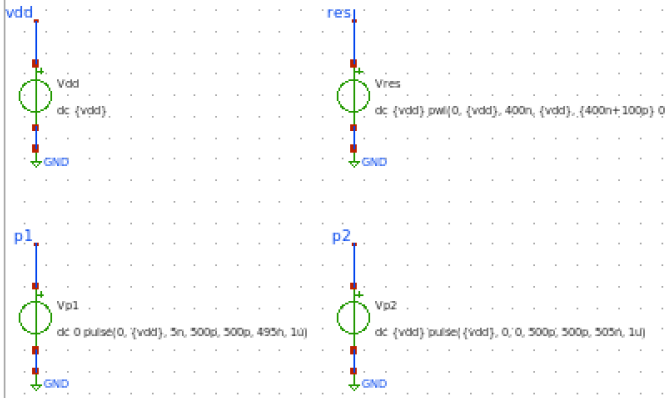




Use channel lengths of at least 1.5 um to get gain close to 50

Inverter-Based Integrator



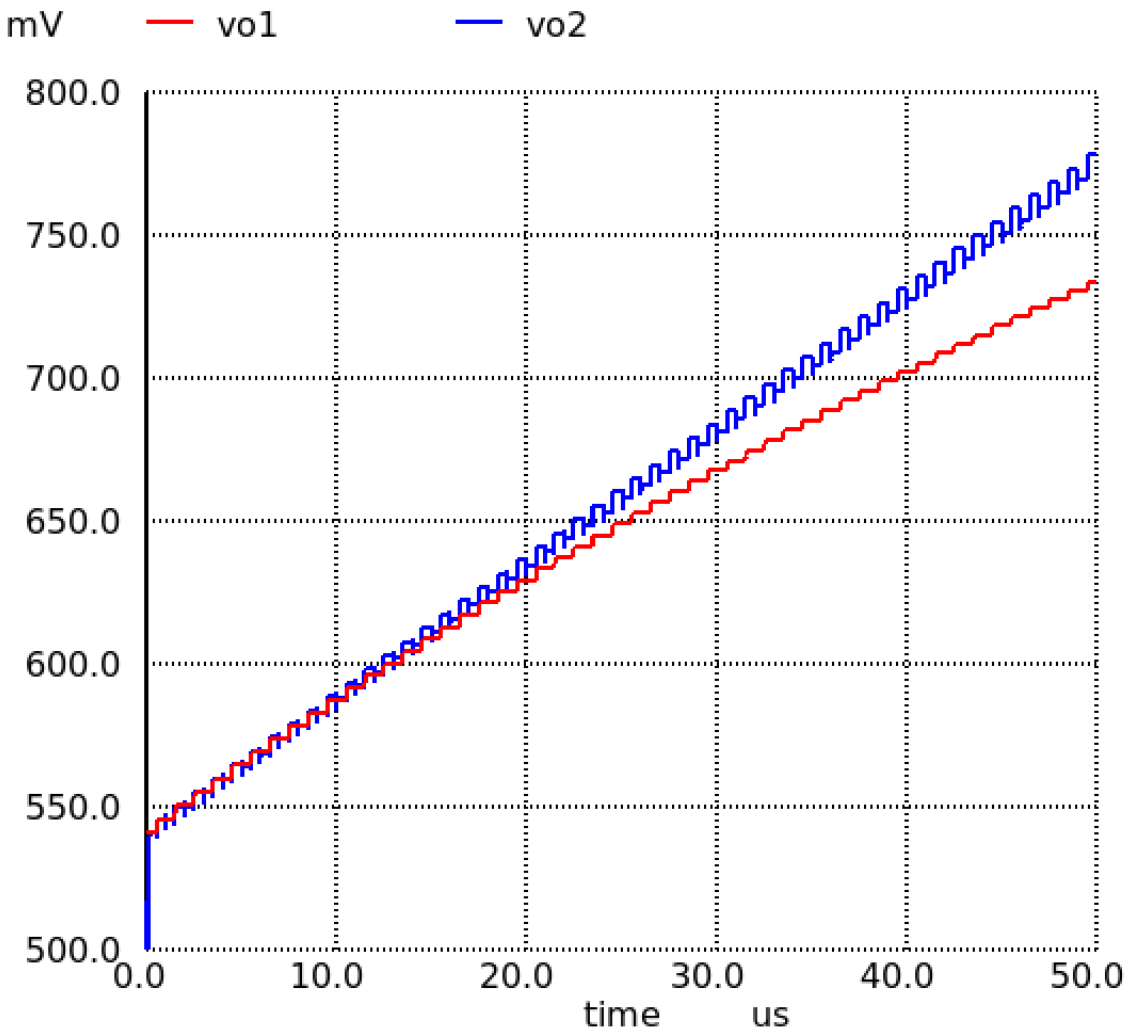


NGSPICE

```
.param temp=27 vdd=1.2
.model mysw SW vt={vdd/2} ron=10k roff=10gig
.control
save all
tran 1n 50u
plot vo1 vo2
.endc
```

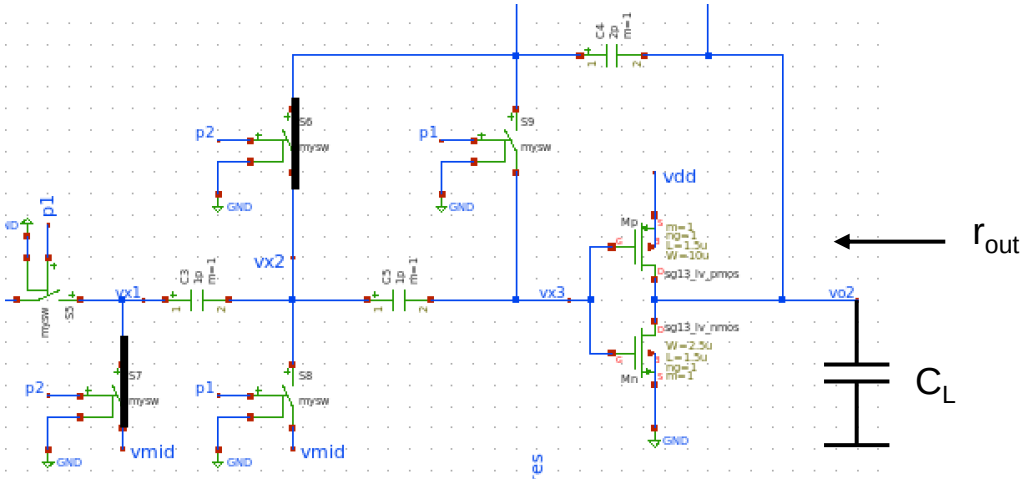
MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
```


mV
vo1
vo2
800.0
750.0
700.0
650.0
600.0
550.0
500.0
0.0
10.0
20.0
30.0
40.0
50.0
time
us

How Large Should the Inverter Be?

Circuit during p2:

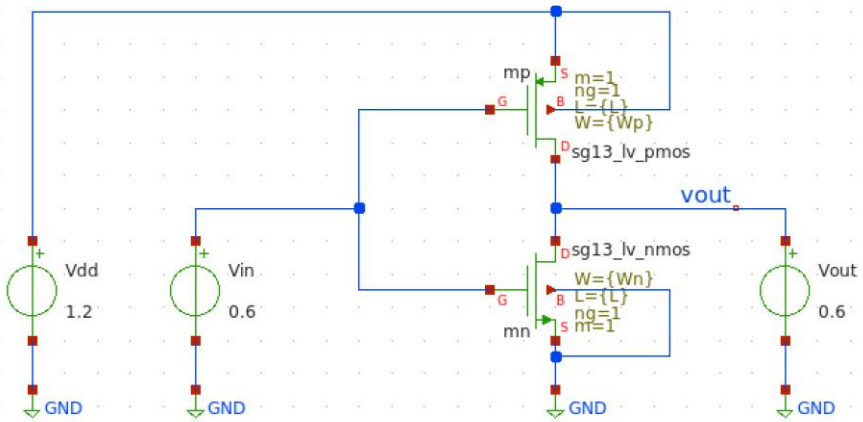


$$r_{out} \approx \frac{1}{\beta(g_{mn} + g_{mp})} \qquad \beta \approx \frac{C_{int}}{C_{int} + C_s} = \frac{2}{2+1} = \frac{2}{3}$$

Need to fit several $\tau = r_{out} C_L$ into half clock period

$$N\tau < \frac{T_s}{2}$$

Measure $g_{mn}+g_{mp}$



COMMANDS

```
.param temp=27
.param Wn=2.5u Wp={4*Wn} L=0.13u

.control
dc Vin 0.2 1 1m
alterparam L=1.5u
reset
dc Vin 0.2 1 1m
set color0 = white
*plot dc1.vout dc2.vout
*plot deriv(dc1.vout) deriv(dc2.vout)
plot i(Vout)
plot deriv(i(Vout))
.endc
```

MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
```

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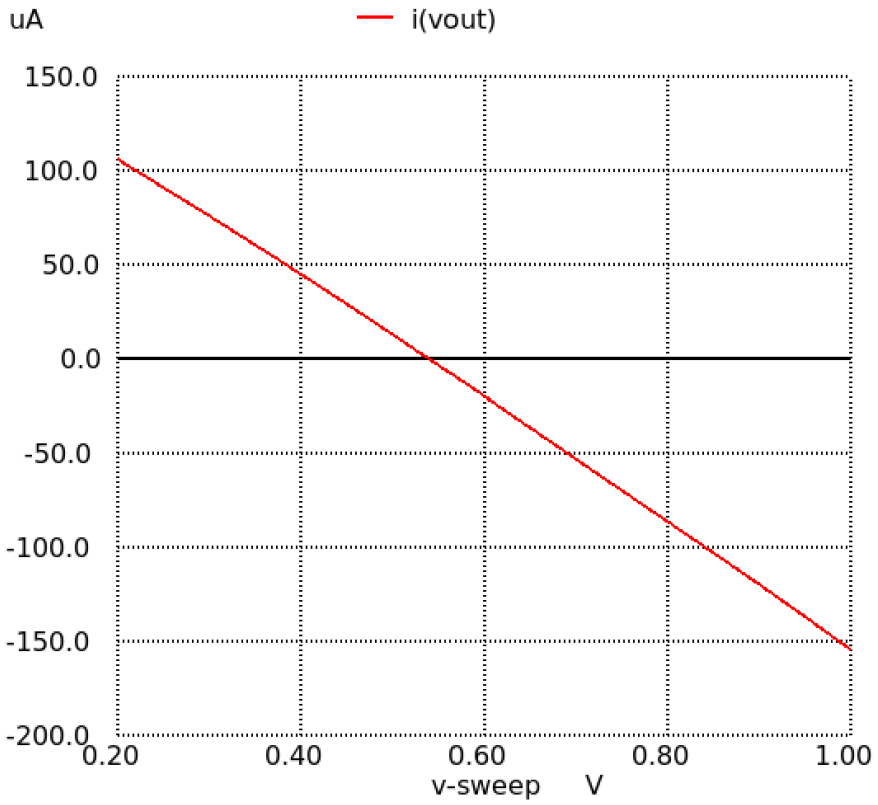
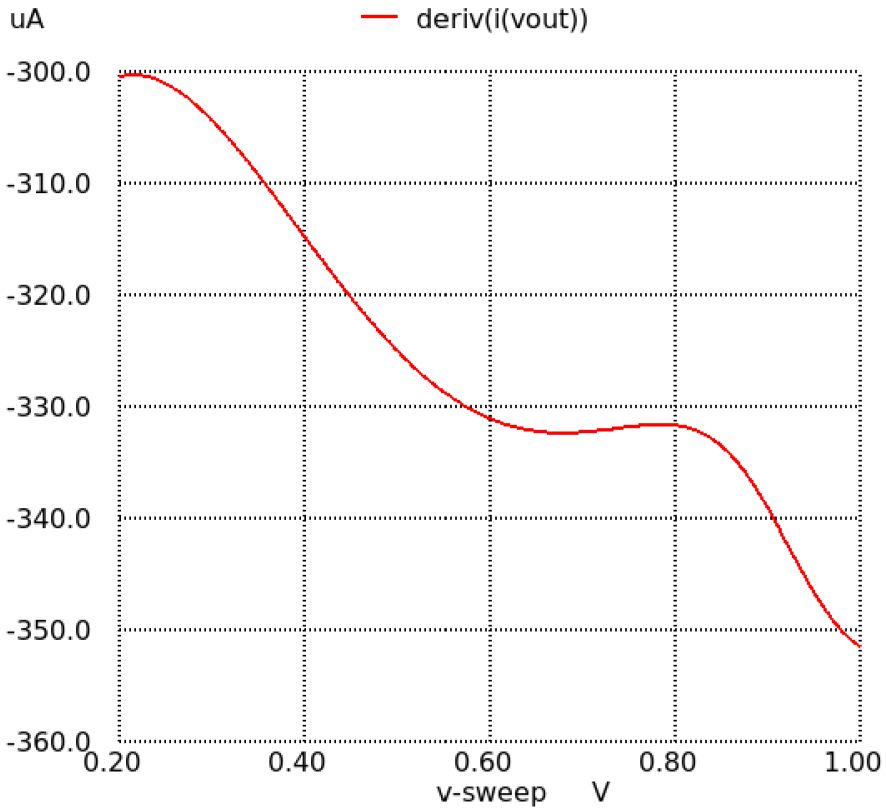
/foss/designs/tb_inv_gain.sch

Result

$g_{mn}+g_{mp}$ ~ 300 uS





Sizing Example

- The example design by Chae is clocked at 48 MHz
- One half clock cycle is 10.4 ns
- Allow settling for 7 time constants → τ = 10.4 ns/7 = 1.5 ns
- If C_L = 1pF, we need r_{out} < 1.5 ns/1 pF = 1.5 kΩ
- $g_{mn}+g_{mp}$ > 1/ 1.5 kΩ / β = 1 mS

- The transconductance of the simulated inverter is about 0.33 mS
- We need to make the inverter about three times bigger
  - N = 7.5/1.5
  - P = 30/1.5

- We'll need to revisit this calculation once we know what C_L should be!