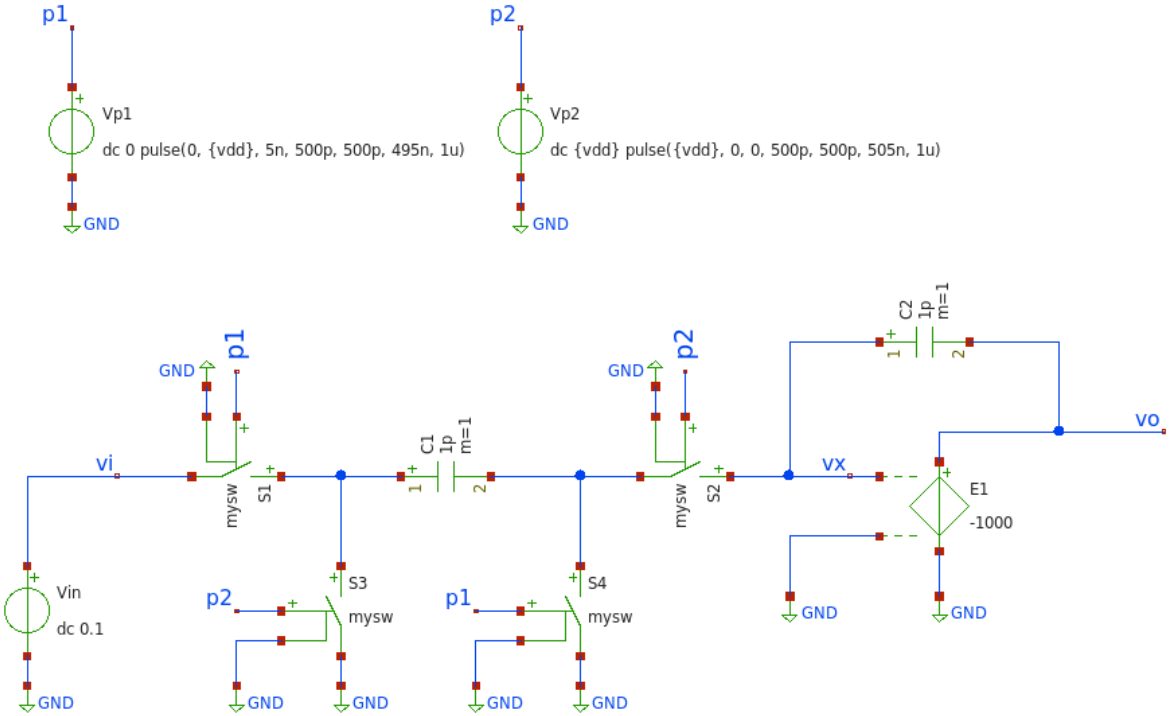
Amplifier

Boris Murmann

bmurmann@hawaii.edu

Switched-Capacitor Integrator



NGSPICE

```
.param temp=27 vdd=1.2
.model mysw SW vt={vdd/2} ron=10k roff=10gig
.control
save all
tran 1n 3u
plot vo
write tb_ideal_integ.raw
.endc
```

MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
.lib $::SG13G2_MODELS/cornerRES.lib res_typ
```

XSCHEM

Boris Murmann 2024-01-12 06:00:17

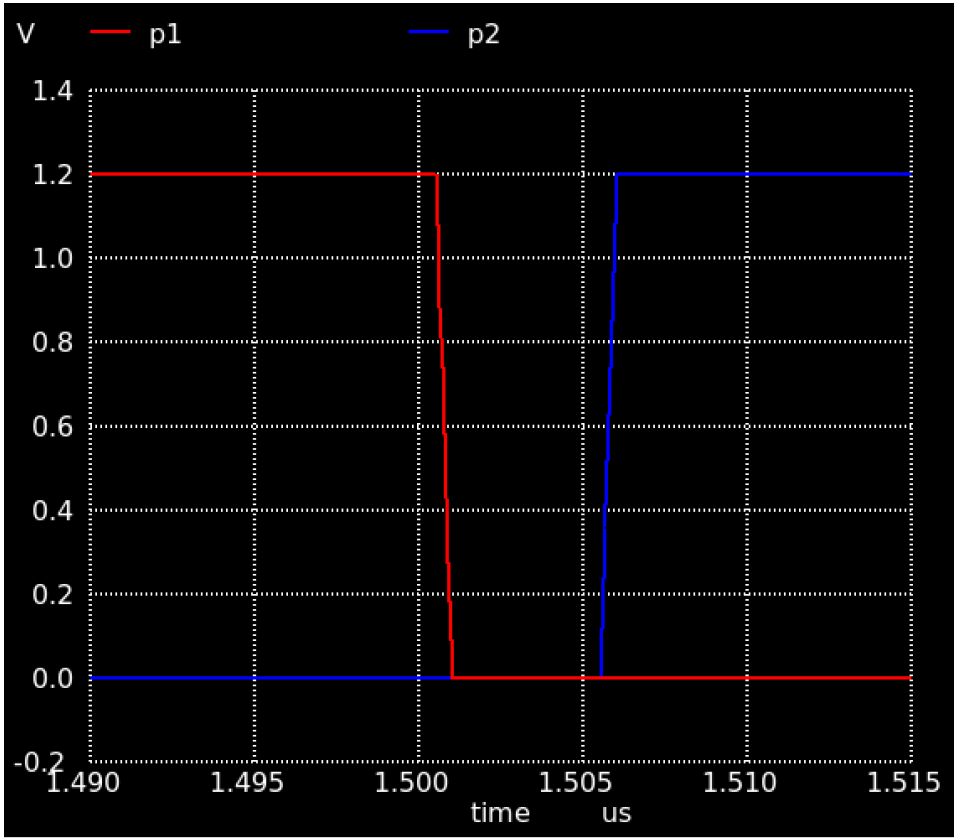
/foss/designs/tb_ideal_integ.sch

Nonidealities

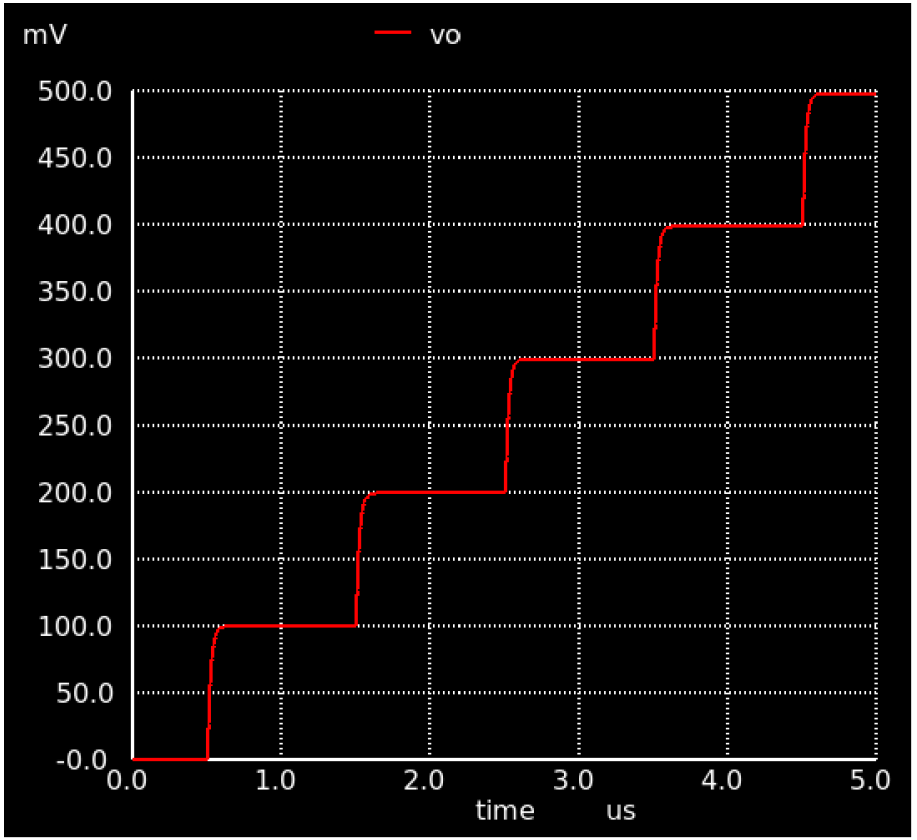
- Many nonidealities to worry about, especially for the amplifier

- Offset
- Finite gain
- Noise (more later)
- …

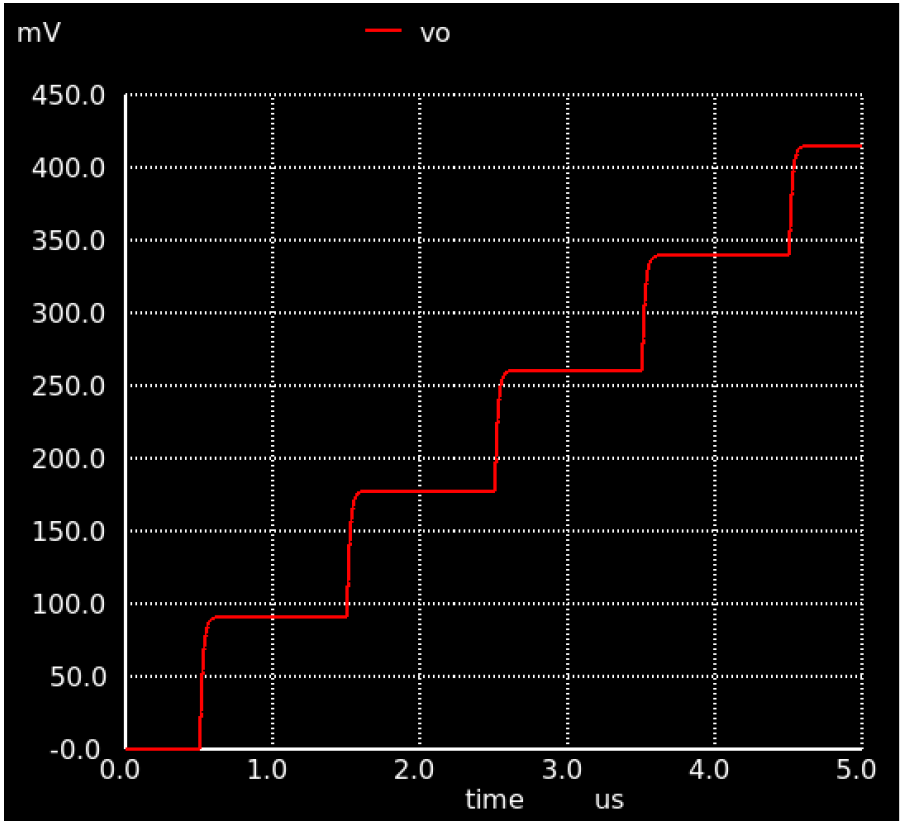
Non-overlapping two-phase clocks

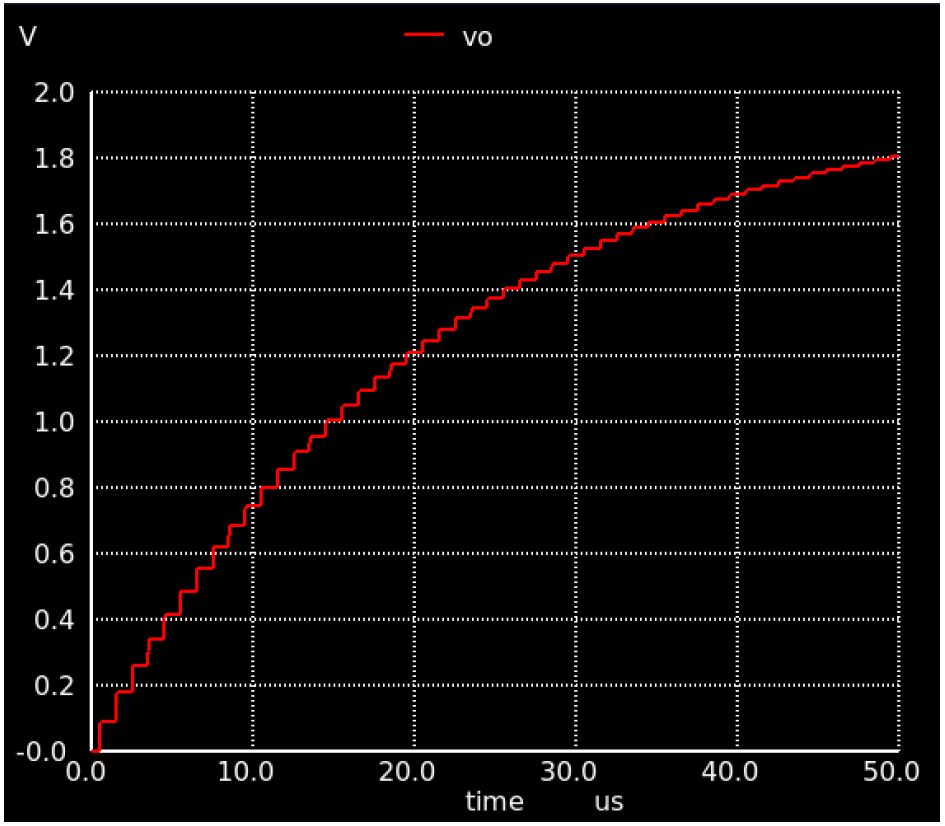


Integrator output
(Amplifier gain = 1000)

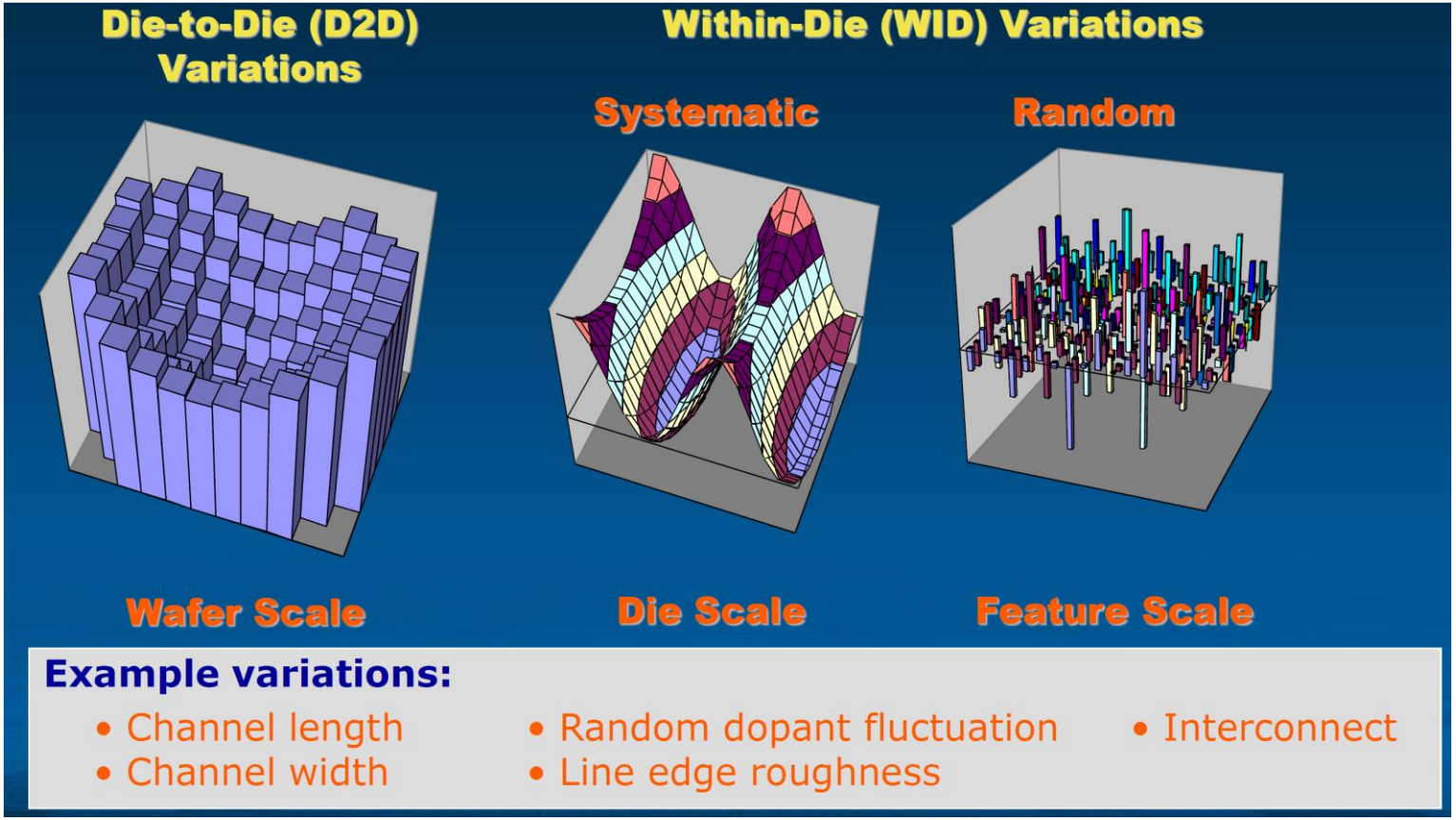


Integrator output
(Amplifier gain = 20)





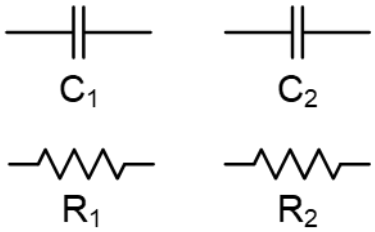
Parameter Variations in Integrated Circuits



[Jim Tschanz, Intel]

Device-to-Device Mismatch

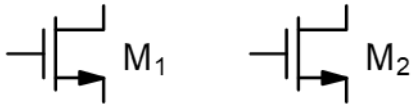
- Differences between nominally identical devices on the same chip



$$\Delta C = C_1 - C_2$$

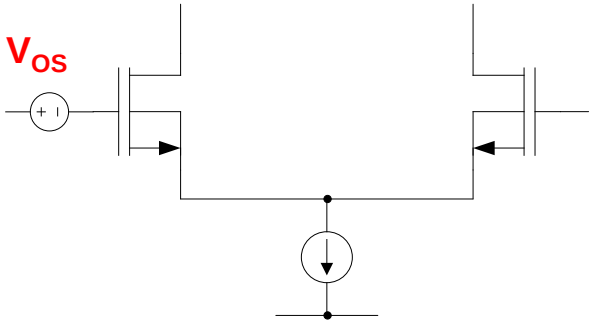
$$\Delta R = R_1 - R_2$$

$$\Delta V_t = V_{t1} - V_{t2}$$



$$\Delta\beta = \left(\mu C_{ox}\frac{W}{L}\right)_1 - \left(\mu C_{ox}\frac{W}{L}\right)_2$$

Equivalent input offset voltage



Statistical Model

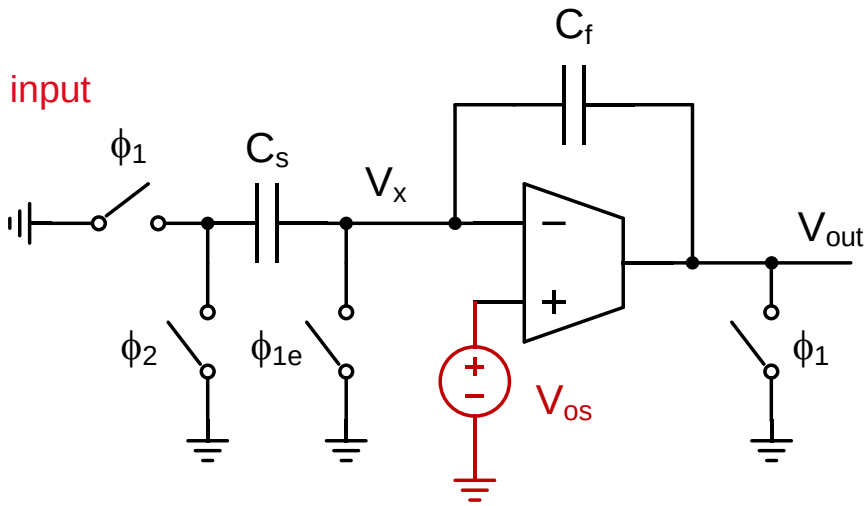
- Experiments have shown that mismatch for closely spaced, properly laid out devices (no systematic errors) is random and Gaussian
- The standard deviation of the parameter mismatch between two devices can be (approximately) modeled using Pelgrom's formula

$$\sigma_{\Delta P} = \frac{A_P}{\sqrt{WL}}$$

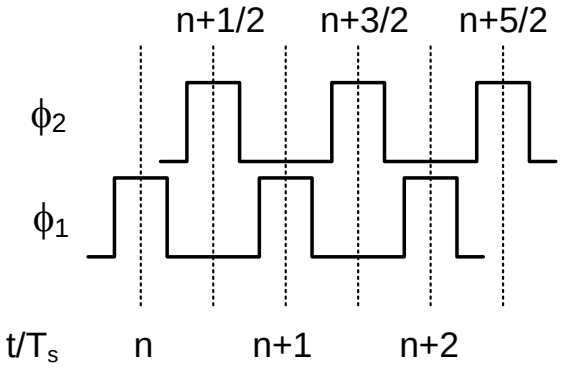
- A_P is the Pelgrom matching coefficient
- WL is the device area

Parameter	Value for 0.18 μm CMOS
A_{V_t} (MOSFET)	5 mV-μm
$A_{\Delta\beta/\beta}$(MOSFET)	1 %-μm
$A_{\Delta C/C}$ (MIM capacitor)	1 %-μm
$A_{\Delta R/R}$ (Poly resistor)	3 %-μm

Example: SC Gain Stage with Offset



Output sampled at the end of ϕ_2



n: $Q_x = 0$

n+1/2: $Q_x = -V_{os}C_s + [V_{out} - V_{os}]C_f$

$$V_{out} = V_{os}\left(1 + \frac{C_s}{C_f}\right)$$

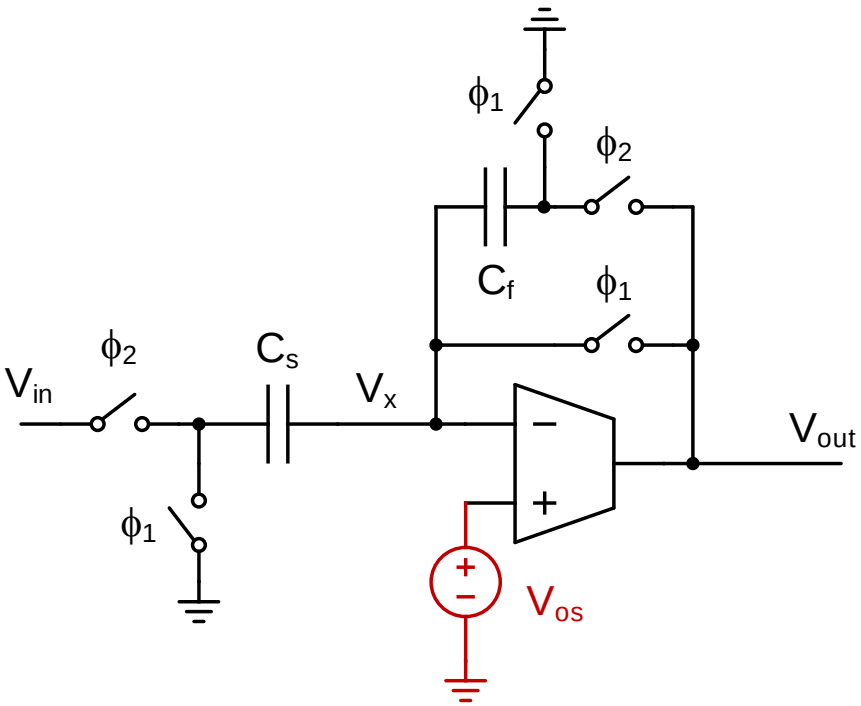
- Offset propagates to output

Correlated Double Sampling (CDS)

- Aims to suppress the offset error by separating it from the signal in the time domain
- There also exists a “chopping” technique that separates the two in the frequency domain

- Basic idea of CDS
  - Subtract two samples, one of which contains the error while the second sample contains the signal + error
  - If the error is strongly correlated between the two samples (error is DC or low frequency) it is cancelled or highly attenuated by the subtraction

SC Gain Stage with CDS

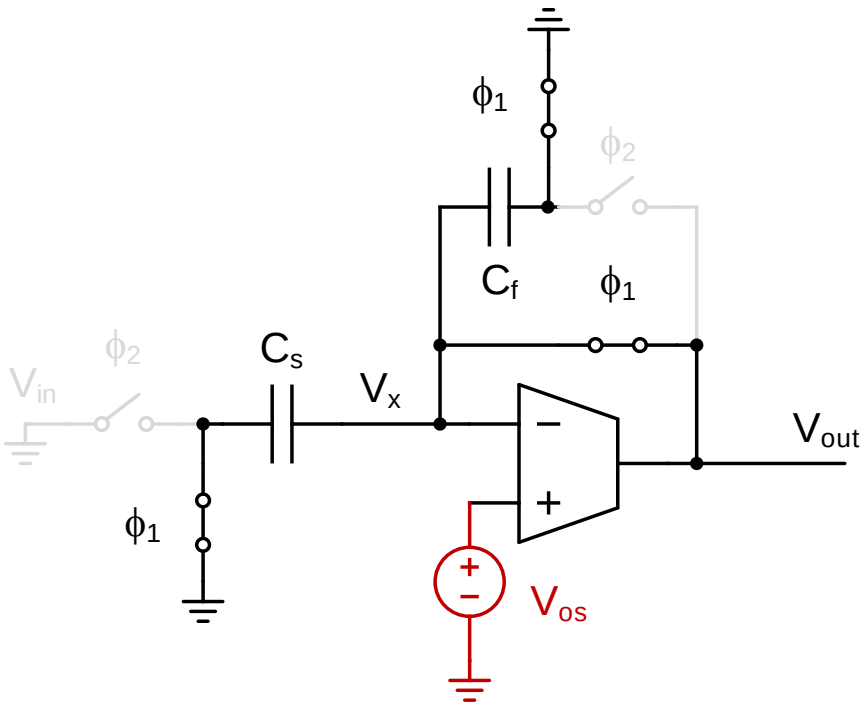


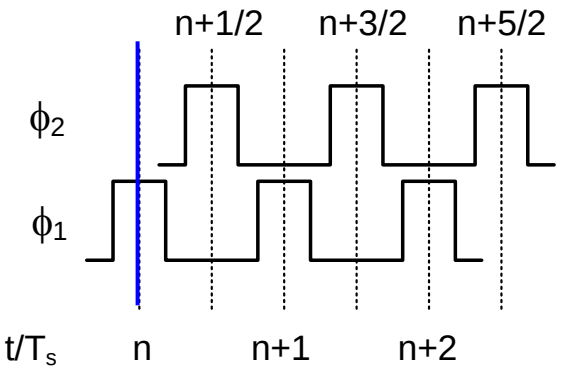
ϕ_1: Autozero phase

ϕ_2: Amplification phase

Output sampled at the end of ϕ_2

Autozero Phase

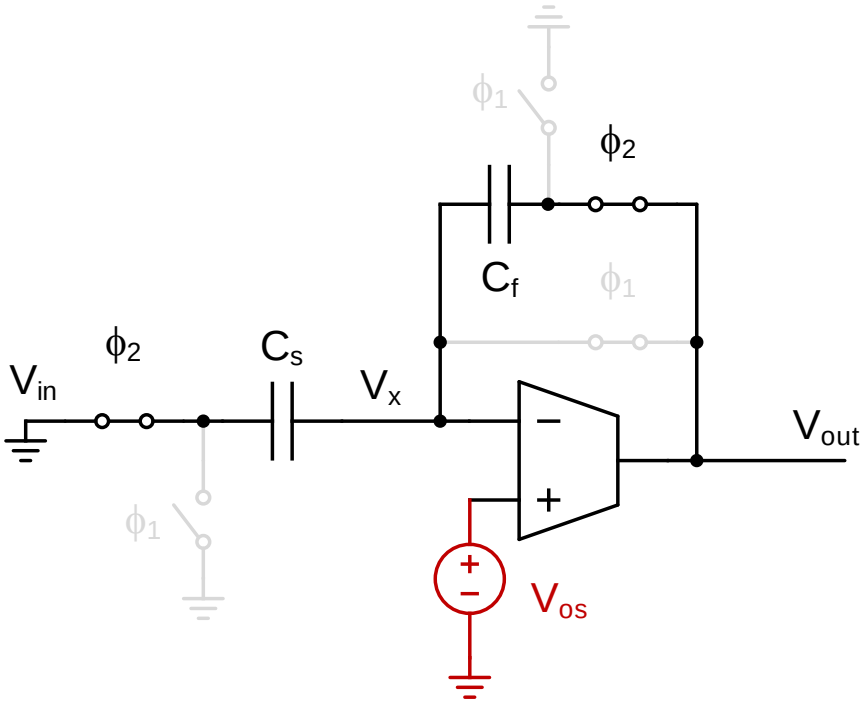


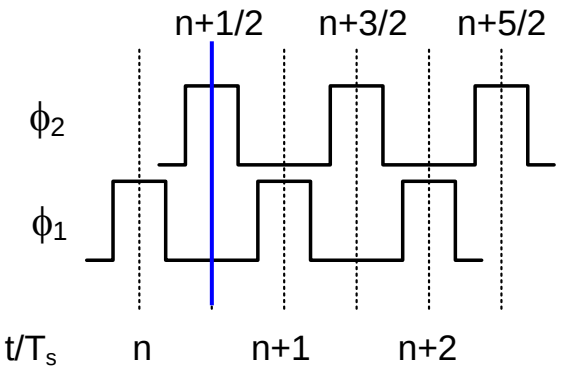


$$Q_x = -V_{os}C_s - V_{os}C_f$$

(assuming infinite amplifier gain)

Amplification Phase





$$Q_x = -V_{os}C_s + [V_{out} - V_{os}]C_f$$

$$-V_{os}C_s - V_{os}C_f = -V_{os}C_s + [V_{out} - V_{os}]C_f \qquad V_{out} = 0$$

Verdict on CDS

- CDS works well for suppressing the offset error and it is widely used

- Unfortunately, it does not help us with errors due to finite amplifier gain
  - The error due to finite gain is proportional to the signal, but CDS measures the error without the signal being present…
- There exists a variety of clever ideas to reduce the gain error
  - Sometimes leading to the effective “squaring” of the amplifier gain
  - K. Nagaraj, T. Viswanathan, K. Singhal and J. Vlach, "Switched-capacitor circuits with reduced sensitivity to amplifier gain," in IEEE Transactions on Circuits and Systems, vol. 34, no. 5, pp. 571-574, May 1987. https://ieeexplore.ieee.org/document/1086170

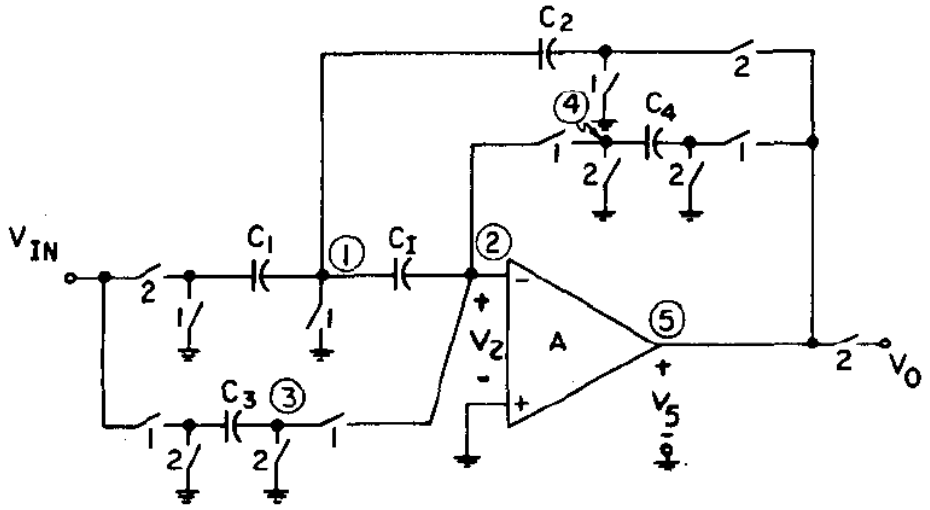


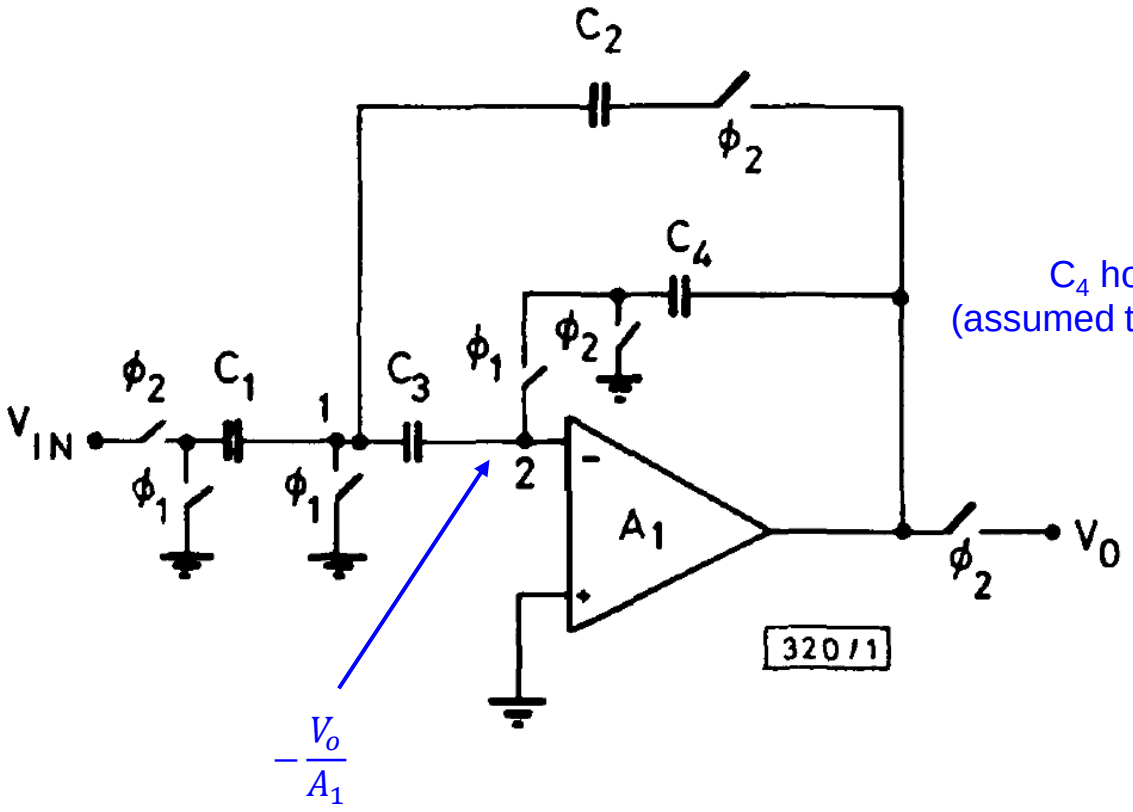
Fig. 1. Circuit schematic of the amplifier/attenuator incorporating the proposed technique.

$$V_0(n) = -\frac{C_1}{C_2} V_{\mathrm{IN}}(n) - \epsilon \qquad \epsilon = \frac{1}{A^2}\left[1+\frac{C_1}{C_2}\right]\left[\left(1+\frac{C_1}{C_2}+\frac{C_I}{C_2}\right)V_0(n) - \frac{C_I}{C_2}V_0(n-1)\right]$$

- Great improvement, but need to process input sample in both half cycles
- Often not practical. Can we do something simpler?

Nagaraj, K., Singhal, K., Viswanathan, T.R., & Vlach, J., “Reduction of finite-gain effect in switched-capacitor filters,” Electronics Letters, 21, 644-645, 1985.
https://designers-guide.org/forum/Attachments/04250650.pdf

Introduction: One of the important factors limiting the performance of MOS switched-capacitor (SC) filters is the finite gain of amplifiers. It has been shown that in SC filters the effect of finite gain is more serious than that of finite bandwidth.[1] In this letter we propose a simple technique to significantly reduce the finite-gain effect. It is based on the fact that in a vast majority of practical SC filters the sampling frequency is made much higher than the signal frequencies of interest in order to make the required continuous-time anti-aliasing and reconstruction filters easily realisable on silicon (an extensive survey of the literature has revealed that a ratio of at least 20:1 is maintained in most cases). Thus there would be considerable correlation between successive signal samples. This is exploited here to reduce the finite-gain effect.



C_4 holds previous output
(assumed to be close to next output)

Stored on C3 during $\phi 1$