Schematic & Layout Deliberations

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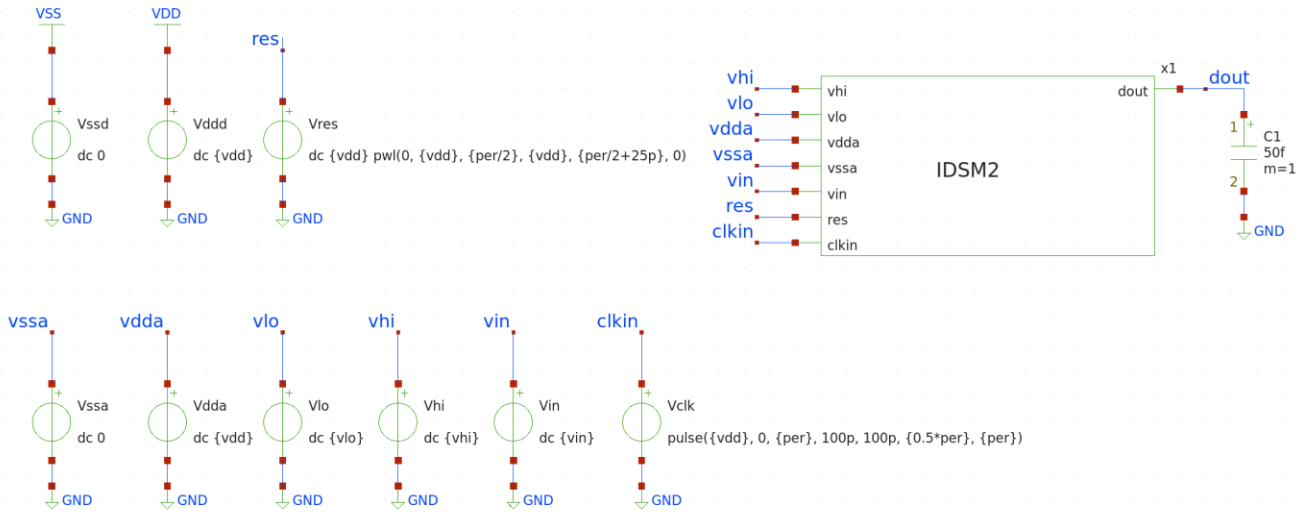
Top-Level Testbench

Simulating 5 input voltages:



MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
.lib $::SG13G2_MODELS/cornerCAP.lib cap_typ
.inc $::PDK_ROOT/sg13g2/libs.ref/sg13g2_stdcell/spice/sg13g2_stdcell.spice
```

NGSPICE

```
.param temp=27 per=20n N=110
.param vlo=0.3 vhi=0.9 vdd=1.2 vin=0.6
.option method=gear reltol=1e-5
.ic v(x1.x3.out1p)=0
.tran 100p {per*N} uic
.meas tran iavg_ana AVG i(Vdda)
.meas tran iavg_dig AVG i(Vddd)

.control
set wr_singlescale
set wr_vecnames
option numdgt = 3
let index = 1
foreach vin_val 0.5 0.55 0.6 0.65 0.7
  alterparam vin = $vin_val
  reset
  run
  set file = {tb_idsm2_}{$&index}{.txt}
  wrdata $file x1.vout1 x1.vout2 dout x1.p1 x1.p2
  destroy $curplot
  let index = index + 1
end
.endc
```

XSCHEM

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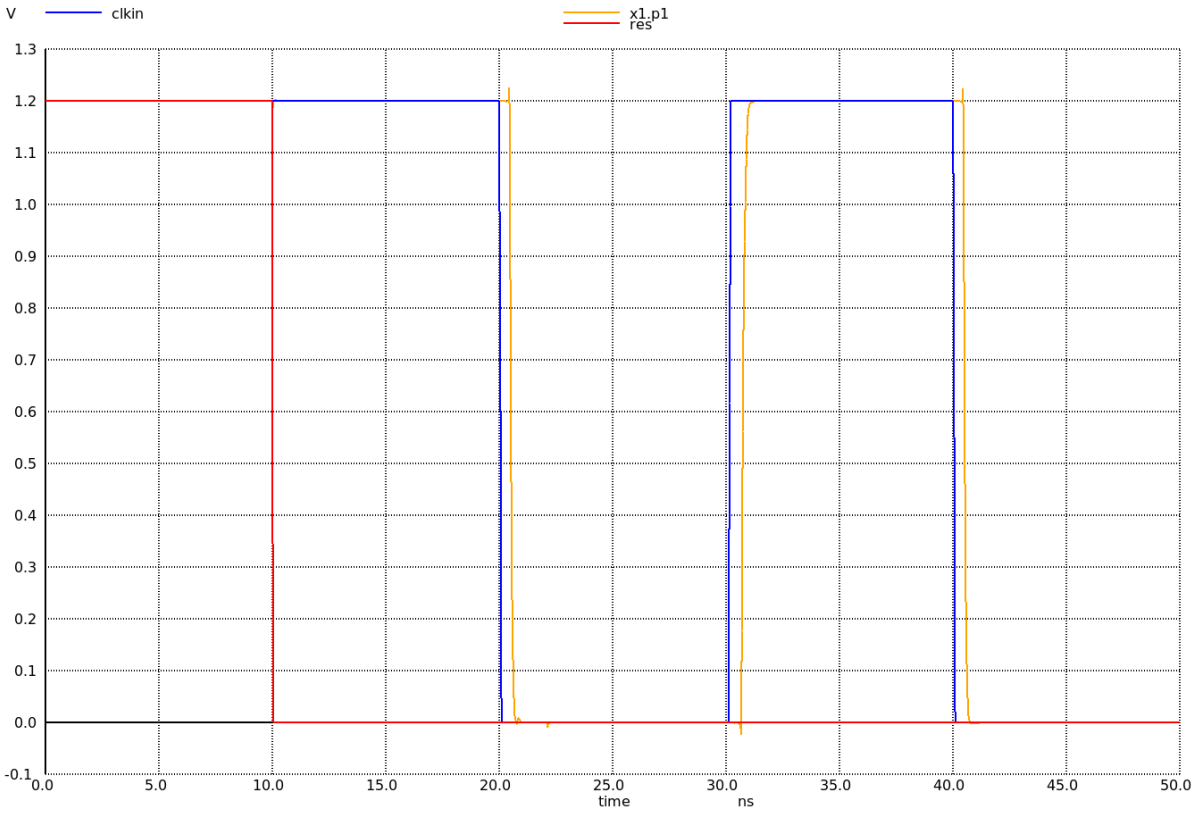
/foss/designs/tb_IDSM2.sch

2024-03-27 04:26:06

Reset Timing

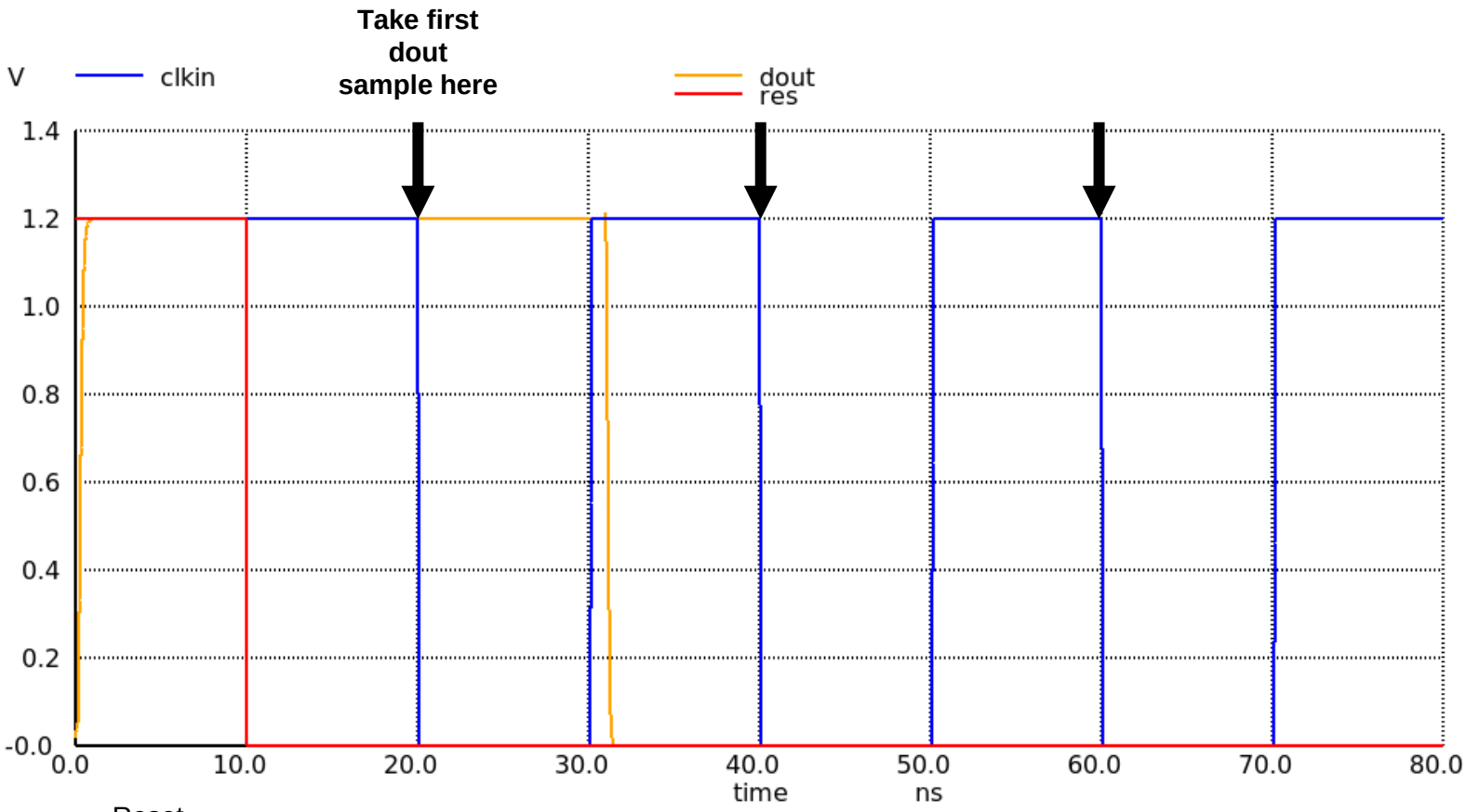


Reset
Stage 1: Sample
Stage 2: Redistr.

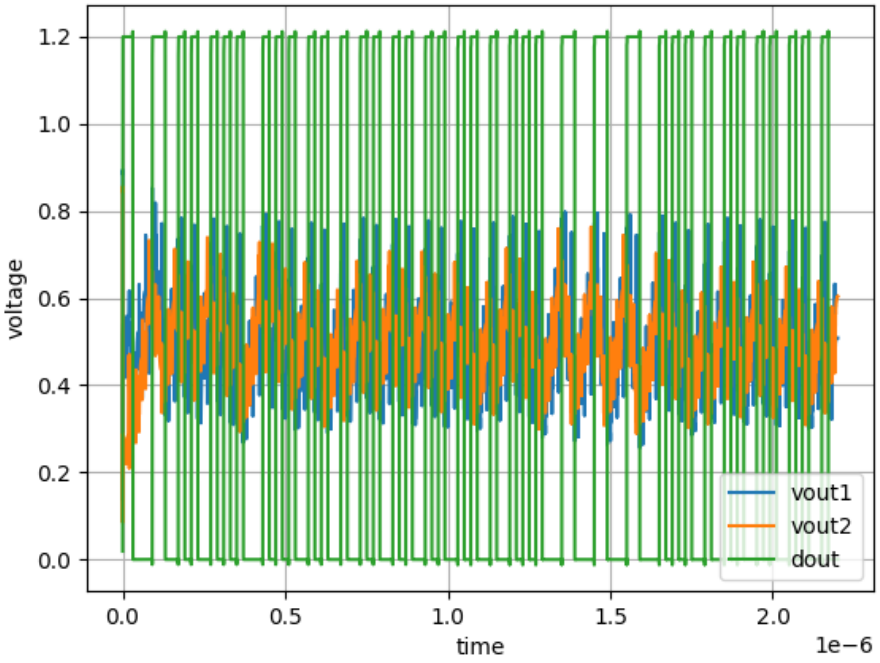
Stage 1: Sample
Stage 2: Redistr.

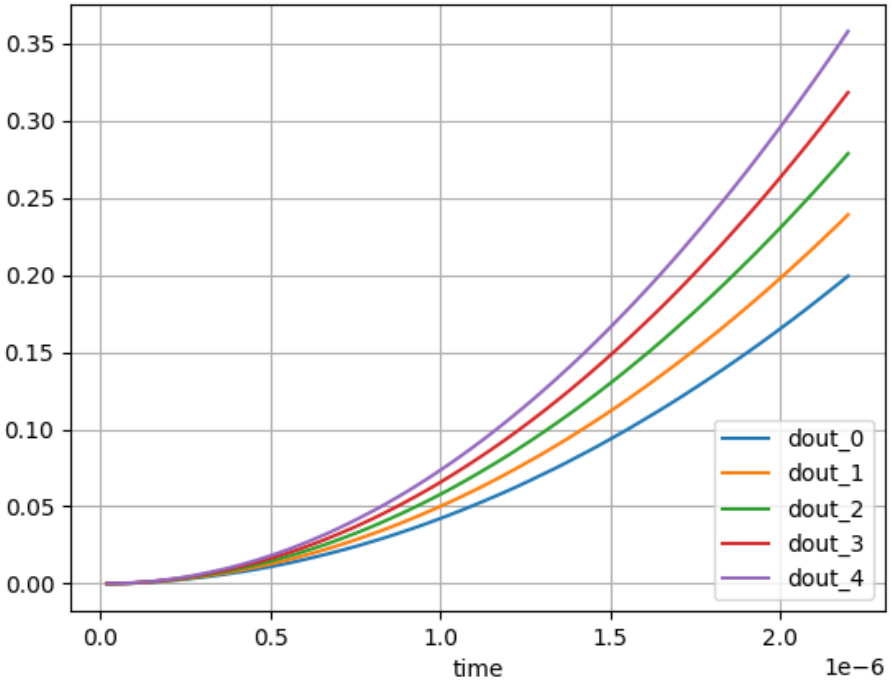
Stage 1: Redistr.
Stage 2: Sample

Output Timing



Output and Decimated Output for 5 Input Voltages





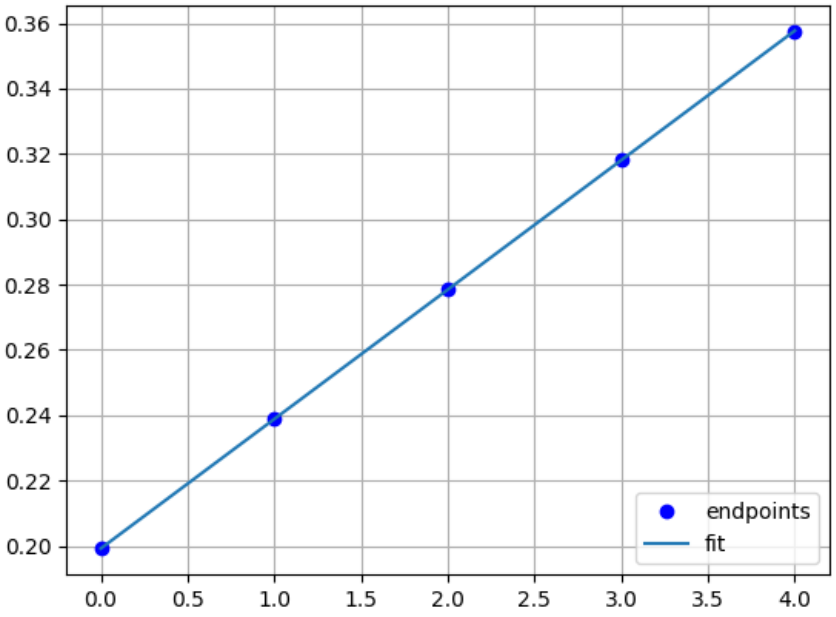
https://github.com/bmurmann/EE628/blob/main/5_Design/3_Real_circuits/tb_IDSM2.ipynb

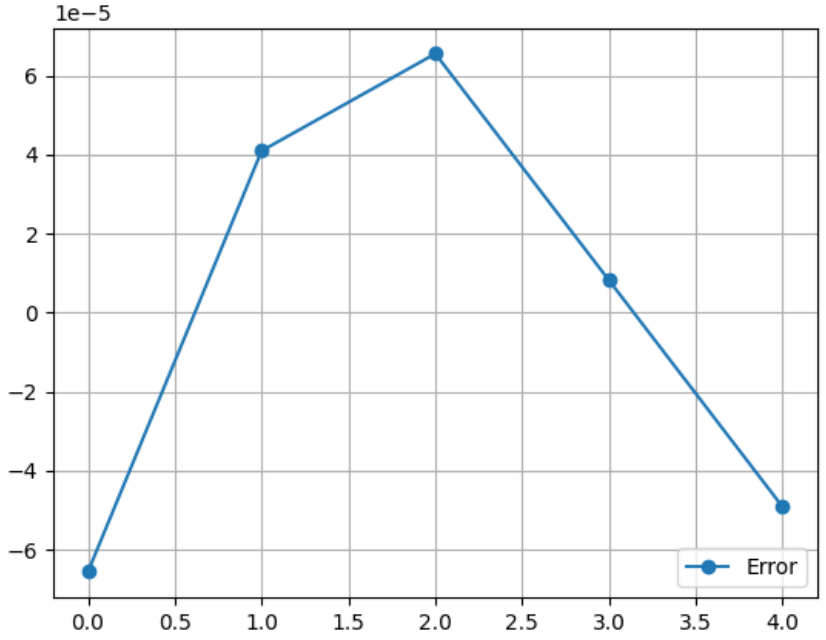
Code

```
nfiles = 5
per = 20e-9
tstart = 20e-9
N = 110
out = np.zeros([5, N])
for i in range(nfiles):
  file = "./simulations/tb_idsm2_" + str(i+1) + ".txt"
  df = pd.read_csv(file, sep='\s+')
  dout = df['dout']
  t = df['time']
  ts = np.arange(tstart, tstart+N*per, per)
  interp_func = interp1d(t, dout)
  dsamp = interp_func(ts)
  dsamp[dsamp > 0.6] = 1
  dsamp[dsamp < 0.6] = 0
  csum = np.cumsum(dsamp)
  out[i,:] = np.cumsum(csum)/N/(N+1)
```

https://github.com/bmurmann/EE628/blob/main/5_Design/3_Real_circuits/tb_IDSM2.ipynb

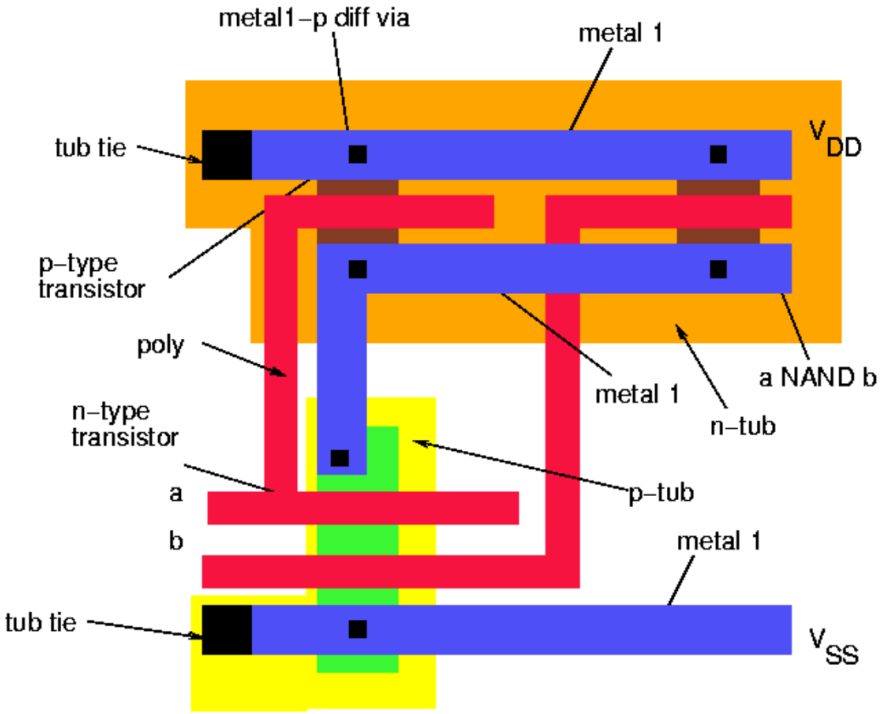
Linear Fit

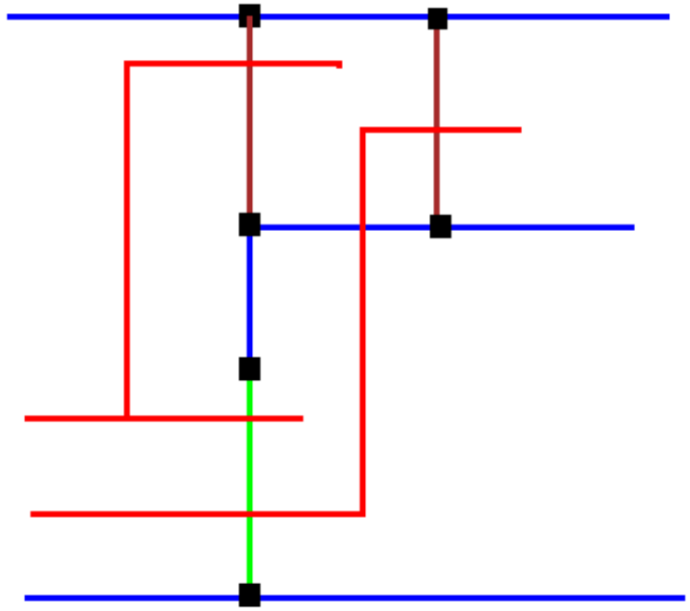




https://github.com/bmurmann/EE628/blob/main/5_Design/3_Real_circuits/tb_IDSM2.ipynb

Stick Diagrams for Cell Layout Floorplanning

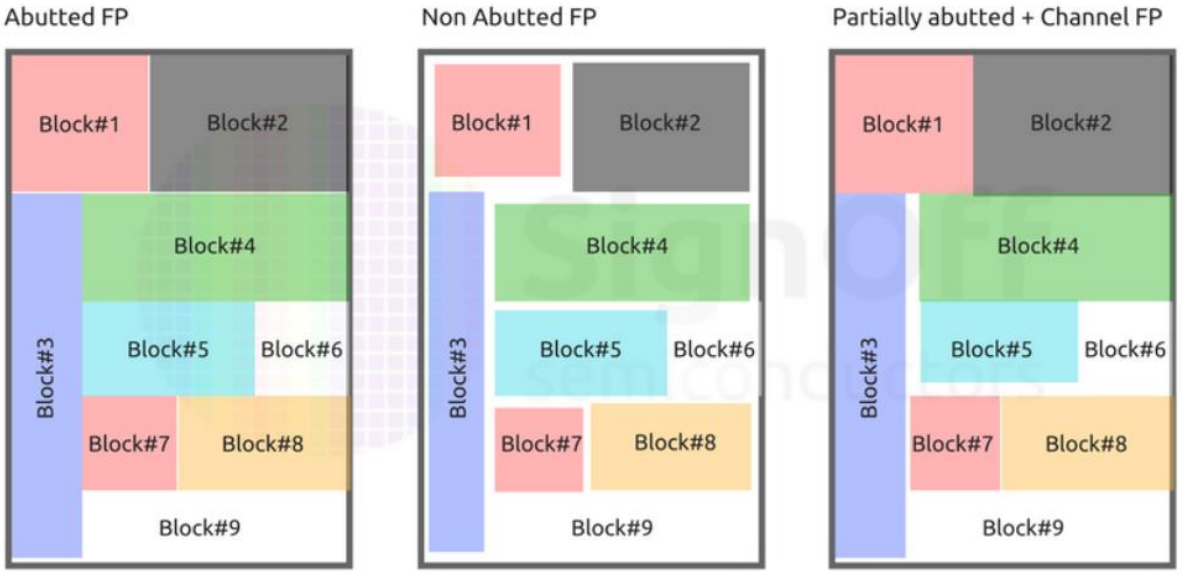




https://users.ece.utexas.edu/~mcdermot/vlsi1/main/lectures/lecture_3.pdf

Types of floorplan techniques used in Full Chip plan

1. Abutted (All inter block pin connections are done through FTs)
2. Non abutted (Channel based. All inter block pin connections are routed in channels)
3. Mix of both – partially abutted with some channels



https://signoffsemiconductors.com/floorplan/