Comparator

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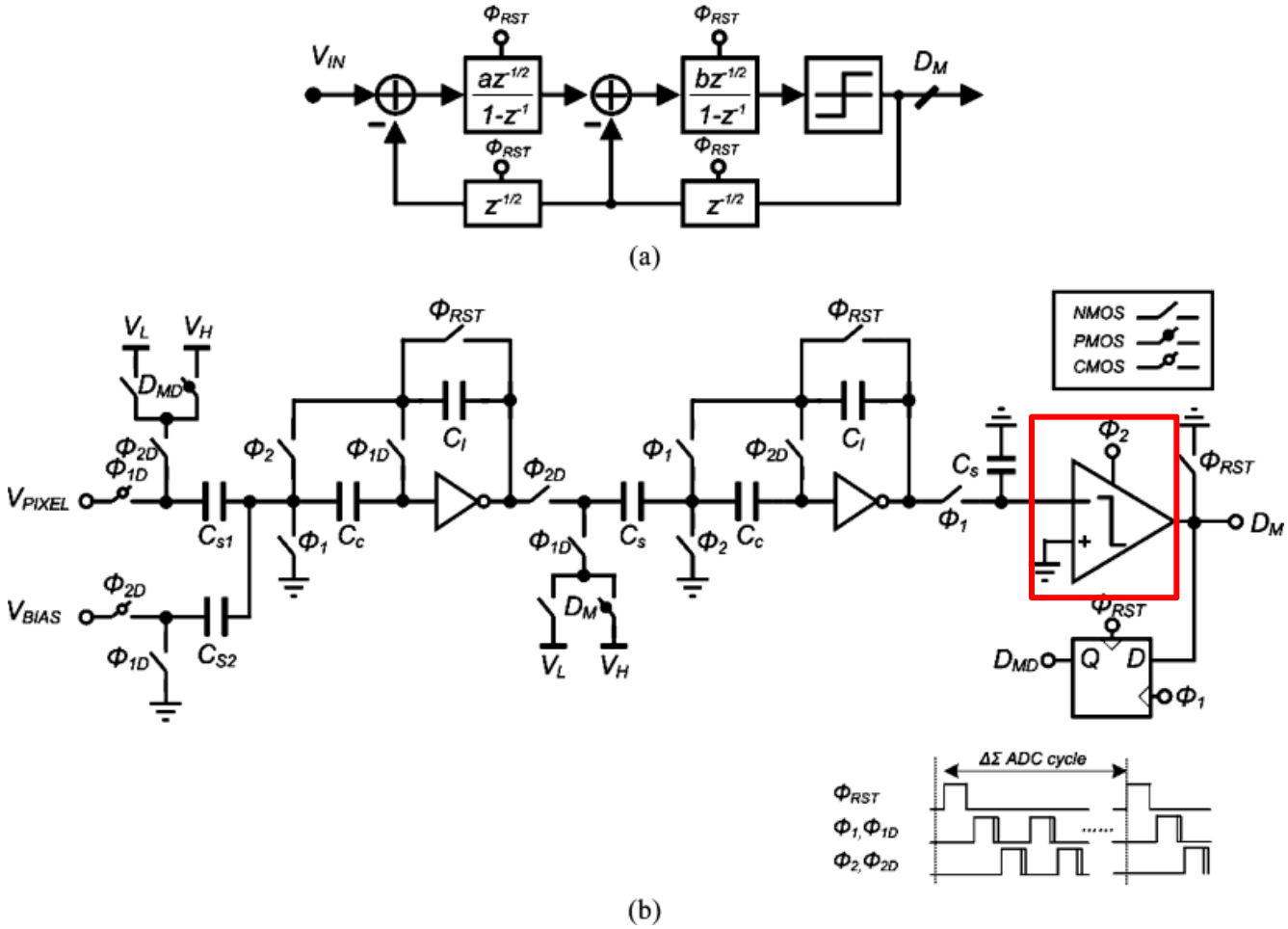
Next Steps

- Add second integrator (second-order modulator)
- Write some post-processing scripts
  - Detailed measurements
  - Emulate counters to create final digital output

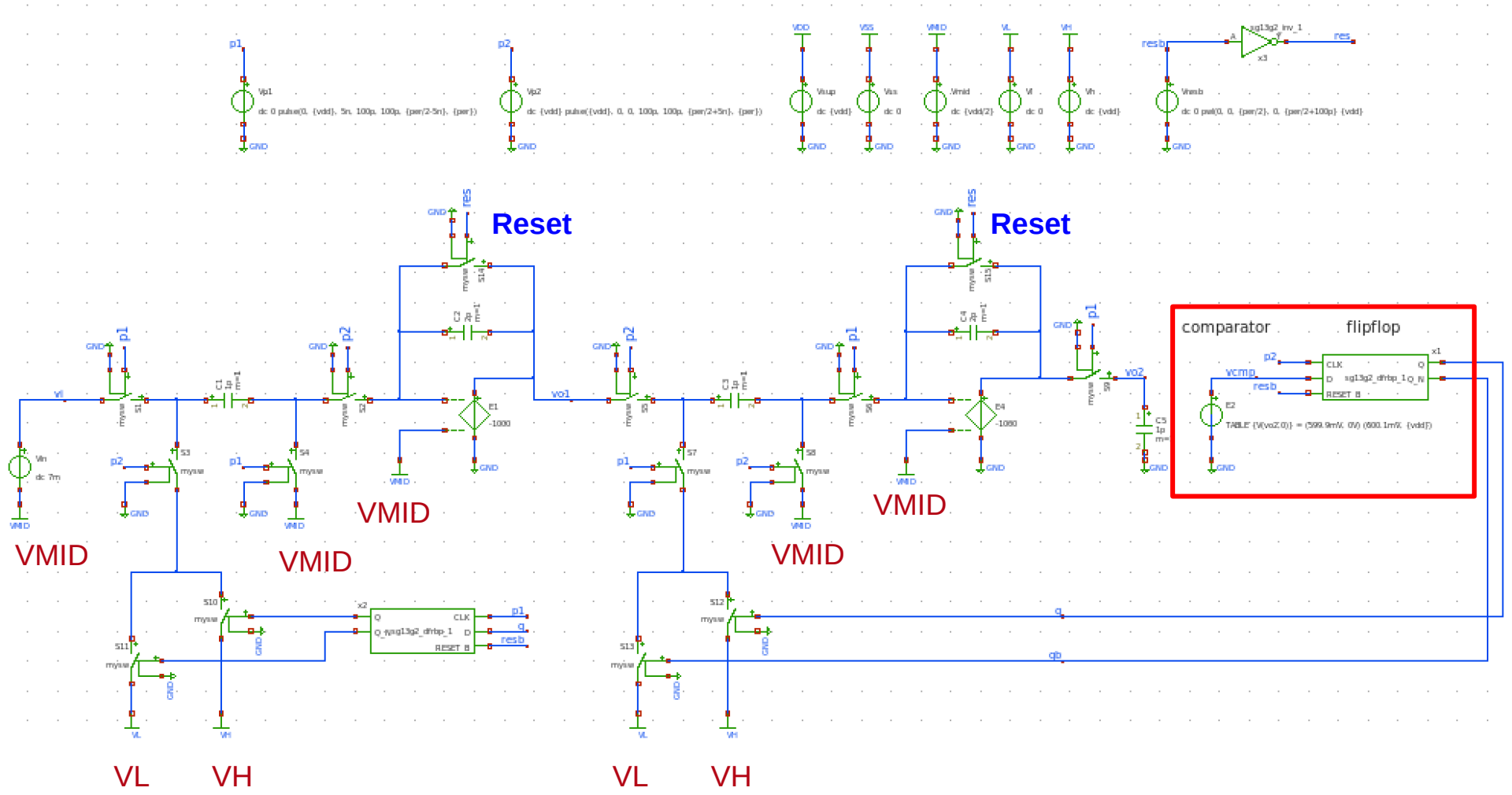
- Increasingly “transistorize” the implementation
  - Shift voltages to practical levels (can’t have negative voltages)
  - Comparator
  - Inverter-based amplifier with CDS
  - MOSFET switches & clock generator

Template Circuit

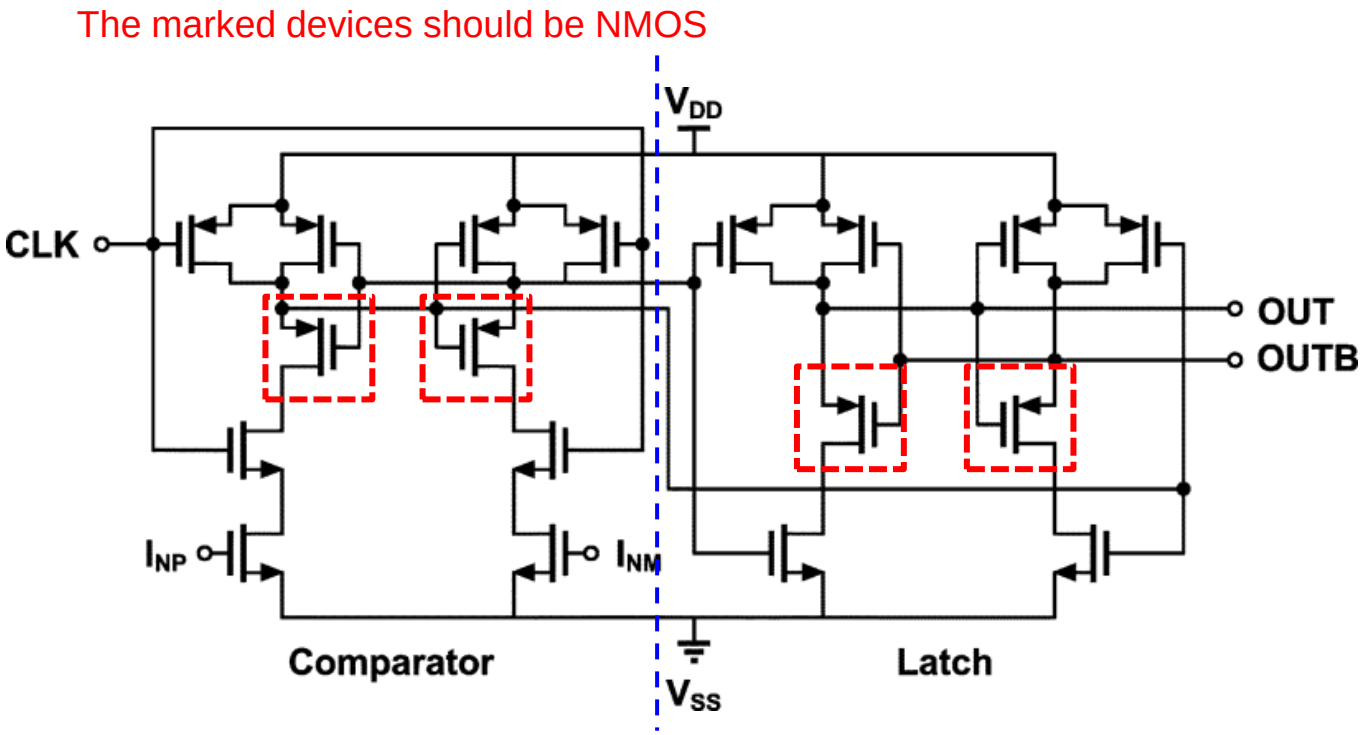


Y. Chae et al., "A 2.1 M Pixels, 120 Frame/s CMOS Image Sensor With Column-Parallel ADC Architecture," in IEEE Journal of Solid-State Circuits, Jan. 2011. https://ieeexplore.ieee.org/document/5641589

Current Model Schematic (IDSM2)

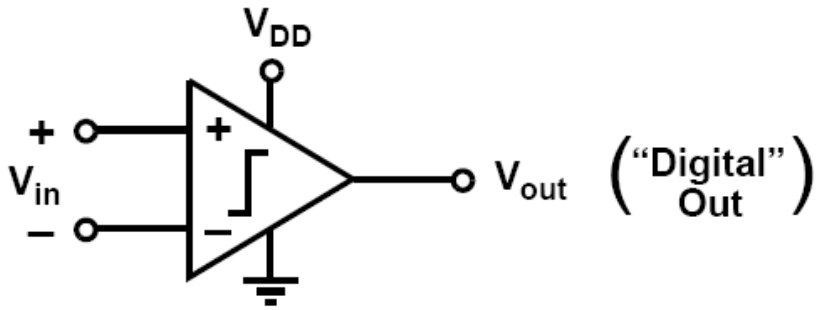


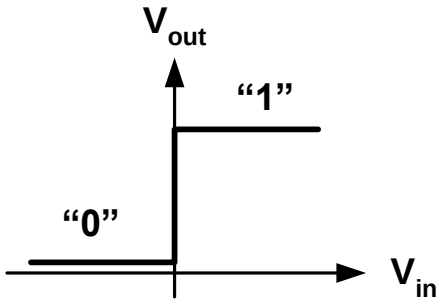
Circuit Used in The Original Template Design



Y. Chae and G. Han, "Low Voltage, Low Power, Inverter-Based Switched-Capacitor Delta-Sigma Modulator," in IEEE Journal of Solid-State Circuits, Feb. 2009.
https://ieeexplore.ieee.org/abstract/document/4768910

Ideal Voltage Comparator



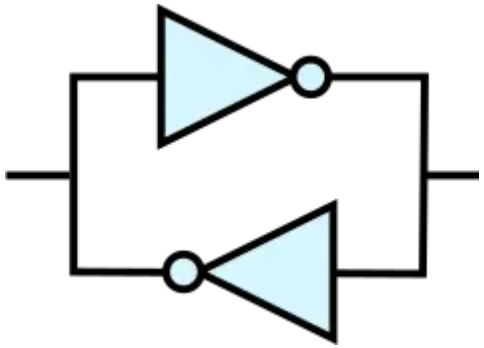


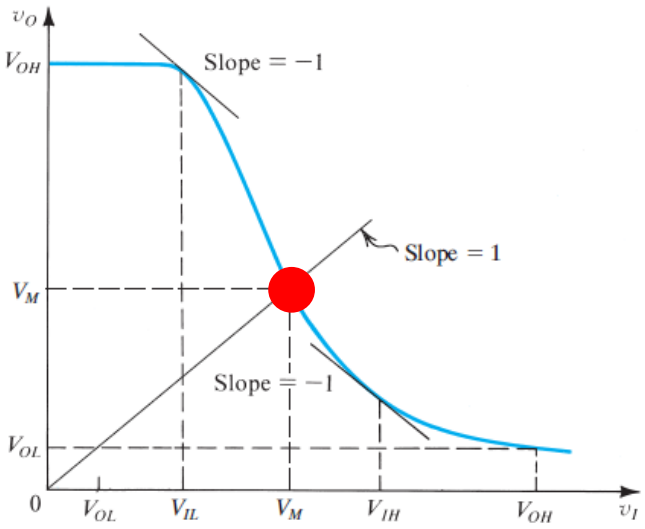
- Function
  - Compare the values of two analog voltages (e.g., an input signal and a reference voltage) and generate a digital 1 or 0 indicating the polarity of the difference

The Fasted Way to Find the Polarity Comparison: Latch Circuit

Stable states: 0 1 1 0

Metastable state 0.5 0.5

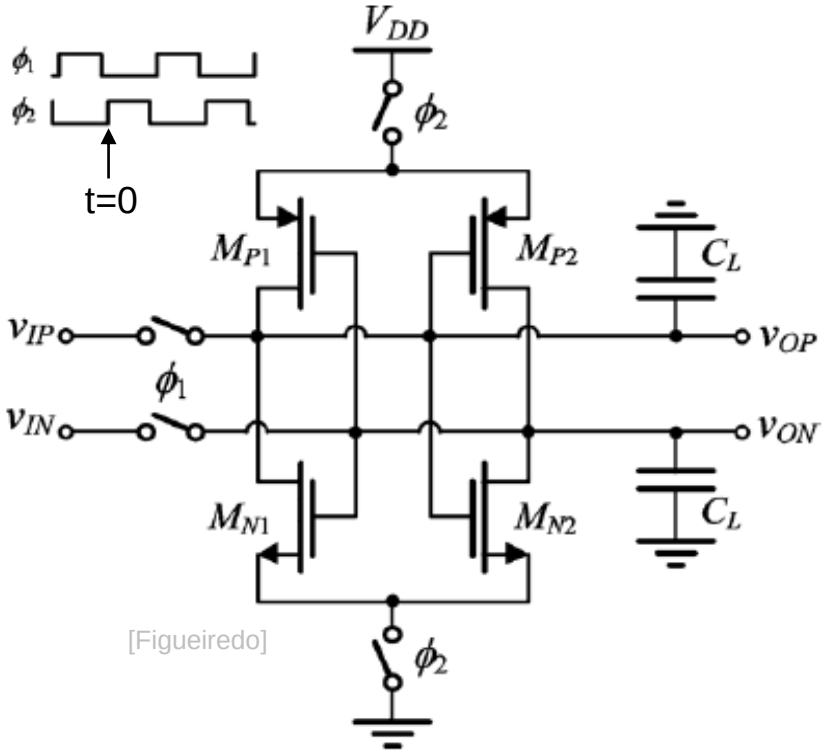




The slightest imbalance will push the circuit out of the metastable state and latch to one of the stable states

Detailed Analysis

Conceptual Circuit



[Figueiredo]

ϕ1: Set up initial condition (v_{OD0})
ϕ2: Enable positive feedback

Inverter Transconductance

$$G_m = g_{mN} + g_{mP}$$

$$\frac{dv_{OP}}{dt} = \frac{i_1(t)}{C_L} = -\frac{G_m v_{ON}(t)}{C_L}$$

$$\frac{dv_{ON}}{dt} = \frac{i_2(t)}{C_L} = -\frac{G_m v_{OP}(t)}{C_L}$$

$$\tau = \frac{C_L}{G_m}$$

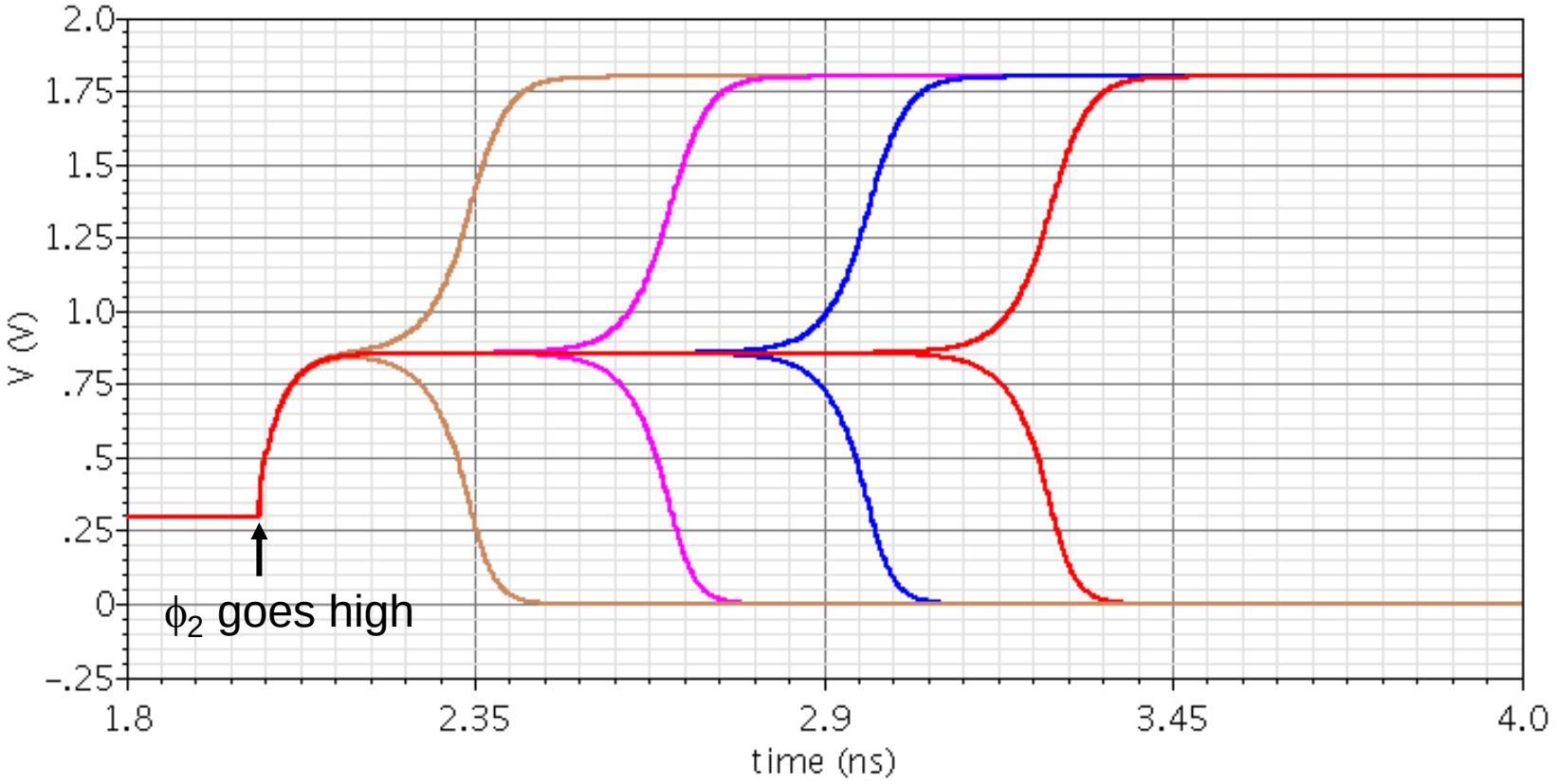
$$v_{OD}(t) = v_{OP}(t) - v_{ON}(t)$$

$$v_{OD}(t) = v_{OD0} \cdot e^{t/\tau}$$

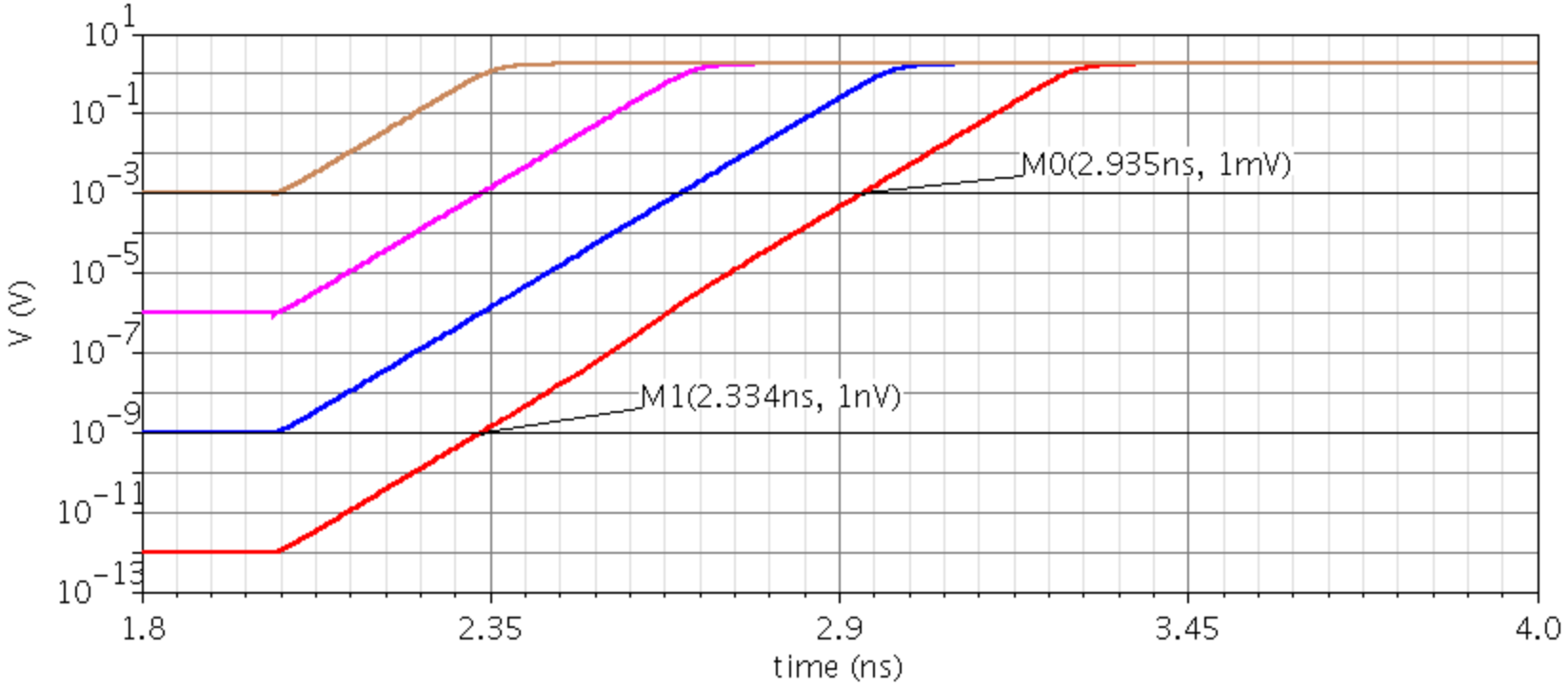
$$A(t) = \frac{v_{OD}(t)}{v_{OD0}} = e^{t/\tau}$$

Transient Response

Nodes v_{OP} and v_{ON} for differential inputs of 1mV, 1μV, 1nV and 1pV



Transient Response of Voltage Difference (Log Scale)

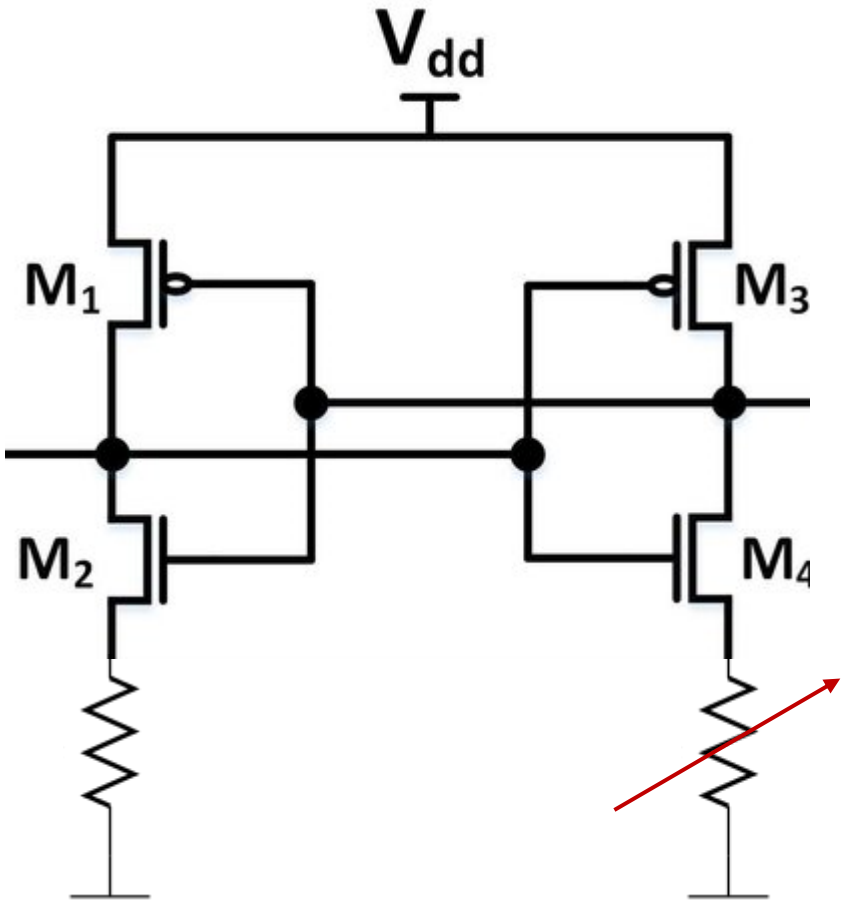


$$v_{OD1} = v_{OD0} \cdot e^{t_1/\tau}$$

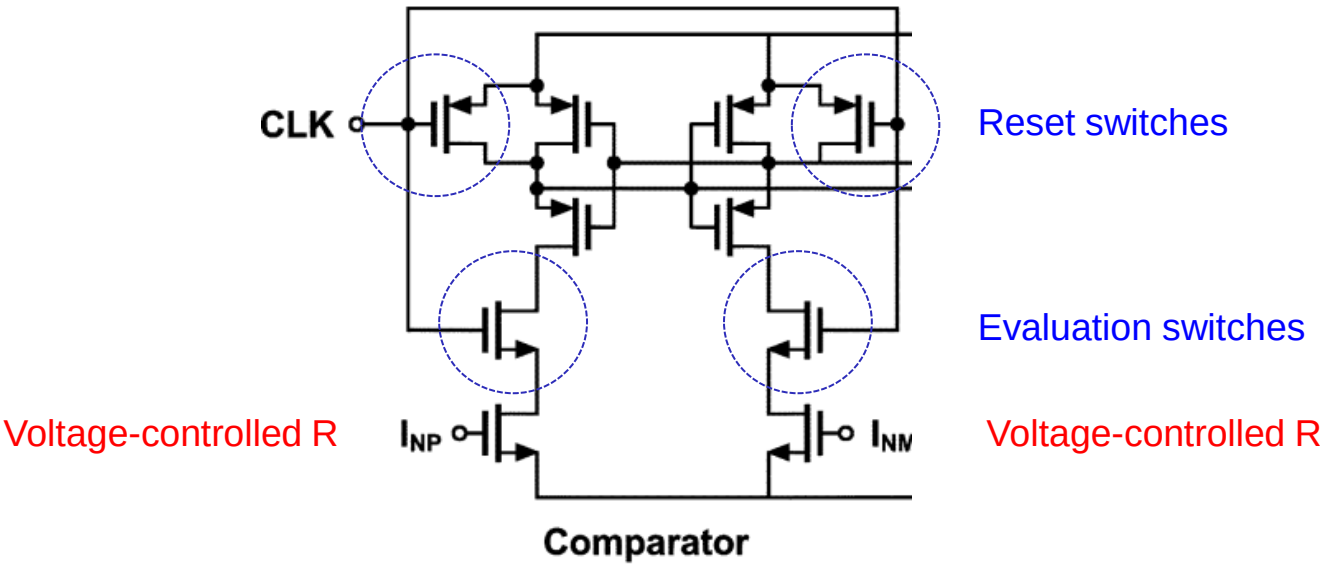
$$v_{OD2} = v_{OD0} \cdot e^{t_2/\tau}$$

$$\tau = \frac{t_2 - t_1}{\ln\left(\frac{v_{OD2}}{v_{OD1}}\right)} = \frac{600\text{ps}}{\ln(10^6)} = \frac{600\text{ps}}{6 \cdot 2.3} = 43ps$$

Another Way to Dial in Imbalance



Circuit Used in The Original Template Design



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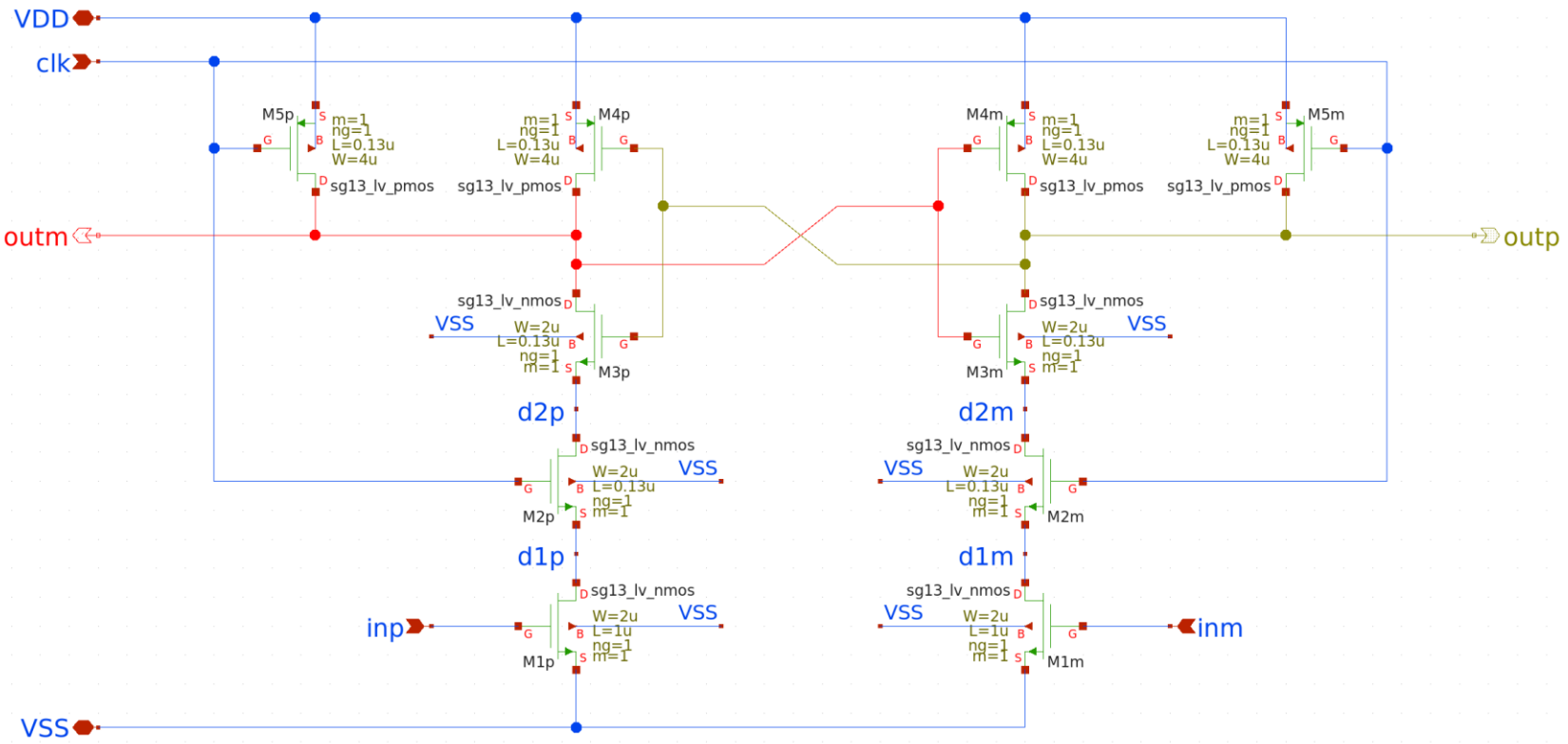
Prototype Circuit



XSCHEM

Boris Murmann 2024-01-26 23:04:10

x1. /foss/designs/comp.sch

Testbench

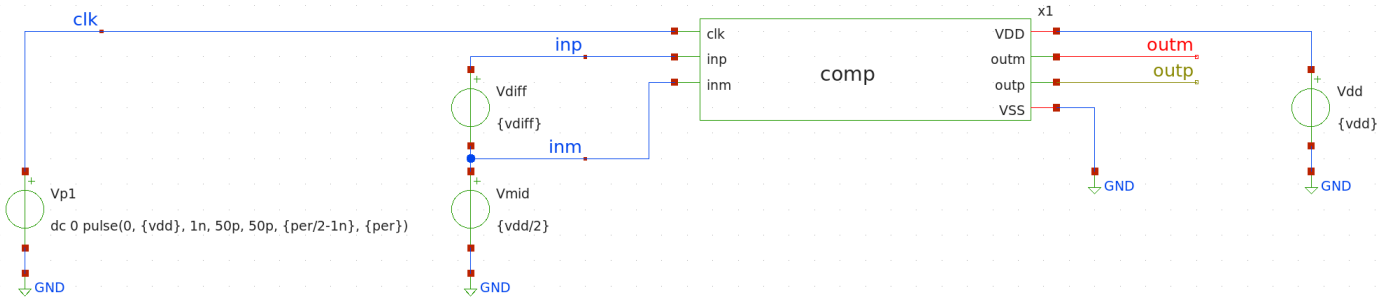
NGSPICE

```
.param temp=27 vdd=1.2 per=1u vdiff=1m
.option method=gear reltol=1e-5

.control
save all
tran 10p 4n
alterparam vdiff=1u
reset
tran 10p 4n
plot clk tran1.outm tran1.outp tran2.outm tran2.outp
.endc
```

MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
```

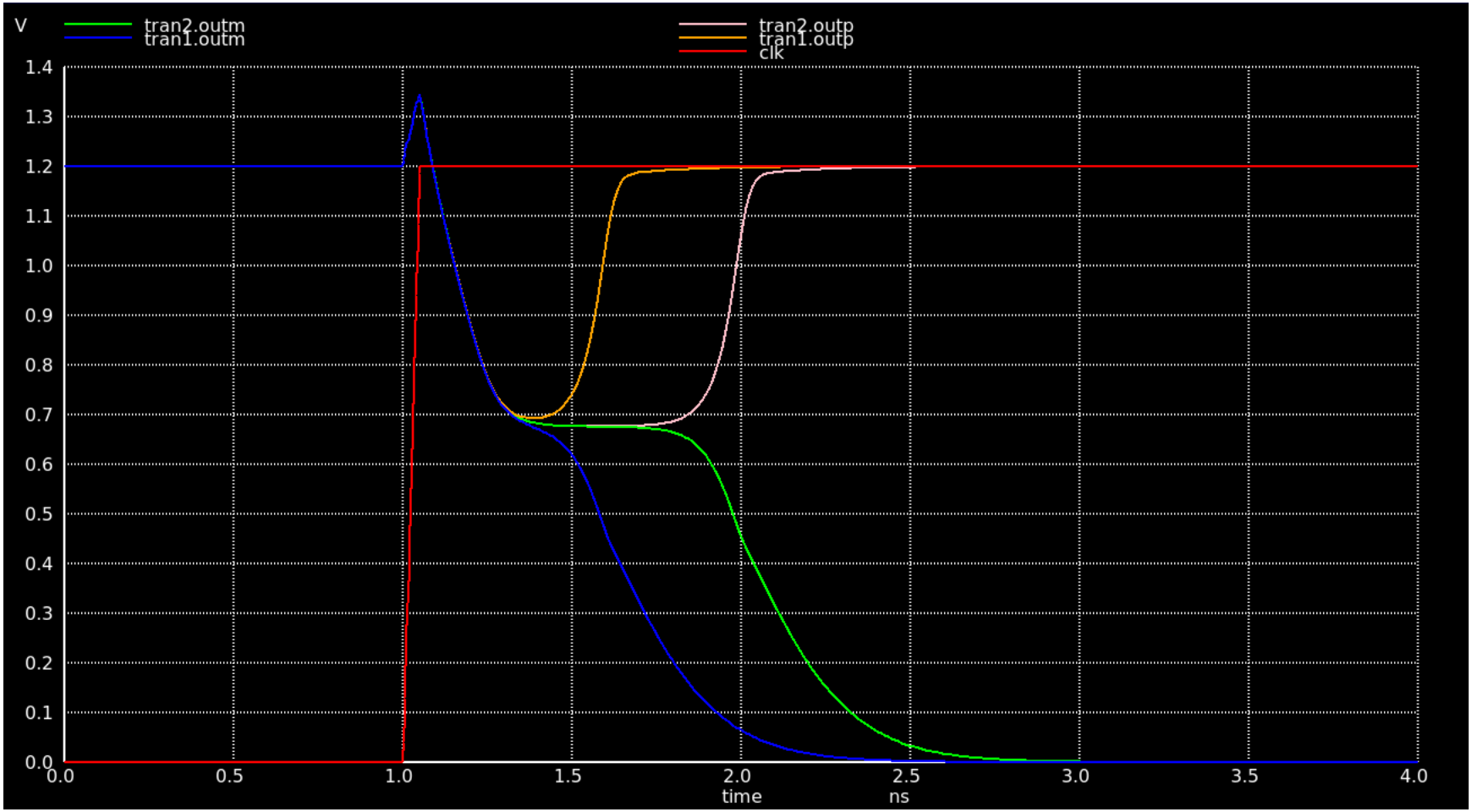


XSCHEM

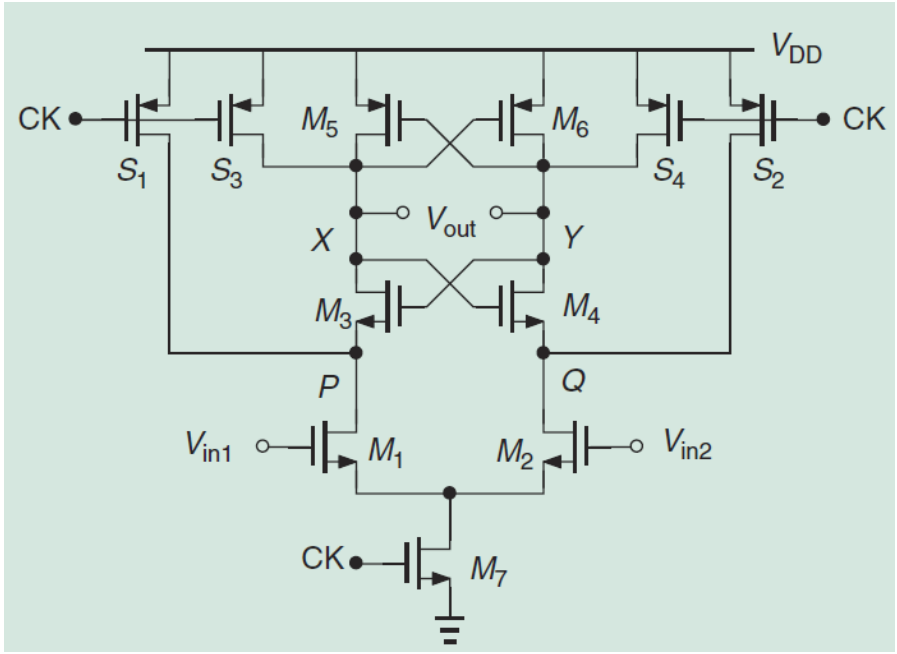
Boris Murmann 2024-01-27 00:04:56

/foss/designs/tb_comp

Simulation Result



Alternative (Classical) Implementation



"Strong ARM Latch"

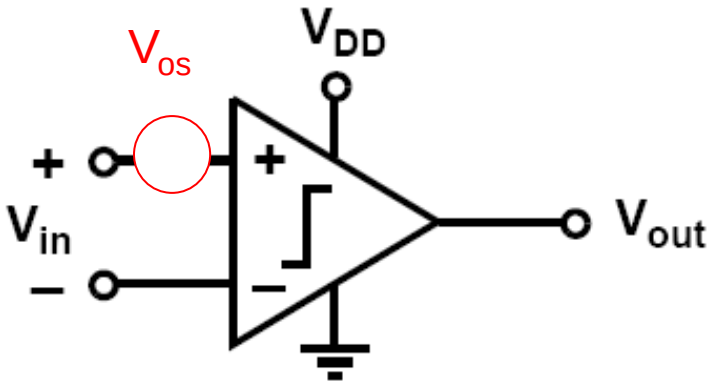
Madden & Bowhill, US Patent 4910713, Mar. 20, 1990

First journal paper:
[Kobayashi et al., JSSC, Apr. 1993]

"Strong ARM" paper:
[Montanaro, Madden et al., JSSC, Nov. 1996]

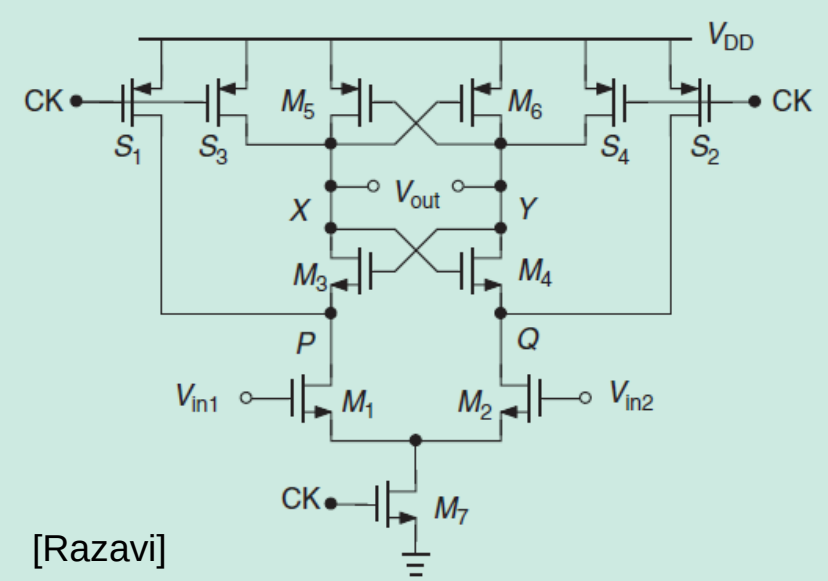
B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," in IEEE Solid-State Circuits Magazine, Spring 2015. https://ieeexplore.ieee.org/abstract/document/7130773

General Issue for all Implementations: Offset Voltage



- Biases the decision in one direction

Offset in a StrongARM Latch

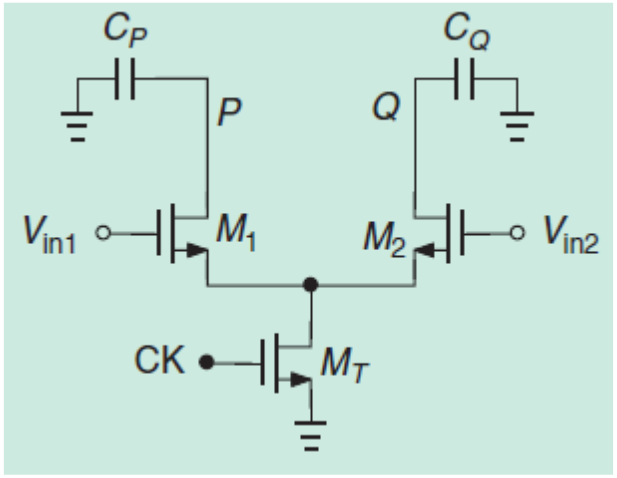


[Razavi]

- Static offset due to V_t mismatch in input pair
- Other mismatch sources attenuated by gain from initial amplification phase

$$\sigma_{VOS,stat} \approx \frac{A_{VT}}{\sqrt{W_1 L_1}}$$ Pelgrom's formula

Amplification phase:



- Dynamic offset due to mismatch in C_P and C_Q

$$V_{OS,dyn} \approx \frac{V_{tn}}{2}\left(\frac{C_P}{C_Q} - \frac{C_Q}{C_P}\right) = V_{tn}\frac{\Delta C}{C}$$

Example: $500mV \cdot 5\% = 25mV$

Kickback

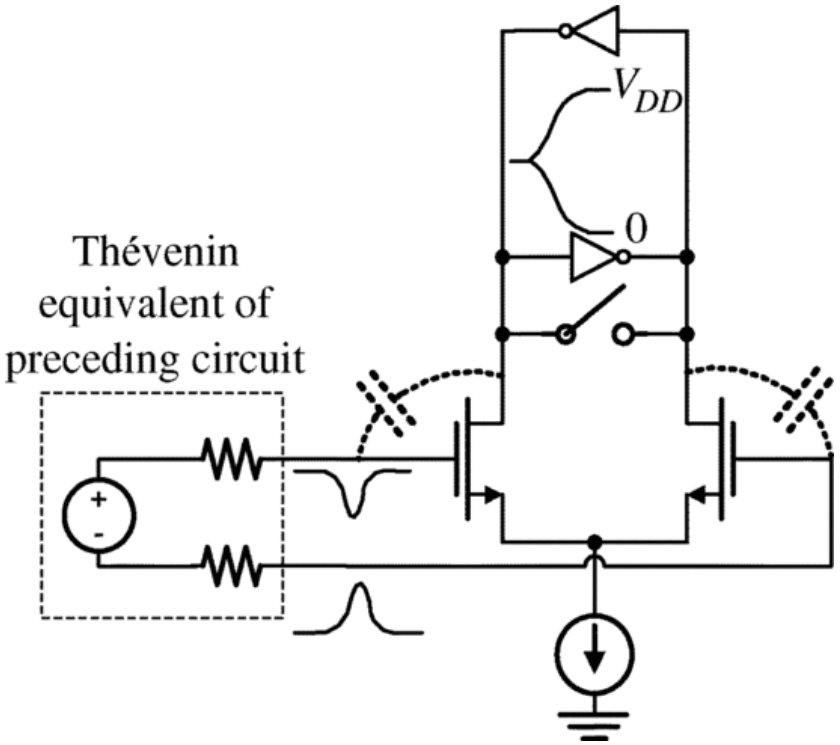


Figure from [Figueiredo, TCAS2, July 2006]