Project Specifications

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Fixing the IHP Standard Cell Symbols – Updated sed Command

- Enter the container as root

```
docker exec -u root -t -i iic-osic-tools_xserver_uid_1000 /bin/bash
```

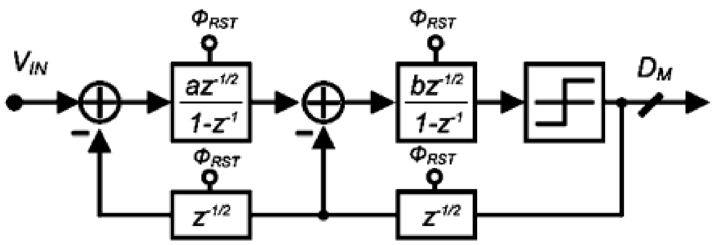
- Go to directory containing the IHP standard cell symbols

```
cd /foss/pdks/sg13g2/libs.tech/xschem/sg13g2_stdcells
```

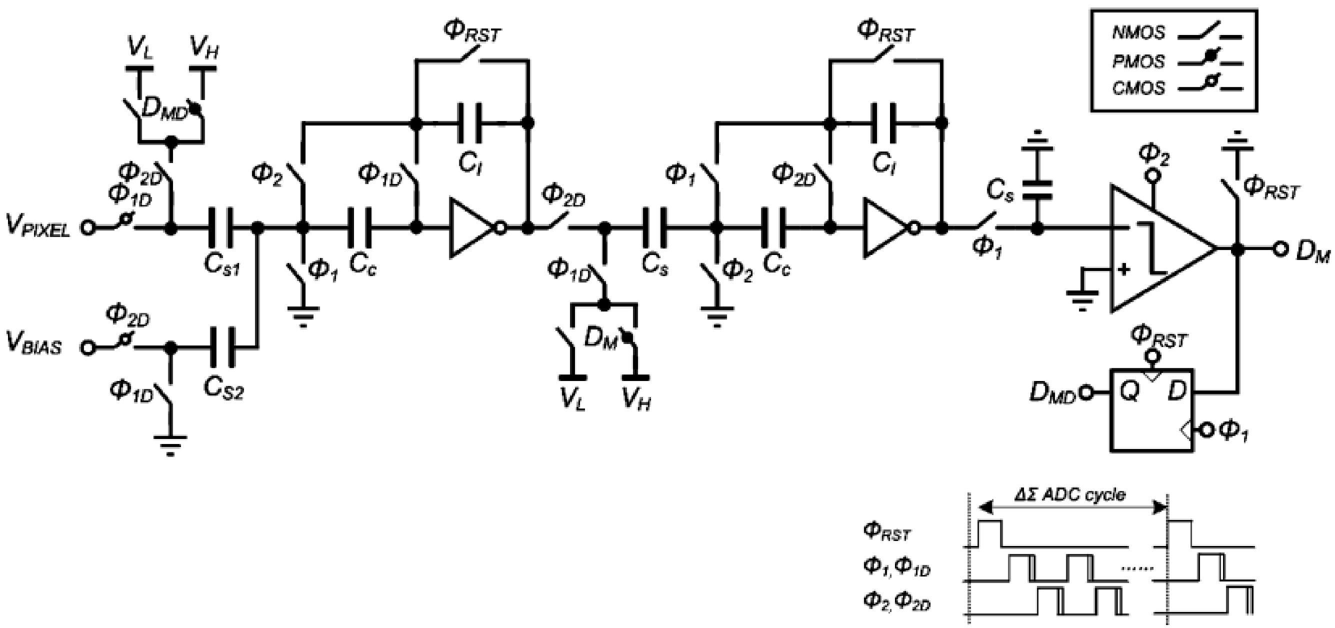
- Run this command to fix the symbols' pin order (courtesy Mitch Bailey)

```
sed -i  \
-e 's/@VGND @VNB @VPB @VPWR/@VDD @VSS/' \
-e 's/VGND=VGND VNB=VNB VPB=VPB VPWR=VPWR/VDD=VDD VSS=VSS/' \
-e 's/VGND VNB VPB VPWR/VDD VSS/' \
-e 's/@VDD @VSS @@Q @@Q_N/@@Q @@Q_N @VDD @VSS/' \
-e 's/\(@@RESET.*\)@@Q @@Q_N /@@Q @@Q_N \1/' *.sym
```

Template Circuit



(a)

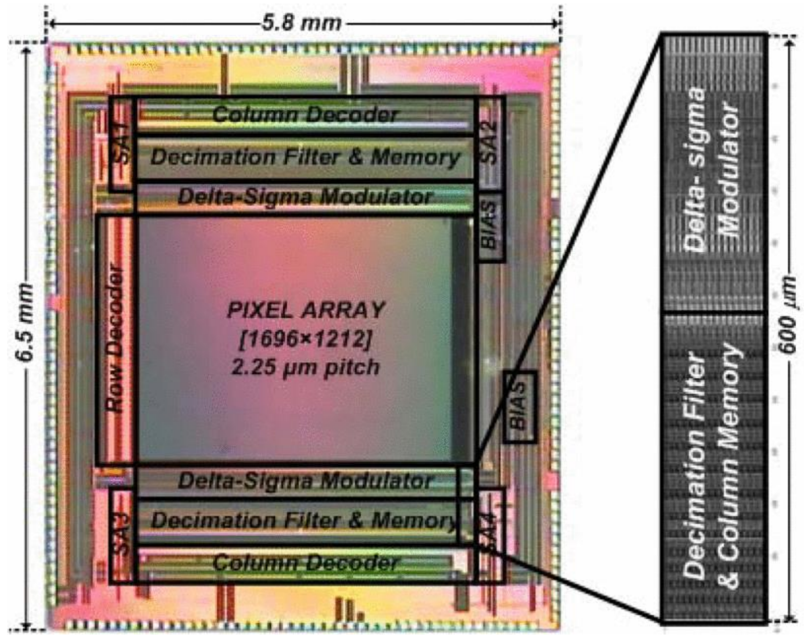


(b)

Y. Chae et al., "A 2.1 M Pixels, 120 Frame/s CMOS Image Sensor With Column-Parallel ADC Architecture," in IEEE Journal of Solid-State Circuits, Jan. 2011. https://ieeexplore.ieee.org/document/5641589

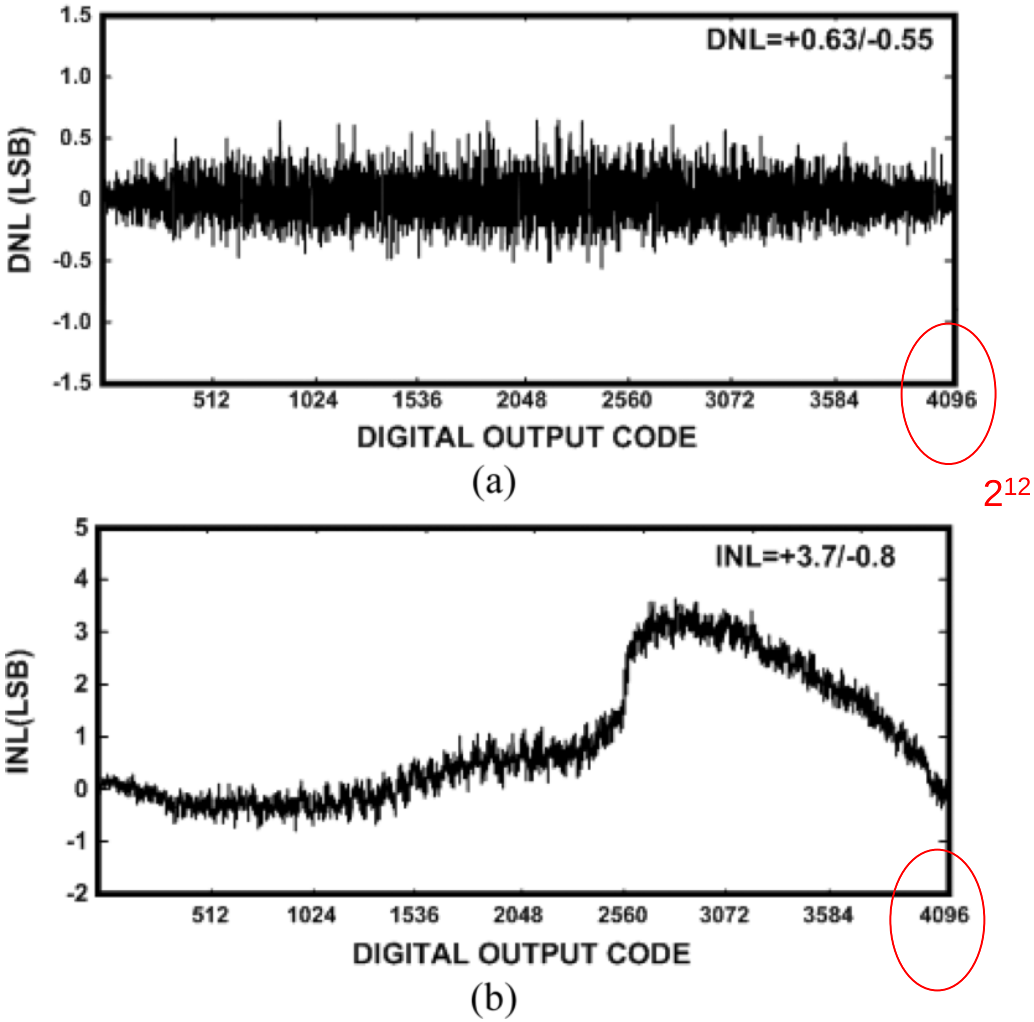
Reported ADC Specifications

- Resolution = 12 bits
- DNL = +0.63/-0.53
- INL = 3.7/-0.8
- SNR = 66 dB
- DR = 75 dB
- Bandwidth = 220 kHz
- Clock frequency = 48 MHz
- Power consumption = 40 μW
- Supply voltage = 1.2 V
- Area ~ 4.5 um x 300 um ~ 1500 um^2



16 cols

DNL/INL Plots

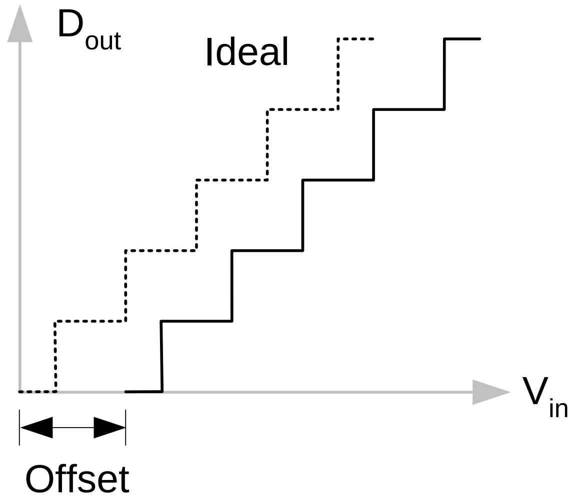


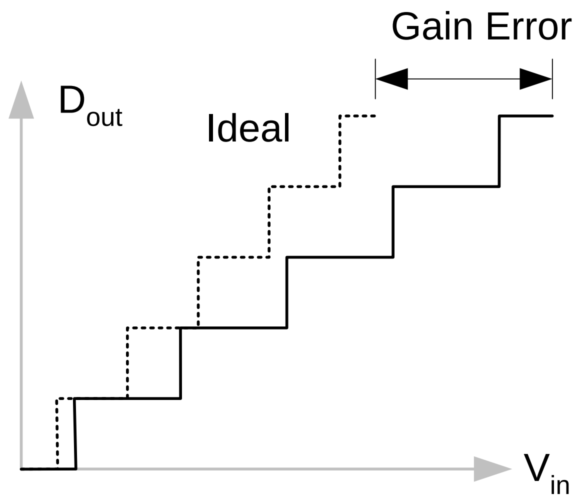
DNL = Differential Nonlinearity

INL = Integral Nonlinearity

Quantifying Static ADC Nonidealities

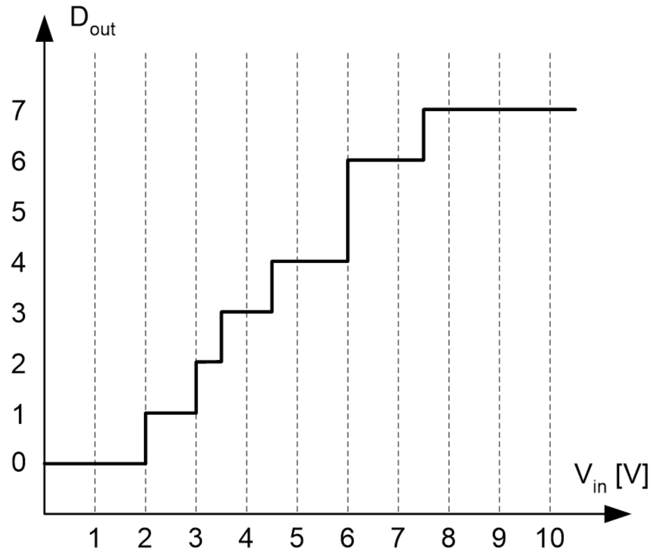
- Static deviations of transfer characteristics from ideality
  - Differential Nonlinearity (DNL)
  - Integral Nonlinearity (INL)
  - Offset and gain error
    - Important for instrumentation, typically don't care in communication systems





Differential Nonlinearity (DNL)

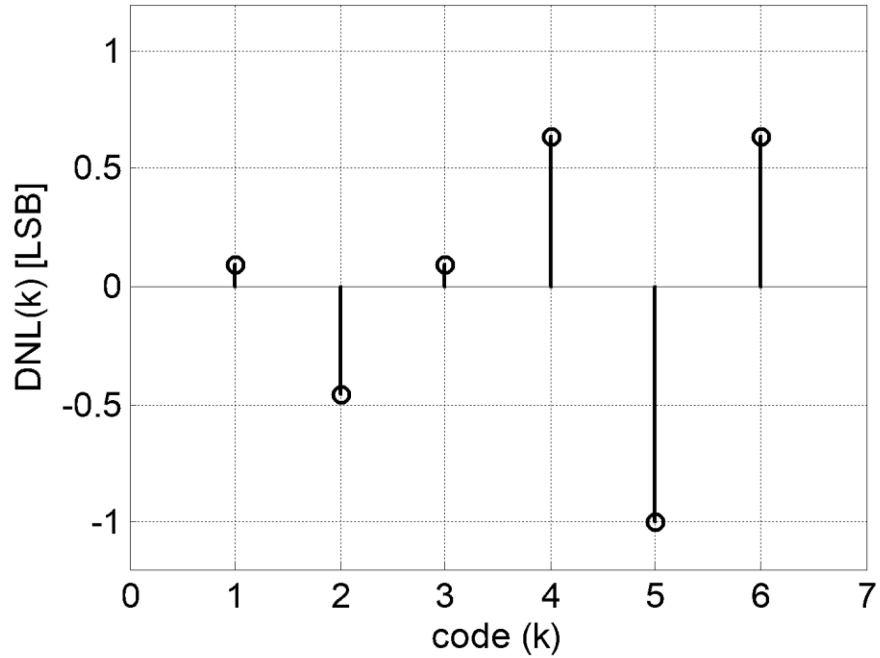
- In an ideal world, all ADC codes would have equal width
- DNL(k) is a vector that quantifies for each code k the deviation of this width from the "average" width (step size)
- DNL(k) is a measure of uniformity
  - It does not depend on gain and offset errors
  - Scaling and shifting a transfer characteristic does not alter its uniformity and hence does not affect DNL(k)



Code (k)	W [V]
0	undefined
1	1
2	0.5
3	1
4	1.5
5	0
6	1.5
7	undefined

$$DNL(k) = \frac{W(k) - W_{AVG}}{W_{AVG}}$$

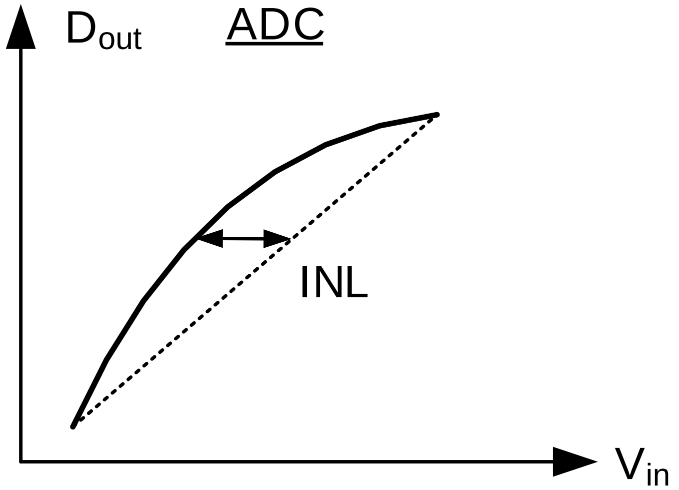
Code (k)	DNL [LSB]
1	0.09
2	-0.45
3	0.09
4	0.64
5	-1.00
6	0.64



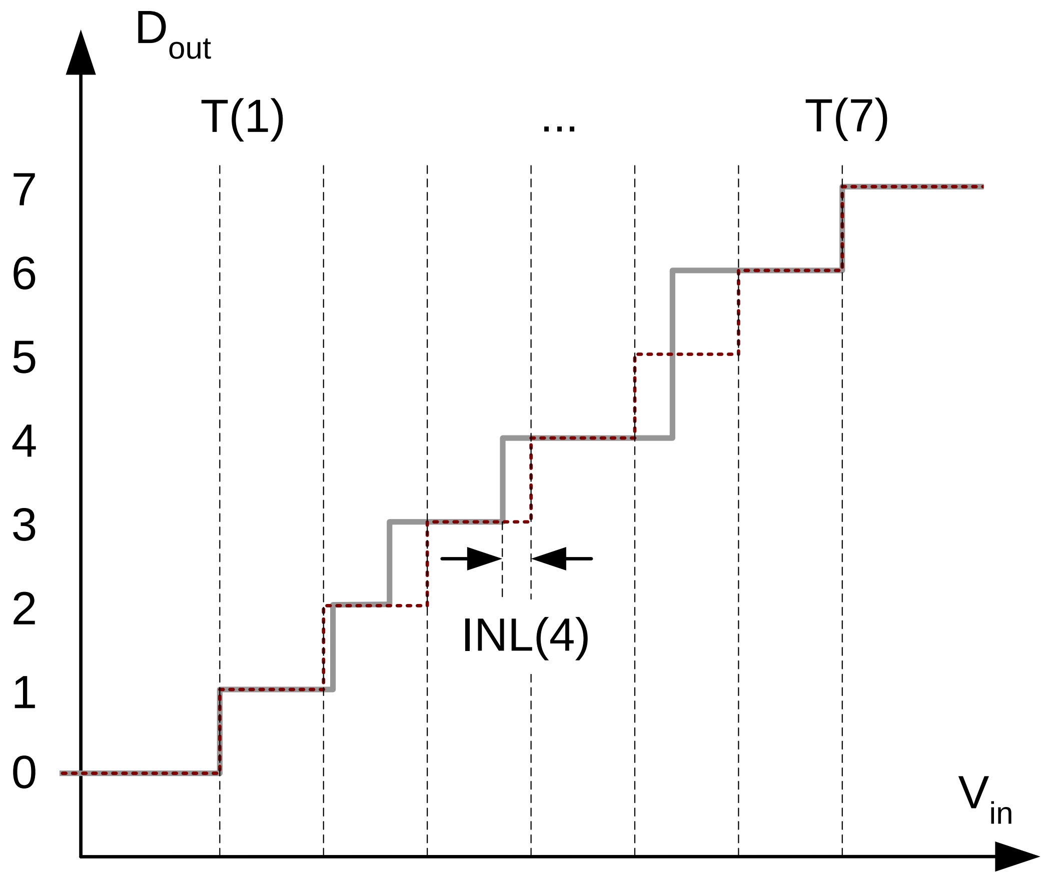
- Positive/negative DNL implies wide/narrow code, respectively
- DNL = -1 LSB implies missing code
- Impossible to have DNL < -1 LSB for an ADC, but DNL > +1 LSB is possible
- Can show that sum over all DNL(k) is equal to zero

Integral Nonlinearity (INL)

- General idea
  - For each "relevant point" of the transfer characteristic, quantify distance from a straight line drawn through the endpoints
    - An alternative, a less common definition uses a least square fit line as a reference
  - Just as with DNL, the INL of a converter is independent of gain and offset errors



ADC INL Example



- "Straight line" reference is uniform staircase between first and last transition
- INL for each code is

$$INL(k) = \frac{T(k) - T_{uniform}(k)}{W_{AVG}}$$

- Obviously INL(1) = 0 and INL(7) = 0
- INL(0) is undefined

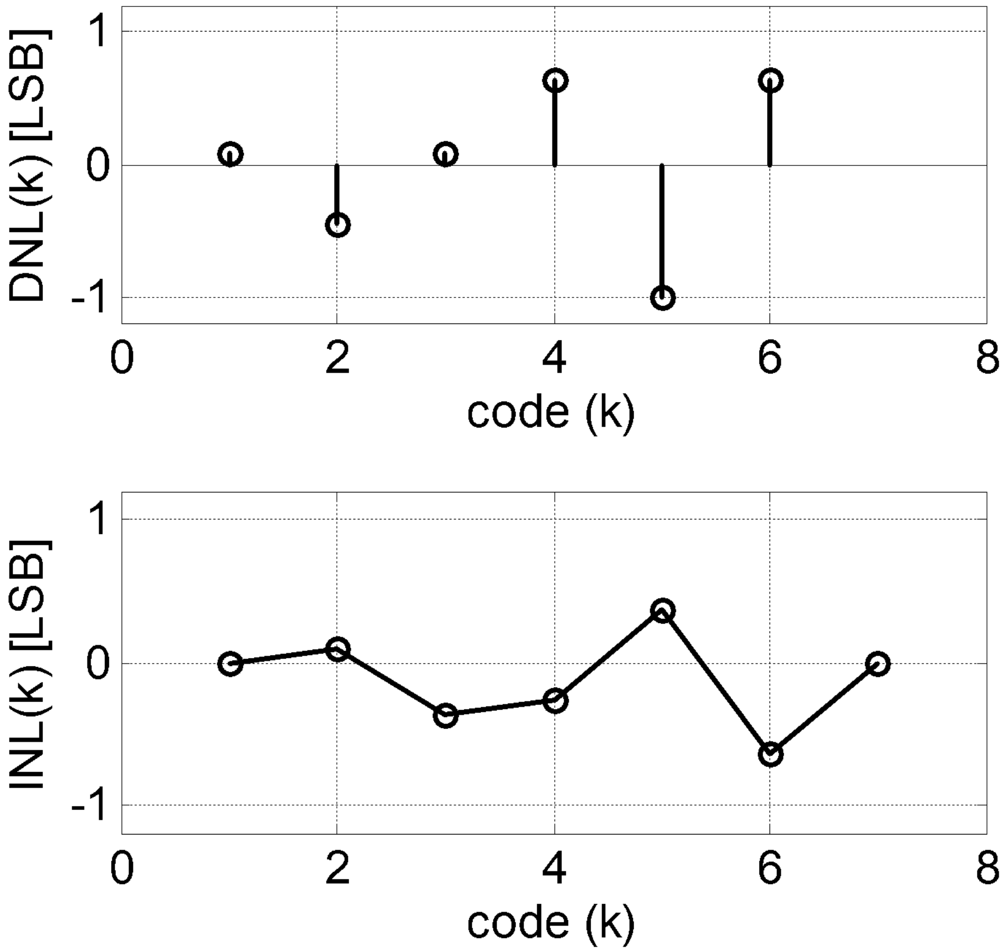
- Can show that

$$INL(k) = \sum_{i=1}^{k-1} DNL(i)$$

- Means that once we've computed DNL, we can easily find INL using a cumulative sum operation on the DNL vector

Code (k)	DNL [LSB]	INL [LSB]
1	0.09	0
2	-0.45	0.09
3	0.09	-0.36
4	0.64	-0.27
5	-1.00	0.36
6	0.64	-0.64
7	undefined	0

Example

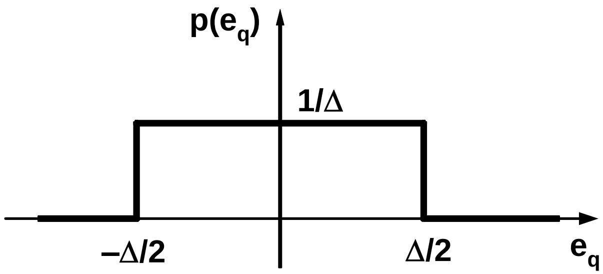


Spectral Performance Metrics

SQNR	Signal-to-quantization-noise ratio
SNR	Signal-to-noise ratio
SNDR	Signal-to-(noise+distortion) ratio
ENOB	Effective number of bits
DR	Dynamic range
SFDR	Spurious free dynamic range
HD	Harmonic distortion
THD	Total harmonic distortion
IM	Intermodulation distortion

Quantization Error – Statistical Model

- Uniform PDF approximation holds reasonably well when
  - Signal spans many quantization steps
  - Signal is "sufficiently active"
  - Quantizer does not overload (input stays within full-scale range)



Mean $$\overline{e_q} = \int_{-\Delta/2}^{+\Delta/2} \frac{1}{\Delta} e_q \, de_q = 0$$

Variance $$\overline{e_q^2} = \int_{-\Delta/2}^{+\Delta/2} \frac{1}{\Delta} e_q^2 \, de_q = \frac{\Delta^2}{12}$$

Signal-to-Quantization-Noise Ratio

- Assuming a full-scale sinusoidal input, we have

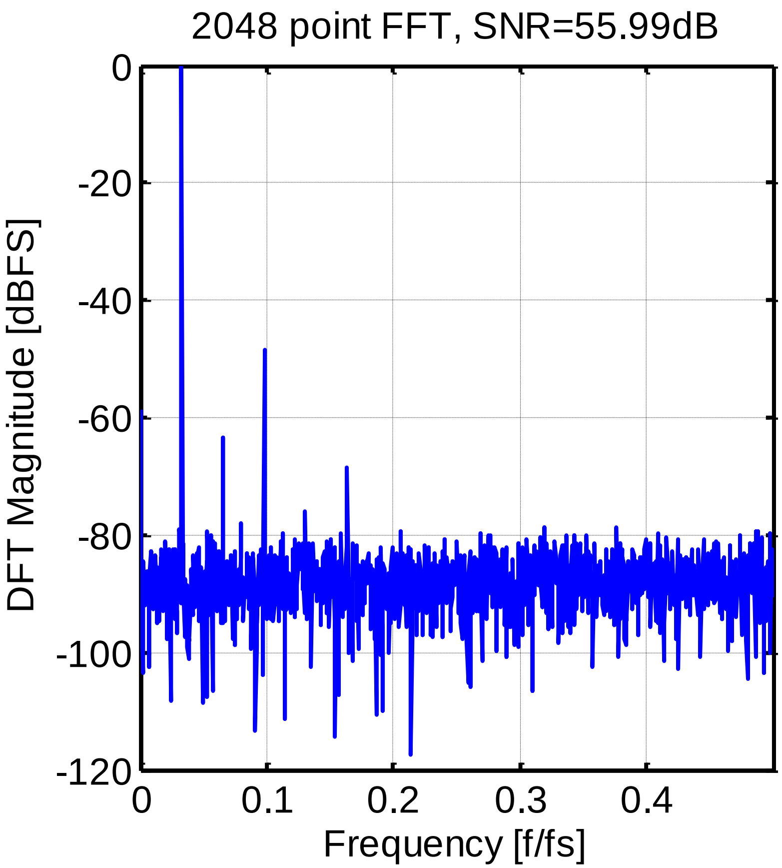
$$SQNR = \frac{P_{sig}}{P_{qnoise}} = \frac{\frac{1}{2}\left(\frac{2^{B}\Delta}{2}\right)^{2}}{\frac{\Delta^{2}}{12}} = 1.5 \cdot 2^{2B} = 6.02 \cdot B + 1.76\ dB$$

B (Number of Bits)	**SQNR**
8	50 dB
10	62 dB
12	74 dB
16	98 dB
20	122 dB

SNR

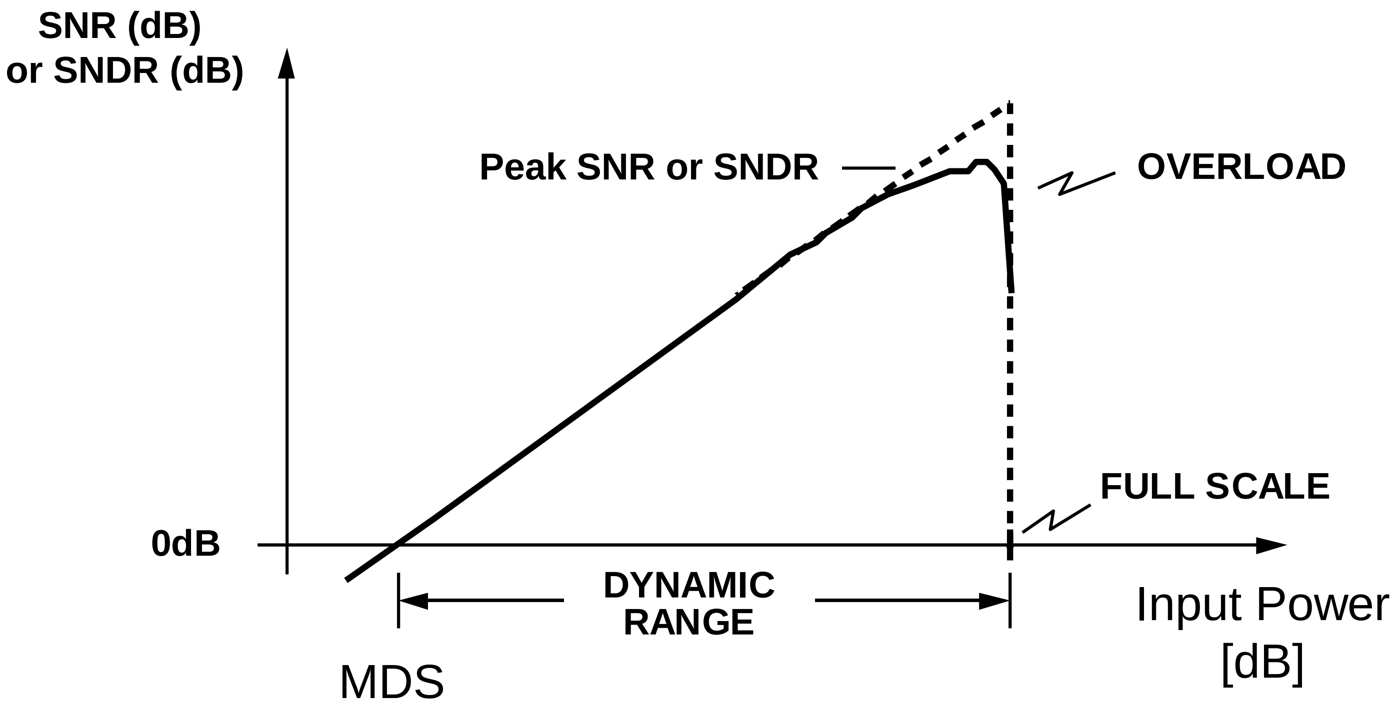
$$SNR = \frac{Signal\ Power}{Noise\ Power}$$

- Total noise power includes all FFT bins except DC, signal, and 2^{nd} through 7^{th} harmonic
- SNR captures
  - Quantization noise
  - DNL noise
  - Thermal noise
  - Sampling jitter



Dynamic Range

$$DR = \frac{Maximum\ Signal\ Power}{Minimum\ Detectable\ Signal} \geq SNR_{peak} \geq SNDR_{peak}$$

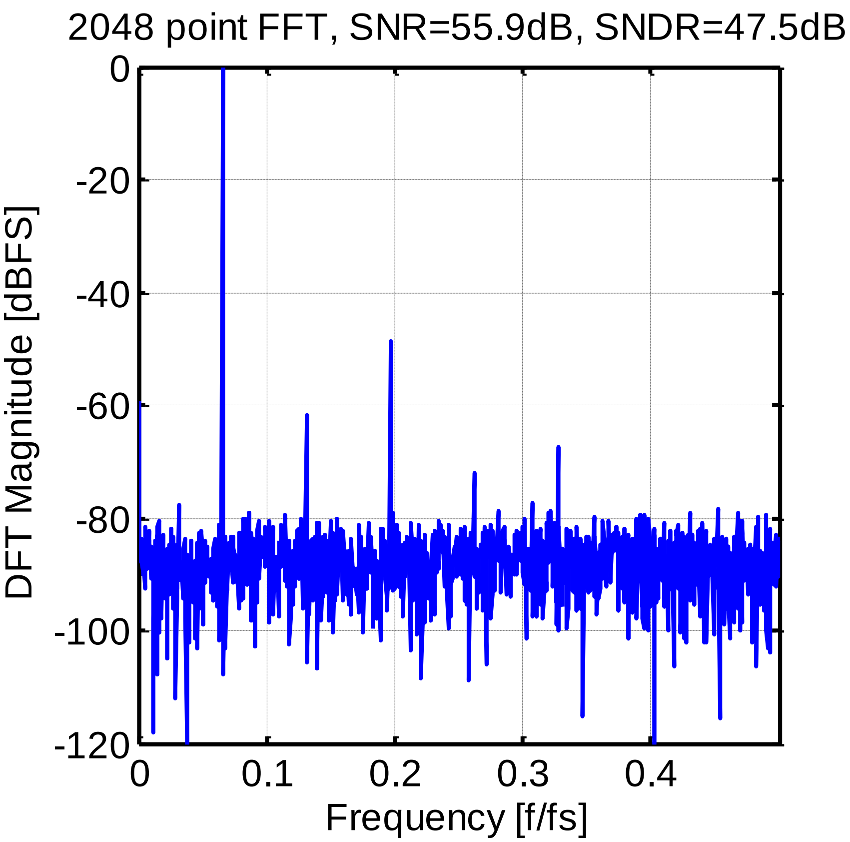


SNDR and ENOB

$$SNDR = \frac{Signal\ Power}{Noise\ and\ Distortion\ Power}$$

$$ENOB = \frac{SNDR(dB) - 1.76}{6.02}$$

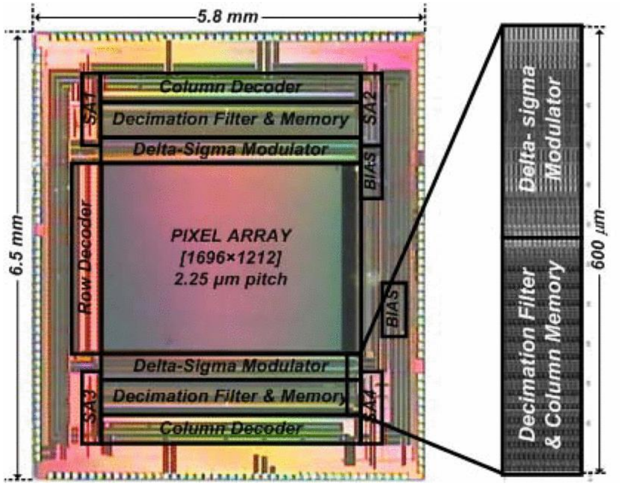
- Noise and distortion power includes all FFT bins except DC and signal
- ENOB of practical ADCs is typically 0.5-2 bits below quantizer resolution



ENOB of Reported ADC?

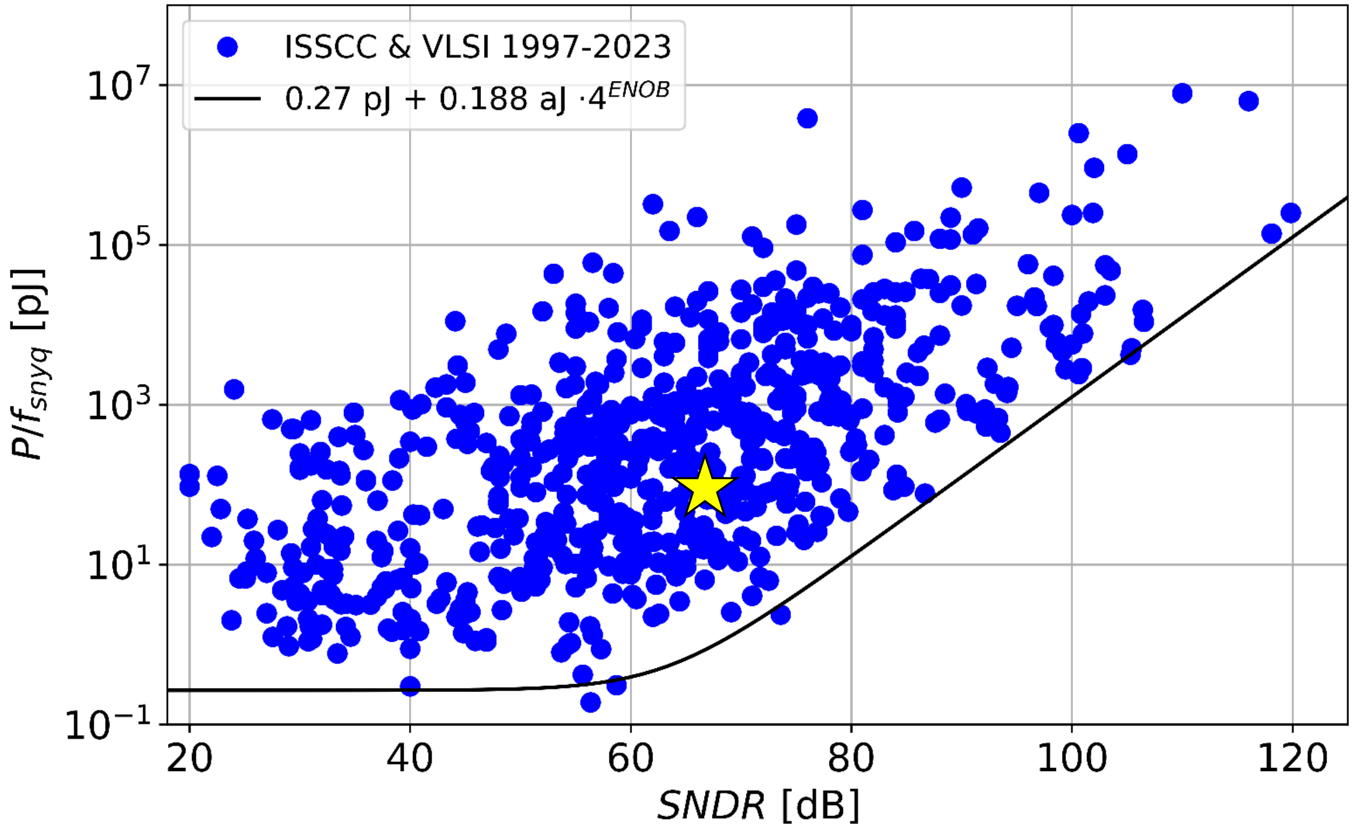
- SNR = 66 dB
- DR = 75 dB

- SNDR not reported
  - Does not matter for image sensor application
- We can still estimate
  - ENOB ~ (SNR-1.76)/6.02
  - ENOB ~ 10.67 bits



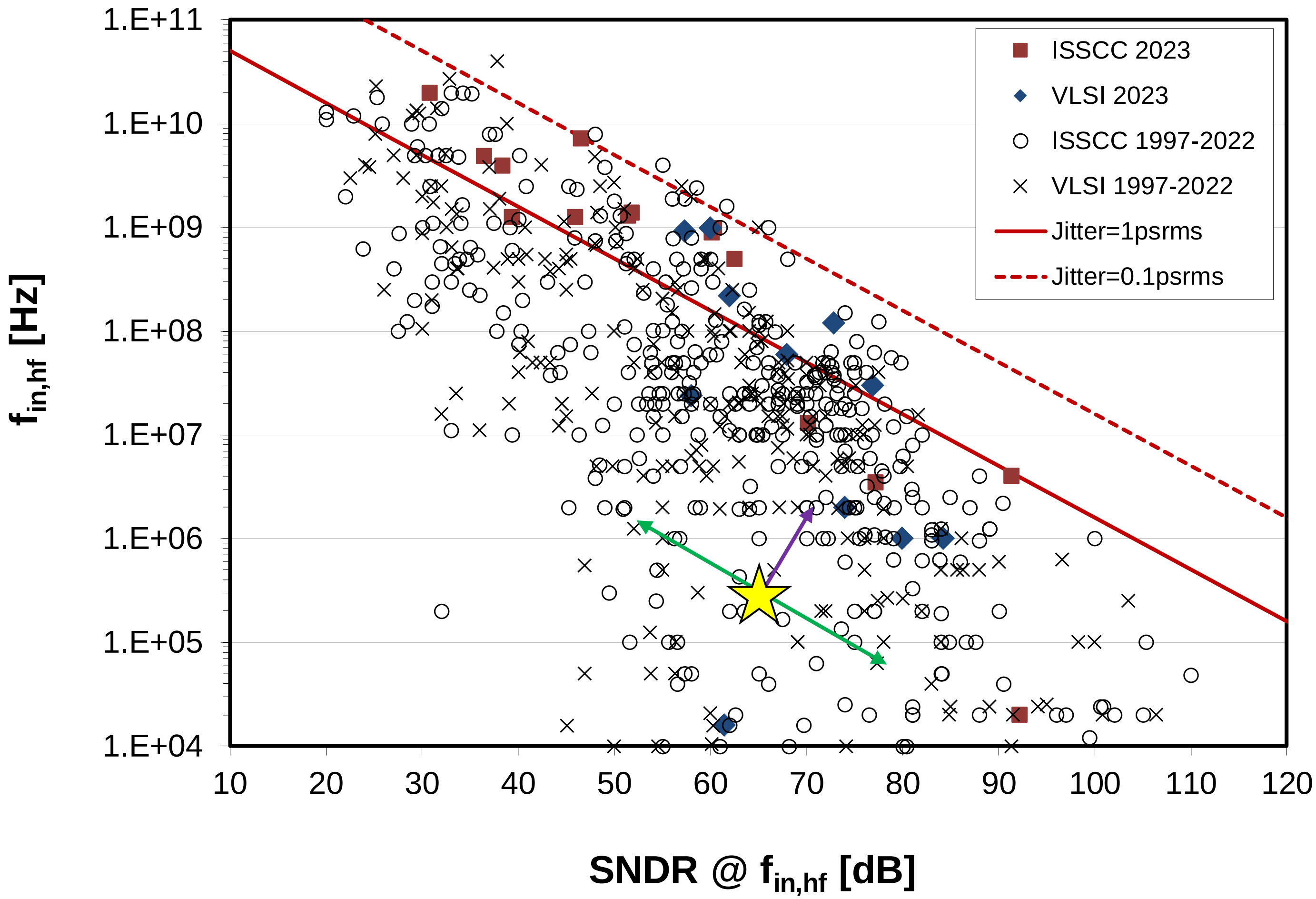
Energy Efficiency

$$\frac{P}{f_{snyq}} = \frac{40\mu W}{2 \times 220kHz} = 90pJ$$



https://github.com/bmurmann/ADC-survey

Speed-Resolution Product



https://github.com/bmurmann/ADC-survey

Team Decisions Needed

- **What will be your team's optimization angle?**
- Some options
  a) Try to hit exactly same speed, SNR & power as template → boring!
  b) Go for same speed & SNR, look for power reductions
  c) Maintain same speed-resolution product, increase speed or resolution
     - E.g., go for 3 dB higher SNR, but drop speed by 2x (green arrow)
  d) Aim at pushing the speed-resolution envelope (purple arrow)
     - E.g., double speed without lowering SNR, then see what that does to the power consumption
- Each team should make a preliminary decision based on their interests
- You can change your mind later once you develop a better feel for the circuit, but having an initial direction is important for any development