Finishing Up

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Timeline

- 04/23: IHP expected to update DRC (stay tuned…)
- 04/26: Pull request (preliminary files)
- 04/29: Team updates: 2, 5, 6
- 05/01: Team updates: 1, 3, 4
- 05/03: Pull request (“final” files)
- 05/22: GDS deadline

Pull Request Contents

EE628/5_Design/4_Layout/Team X

TeamX.oas → Top level layout, contains all layout cells

TeamX.spice → Top level spice netlist

TeamX.sym → Top level symbol

TeamX.readme → Pin list + any notes you want to convey

TeamX_logo.oas → In case you want to include a logo

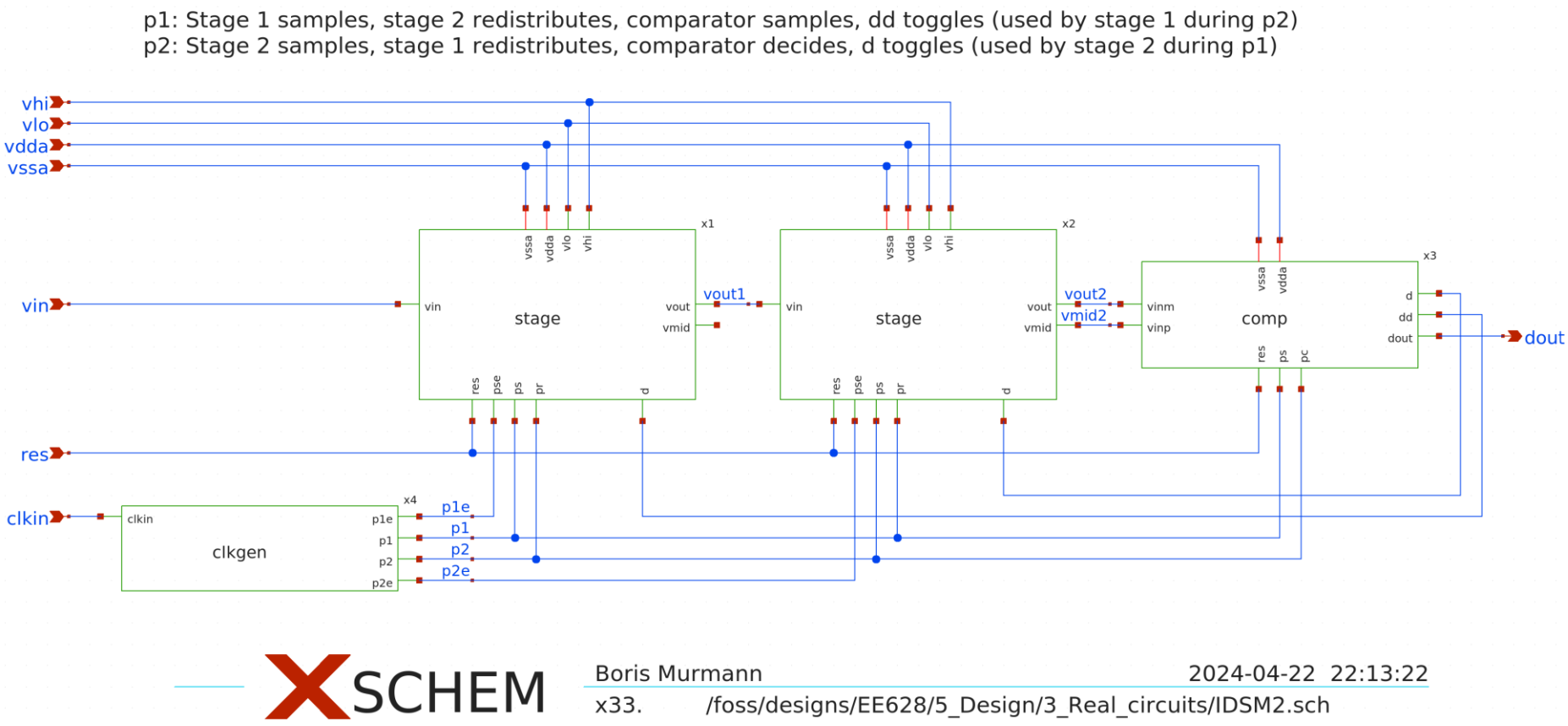
Please submit preliminary versions of all these files by 4/26

TeamX.readme Example

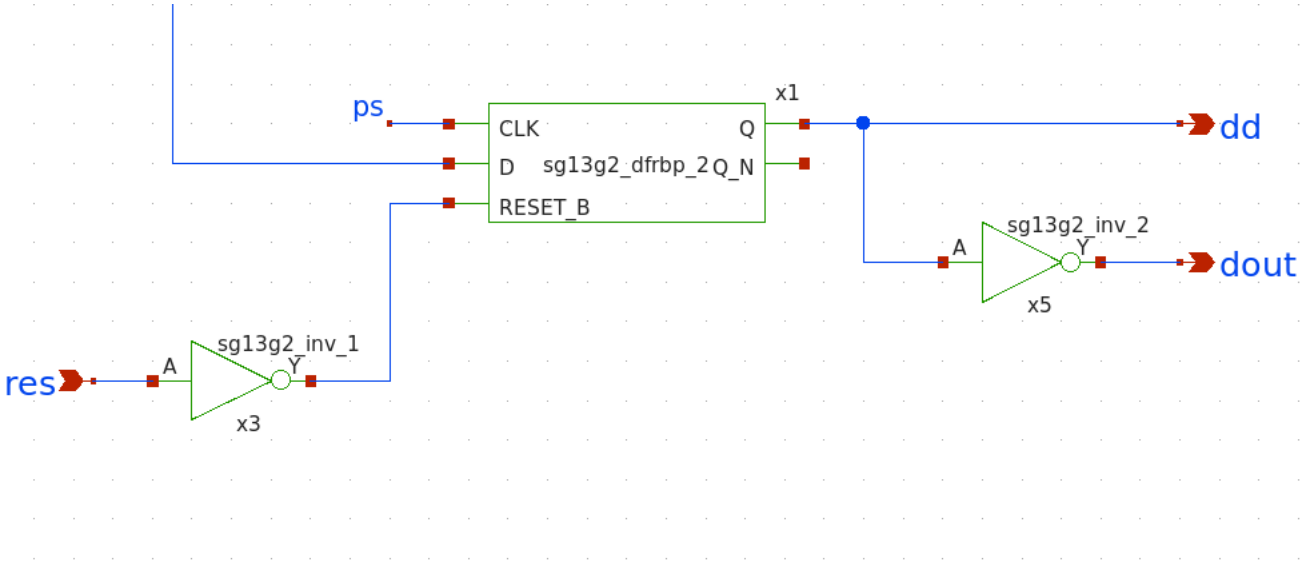
```
TeamX pin list:

Name   Type          Purpose
-------------------------------------------------
vin    input         Analog input of ADC
dout   output        Digital output of ADC
res    input         Digital rese signal (active high)
avdd   supply        Analog supply voltage
...

Current status:
These are the final files
```

Block Schematic

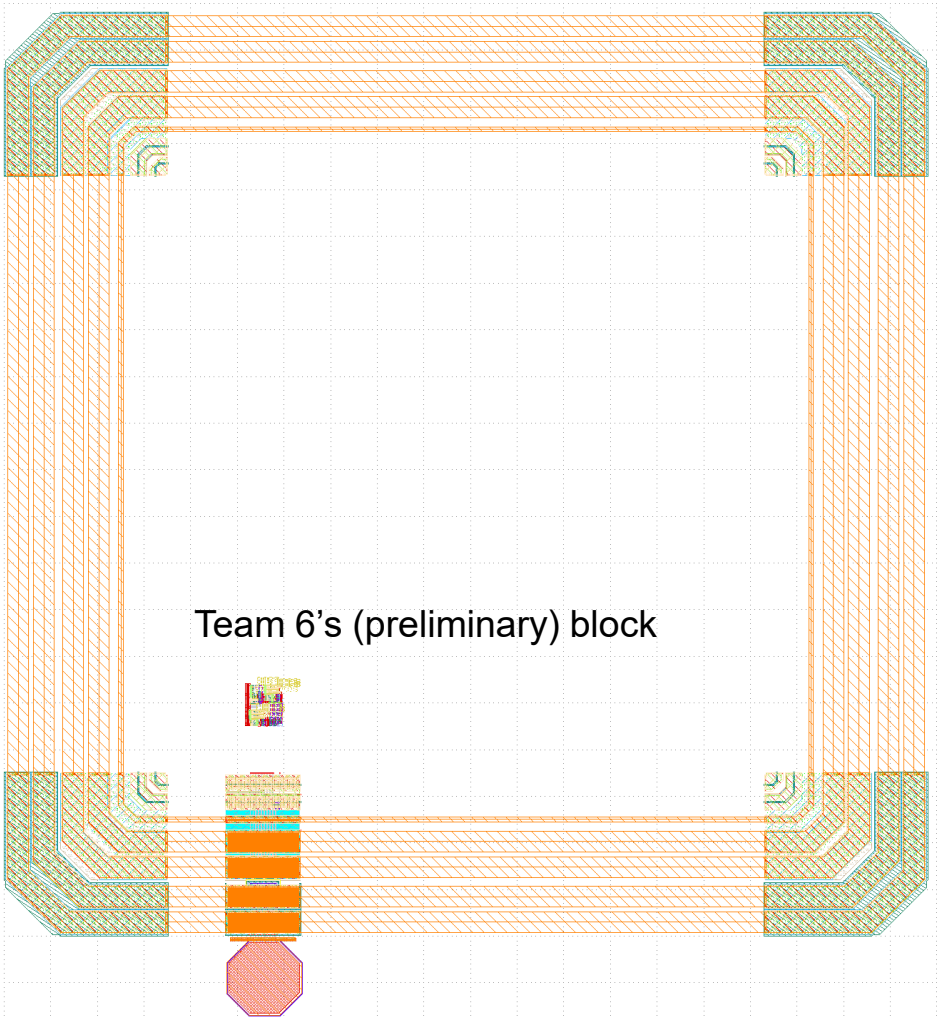
- Create both netlist and symbol form this schematic
  - Make sure there are no ideal spice elements!



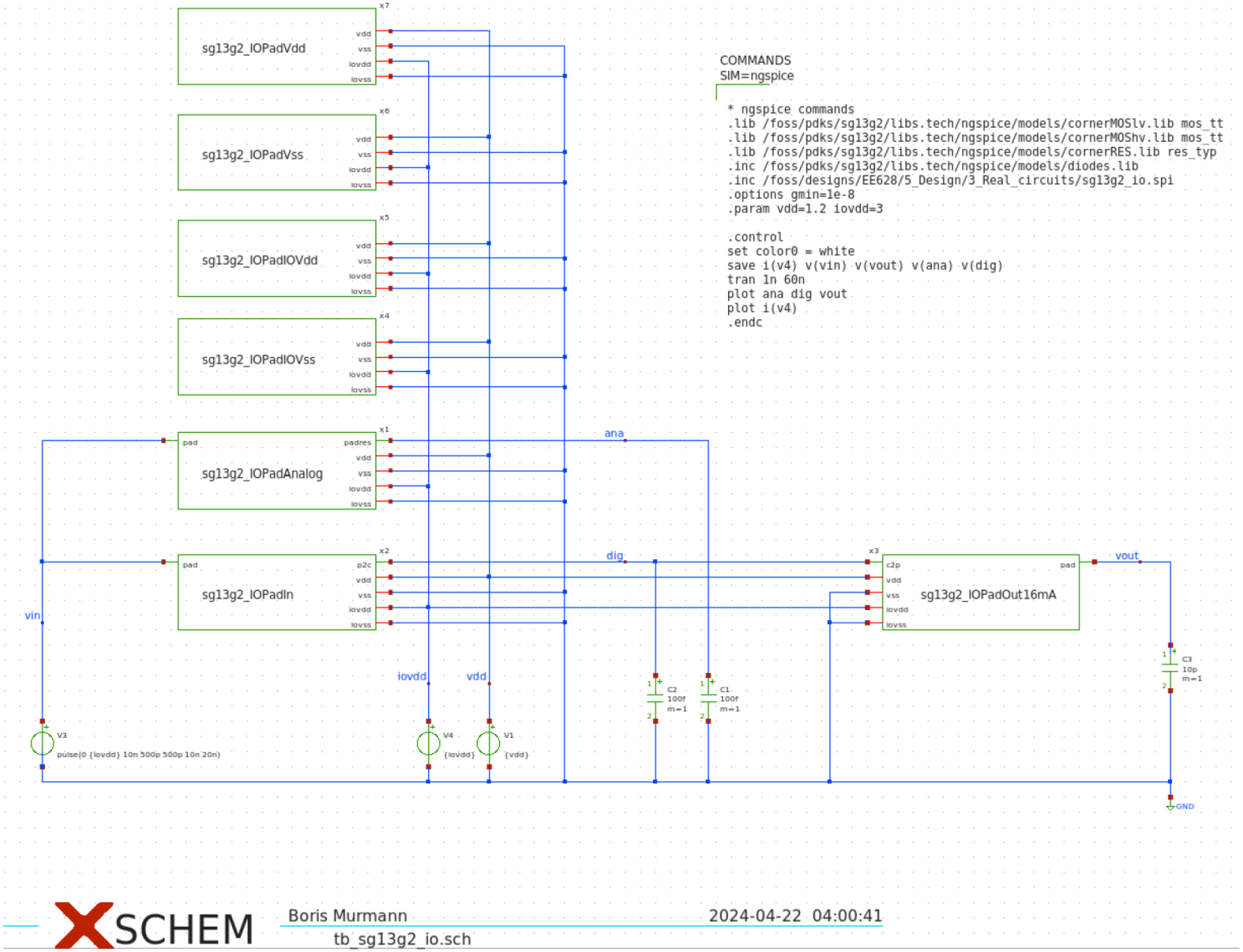
Recommended Output Signal (dout)



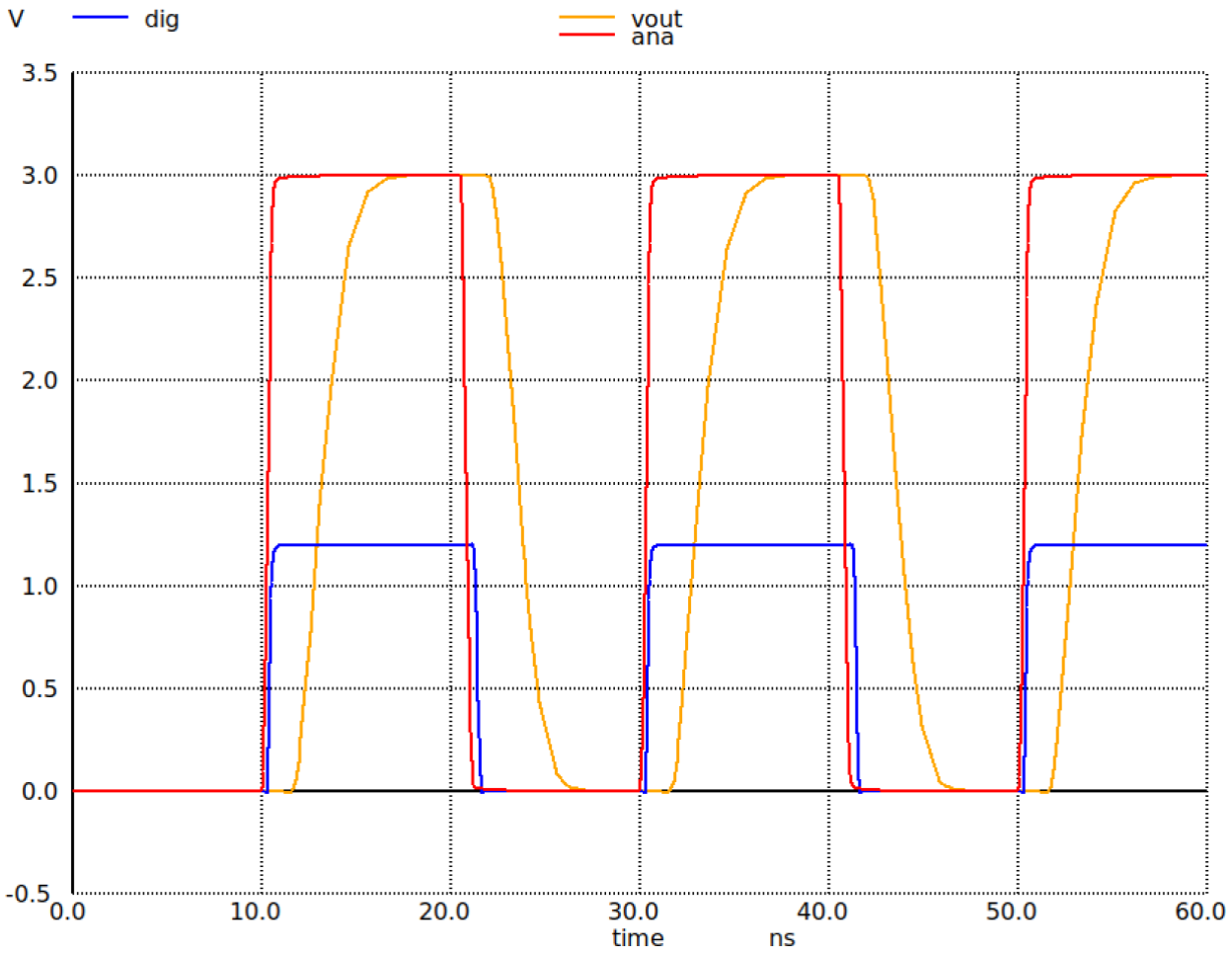
Preview of Chip Layout



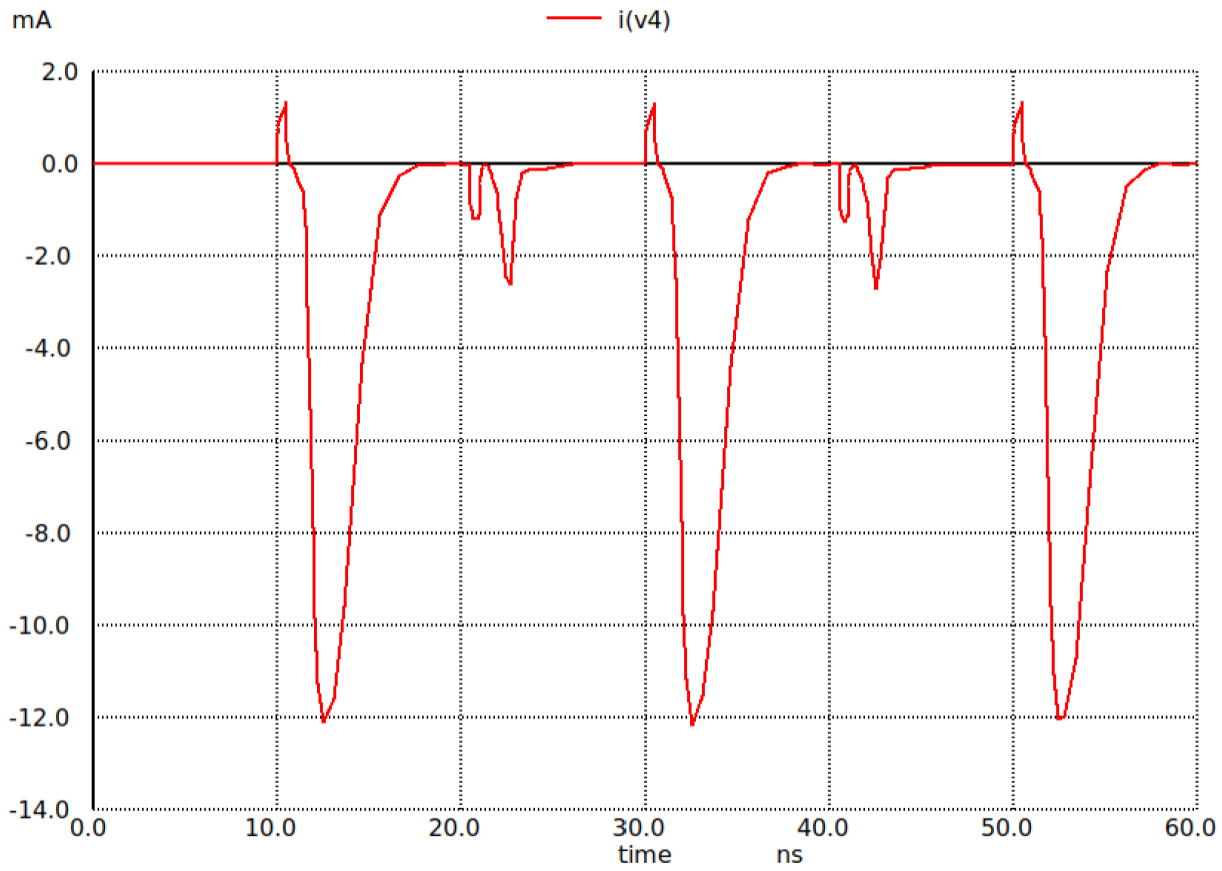
IO Cell Test

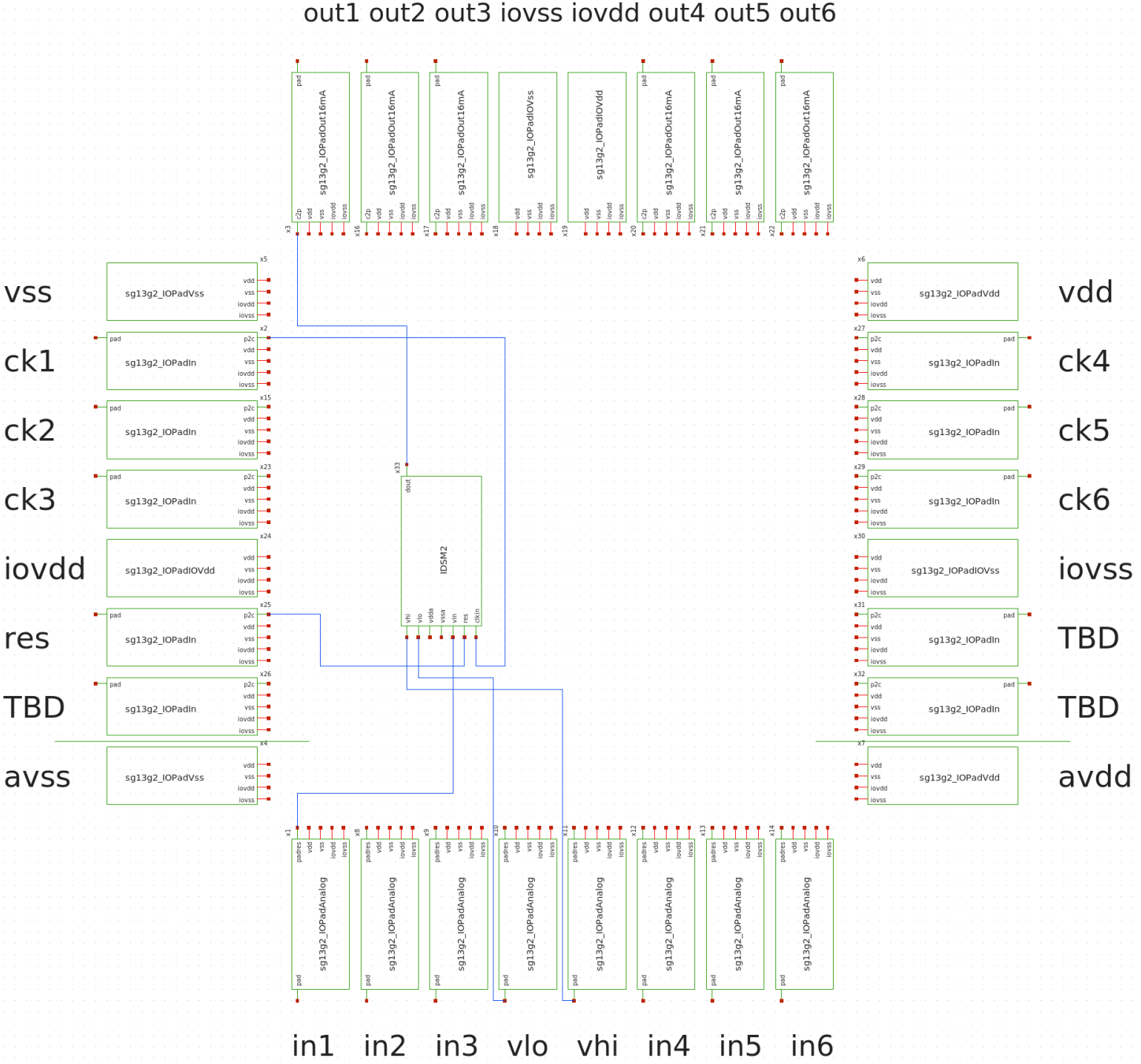

sg13g2_IOPadVdd
sg13g2_IOPadVss
sg13g2_IOPadIOVdd
sg13g2_IOPadIOVss
sg13g2_IOPadAnalog
sg13g2_IOPadIn
sg13g2_IOPadOut16mA
vdd
vss
iovdd
iovss
pad
padres
p2c
c2p
ana
dig
vout
vin
iovdd
vdd
C2 100f m=1
C1 100f m=1
C3 10p m=1
V3 pulse(0 {iovdd} 10n 500p 500p 10n 20n)
V4 {iovdd}
V1 {vdd}
GND
COMMANDS
SIM=ngspice
* ngspice commands
.lib /foss/pdks/sg13g2/libs.tech/ngspice/models/cornerMOSlv.lib mos_tt
.lib /foss/pdks/sg13g2/libs.tech/ngspice/models/cornerMOShv.lib mos_tt
.lib /foss/pdks/sg13g2/libs.tech/ngspice/models/cornerRES.lib res_typ
.inc /foss/pdks/sg13g2/libs.tech/ngspice/models/diodes.lib
.inc /foss/designs/EE628/5_Design/3_Real_circuits/sg13g2_io.spi
.options gmin=1e-8
.param vdd=1.2 iovdd=3
.control
set color0 = white
save i(v4) v(vin) v(vout) v(ana) v(dig)
tran 1n 60n
plot ana dig vout
plot i(v4)
.endc
XSCHEM
Boris Murmann
2024-04-22 04:00:41
tb_sg13g2_io.sch

Voltage Waveforms



Digital Drive Current (VDDIO = 3V)




out1 out2 out3 iovss iovdd out4 out5 out6
sg13g2_IOPadOut16mA
sg13g2_IOPadIOVss
sg13g2_IOPadIOVdd
vss
ck1
ck2
ck3
iovdd
res
TBD
avss
sg13g2_IOPadVss
sg13g2_IOPadIn
sg13g2_IOPadIOVdd
IDSM2
vdd
ck4
ck5
ck6
iovss
TBD
TBD
avdd
sg13g2_IOPadVdd
sg13g2_IOPadAnalog
in1 in2 in3 vlo vhi in4 in5 in6

Possible Outline for Next Week's Presentations

- What is your status?
  - What have you done since the last presentation?
  - What remains to be done?
  - What problems are you facing?

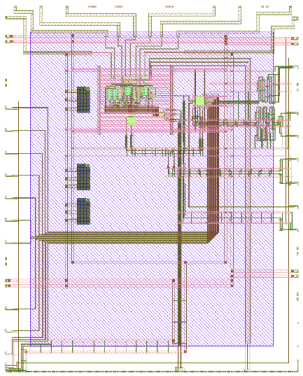
- What does your final block look like?
  - Top level schematic, pins, layout

- What have you done to check that your schematic and layout are correct?
  - Which simulations, corners?
  - How did you ensure that your layout has all the required connections?
    - In absence of LVS…

Guidelines for a Full Design Review Presentation

- Design overview
  - Walk through the system block diagram, give a big picture overview of the full system, clearly explain what is the input and what is the output
  - Show the datapath/circuit diagram of each sub-block, explain how it works
  - Talk about design decisions you made and the rationale behind them, explain the tradeoffs
- Verification of each sub-block and the entire system
  - Spice simulations, which tests did you perform?
  - How did you generate the stimuli?
  - What portions of the design are untested and what is your plan for testing them?
- Initial results
  - Estimate all design specific metrics you care about from spice simulation.
  - How do these compare with your initial specification?
  - If any devices other than MOSFETs are used, provide simulation plots showing extracted characteristics and describe the test setup.
- Integration
  - What is the approximate area of the entire circuit
  - Provide details regarding metals used for signal routing, power routing, layout methodology adopted for devices other than MOSFETs (Capacitor, Resistor, etc.)
  - I/O pin details: How many analog I/O pins, digital I/O pins, VDD, VSS pins are required?
- Plan for the remaining weeks
  - Particularly talk about your layout strategy
  - Provide a schedule with all milestones that you still need to complete for successful tapeout

- Design review example: https://priyanka-raina.github.io/ee372-spring2022/

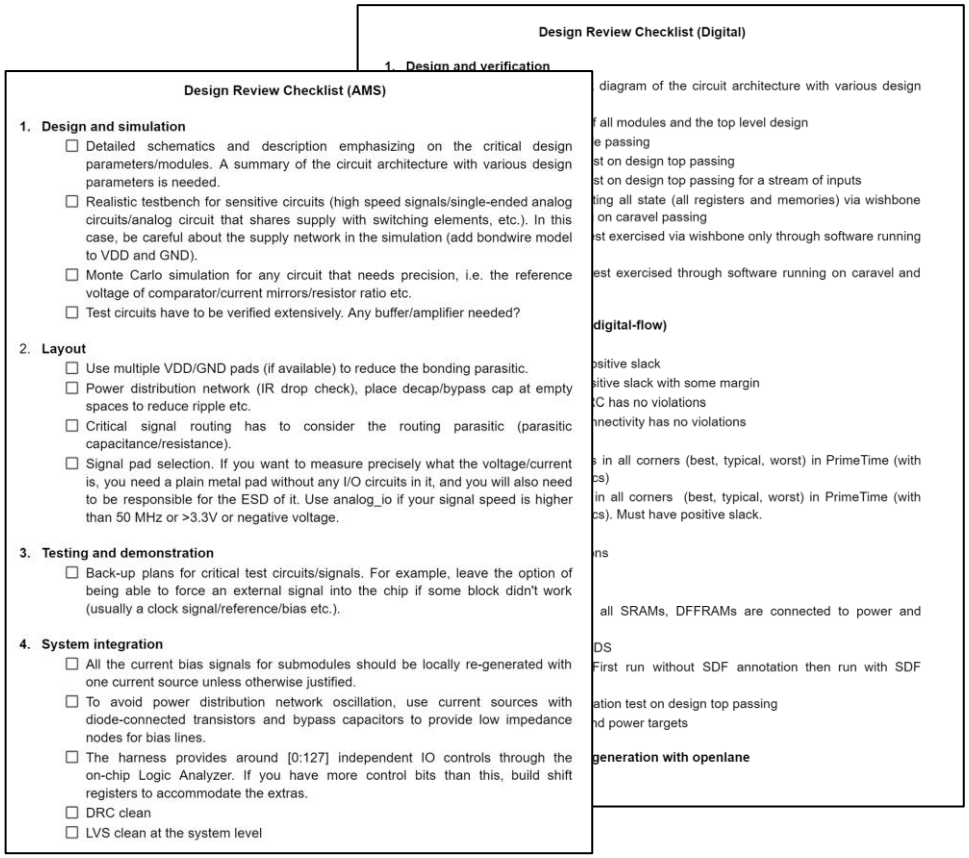


12-bit 10-KSPS Incremental Delta-Sigma ADC in Skywater 130 nm

Raymond Yang, Yaqing Xia

Code: Design, Caravel User Project Analog
Documentation: Proposal, Design Review, Final Presentation, Report
This project is a 12-bit 10 KSPS incremental delta-sigma analog-to-digital converter (ADC) designed for sensor interface and instrumentation applications. The ADC consists of a second-order incremental modulator and three post-integrators. The total area of the ADC is 0.55 square mm, with 0.53 square mm for analog modulator and 0.02 square mm for digital filter.

Good Practice: Maintain a Checklist



Design Review Checklist (AMS)

1. **Design and simulation**
   - ☐ Detailed schematics and description emphasizing on the critical design parameters/modules. A summary of the circuit architecture with various design parameters is needed.
   - ☐ Realistic testbench for sensitive circuits (high speed signals/single-ended analog circuits/analog circuit that shares supply with switching elements, etc.). In this case, be careful about the supply network in the simulation (add bondwire model to VDD and GND).
   - ☐ Monte Carlo simulation for any circuit that needs precision, i.e. the reference voltage of comparator/current mirrors/resistor ratio etc.
   - ☐ Test circuits have to be verified extensively. Any buffer/amplifier needed?
2. **Layout**
   - ☐ Use multiple VDD/GND pads (if available) to reduce the bonding parasitic.
   - ☐ Power distribution network (IR drop check), place decap/bypass cap at empty spaces to reduce ripple etc.
   - ☐ Critical signal routing has to consider the routing parasitic (parasitic capacitance/resistance).
   - ☐ Signal pad selection. If you want to measure precisely what the voltage/current is, you need a plain metal pad without any I/O circuits in it, and you will also need to be responsible for the ESD of it. Use analog_io if your signal speed is higher than 50 MHz or >3.3V or negative voltage.
3. **Testing and demonstration**
   - ☐ Back-up plans for critical test circuits/signals. For example, leave the option of being able to force an external signal into the chip if some block didn't work (usually a clock signal/reference/bias etc.).
4. **System integration**
   - ☐ All the current bias signals for submodules should be locally re-generated with one current source unless otherwise justified.
   - ☐ To avoid power distribution network oscillation, use current sources with diode-connected transistors and bypass capacitors to provide low impedance nodes for bias lines.
   - ☐ The harness provides around [0:127] independent IO controls through the on-chip Logic Analyzer. If you have more control bits than this, build shift registers to accommodate the extras.
   - ☐ DRC clean
   - ☐ LVS clean at the system level

Design Review Checklist (Digital)

1. **Design and verification**

diagram of the circuit architecture with various design

f all modules and the top level design
e passing
st on design top passing
st on design top passing for a stream of inputs
ting all state (all registers and memories) via wishbone
on caravel passing
st exercised via wishbone only through software running

est exercised through software running on caravel and

digital-flow)

positive slack
itive slack with some margin
C has no violations
nnectivity has no violations

s in all corners (best, typical, worst) in PrimeTime (with
cs)
in all corners (best, typical, worst) in PrimeTime (with
cs). Must have positive slack.

ns

all SRAMs, DFFRAMs are connected to power and

DS
First run without SDF annotation then run with SDF

ation test on design top passing
nd power targets

generation with openlane

https://docs.google.com/document/d/14fVJJB9oHs8LzoYUo322H58PTyj044MYgDIjb1f664o/edit

https://www.youtube.com/watch?v=aBDJQ9NYTEU