Noise

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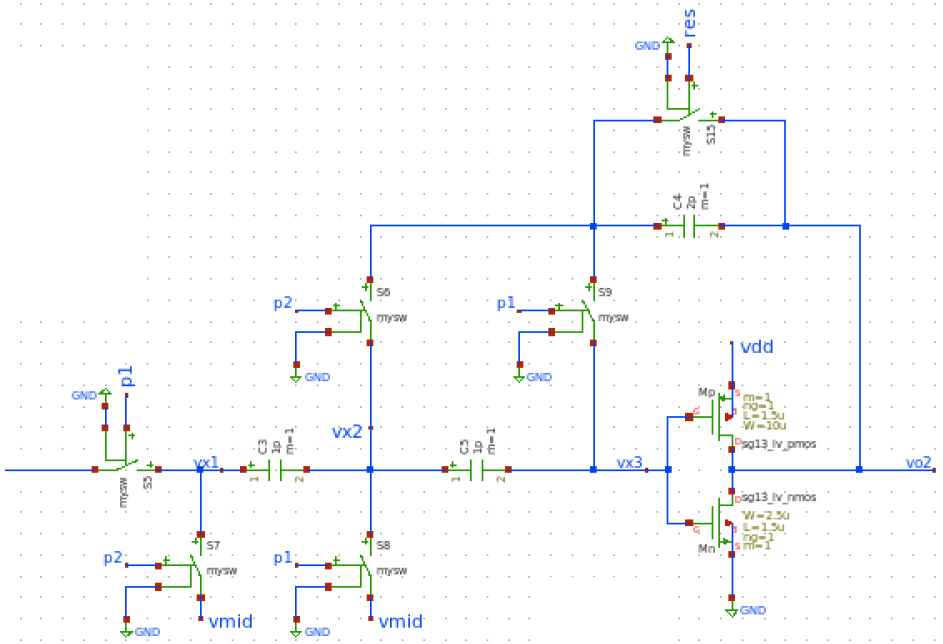
Motivation

- To complete the design of our inverter-based integrator we need to decide on the size of the capacitors
- It turns out that the capacitor sizes follow from the required thermal noise specifications
- Let's have a look at the basics…

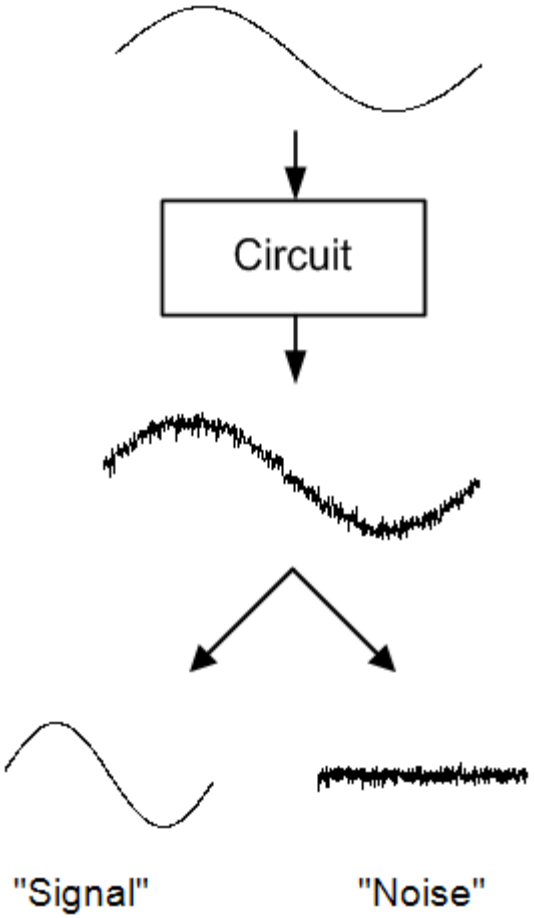


Types of Noise

- "Man made noise" or interference noise
  - Signal coupling
  - Substrate coupling
  - Finite power supply rejection
  - Solutions
    - Fully differential circuits
    - Layout techniques

- Electronic noise or "device noise" (our focus)
  - Fundamental
    - Thermal noise (or shot noise) caused by random carrier motion
  - Technology related
    - Flicker noise caused by material defects and "roughness"

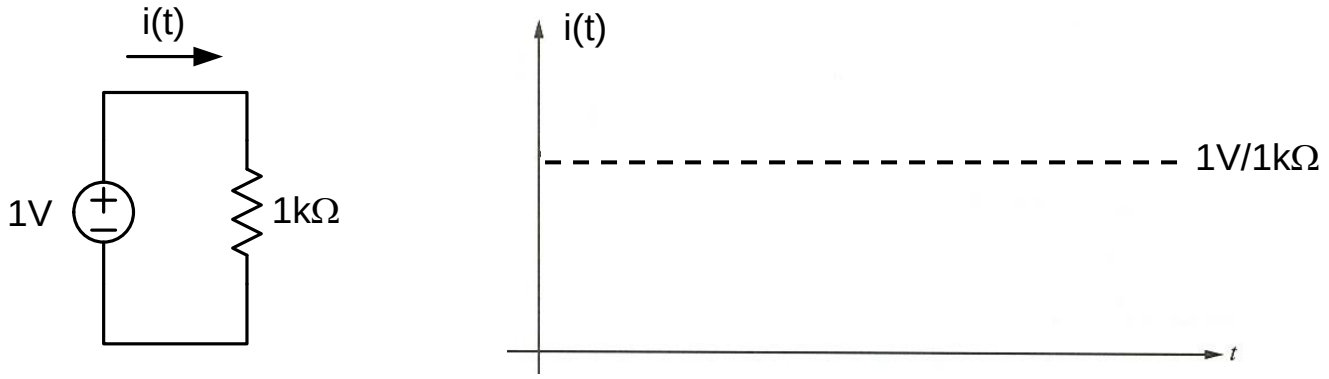
Significance of Electronic Noise (1)



Signal-to-Noise Ratio

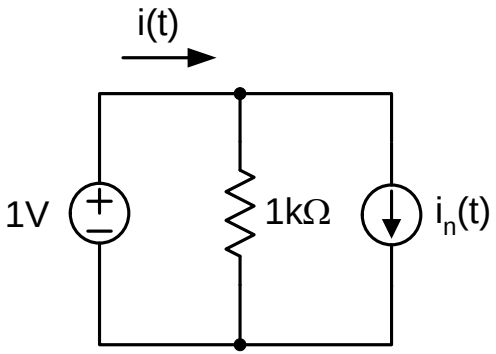
$$SNR = \frac{P_{signal}}{P_{noise}} \propto \frac{V_{signal}^2}{V_{noise}^2}$$

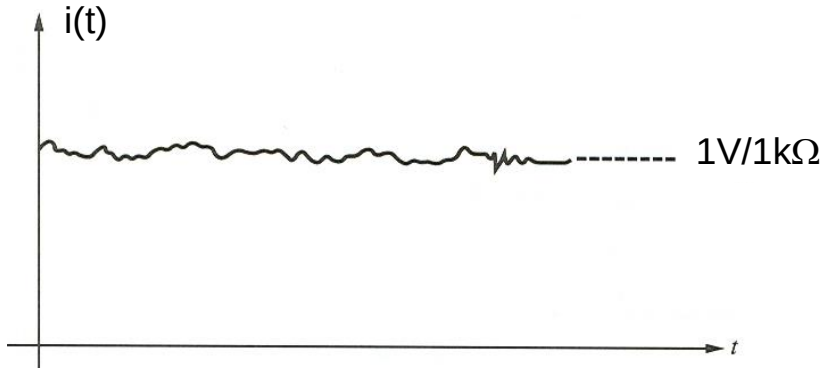
Ideal Resistor



- Constant current, independent of time
- Non-physical
  - In a physical resistor, carriers "randomly collide" with lattice atoms, giving rise to small current variations over time

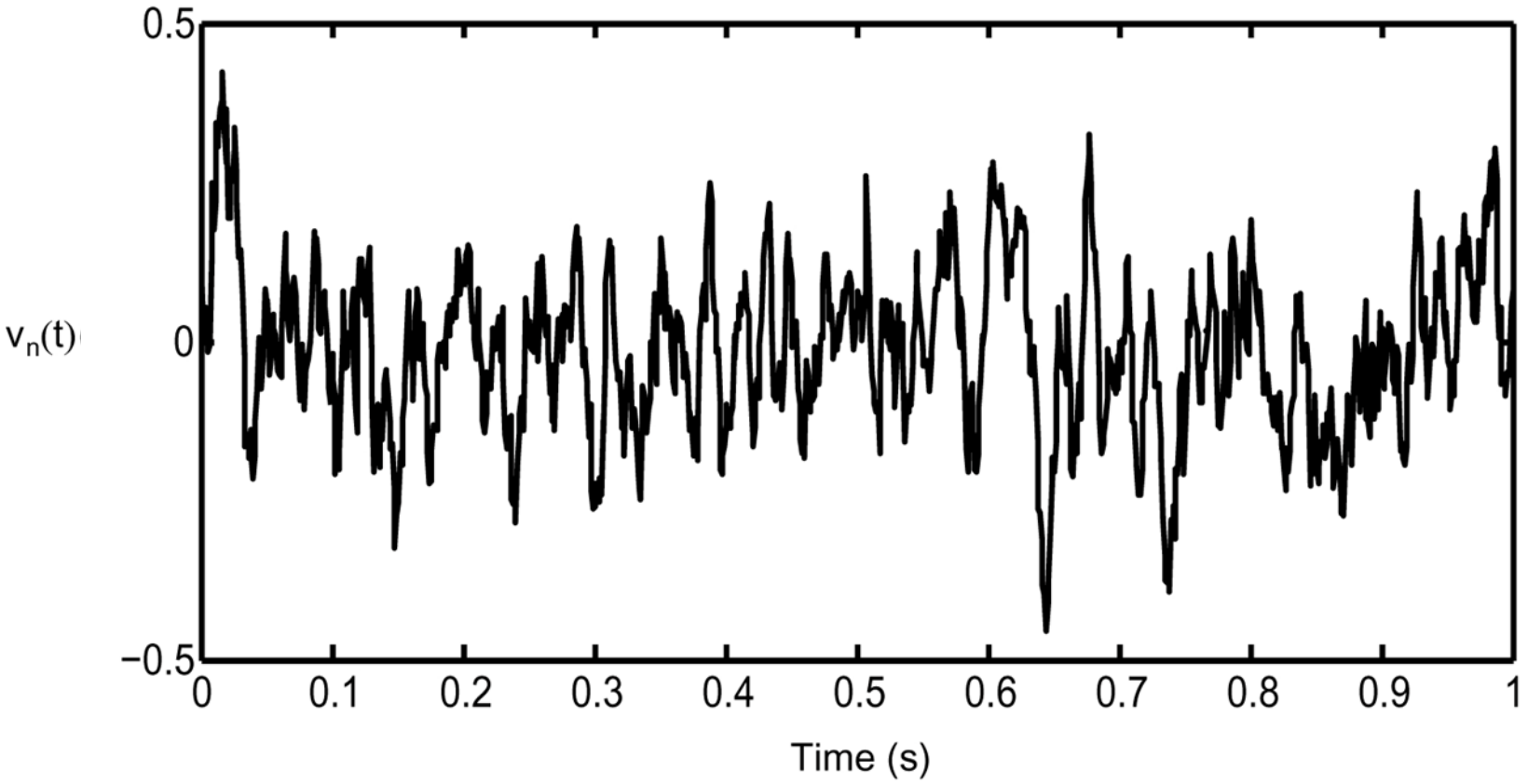
Physical Resistor





- "Thermal Noise" or "Johnson Noise"
  - J.B. Johnson, "Thermal Agitation of Electricity in Conductors," Phys. Rev., pp. 97-109, July 1928
- Can model random current component using a noise current source $i_n(t)$

Example Voltage Noise Waveform



Chan Carusone, p. 364

Properties of Thermal Noise

- Present in any conductor
- Independent of DC current flow
- Instantaneous noise value is unpredictable since it is a result of a large number of random, superimposed collisions with relaxation time constant $\tau_0 \cong 0.17$ps
  - Consequences:
    - Gaussian amplitude distribution (central limit theorem)
    - Knowing $i_n(t)$ does not help predict $i_n(t+\Delta t)$, unless Δt is on the order of 0.17ps (cannot sample signals this fast)
    - The power generated by thermal noise is spread up to very high frequencies ($1/\tau_0 \cong 6{,}000$Grad/s)
- The only predictable property of thermal noise is its average power!

Average Power

- For a deterministic current signal with period T, the average power is

$$P_{av} = \frac{1}{T} \int_{-T/2}^{T/2} i^2(t) \cdot R \cdot dt$$

- This definition can be extended to random signals
- Assuming a real, stationary and ergodic random process, we can write

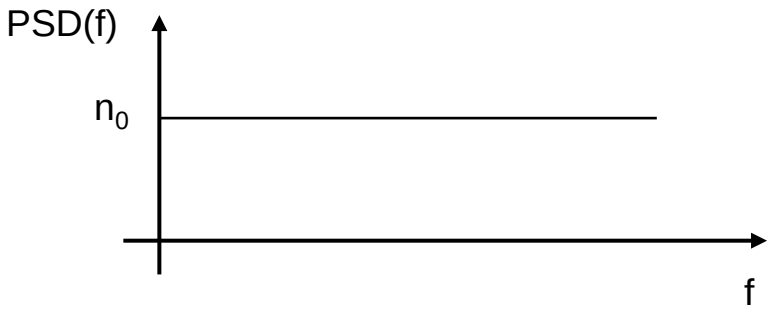
$$P_n = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{T/2} i_n^2(t) \cdot R \cdot dt$$

- For notational convenience, we typically drop R in the above expression and work with "mean square" currents (or voltages)

$$\overline{i_n^2} = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{T/2} i_n^2(t) \cdot dt$$

Thermal Noise Spectrum

- The so-called power spectral density (PSD) shows how the power is distributed across frequency
- In the case of thermal noise, the power is spread uniformly up to very high frequencies (about 10% drop at 2,000GHz)



- The total average noise power P_n in a particular frequency band is found by integrating the PSD

$$P_n = \int_{f_1}^{f_2} PSD(f) \cdot df$$

Thermal Noise Power

- Nyquist showed that the noise PSD of a resistor is

$$PSD(f) = n_0 = 4 \cdot kT$$

- k is the Boltzmann constant and T is the absolute temperature
- $4kT = 1.66 \cdot 10^{-20}$ Joules at room temperature
- The total average noise power of a resistor in a certain frequency band is therefore

$$P_n = \int_{f_1}^{f_2} 4kT \cdot df = 4kT \cdot (f_2 - f_1) = 4kT \cdot \Delta f$$

Equivalent Noise Generators

- We can model the noise using an equivalent voltage or current generator

$$\overline{v_n^2} = P_n \cdot R = 4kT \cdot R \cdot \Delta f$$

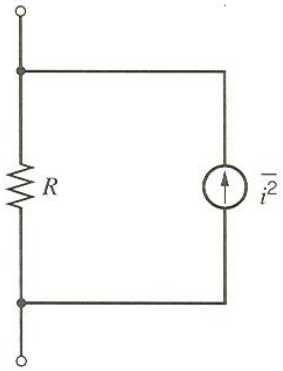
$$\overline{i_n^2} = \frac{P_n}{R} = 4kT \cdot \frac{1}{R} \cdot \Delta f$$

For $R = 1k\Omega$:

$$\frac{\overline{v_n^2}}{\Delta f} = 16 \cdot 10^{-18} \frac{V^2}{Hz}$$

$$\sqrt{\frac{\overline{v_n^2}}{\Delta f}} = 4nV / \sqrt{Hz}$$

$$\Delta f = 1MHz \Rightarrow \sqrt{\overline{v_n^2}} = 4\mu Vrms$$



For $R = 1k\Omega$:

$$\frac{\overline{i_n^2}}{\Delta f} = 16 \cdot 10^{-24} \frac{A^2}{Hz}$$

$$\sqrt{\frac{\overline{i_n^2}}{\Delta f}} = 4pA / \sqrt{Hz}$$

$$\Delta f = 1MHz \Rightarrow \sqrt{\overline{i_n^2}} = 4nArms$$

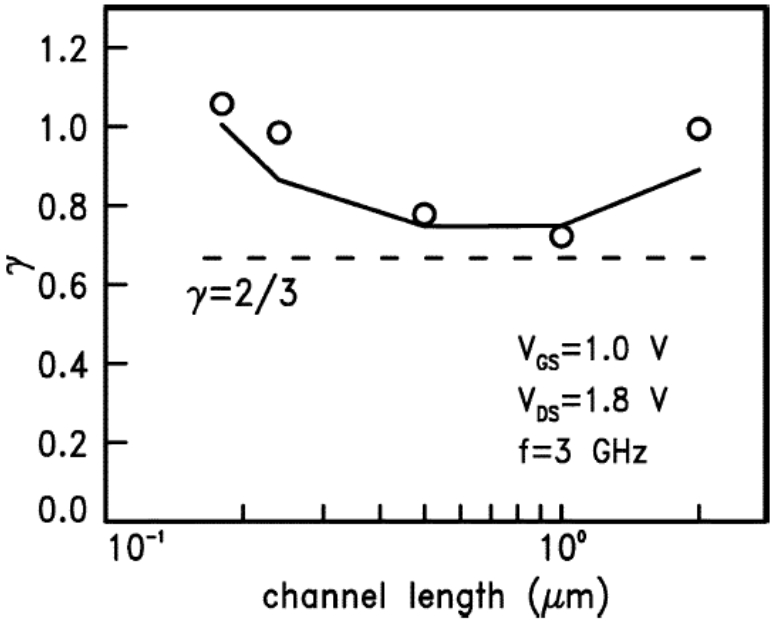
MOSFET Thermal Noise (1)

- The noise of a MOSFET operating in the triode region is approximately equal to that of a resistor
- In the saturation region, the thermal noise of a MOSFET can be modeled using a drain current source with spectral density

$$\overline{i_d^2} = 4kT \cdot \gamma \cdot g_m \cdot \Delta f$$

- For an idealized long channel MOSFET, it can be shown that $\gamma = 2/3$
- In short channel devices, γ is somewhat larger, typically 0.8…2

MOSFET Thermal Noise (2)

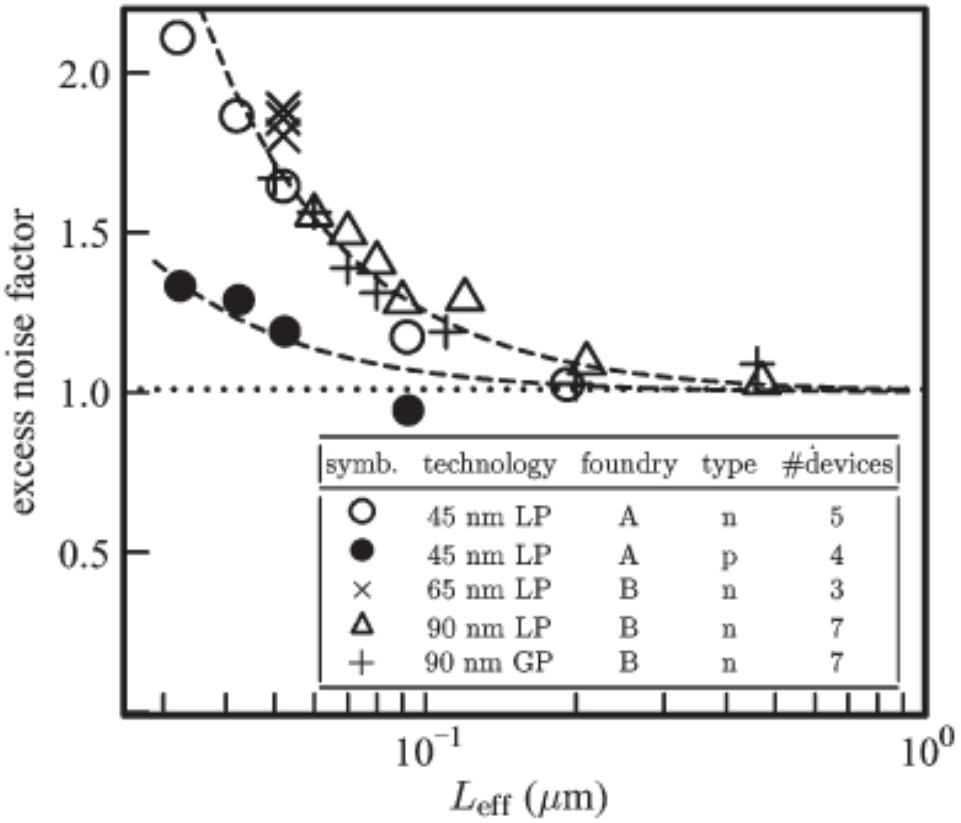


[Scholten, 2003]

- At moderate gate bias in strong inversion, the γ values for short-channel MOSFETS are slightly larger than 2/3
  - A. J. Scholten et al., "Noise modeling for RF CMOS circuit simulation," IEEE Trans. Electron Devices, pp. 618-632, Mar. 2003.
  - R. P. Jindal, "Compact Noise Models for MOSFETs," IEEE Trans. Electron Devices, pp. 2051-2061, Sep. 2006.

MOSFET Thermal Noise (3)

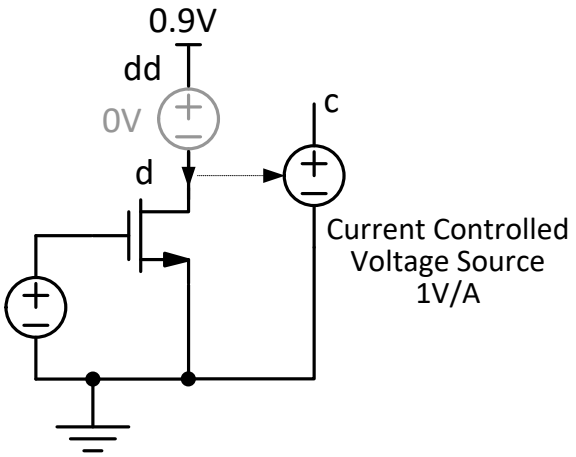
Measured γ relative to 2/3



G.D.J. Smit, A.J. Scholten, R.M.T. Pijper, R. van Langevelde, L.F. Tiemeijer, and D.B.M. Klaassen, "Experimental Demonstration and Modeling of Excess RF Noise in Sub-100-nm CMOS Technologies," IEEE Electron Device Letters, vol.31, no.8, pp. 884-886, Aug. 2010.

Extracting γ from a Spice Simulation (Generic Netlist)

```
vd      dd   0   0.9
vm      dd   d   0
vg      g    0   dc 0.7 ac 1
mn1     d    g   0   0   nch   L=0.18u W=10u
h1      c    0   ccvs   vm   1

.op
.ac dec 100 10k 1gig
.noise v(c) vg
```

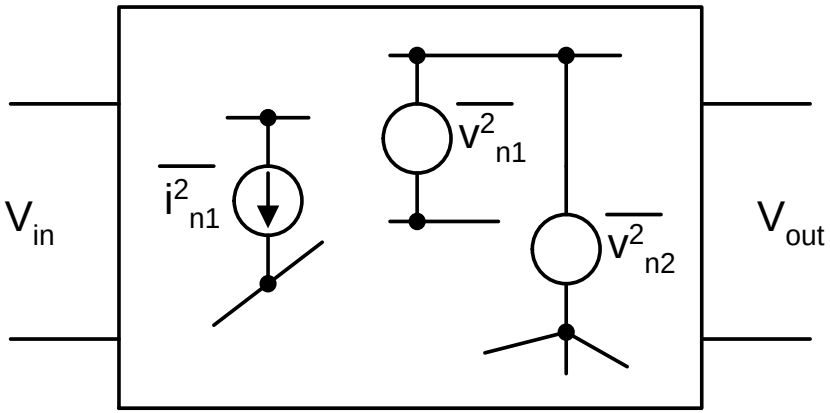


$$\gamma = \frac{\overline{i_d^2}/\Delta f}{4kTg_m}$$

From noise at node c

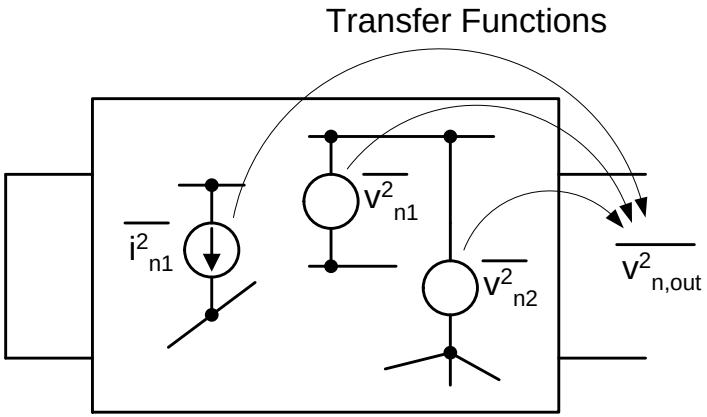
From operating point

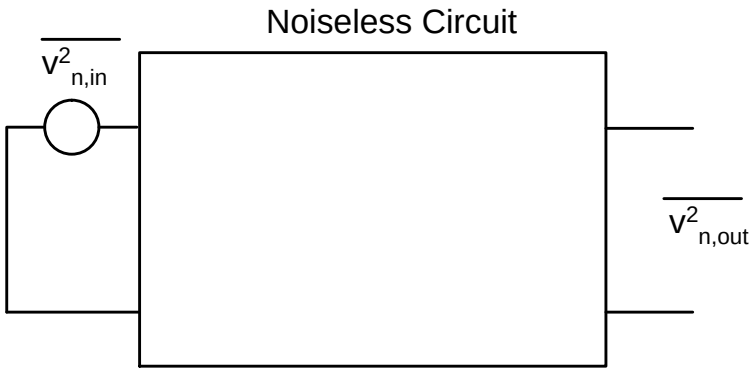
Noise in Circuits (1)



- Most circuits have more than one relevant noise source
- To quantify the net effect of all noise sources, we must refer the noise sources to a single "interesting" port of the circuit
  - Usually the output or input

Noise in Circuits (2)



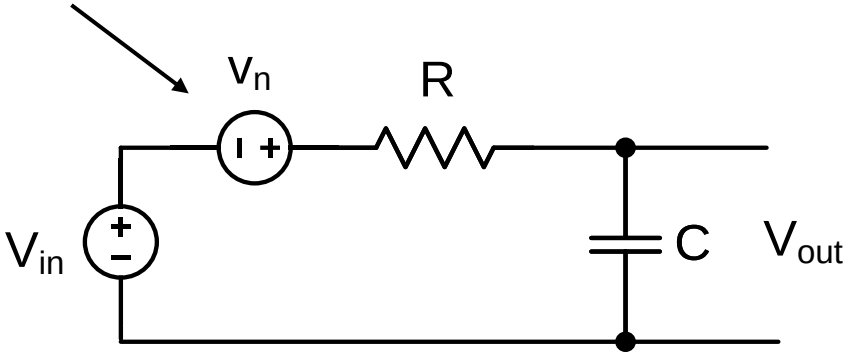


- Output referred noise
  - Refer noise to output via individual noise transfer functions
  - Physical concept, exactly what one would measure in the lab
- Input referred noise
  - Represent total noise via a fictitious input source that captures all circuit-internal noise sources
  - Useful for direct comparison with input signal

RC Lowpass Filter

Models resistor noise

$$\frac{\overline{v_n^2}}{\Delta f} = 4kTR$$



- Best to start by ignoring the fact that v_n is a noise source; treat it like any other signal that is injected into the circuit

$$v_{out} = \frac{1}{1 + j\omega RC} v_n = H(j\omega) \cdot v_n$$

Power Transfer Function

- The only thing we know about v_n is its power spectral density
- We can use the system's power transfer function to refer it to the output

$$\frac{\overline{v_{out}^2}}{\Delta f} = |H(j\omega)|^2 \cdot \frac{\overline{v_n^2}}{\Delta f}$$

$$|H(j\omega)|^2 = \left|\frac{1}{1+j\omega RC}\right|^2 = \frac{1}{1+(\omega RC)^2}$$

- The output noise power contained in a given frequency band is therefore

$$\overline{v_{out}^2} = \int_{f_1}^{f_2} \frac{4kTR}{1+(2\pi fRC)^2}\,df$$

Signal-to-Noise Ratio

- Assuming a sinusoidal signal with amplitude $\hat{V}_{out}$, we could now compute the SNR at the output of the circuit using

$$SNR = \frac{P_{signal}}{P_{noise}} = \frac{\frac{1}{2}\hat{V}_{out}^2}{\overline{v_{out}^2}}$$

- But, over which bandwidth should we integrate in the calculation of $\overline{v_{out}^2}$?
- Two interesting cases
  - The output is measured (or observed) by a system with finite bandwidth (e.g. human ear, or some other circuit with finite bandwidth)
    - Use frequency range of that system as integration limits
    - Applies on a case-by-case basis
  - Total integrated noise
    - Integrate noise from zero to “infinite” frequency
    - Means that the analyzed circuit limits the noise bandwidth
      - Not a bad assumption for a filter

Total Integrated Noise Calculation

$$\overline{v_{out,tot}^2} = \int_0^\infty \frac{4kTR}{1+(2\pi fRC)^2}\,df \qquad \int \frac{du}{1+u^2} = \operatorname{atan}(u)$$

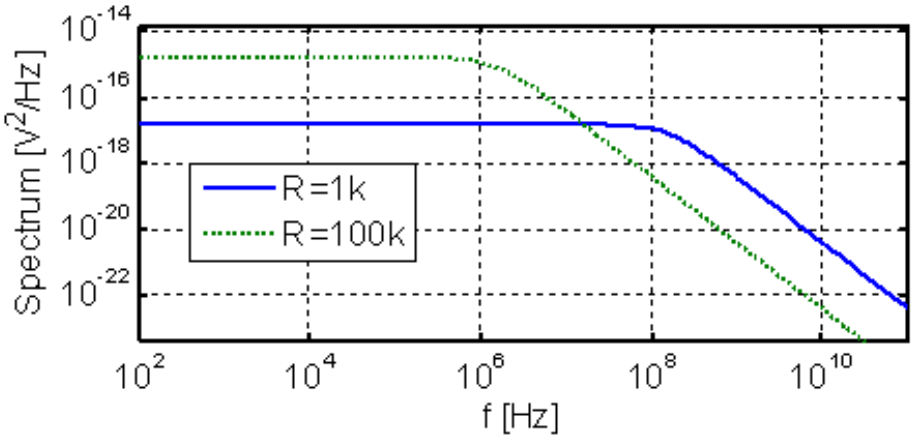
$$\overline{v_{out,tot}^2} = 4kTR\,\frac{1}{4RC}$$

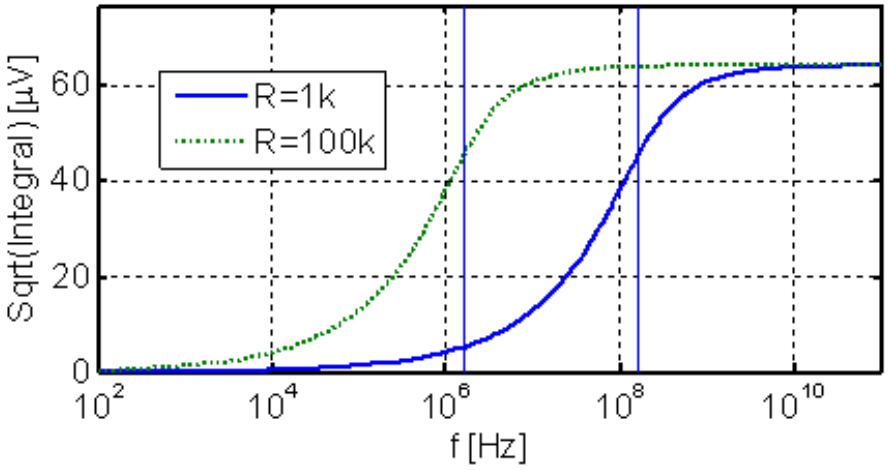
$$\overline{v_{out,tot}^2} = \frac{kT}{C}$$

- Interesting result
  - The total integrated noise at the output depends only on C, even though R is generating the noise

Effect of Varying R

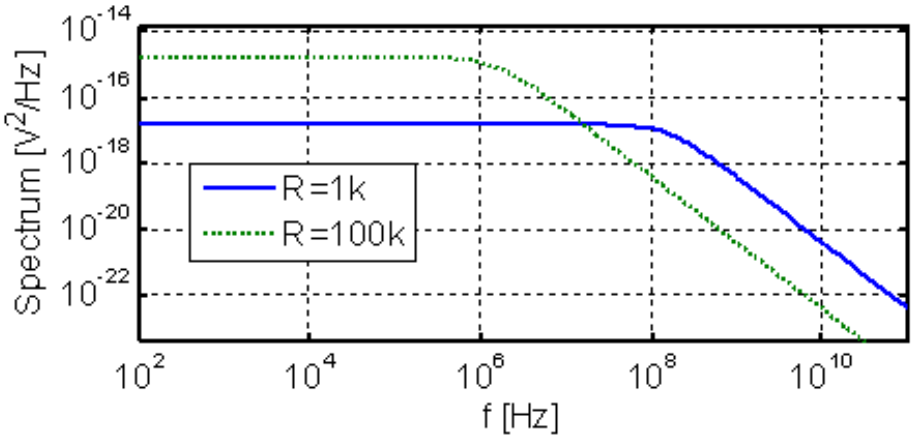
- Increasing R increases the noise power spectral density, but also decreases the bandwidth
  - R drops out in the end result
- For C = 1pF (example to the right), the total integrated noise is approximately 64μV_{rms}

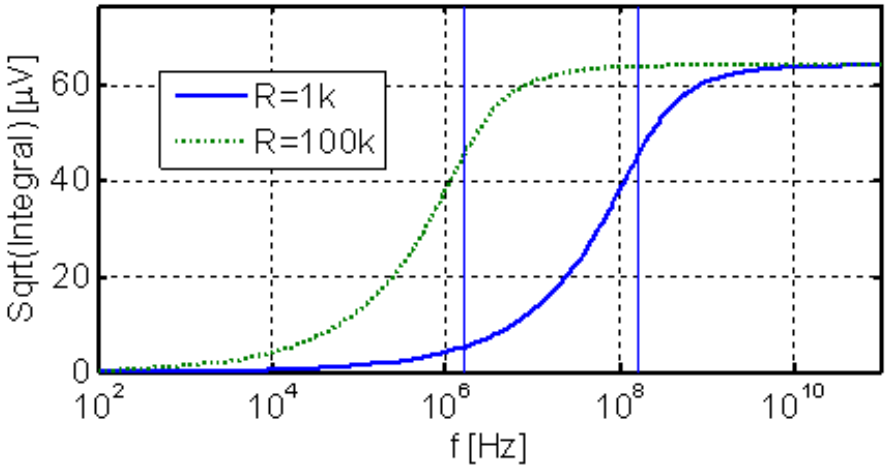




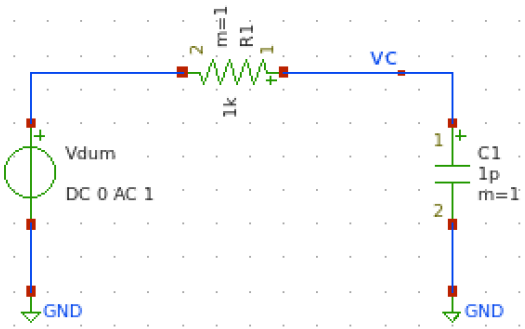
Aside: Integral Convergence

- Note that the noise integrals converge about 1-2 decades beyond the pole frequency
- This is useful info for simulations and numerical calculations





Test Schematic



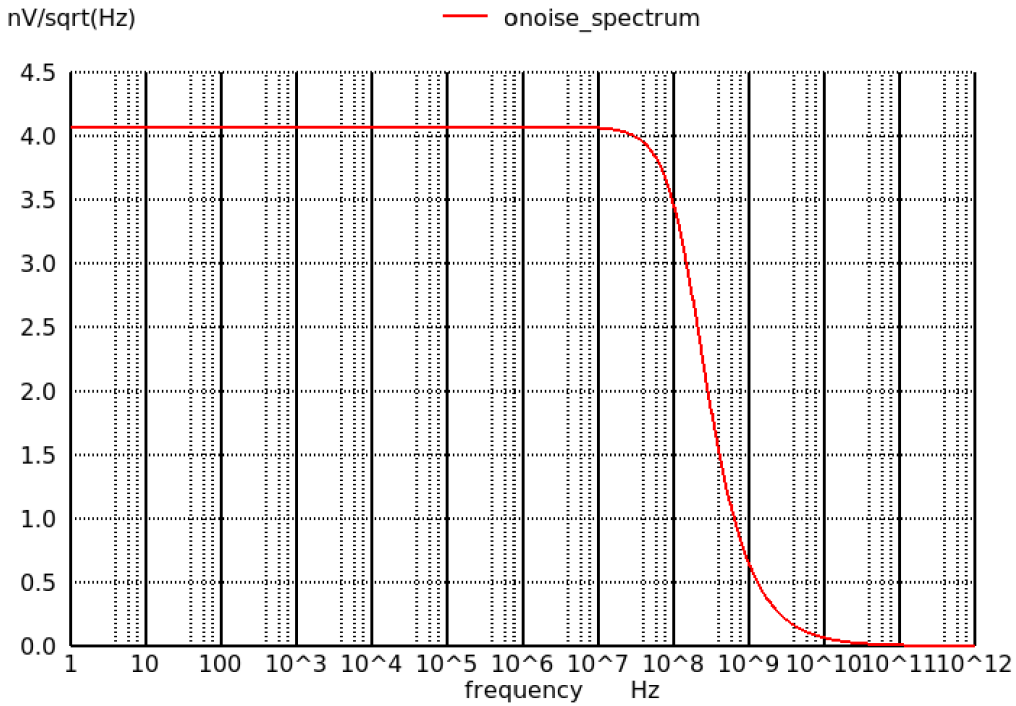
COMMANDS

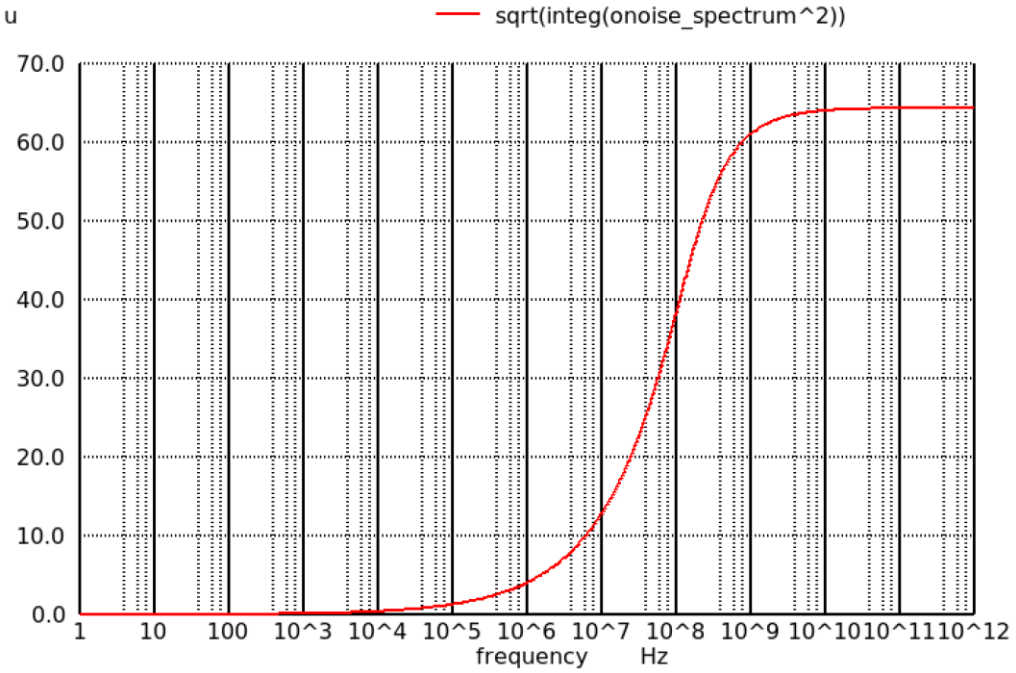
```
.param temp=27

.control
save all
noise v(vc) vdum dec 100 1 1000gig
print v(onoise_total)
set color0 = white
setplot noise1
plot onoise_spectrum
plot sqrt(integ(onoise_spectrum^2))
.endc
```

XSCHEM

Boris Murmann 2024-02-14 02:26:47

/foss/designs/tb_res_noise.sch


nV/sqrt(Hz)
onoise_spectrum
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
1
10
100
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^10
10^11
10^12
frequency
Hz


u
sqrt(integ(onoise_spectrum^2))
70.0
60.0
50.0
40.0
30.0
20.0
10.0
0.0
1
10
100
10^3
10^4
10^5
10^6
10^7
10^8
10^9
10^10
10^11
10^12
frequency
Hz

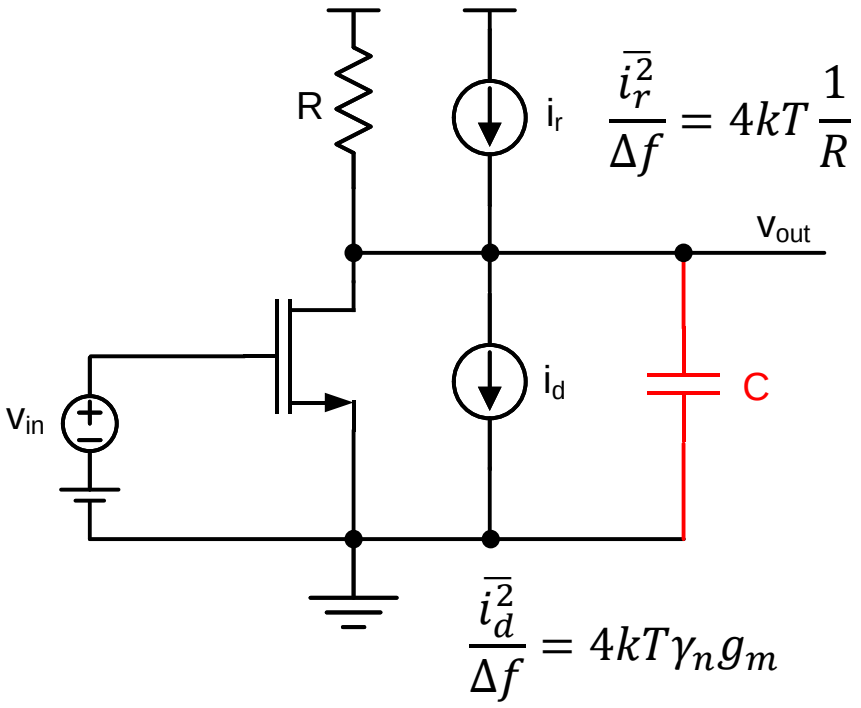
Alternative Derivation of kT/C

- The equipartition theorem states that each degree of freedom (or energy state) of a system in thermal equilibrium holds an average energy of kT/2
- In our circuit, the degree of freedom is the energy stored on the capacitor

$$\overline{\frac{1}{2}Cv_{out}^{2}} = \frac{1}{2}kT$$

$$\overline{v_{out}^{2}} = \frac{kT}{C}$$

Common-Source Stage with Load Capacitance

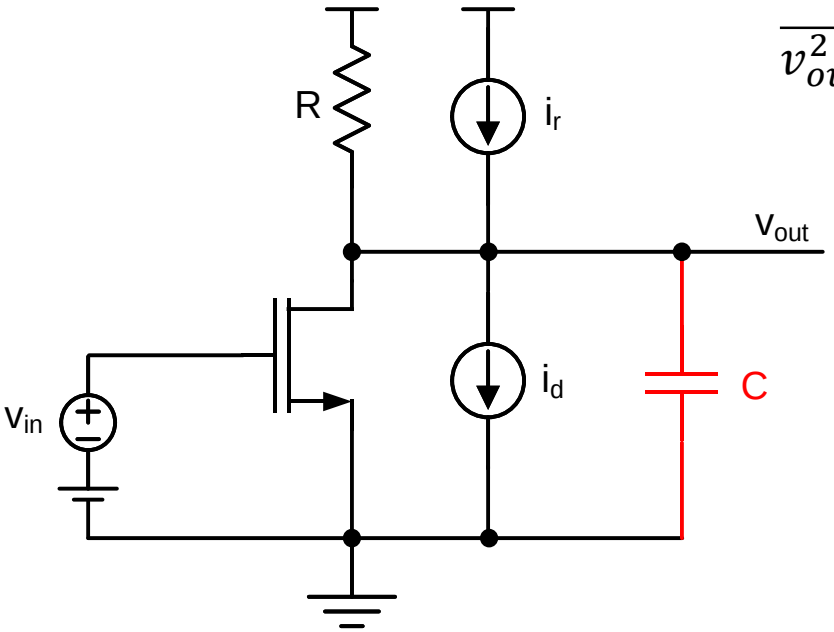


$$\overline{v_{out}^2} = \left(\frac{4kT}{R}\Delta f + 4kT\gamma_n g_m \Delta f\right)\left|R \| \frac{1}{j\omega C}\right|^2$$

$$\overline{v_{out}^2} = 4kTR\Delta f(1+\gamma_n g_m R)\left|\frac{1}{1+j\omega RC}\right|^2$$

- Noise currents drop into the parallel combination of R and C
- PSD is shaped by squared magnitude of first-order response

Total Integrated Noise



$$\overline{v_{out,tot}^2} = \int_0^\infty \underbrace{4kTR(1+\gamma_n g_m R)} \left|\frac{1}{1+j\omega RC}\right|^2 df$$

Was 4kTR in RC low-pass

$$\overline{v_{out,tot}^2} = 4kTR(1+\gamma_n g_m R)\cdot\frac{1}{4RC}$$

$$\overline{v_{out,tot}^2} = \frac{kT}{C}(1+\gamma_n g_m R)$$

- The noise is some multiple of kT/C
- The “1” in the bracket is the resistor’s contribution

Example SNR Calculation

- Assumptions
  - Output carries a sinusoid with 1V peak amplitude
  - We observe the output without significant band limiting and thus use the total integrated noise in the SNR expression

$$SNR = \frac{P_{signal}}{P_{noise}} = \frac{\frac{1}{2}\hat{V}_{out}^2}{\frac{kT}{C}(1+\gamma_n g_m R)} = \frac{0.5V^2}{\frac{kT}{100fF}(1+0.84\cdot 9.39)} = \frac{0.5V^2}{(606\mu V)^2}$$

$$SNR(dB) = 10\log_{10}\left(\frac{0.5V^2}{(606\mu V)^2}\right) = 58.3dB$$

- Typical system requirements
  - Audio: SNR ≅ 90-100dB
  - Video: SNR ≅ 50-60dB
  - Gigabit Ethernet Transceiver: SNR ≅ 30-35dB

Noise/Power Tradeoff

- Assuming that we're already using the maximum available signal swing, improving the SNR by 6dB means
  - Increase C by 4x
  - Decrease R by 4x to maintain bandwidth
  - Increase g_m by 4x to preserve gain
  - Increase current by 4x

- Bottom line
  - **Improving the SNR in a noise limited circuit by 6dB ("1bit") QUADRUPLES power dissipation!**

Does Thermal Noise Always Matter?

- Let's look at the SNR of the RC filer with a 1-V sinusoid applied, considering the total integrated noise (kT/C)

SNR [dB]	C [pF]
20	0.00000083
40	0.000083
60	0.0083
80	0.83
100	83
120	8300
140	830000

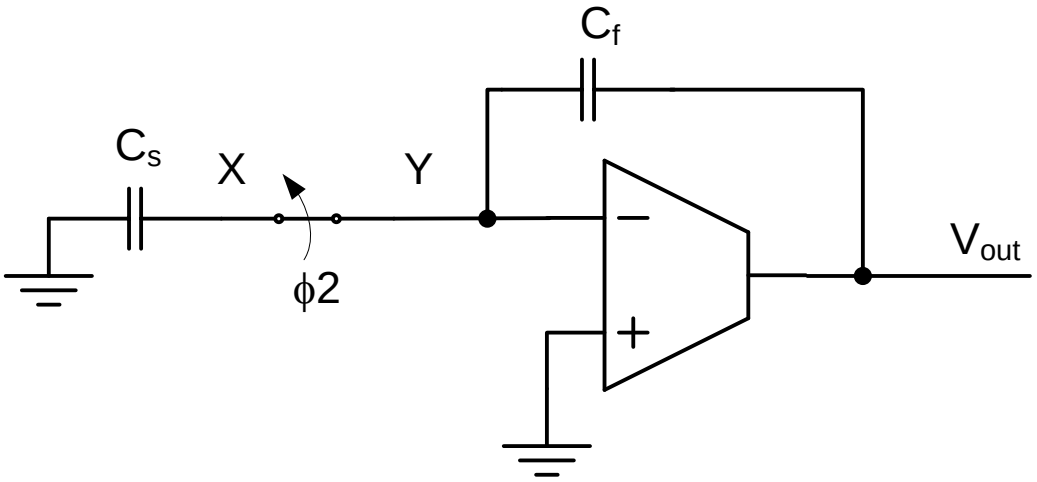
Hard to make such small capacitors…

Designer will be concerned about thermal noise; component sizes often set by SNR

A difficult battle with thermal noise …

- Rules of thumb
  - Up to SNR ~ 30-40dB, integrated circuits are usually not limited by thermal noise
  - Achieving SNR >100dB is extremely difficult
    - Must usually rely on external components, or reduce bandwidth and remove noise by a succeeding filter
    - E.g., oversampling ADCs

Input-Referred Noise of an SC Integrator



[Schreier, TCAS1, 2005]

- At the end of $\phi 2$, find noise charge left behind at node Y → can simulate

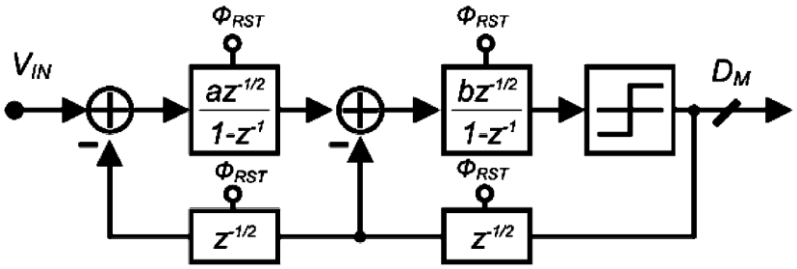
$$\overline{v_s^2} = \underbrace{\frac{kT}{C_s}}_{\phi 1} + \underbrace{\frac{kT}{C_s}\frac{1}{1+\frac{1}{x}} + \alpha\gamma\frac{kT}{C_s}\frac{1}{1+x}}_{\phi 2}$$

$$x = 2g_m R_{on}$$

(switch resistance)

$$\overline{v_s^2} \approx \frac{kT}{C_s} + \alpha\gamma\frac{kT}{C_s} \approx \frac{3kT}{C_s}$$

Input-Referred Noise of Complete Modulator



- Noise from second integrator is negligible (attenuated by first integrator)
- Decimation filter averages noise from M samples
- There is a penalty factor of 4/3 due to nonuniform impulse response of the decimation filter

$$\overline{v_n^2} = \overline{v_s^2} \sum_{i=1}^{M} w_i^2 < \overline{v_s^2} \frac{4}{3M}. \qquad (12)$$

Calculation of Required Integrator Noise and C_s

- Chae's design has an SNR of 66 dB

$$SNR(dB) = 10\log_{10}\left(\frac{\frac{1}{2}(0.3V)^2}{\overline{v_n^2}}\right) = 66dB \qquad \overline{v_n^2} = (106\mu V)^2$$

- Resulting integrator noise spec

$$\overline{v_s^2} = (106\mu V)^2\frac{3M}{4} = (106\mu V)^2\frac{3\times 110}{4} = (963\mu V)^2$$

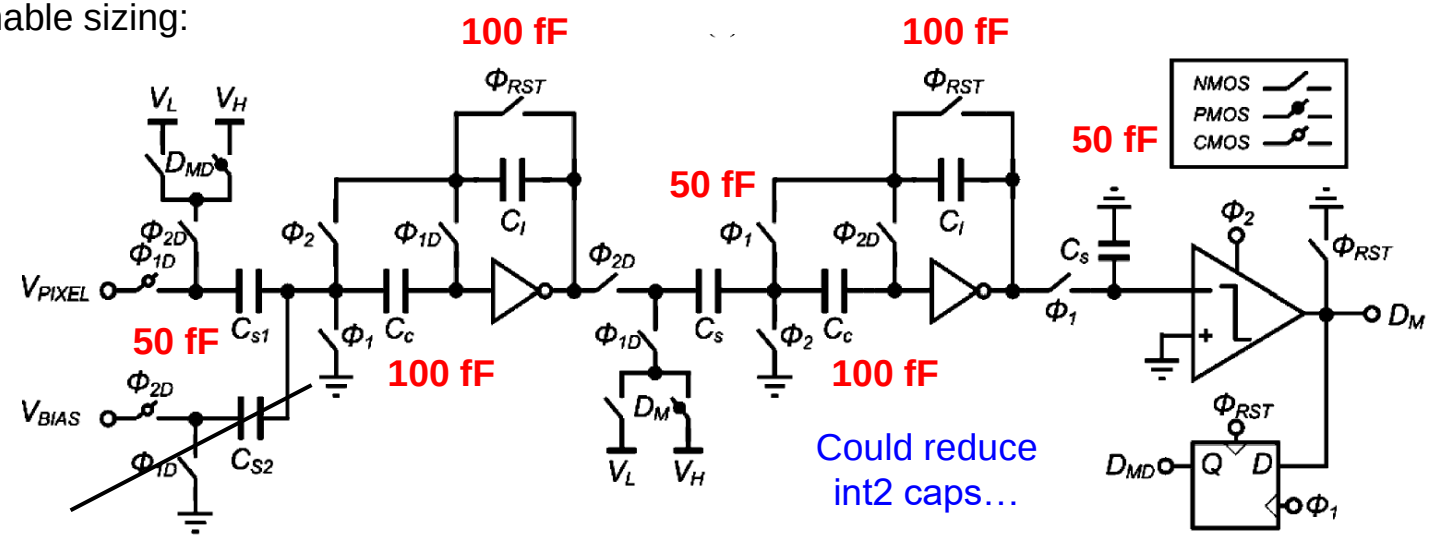
- Sampling capacitor size of first integrator

$$\overline{v_s^2} = (963\mu V)^2 = 3\frac{kT}{C_s} \qquad \boxed{C_s = 14fF}$$

Reality Check

modulator. The first sampling capacitor of the ΔΣ ADC can be much smaller than Nyquist ADC, because the multiple sampling reduces kT/C noise of the sampling capacitor. Details of noise analysis are provided in Section IV. This property is very helpful to minimize the area of an ADC. The total capacitance of the ΔΣ modulator is only 0.55 pF.

Reasonable sizing:



Inverter Sizing Re-Visited

- The example design by Chae is clocked at 48 MHz
- One half clock cycle is 10.4 ns
- Allow settling for 7 time constants → τ = 10.4 ns/7 = 1.5 ns
- If C_L ~ 150 fF (w/ parasitics), we need r_{out} < 1.5 ns/150 fF = 10 kΩ
- $g_{mn}+g_{mp}$ > 1/ 10 kΩ / (2/3) = 150 uS

- The transconductance of the previously simulated inverter (N = 2.5/1.5, P = 10/1.5) is about 330 uS
- We could cut this inverter in half and should still be fine…