Guard Rings

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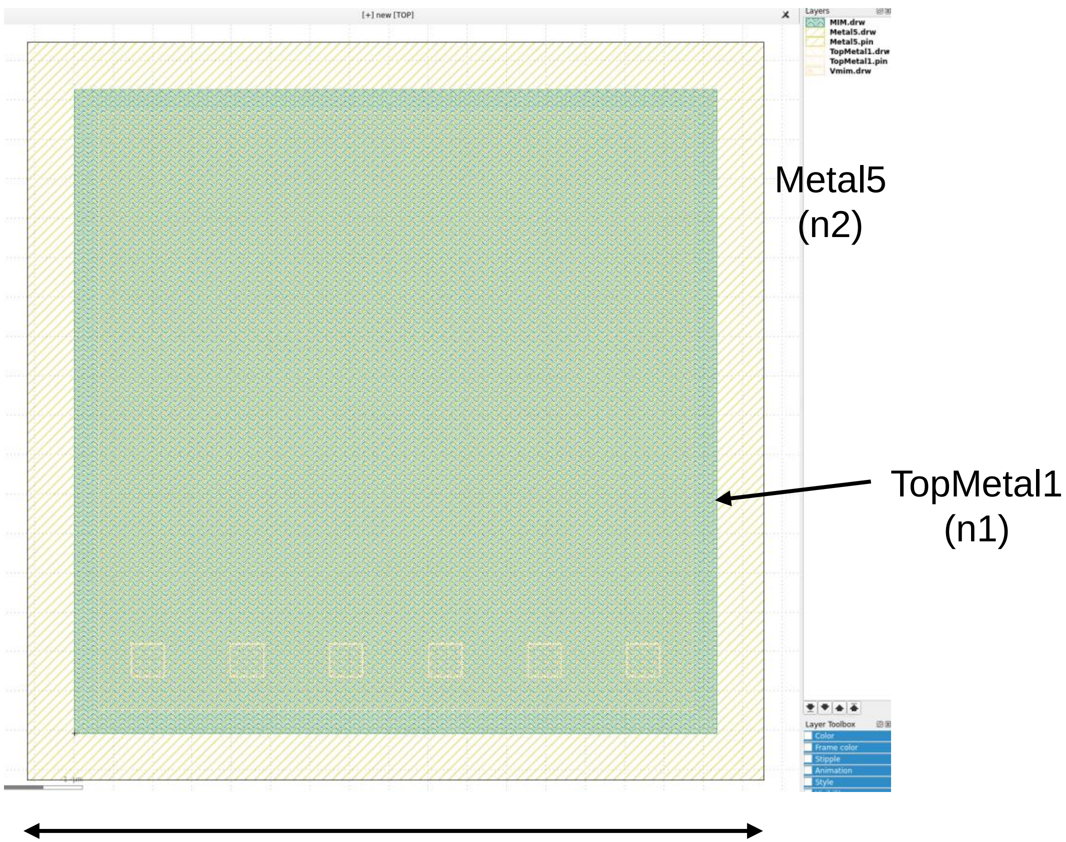
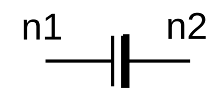
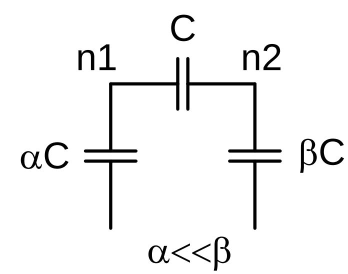
100 fF MIM Capacitor

$$w = l = \sqrt{\frac{100fF}{1.5fF/\mu m^2}} = 8.165\mu m$$



$$9.365\mu m \quad (\sim 10\mu m)$$





How big is βC?

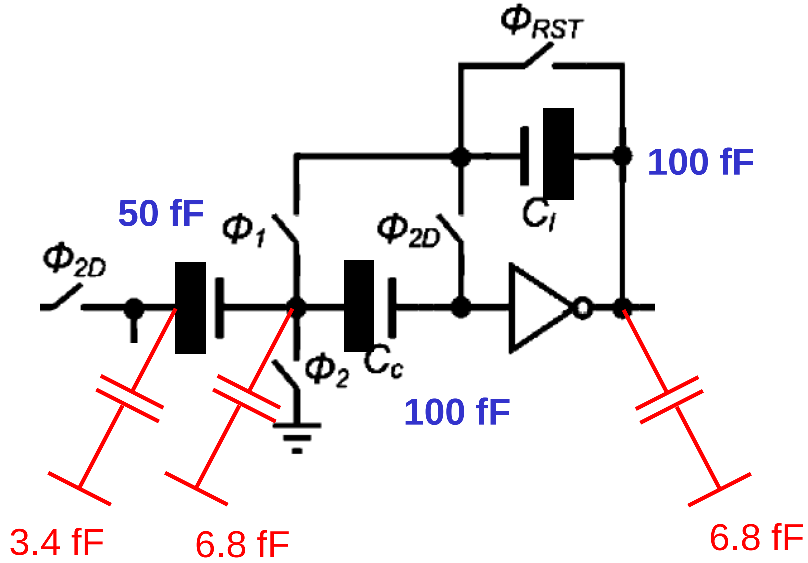
2.17 Parasitic Capacitances

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Metal1 - Activ Area Capacitance	CAMET1ACT	aF/µm²	**49**	**59**	**69**	A.aq	A = 250·1200 µm²
Metal1 - Substrate Area Capacitance	CAMET1SUB	aF/µm²	**31**	**37**	**43**	A.aq	A = 250·1200 µm²
Metal1 - Metal2 Area Capacitance	CAMET1/2	aF/µm²	**54**	**68**	**82**	A.aq	A = 250·1200 µm²
Metal2 - Metal3 Area Capacitance	CAMET2/3	aF/µm²	**54**	**68**	**82**	A.aq	A = 250·1200 µm²
Metal3 - Metal4 Area Capacitance	CAMET3/4	aF/µm²	**54**	**68**	**82**	A.aq	A = 250·1200 µm²
Metal4 - Metal5 Area Capacitance	CAMET4/5	aF/µm²	**54**	**68**	**82**	A.aq	A = 250·1200 µm²
TopMetal1 - Metal5 Area Capacitance	CATOPMET1	aF/µm²	**36**	**42.5**	**49**	A.aq	A = 250·1200 µm²
TopMetal2 - TopMetal1 Area Capacitance	CATOPMET2	aF/µm²	**10**	**13**	**16**	A.aq	A = 250·1200 µm²

$$10\mu m \times 10\mu m \times 68\frac{aF}{\mu m^2} = 6.8fF \qquad \beta \approx 6.8\%$$

https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_process_spec.pdf

Simulation Check to Perform



Guard Rings

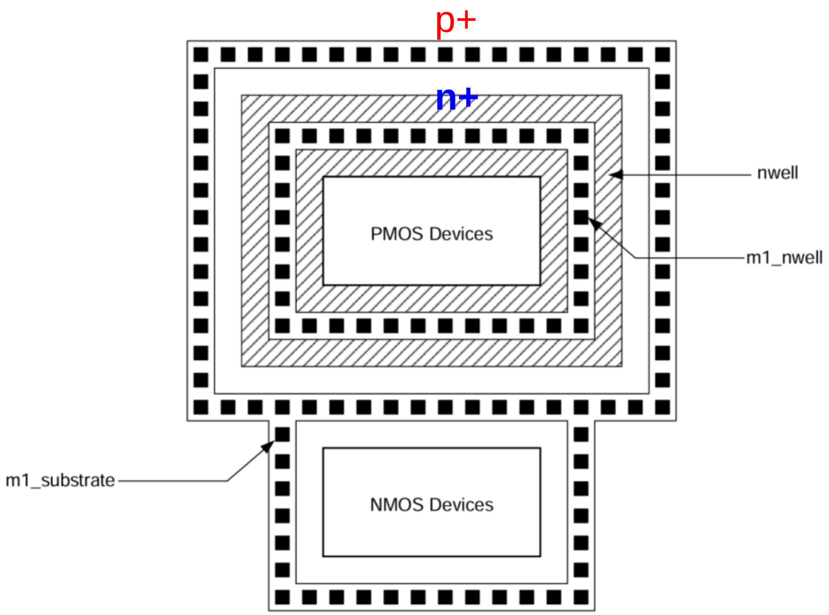
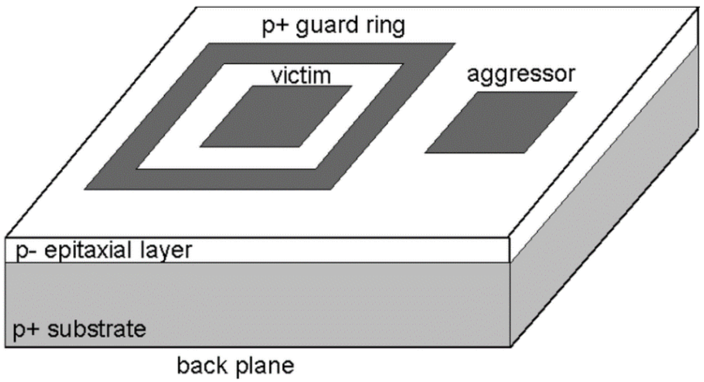


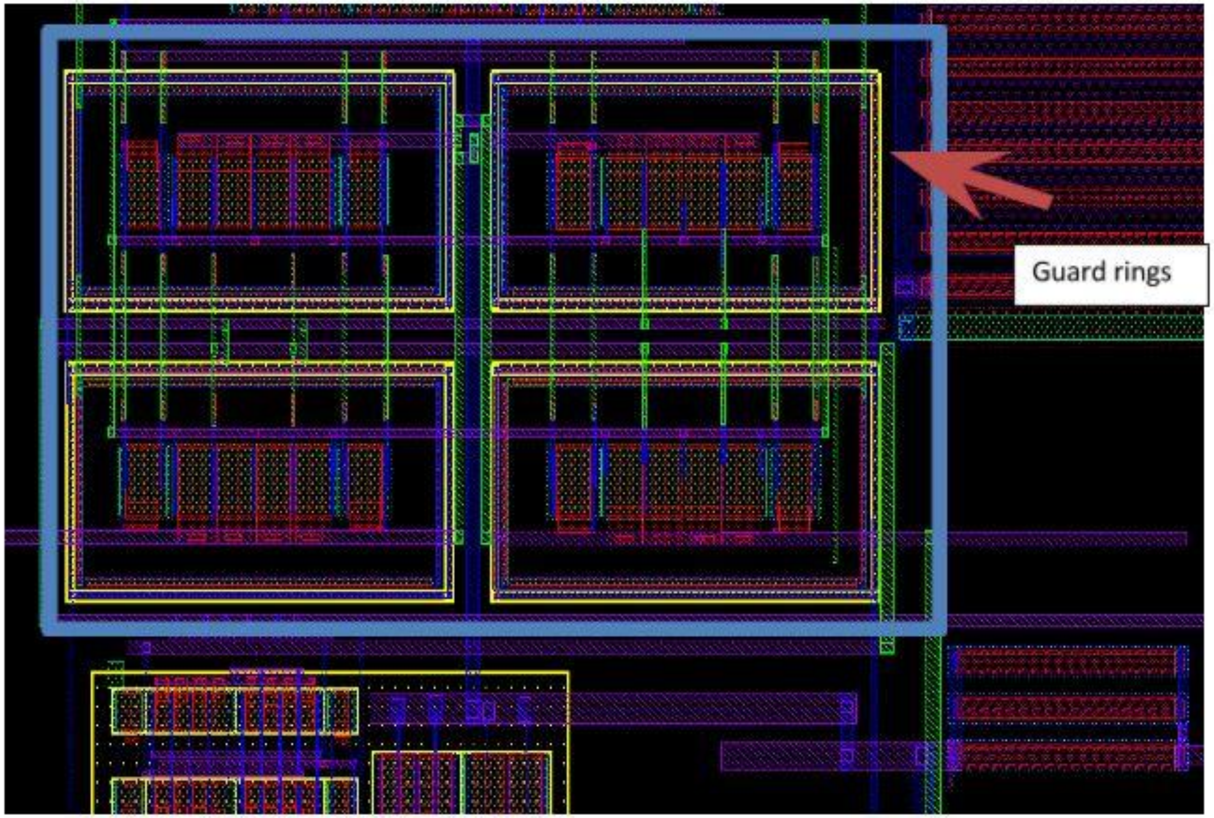
Figure 3-1: Guard Ring Illustration

[Sam Palermo]

- Prevent latch-up
- Isolate sensitive blocks
  - Guard rings collect majority or minority carriers in the substrate so that they don't reach sensitive devices



Example



https://www.ee.columbia.edu/~kinget/EE6350_S16/06_TEMPSENS_Sukanya_Vani/layout.html

Latch-Up

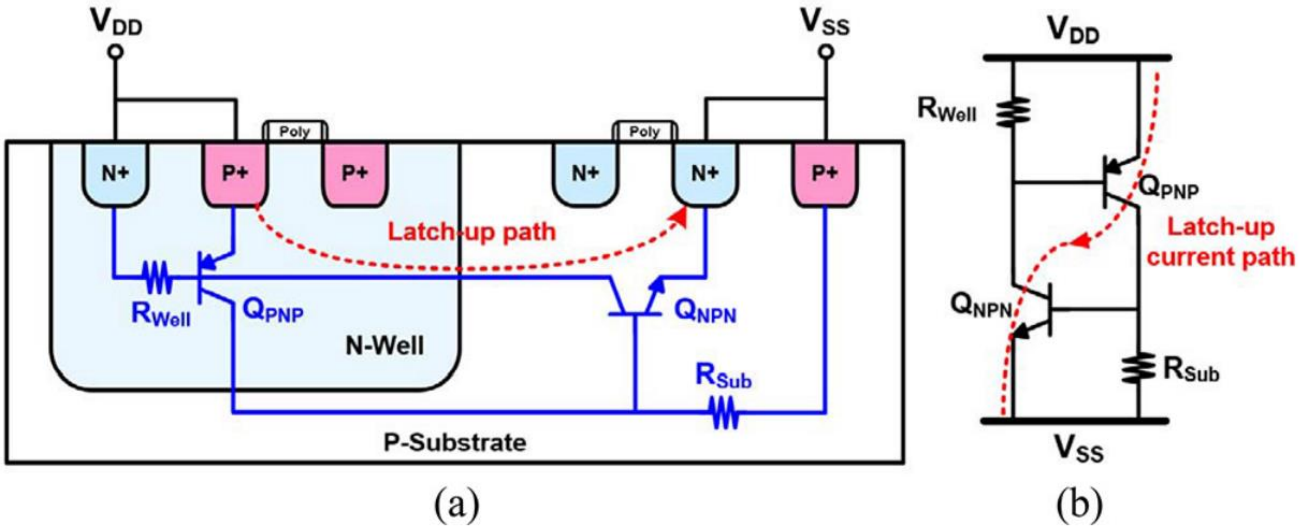


Fig. 1. (a) Device cross-sectional view and (b) equivalent circuit of traditional latch-up structure in a p-substrate bulk CMOS technology.

https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8714051

Take-Homes for EE 628

- Having proper well/substrate taps is important in analog design
  - The DRC checks for some of this

- Adding massive guard rings is a bit of a black art and may backfire if you don’t know what you’re doing

- Our design is not very large or sensitive
  - There is also no major aggressor (like a digital processor)

- We can go light on guard rings in the layout of our core circuitry
  - Just make sure you have solid taps across the substrate/wells

- We’ll certainly have full-fledged guard rings mainly in the I/O cells
  - For latch-up mitigation (we’ll talk about I/O cells later)