Finishing Up

Boris Murmann

bmurmann@hawaii.edu

Pull Request Contents

EE628/5_Design/4_Layout/Team X

TeamX.oas → Top level layout, contains all layout cells

TeamX.spice → Top level spice netlist for LVS

TeamX_sim.spice → Top level spice netlist for simulation

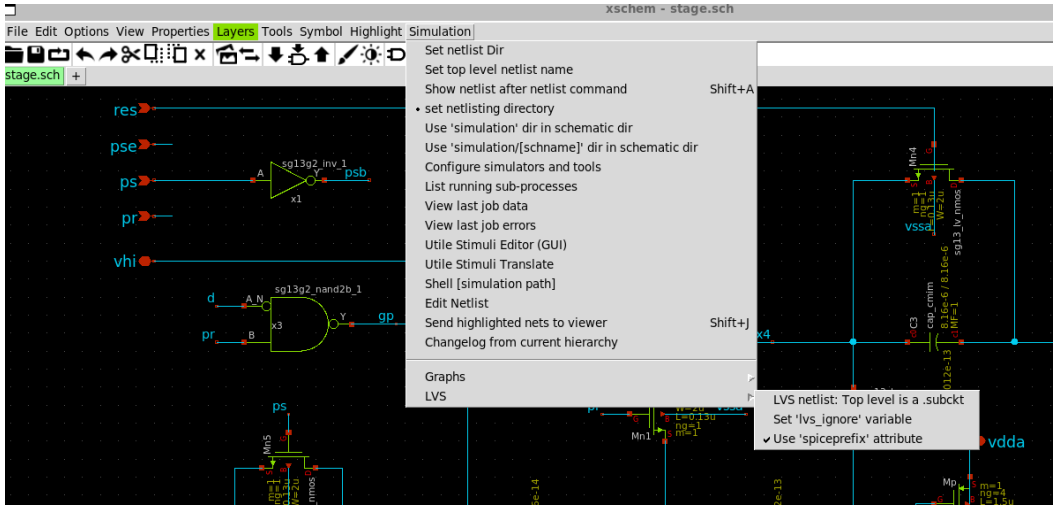
TeamX.sym → Top level symbol

TeamX.readme → Pin list + any notes you want to convey

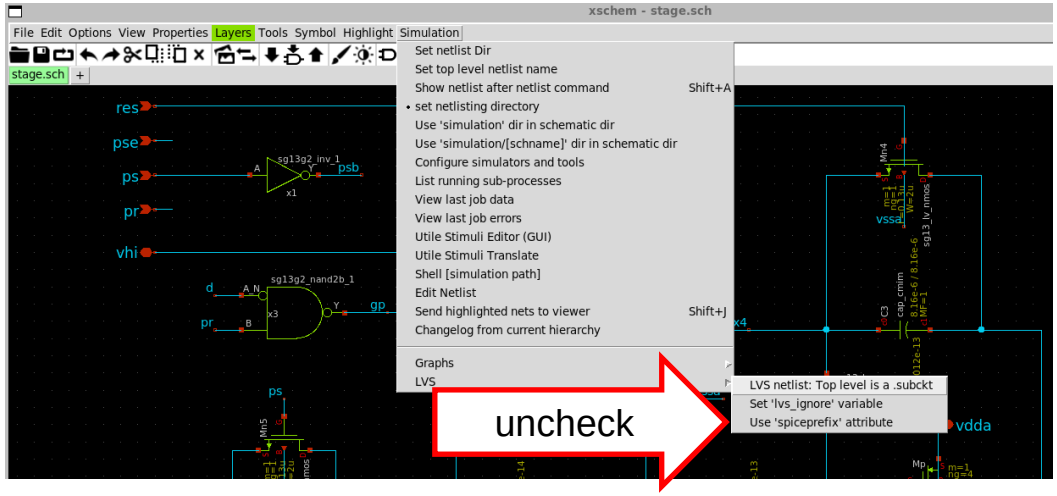
TeamX_logo.oas → In case you want to include a logo

Netlist Creation

For simulation (default):



For LVS:

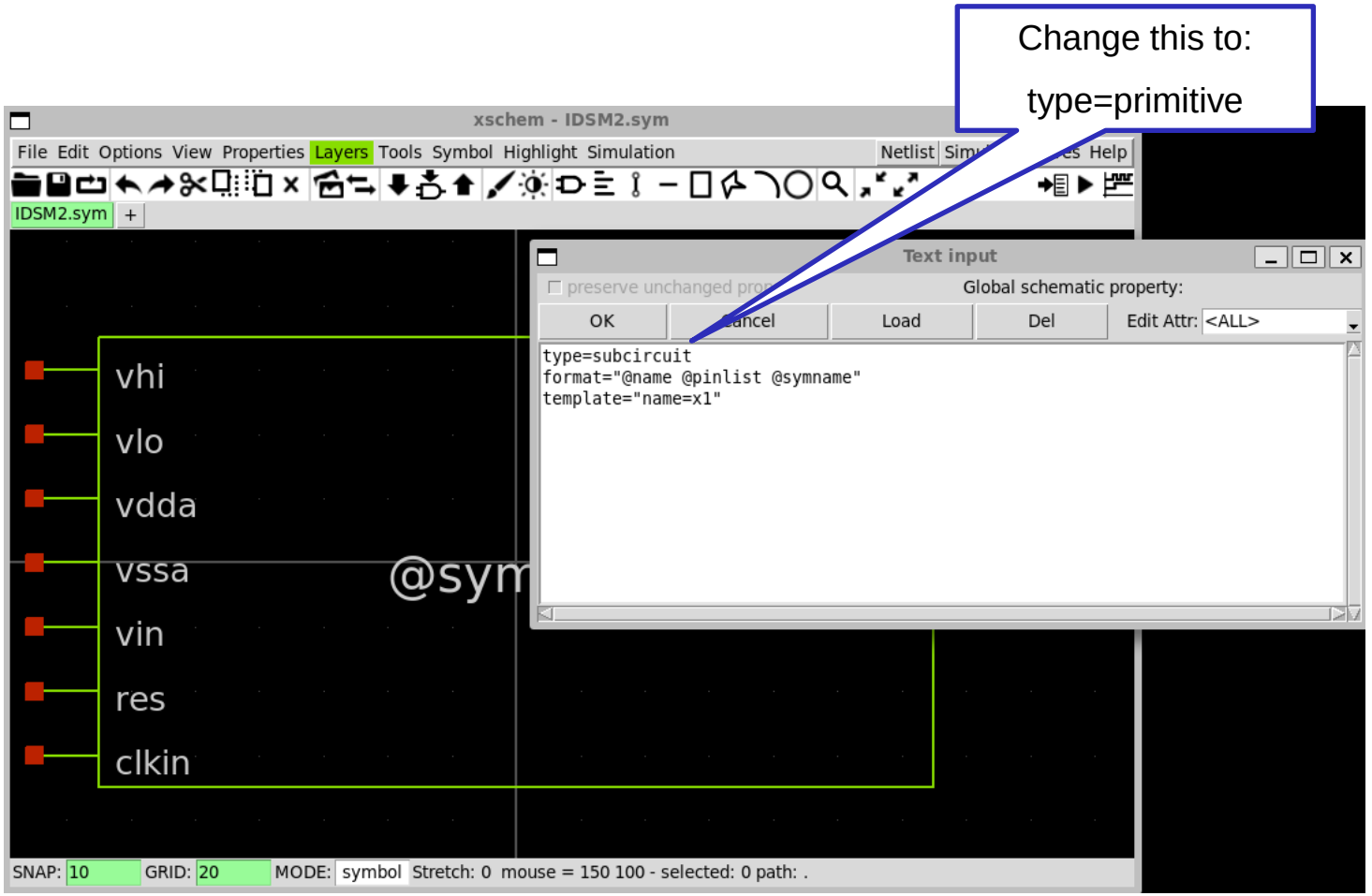


Netlist Examples

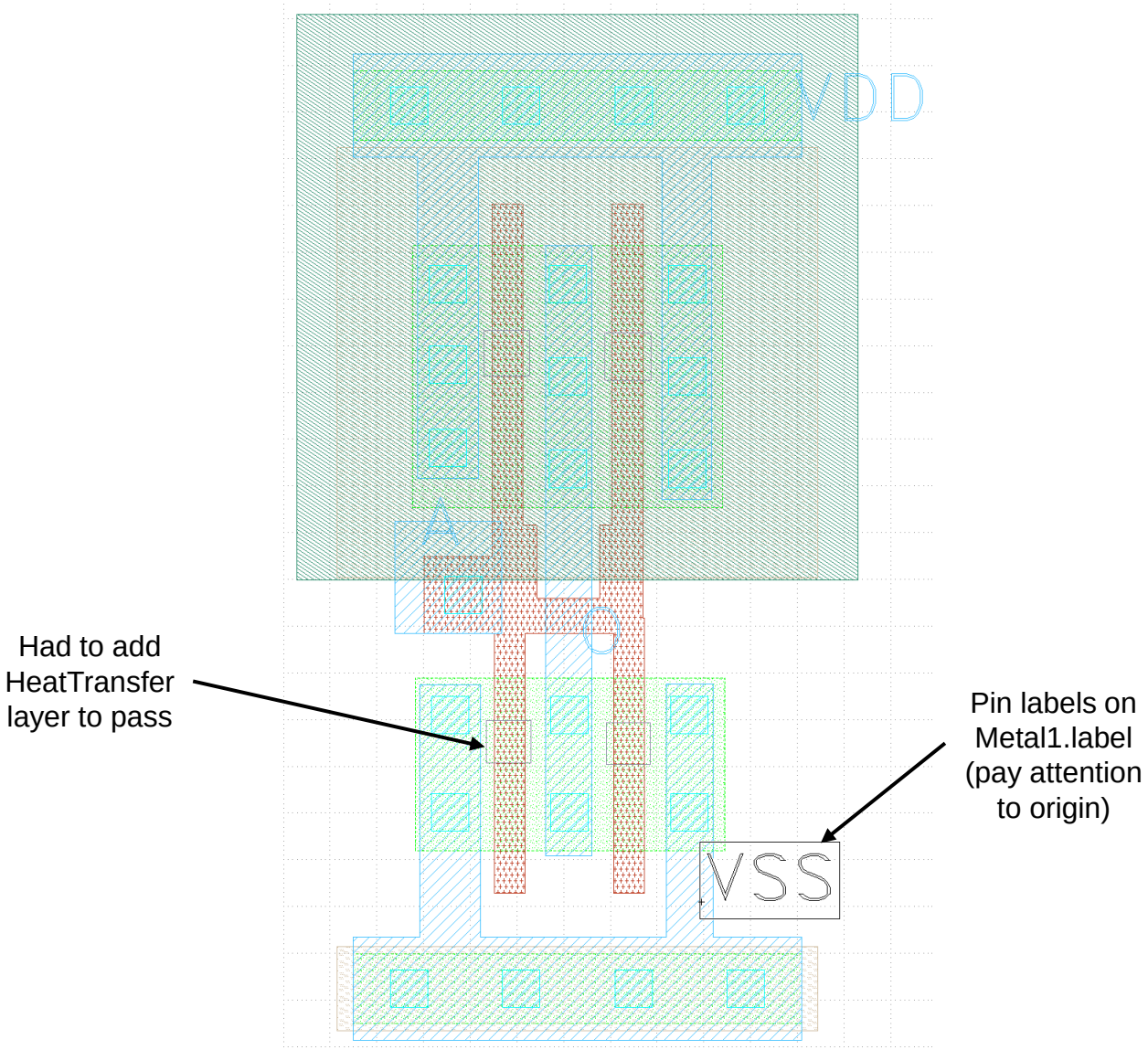
```
* For simulation
.subckt my_inv A VDD VSS Y
XX1 Y A VSS VSS sg13_lv_nmos w=740.00n l=130.00n ng=1 m=2
XX0 Y A VDD VDD sg13_lv_pmos w=1.12u l=130.00n ng=1 m=2
.ends


* For LVS
.subckt my_inv A VDD VSS Y
MX1 Y A VSS VSS sg13_lv_nmos w=740.00n l=130.00n ng=1 m=2
MX0 Y A VDD VDD sg13_lv_pmos w=1.12u l=130.00n ng=1 m=2
.ends
```

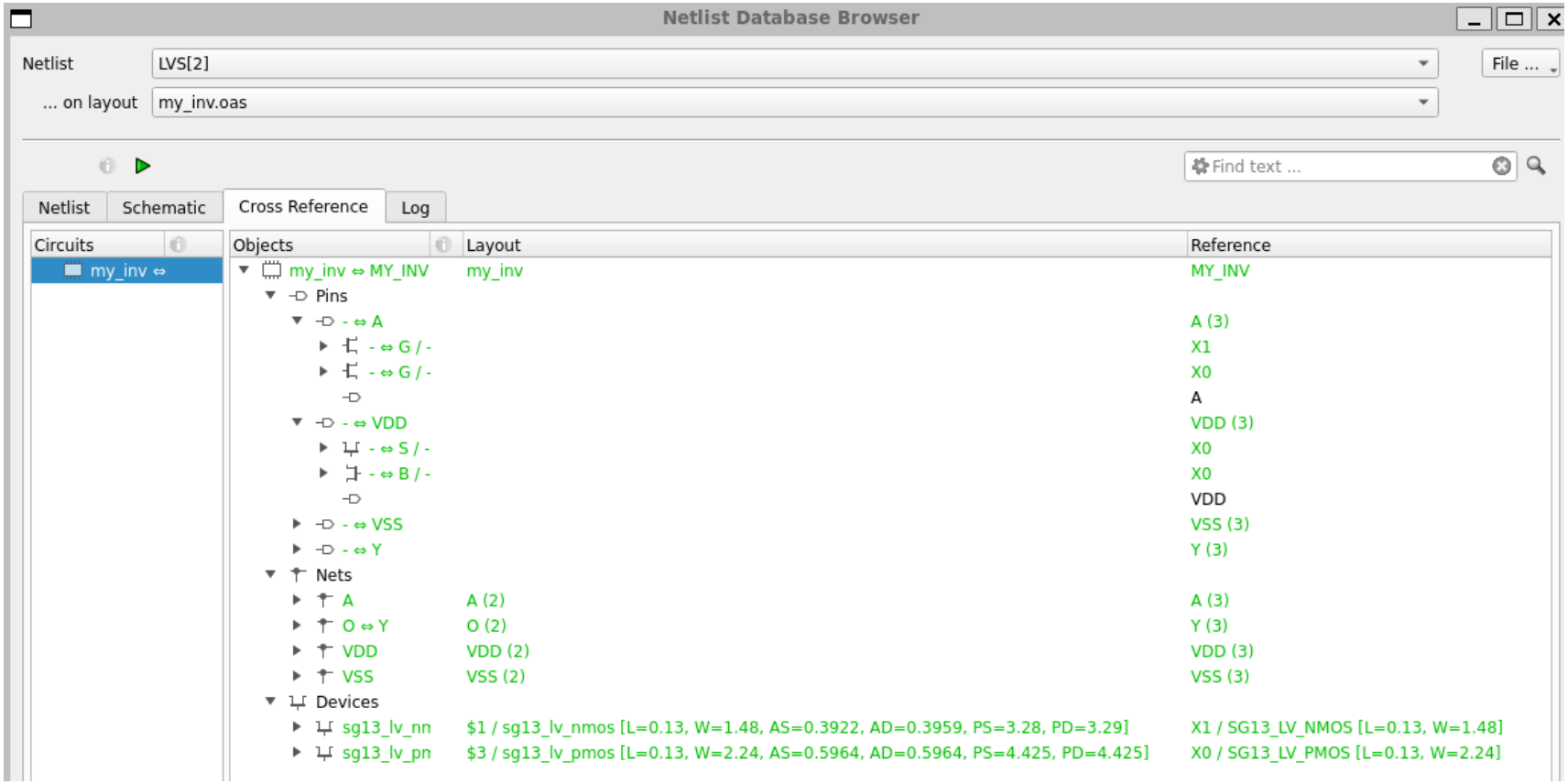
Your Top-Level Symbol



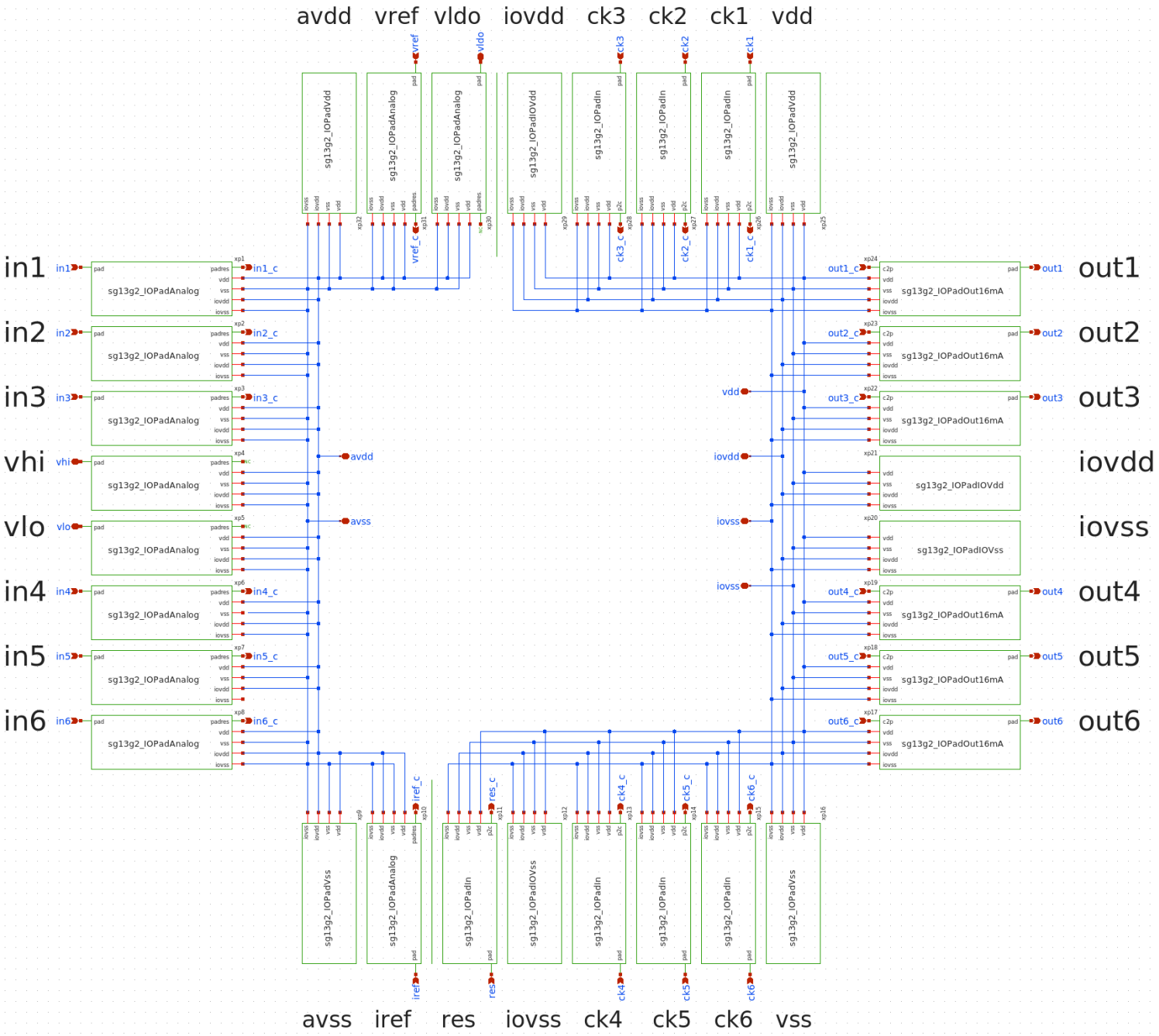
LVS with Standard Cell Inverter



LVS Output



- Be sure to check option “devices combine”
- Click on nets and devices to visualize them in the layout

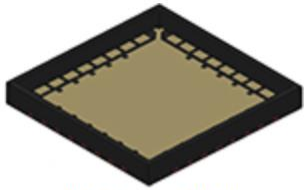


XSCHEM Boris Murmann 2024-04-24 05:39:39
/foss/designs/EE628/5_Design/3_Real_circuits/padring.sch

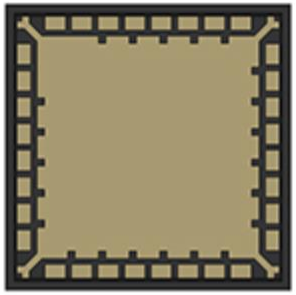
Tentative Package

M-QFN32W.65 Open Cavity

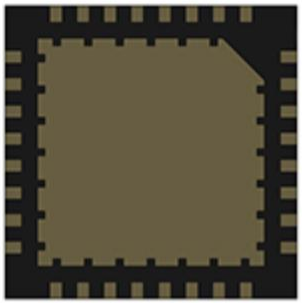
Click Images to Enlarge



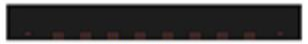
Perspective View
32L 7x7mm
Pitch 0.65mm



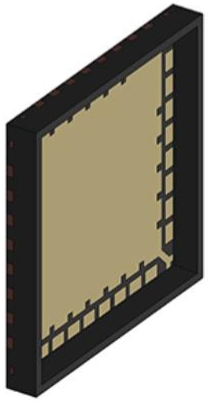
Top Cavity
32L 7x7mm
Pitch 0.65mm



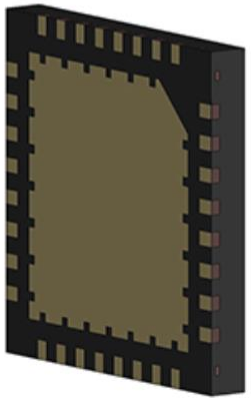
Bottom View
32L 7x7mm
Pitch 0.65mm



Edge View
32L 7x7mm
Pitch 0.65mm



Cavity View
32L 7x7mm
Pitch 0.65mm



Bottom View
32L 7x7mm
Pitch 0.65mm

https://www.mirrorsemi.com/M-QFN32W.65.html

Bonding Diagram (To Be Completed)