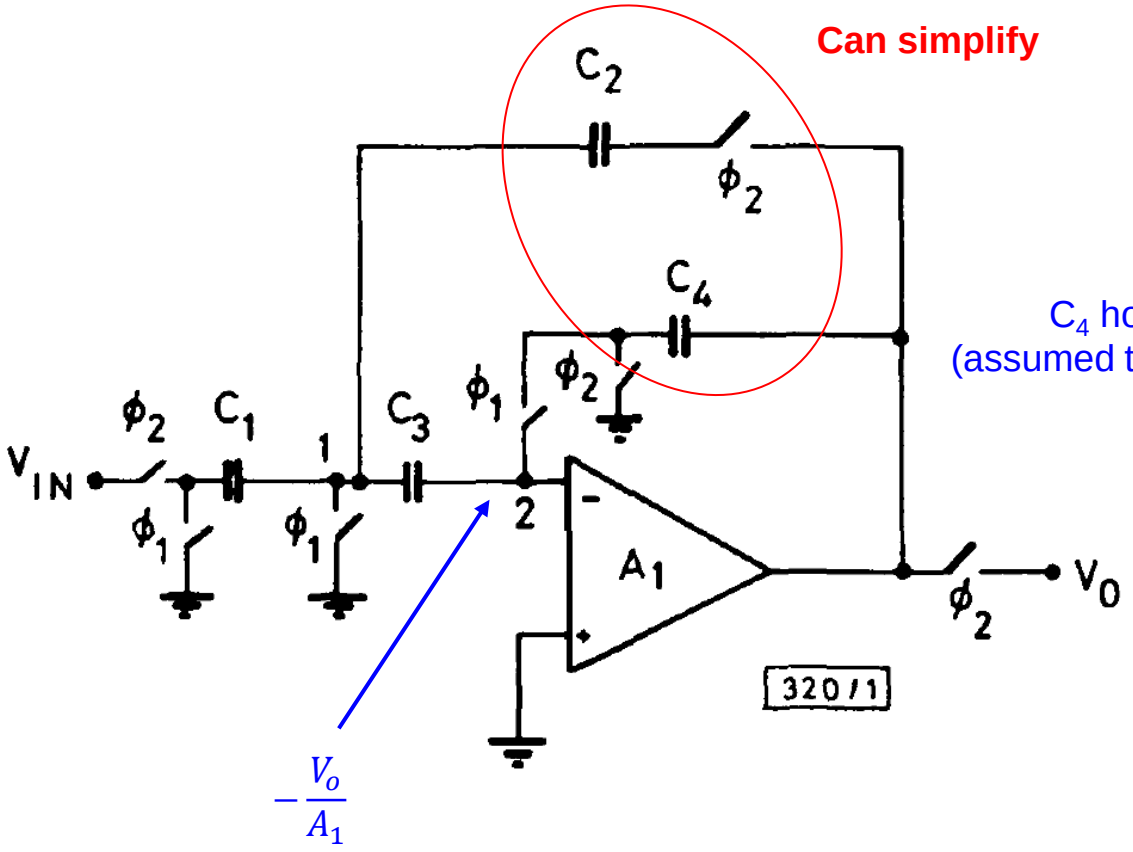
Amplifier

Boris Murmann

bmurmann@hawaii.edu



C_4 holds previous output
(assumed to be close to next output)

Stored on C3 during ϕ1

Technique Used in Our Template Design

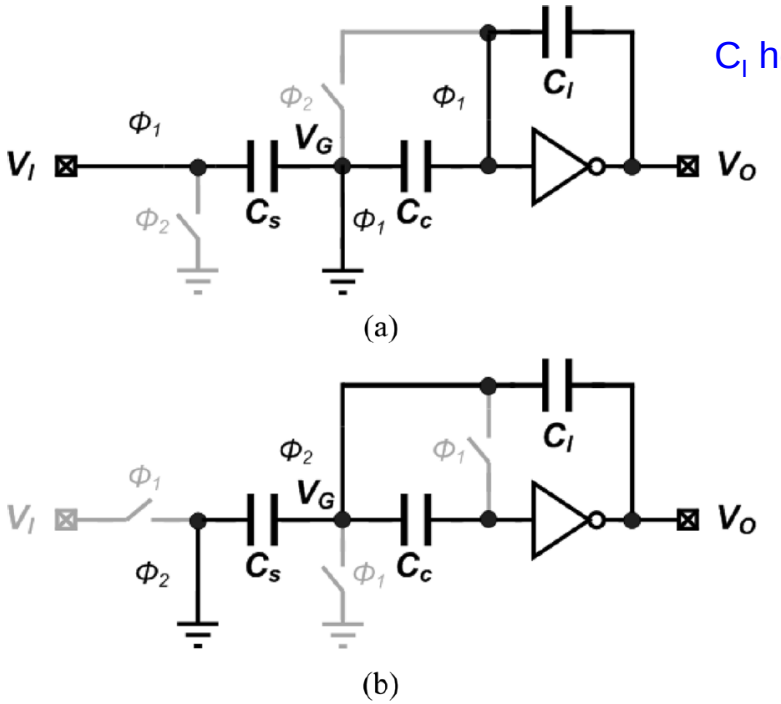
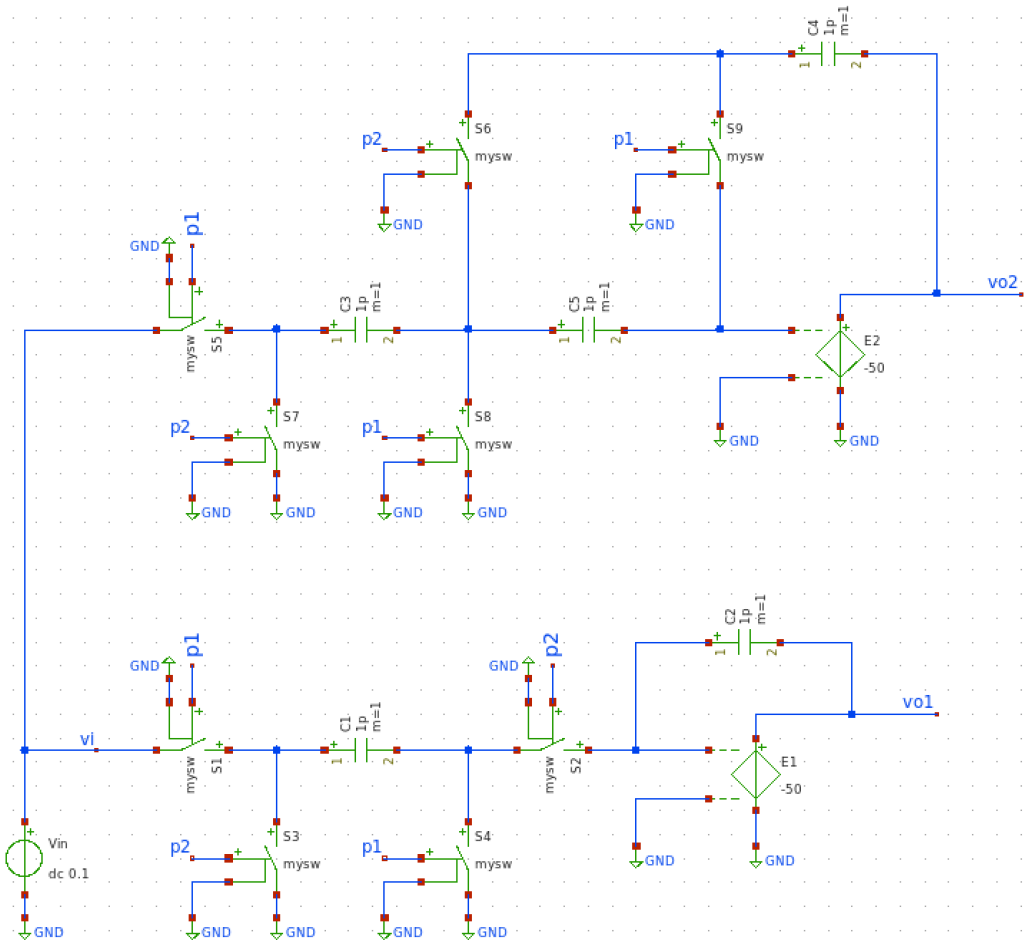
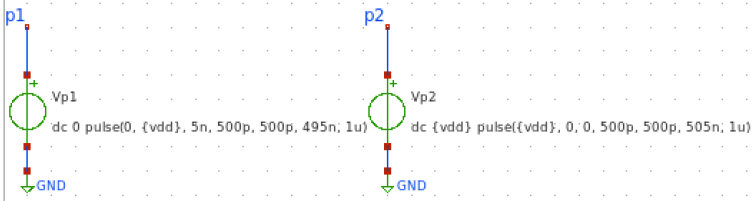


Fig. 4. Inverter-based SC integrator. (a) Sampling phase. (b) Integration phase.

Note: This approach addresses both offset & finite gain

Y. Chae et al., "A 2.1 M Pixels, 120 Frame/s CMOS Image Sensor With Column-Parallel ADC Architecture," in IEEE Journal of Solid-State Circuits, Jan. 2011. https://ieeexplore.ieee.org/document/5641589





NGSPICE

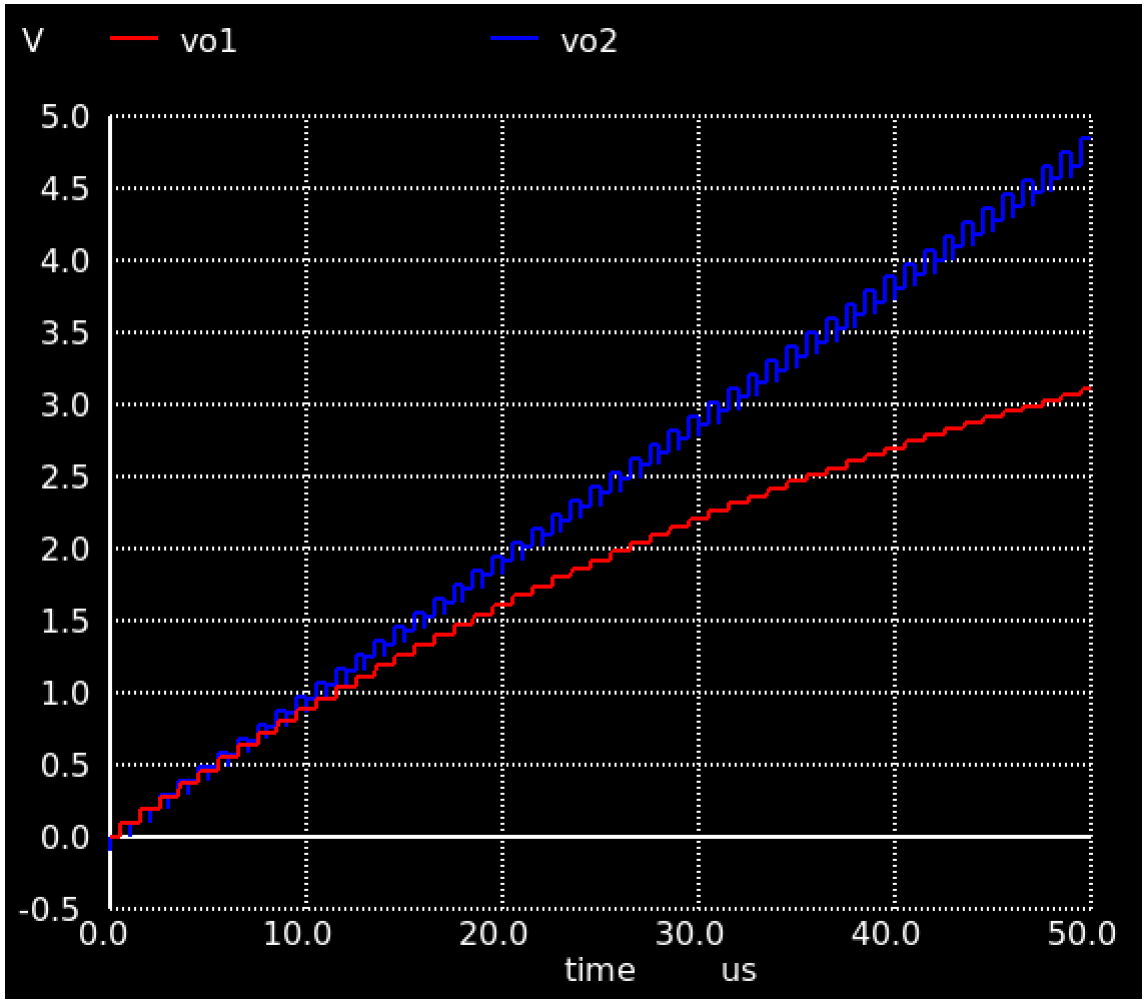
```
.param temp=27 vdd=1.2
.model mysw SW vt={vdd/2} ron=10k roff=10gig
.control
save all
tran 1n 50u
plot vo1 vo2
.endc
```

XSCHEM

Boris Murmann

/foss/designs/tb_chae_integ.sch

2024-02-07 17:32:24



Note: v_{o2} dips down a little during $\phi 1$ during the finite gain; the $\phi 2$ value is what matters

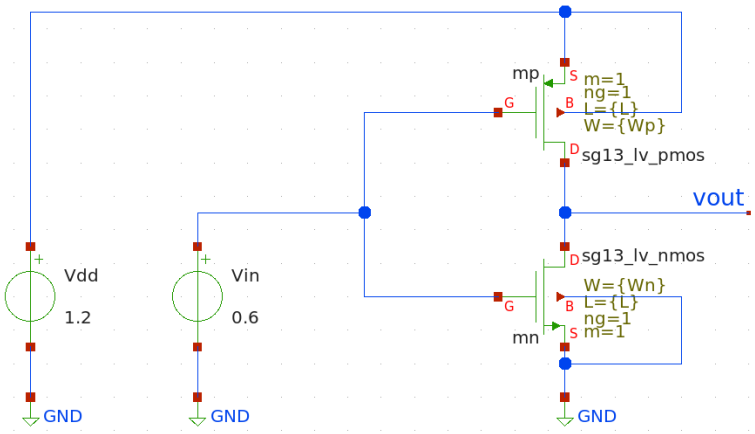
Numbers in Template Design

- Amplifier gain = 35 dB (56)
- Effective amplifier gain with enhancement = 50 dB (316)
- Improvement ~ 5.6x

- Conversion rate = 440 kHz
- Clock rate = 48 MHz
- Oversampling ratio M = 48 / 0.44 = 110

- Effective gain is about 3x larger than oversampling ratio
  - I have mentioned 1x as a design boundary (q-noise explodes)

Inverter Gain in Our Technology



COMMANDS

```
.param temp=27
.param Wn=4u Wp={2*Wn} L=0.13u

.control
dc Vin 0.2 1 1m
alterparam L=1.5u
reset
dc Vin 0.2 1 1m
plot dc1.vout dc2.vout
plot deriv(dc1.vout) deriv(dc2.vout)
.endc
```

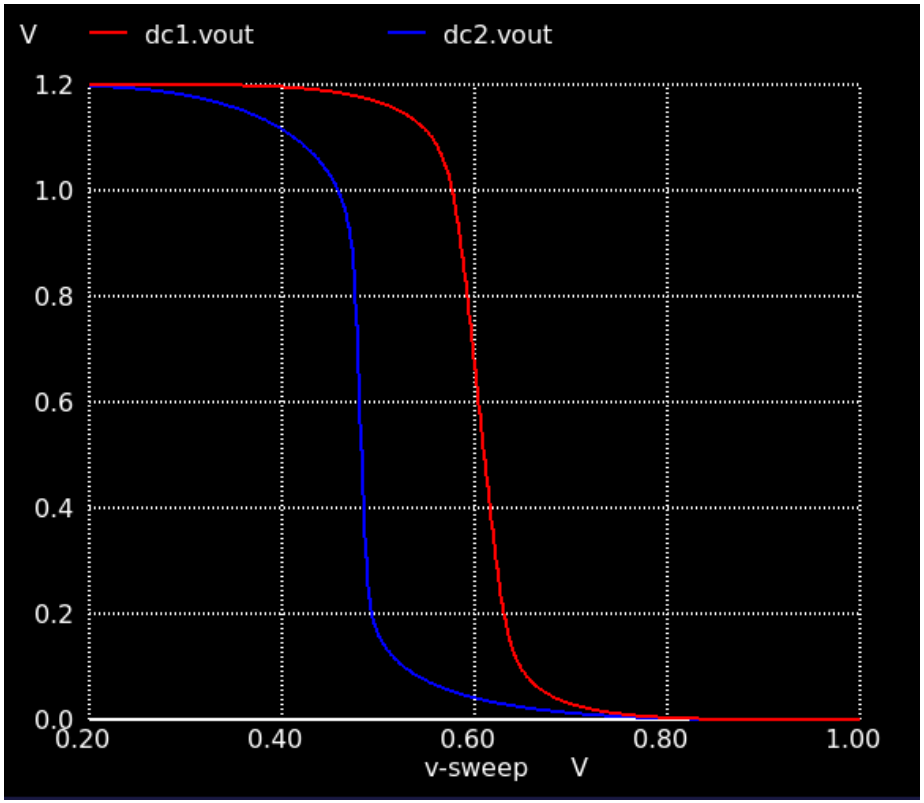
MODEL

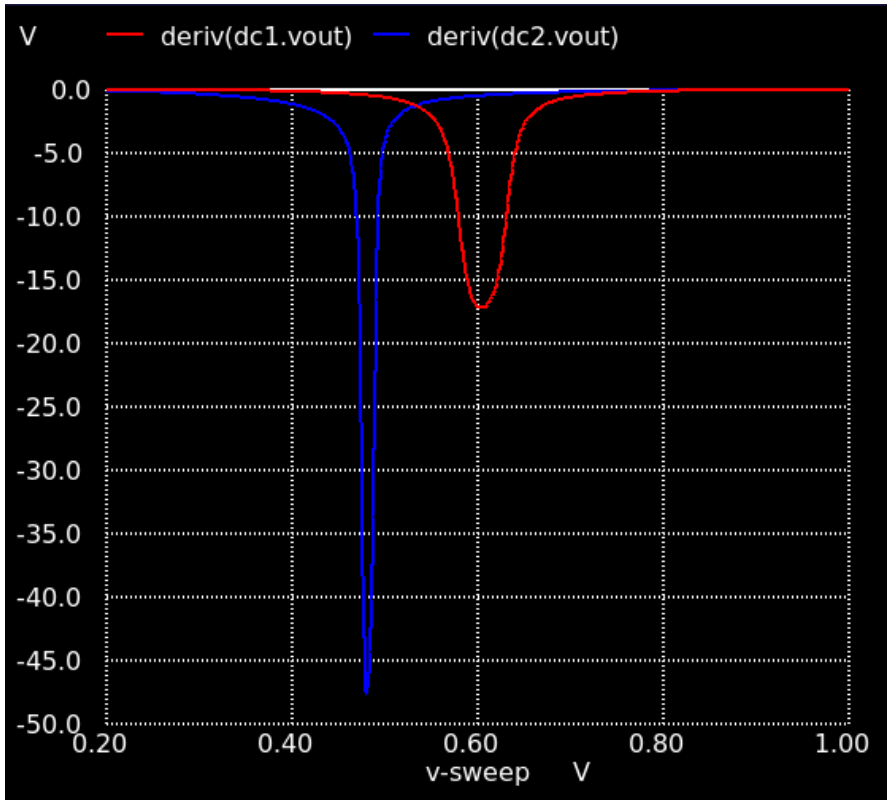
```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
```

XSCHEM

Boris Murmann 2024-02-07 21:43:41

/foss/designs/tb_inv_gain.sch


V
dc1.vout
dc2.vout
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0.20
0.40
0.60
0.80
1.00
v-sweep V


V
deriv(dc1.vout)
deriv(dc2.vout)
0.0
-5.0
-10.0
-15.0
-20.0
-25.0
-30.0
-35.0
-40.0
-45.0
-50.0
0.20
0.40
0.60
0.80
1.00
v-sweep V

Next Steps

- Build integrator with inverter
  - Make sure circuit is practical (using VMID instead of GND, etc.)
  - Use reasonably large L for good initial gain

- Verify operation and see how much “effective gain” we can achieve
  - Compare response to idealized circuit without gain enhancement. Adjust VCVS gain until responses are equal → effective gain
  - Note that the improvement may be somewhat less than expected due to the inverter input capacitance
  - See Chae’s paper for details