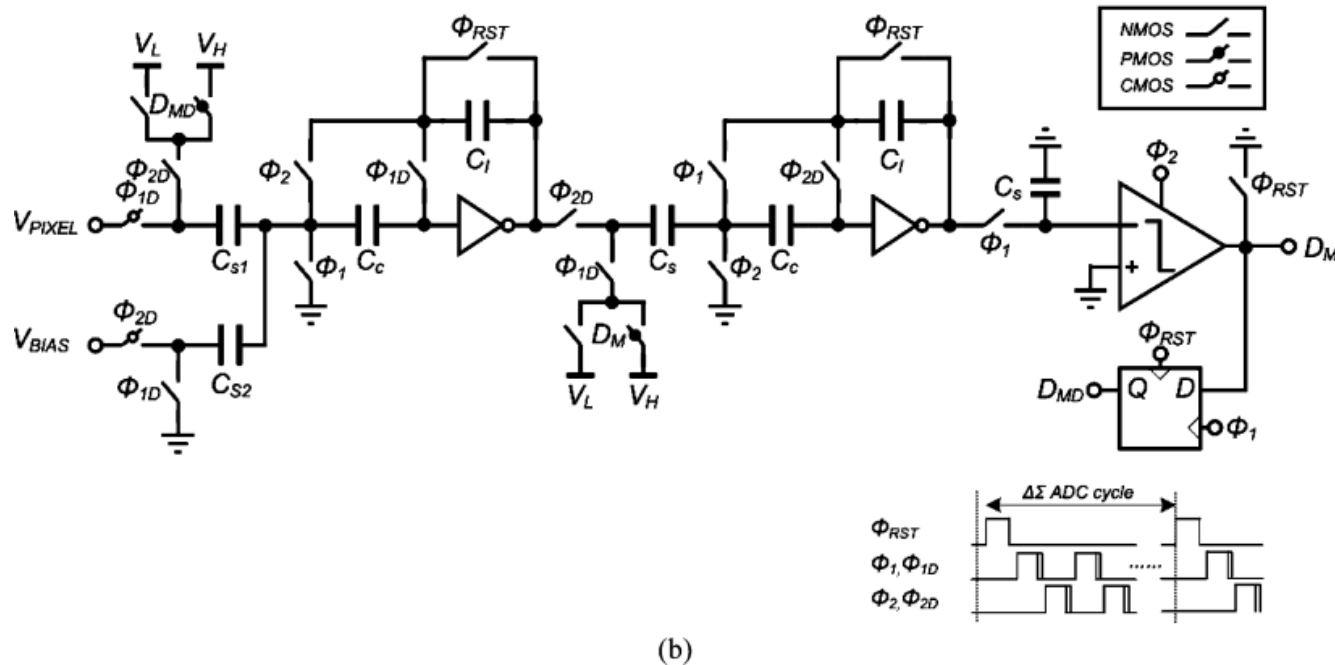
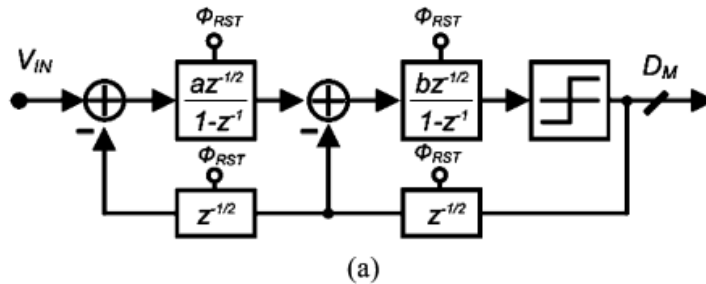


# IDSM1 Circuit Model

**Boris Murmann**

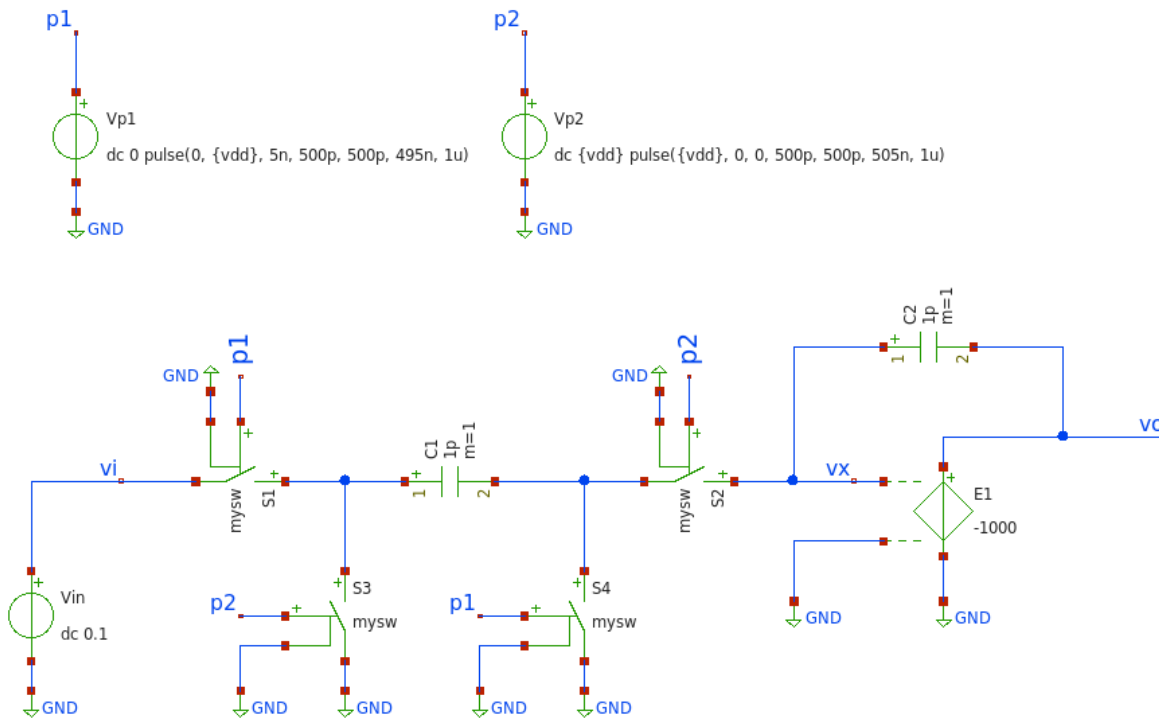
**[bmurmann@hawaii.edu](mailto:bmurmann@hawaii.edu)**

# Template Project



Y. Chae et al., "A 2.1 M Pixels, 120 Frame/s CMOS Image Sensor With Column-Parallel ADC Architecture," in *IEEE Journal of Solid-State Circuits*, Jan. 2011. <https://ieeexplore.ieee.org/document/5641589>

# First Stab at Building an Integrator



## NGSPICE

```
.param temp=27 vdd=1.2
.model mysw SW vt={vdd/2} ron=10k roff=10gig
.control
save all
tran 1n 3u
plot vo
write tb_ideal_integ.raw
.endc
```

## MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
.lib $::SG13G2_MODELS/cornerRES.lib res_typ
```

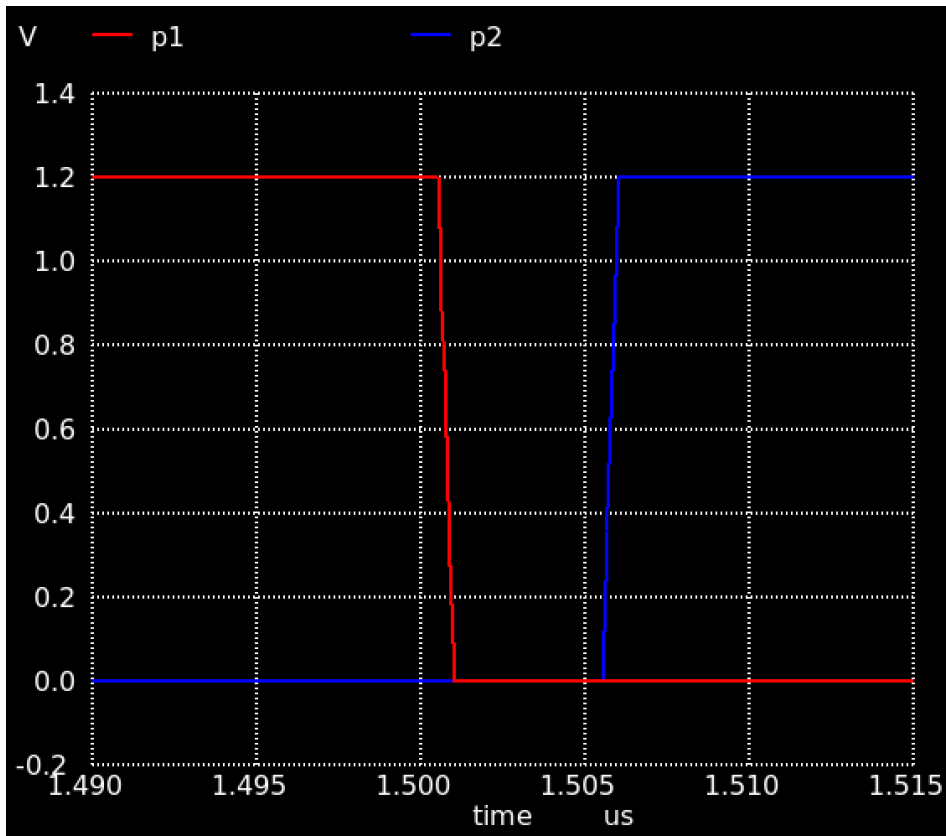


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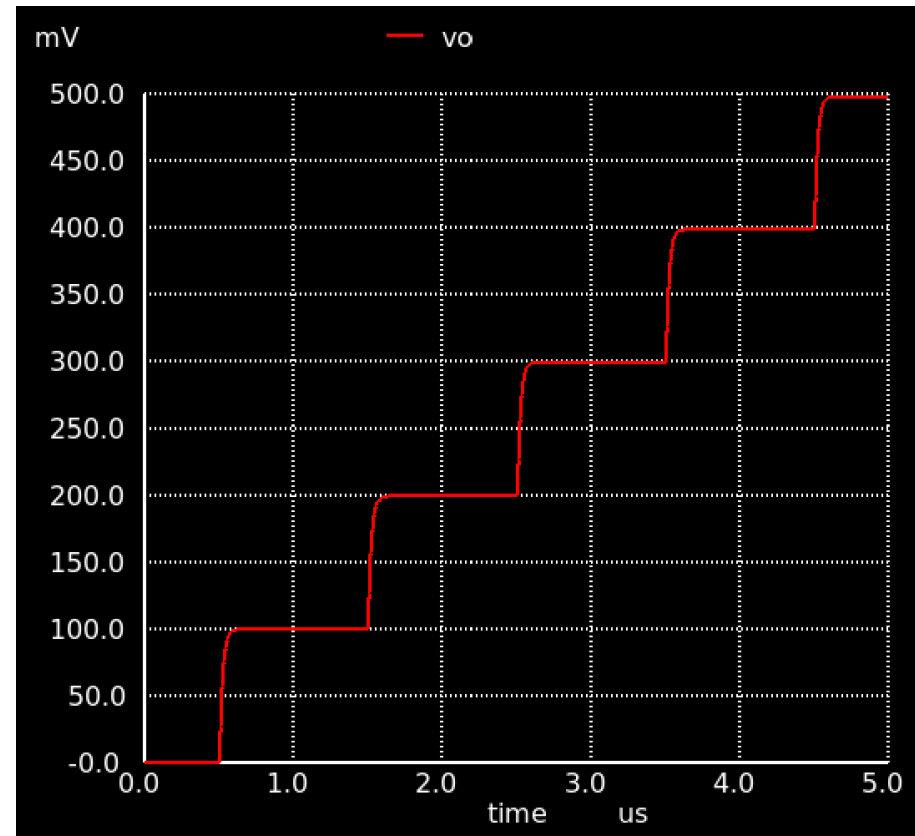
/foss/designs/tb\_ideal\_integ.sch

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Non-overlapping two-phase clocks

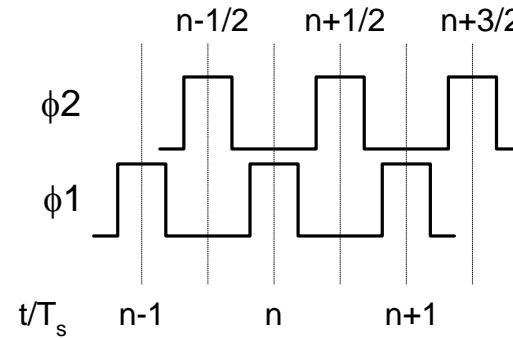
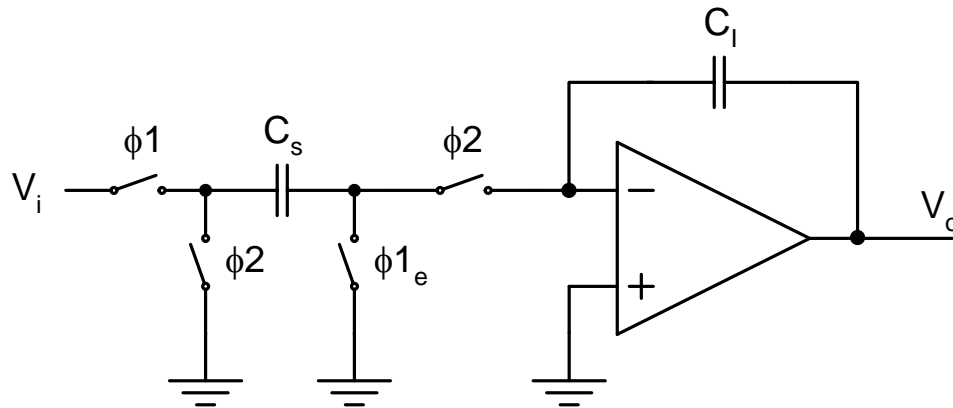


Integrator output  
(Amplifier gain = 1000)



# Integrator Analysis (1)

Nonoverlapping clocks



$t/T_s$	$Q_s$	$Q_f$
$n-1$	$C_s \cdot V_i(n-1)$	$C_f \cdot V_o(n-1)$
$n-1/2$	0	$C_f \cdot V_o(n-1/2) = C_f \cdot V_o(n-1) + C_s \cdot V_i(n-1)$
$n$	$C_s \cdot V_i(n)$	$C_f \cdot V_o(n) = C_f \cdot V_o(n-1) + C_s \cdot V_i(n-1)$
$n+1/2$	...	...

## Integrator Analysis (1)

- Assuming that  $V_o$  is sampled during  $\phi_1$ , we have

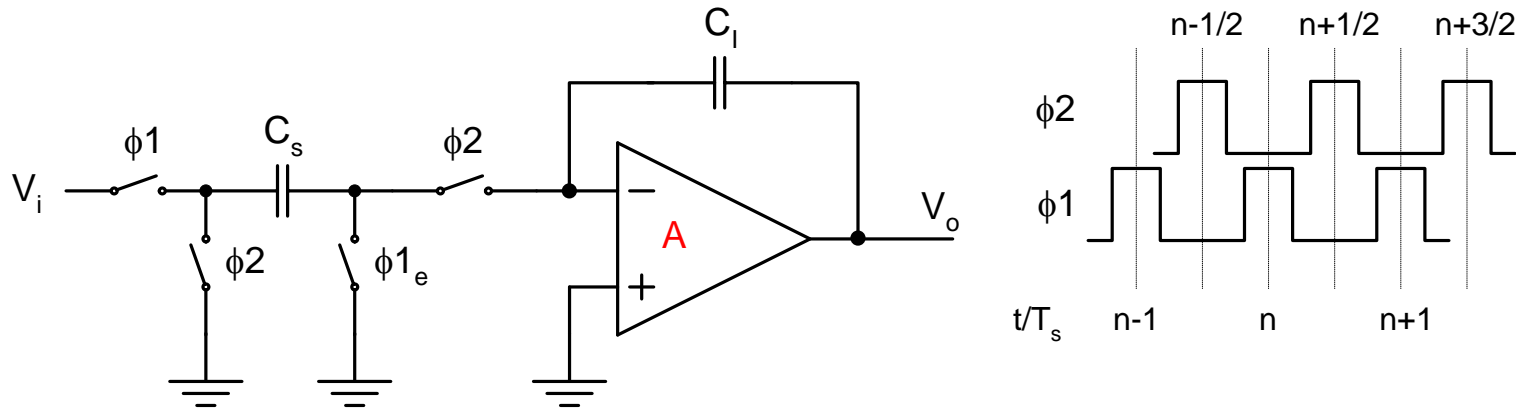
$$C_I V_o(n) = C_I V_o(n-1) + C_S V_i(n-1)$$

$$C_I V_o(z) = z^{-1} C_I V_o(z) + z^{-1} C_S V_i(z)$$

$$\therefore \frac{V_o(z)}{V_i(z)} = \frac{C_S}{C_I} \frac{z^{-1}}{1 - z^{-1}}$$

- This expression holds only for infinite amplifier gain
  - Let's look at impact of finite gain
  - Causes integrator gain error and leakage

# Finite Gain (1)



$t/T_s$	$Q_s$	$Q_f$
$n-1$	$C_s \cdot V_i(n-1)$	$C_f \cdot V_o(n-1) \cdot [1 + 1/A]$
$n-1/2$	$C_s \cdot V_o(n-1/2)/A$	$C_f \cdot V_o(n-1/2) \cdot [1 + 1/A] = C_f \cdot V_o(n-1) \cdot [1 + 1/A] + C_s \cdot V_i(n-1) - C_s \cdot V_o(n-1/2)/A$
$n$	$C_s \cdot V_i(n)$	$C_f \cdot V_o(n) \cdot [1 + 1/A] = C_f \cdot V_o(n-1) \cdot [1 + 1/A] + C_s \cdot V_i(n-1) - C_s \cdot V_o(n)/A$
$n+1/2$	...	...

## Finite Gain (2)

- Again, assuming that  $V_o$  is sampled during  $\phi_1$ , we have

$$C_I V_o(z) \left[ 1 + \frac{1}{A} \right] = z^{-1} C_I V_o(z) \left[ 1 + \frac{1}{A} \right] + z^{-1} C_s V_i(z) - \frac{C_s}{A} V_o(z)$$

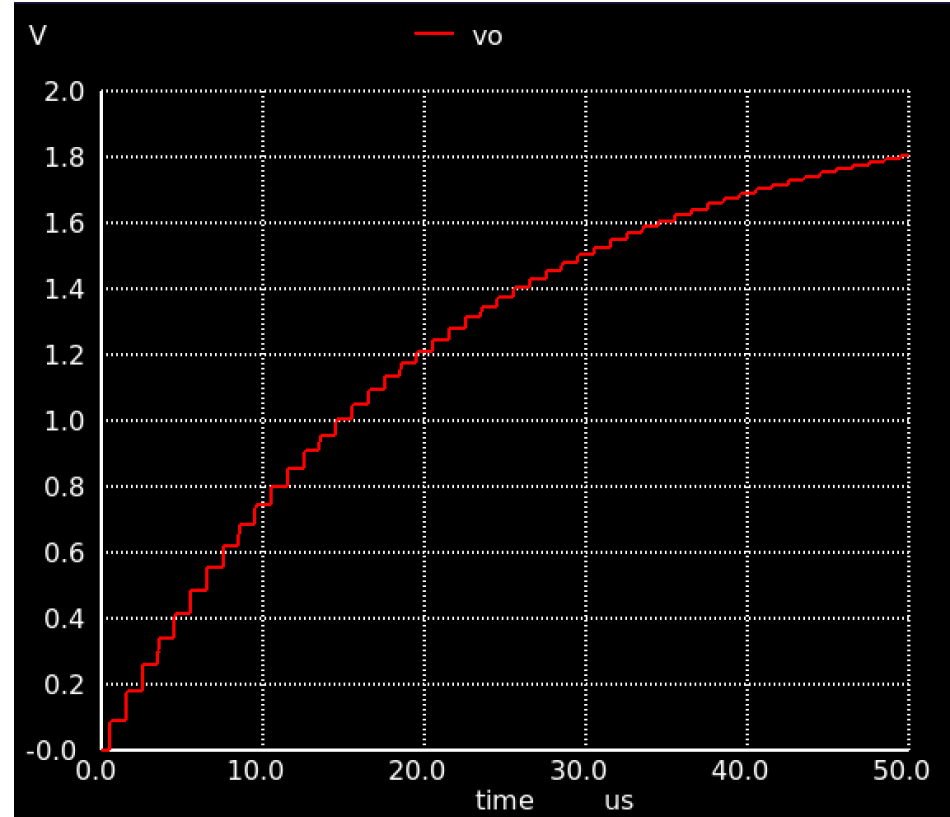
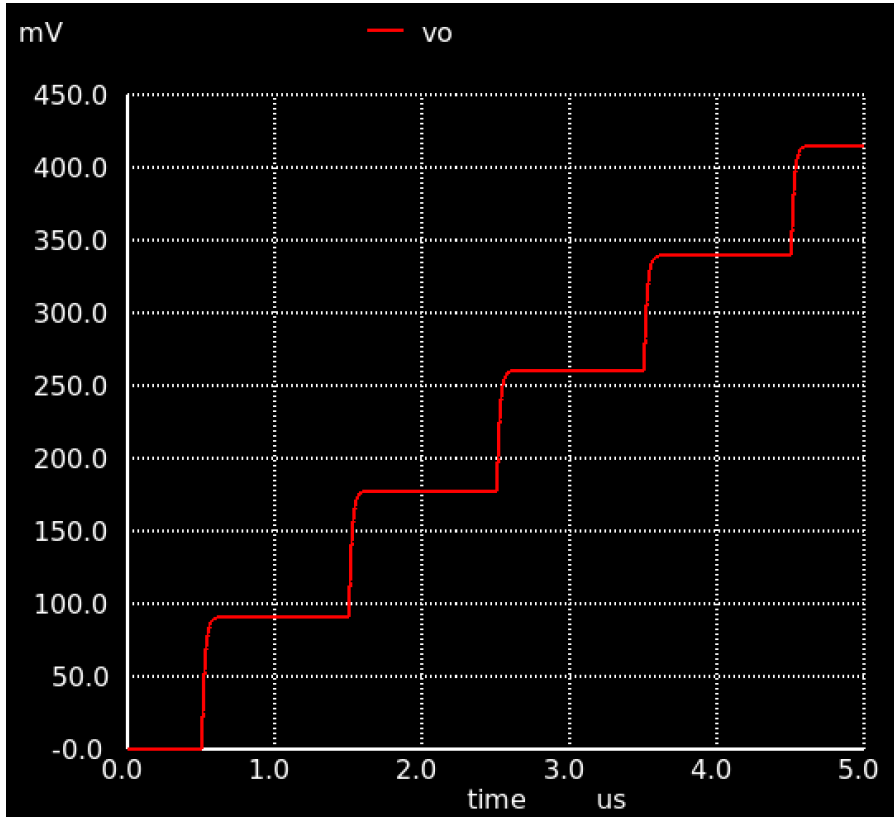
$$\therefore \frac{V_o(z)}{V_i(z)} \cong \frac{C_s}{C_I} \frac{z^{-1} \left( 1 - \frac{1}{A} \left[ 1 + \frac{C_s}{C_I} \right] \right)}{1 - \left( 1 - \frac{1}{A} \frac{C_s}{C_I} \right) z^{-1}} = \frac{g \cdot z^{-1}}{1 - [1 - \alpha] \cdot z^{-1}}$$

$$V_o(z) = [1 - \alpha] \cdot z^{-1} V_o(z) + g \cdot z^{-1} V_i(z)$$

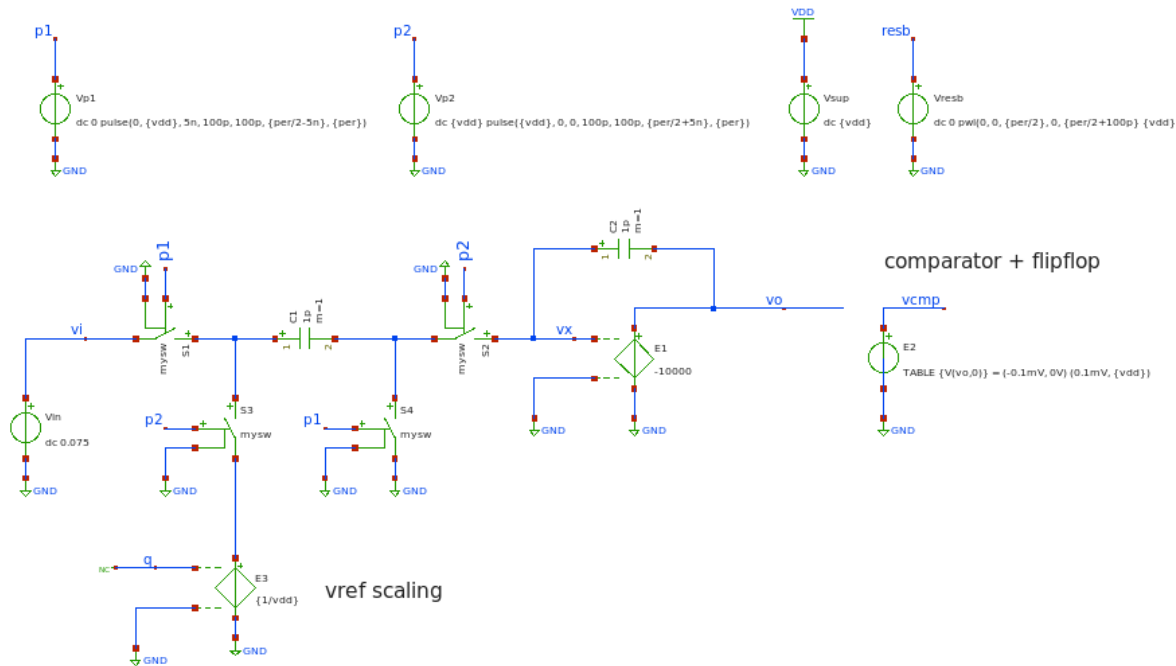
- Finite gain results in "leaky integrator" (and gain error)
  - Some fraction of previous output is lost in new cycle



Integrator output  
(Amplifier gain = 20)



## First Stab at Building A First-Order Modulator



### Flipflop from IHP library



NGSPICE

```
*DFF CLK D Q Q_N RESET_B VDD VSS
x1 p1 vcmp q qn resb VDD GND sg13g2_dfrbp_1
.param temp=27 vdd=1.2 per=1u
.model mysw SW vt={vdd/2} ron=10k roff=10gig
.option method=gear reltol=1e-4
```

```
.control
save all
tran 10n 64u
plot vo q
set wr_singlescale
set wr_vecnames
wrdata tb_ideal_idsm1.txt vo q p1 p2
.endc
```

MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos tt
.lib $::SG13G2_MODELS/cornerRES.lib res typ
.inc /foss/pdks/sq13q2/libs.ref/sq13q2_stdcell/spice/sq13q2_stdcell.spice
```

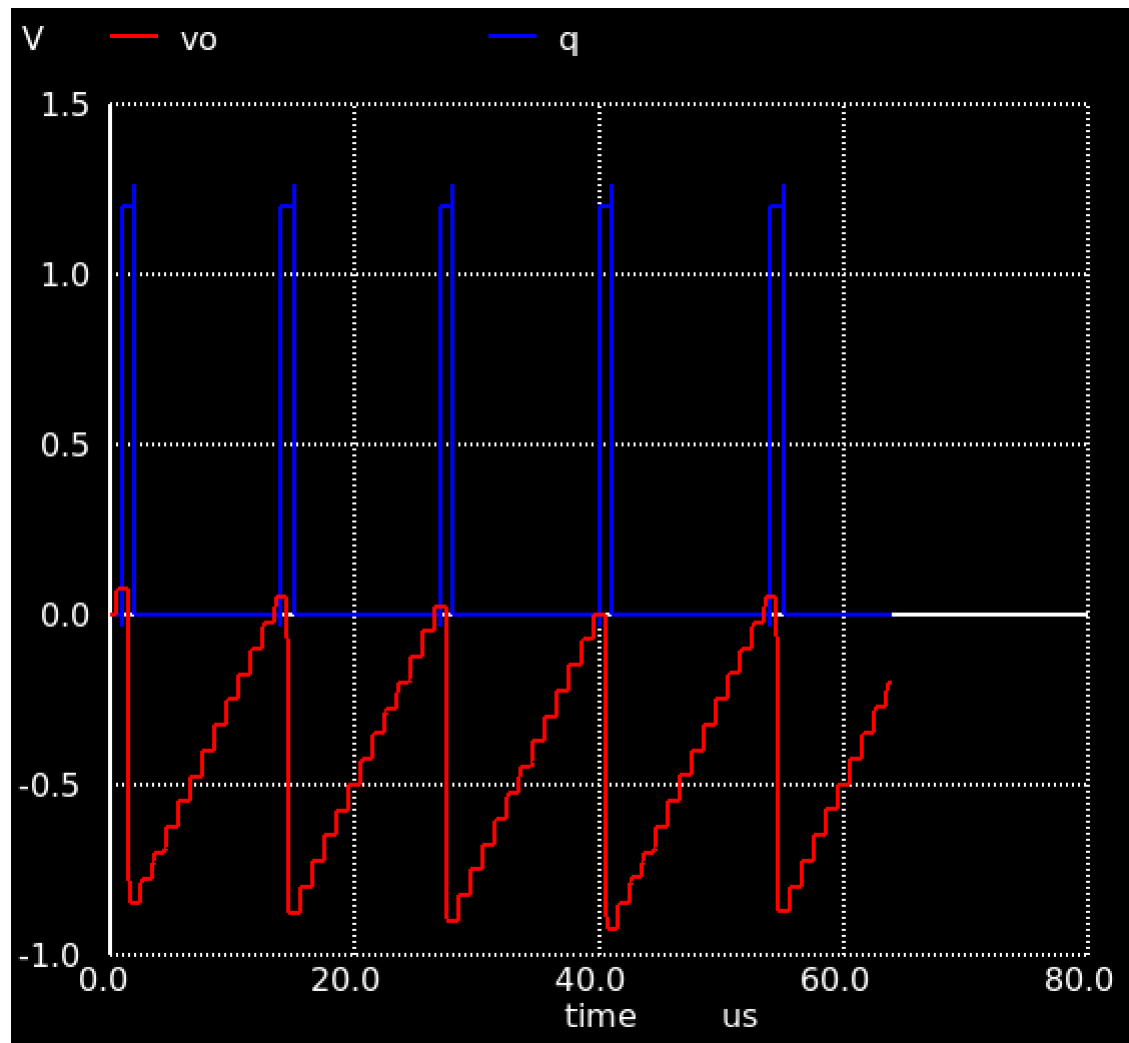


Boris Murmann

```
/foss/designs/tb ideal idsm1.sch
```

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Integrator output and feedback pulses match  
behavioral simulation!



## Next Steps

- Add second integrator (second-order modulator)
- Write some post-processing scripts
  - Detailed measurements
  - Emulate counters to create final digital output
- Increasingly “transistorize” the implementation
  - Shift voltages to practical levels (can’t have negative voltages)
  - MOSFET switches
  - Comparator
  - Inverter-based amplifier
    - With correlated double-sampling to achieve high gain