Parasitics

Boris Murmann

bmurmann@hawaii.edu

Launching KLayout (with IHP tech setup)

9. Create a configuration directory for KLayout and populate it as detailed below. We copy the tech directory (instead of creating a symbolic link) to fix a typo in the current PDK release (change grid to 5 nm).

```
cd /foss/designs
mkdir .klayout
mkdir .klayout/libraries
ln -s $PDKPATH/libs.ref/sg13g2_pr/gds/sg13g2_pr.gds ./.klayout/libraries
ln -s $PDKPATH/libs.ref/sg13g2_stdcell/gds/sg13g2_stdcell.gds ./.klayout/libraries
ln -s $PDKPATH/libs.tech/klayout/python ./.klayout/
cp -r $PDKPATH/libs.tech/klayout/tech ./.klayout/
sed -i 's:<dbu>0.001</dbu>:<dbu>0.005</dbu>:g' ./.klayout/tech/sg13g2.lyt
```

10. Create a subdirectory for your layout work.

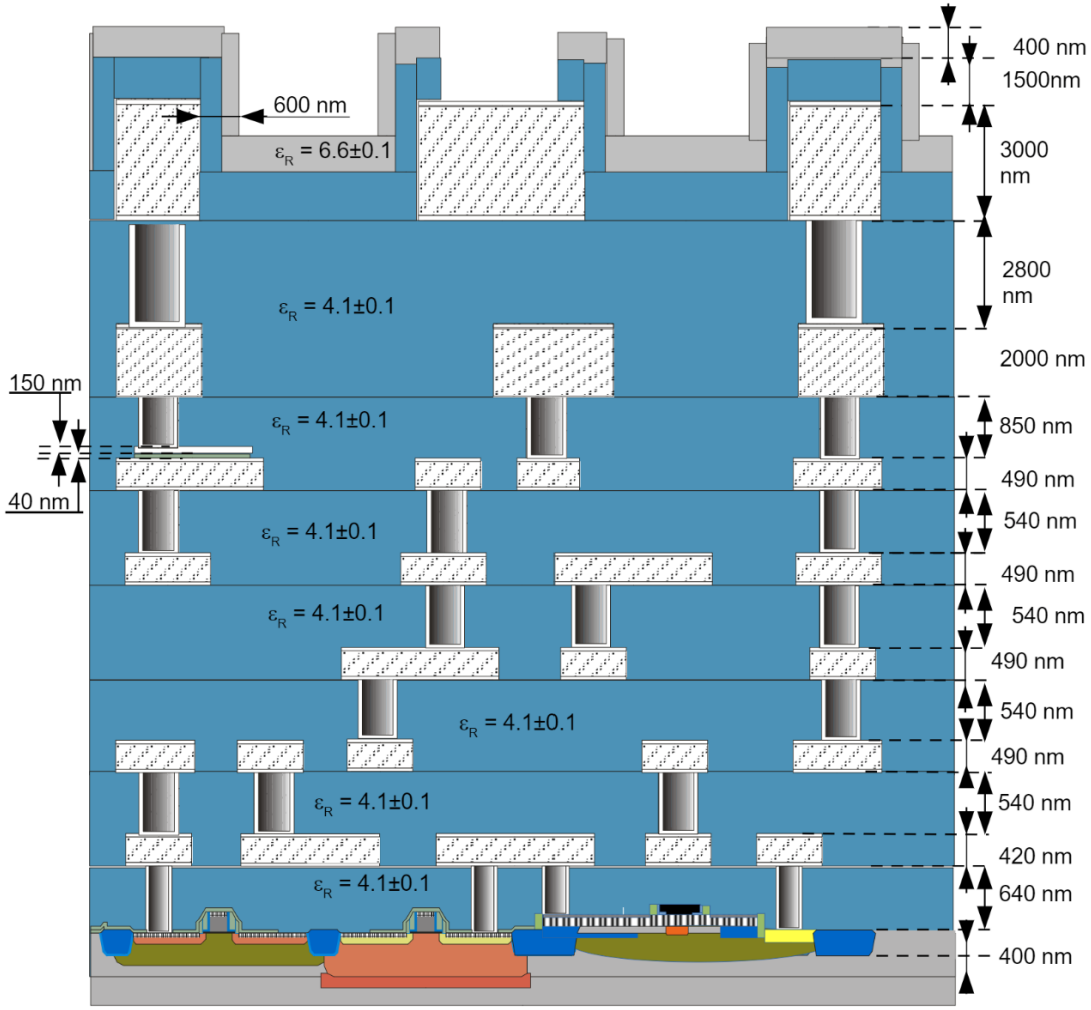
```
cd /foss/designs
mkdir layout
cd layout
```

11. To start KLayout with the proper technology setup, set the KLAYOUT_HOME environment variable, then launch using the -e option (edit mode). The environment variable must be set each time the container is started (this will be fixed in a future release, which will automatically set the proper environment variable for KLayout).

```
export KLAYOUT_HOME=/foss/designs/.klayout
klayout -e &
```

https://github.com/bmurmann/EE628/blob/main/3_Tools/win.md

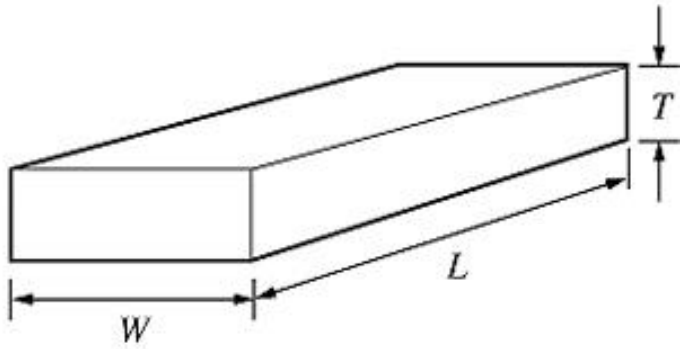
Cross Section (IHP SG13G2 Process)



Designer can only manipulate x & y dimensions, z dimensions are fixed

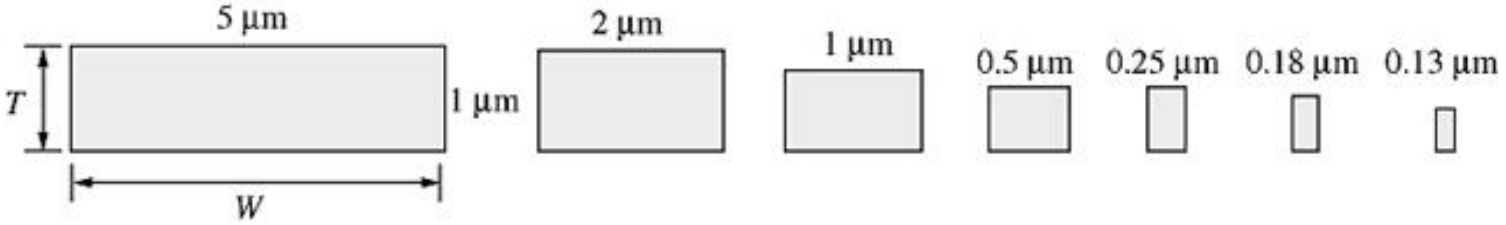
https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_process_spec.pdf

Wire Resistance

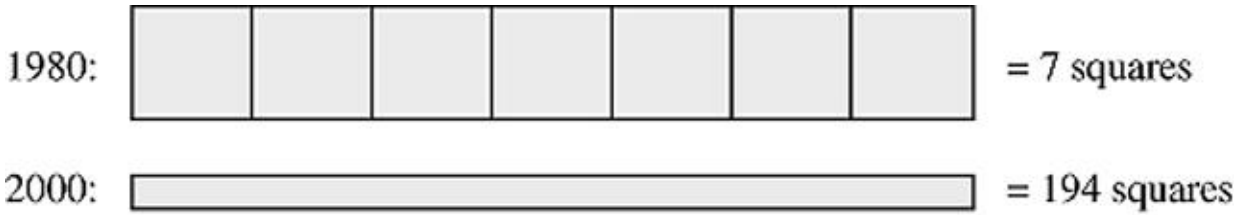


$$R = \frac{\rho L}{TW} \qquad R_{sq} = \frac{\rho}{T}$$

$$R = R_{sq}\frac{L}{W} = R_{sq}N_{sq}$$

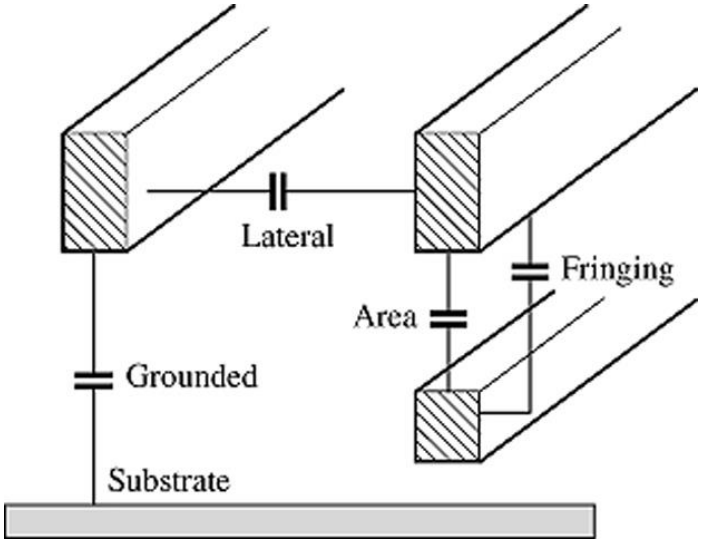


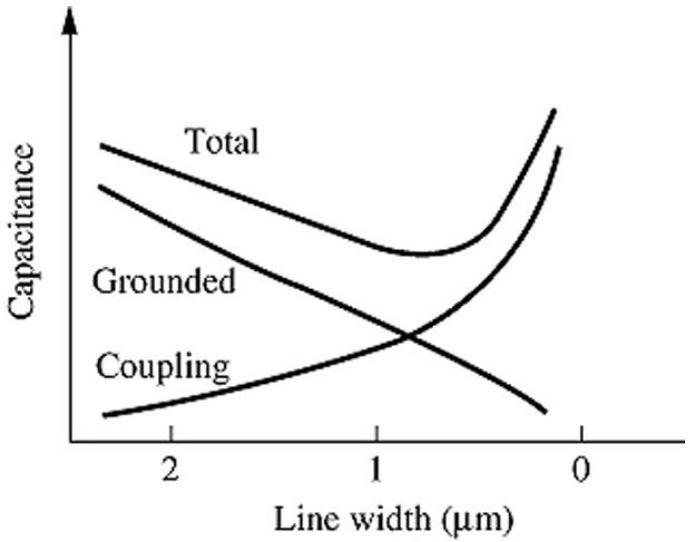
35 µm wire in 5 µm CMOS



35 µm wire in 0.18 µm CMOS

Wire Capacitance

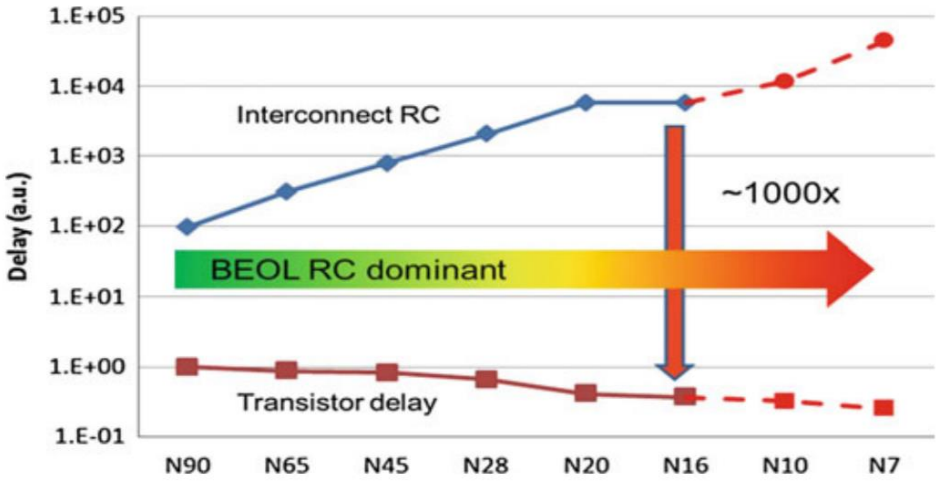




- In modern technology, most of the wire capacitance (70% or more) is coupling capacitance to other wires
  - Wires have become denser and “taller”
- Total capacitance is typically in the range of 0.1…0.2 fF/μm
- May need to consider “Miller effect” when adjacent wires switch in opposite directions

Typical Parameters

		180nm	90nm	45nm	22nm
Metal 1	R’ (kΩ/mm)	1	2	9	35
	C’ (fF/mm)	200	180	160	130
Global	R’ (kΩ/mm)	0.25	0.5	3	11
	C’ (fF/mm)	250	210	180	150



[Or-Bach, Chips 2020 Rev. 2]

2.13 Resistances, Line Width Deltas, Temperature Coefficients

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Substrate Resistivity	RSBLK	Ωcm	*37.5*	*50*	*62.5*		Specification: WAFPR3763
Salicided GatPoly (n^+)	refer section 2.13						
Unsalicized GatPoly (n^+)	refer section 2.14						
Unsalicided GatPoly (p^+)	refer section 2.15						
Metal1 Snake Sheet Resistance	SNAKEM1	mΩ	90	115	145		width = 0.16 µm
Unsalicided nSD-Activ Sheet Resistance	RSNSD0	Ω	55	67	79		
Unsalicided pSD-Activ Sheet Resistance	RSPSD0	Ω	69	79	89		
Metal2 Snake Sheet Resistance	SNAKEM2	mΩ	70	88	110		width = 0.20 µm
Metal3 Snake Sheet Resistance	SNAKEM3	mΩ	70	88	110		width = 0.20 µm
Metal4 Snake Sheet Resistance	SNAKEM4	mΩ	70	88	110		width = 0.20 µm
Metal5 Snake Sheet Resistance	SNAKEM5	mΩ	70	88	110		width = 0.20 µm
TopMetal1 Snake Sheet Resistance	SNAKETM1	mΩ	14	18	22		width = 1.5 µm
TopMetal2 Snake Sheet Resistance	SNAKETM2	mΩ	7.5	11	14.5		width = 2.0 µm

https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_process_spec.pdf

2.14 Contact & Via Resistances

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Metal1 to Silicide on nSD-Activ	RCM1NSD	Ω/CNT	8	17	22	V = 1 V	93740 contact chain
Metal1 to Silicide on pSD-Activ	RCM1PSD	Ω/CNT	8	17	22	V = 1 V	93740 contact chain
Metal1 to Silicide on GatPoly (n^+)	RCM1NPLY	Ω/CNT	8	15	20	V = 1 V	98566 contact chain
Metal1 to Silicide on GatPoly (p^+)	RCM1PPLY	Ω/CNT	8	15	20	V = 1 V	98566 contact chain
Metal2 – Metal1	RVIA1	Ω/VIA	5	9	20	V = 1 V	103840 contact chain
Metal3 – Metal2	RVIA2	Ω/VIA	5	9	20	V = 1 V	103840 contact chain
Metal4 – Metal3	RVIA3	Ω/VIA	5	9	20	V = 1 V	103840 contact chain
Metal5 – Metal4	RVIA4	Ω/VIA	5	9	20	V = 1 V	103840 contact chain
TopMetal1 – Metal5	RTV1	Ω/VIA	1	2.2	4	V = 1 V	3276 contact chain
TopMetal2 – TopMe-tal1	RTV2	Ω/VIA	0.5	1.1	2.2	V = 1 V	1140 contact chain

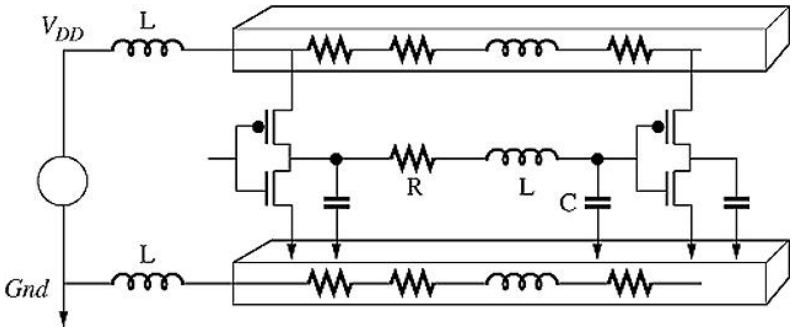
https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_process_spec.pdf

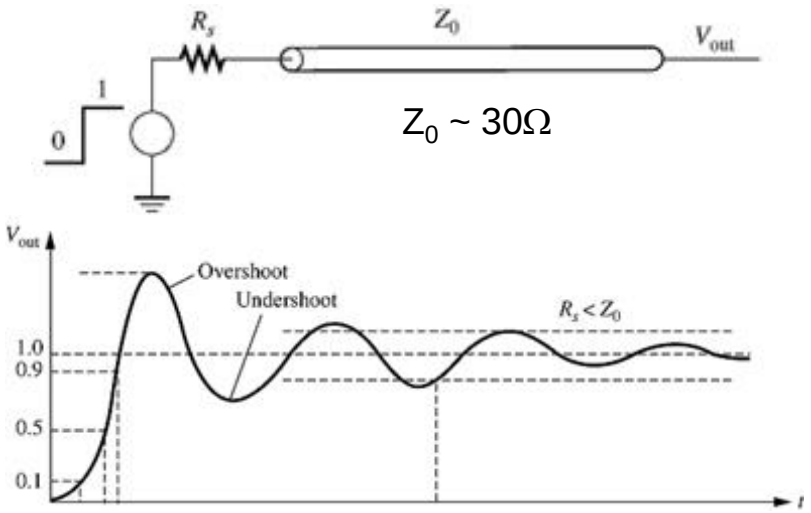
2.17 Parasitic Capacitances

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Metal1 - Activ Area Capacitance	CAMET1ACT	aF/µm²	49	59	69	A.aq	A = 250·1200 µm²
Metal1 - Substrate Area Capacitance	CAMET1SUB	aF/µm²	31	37	43	A.aq	A = 250·1200 µm²
Metal1 - Metal2 Area Capacitance	CAMET1/2	aF/µm²	54	68	82	A.aq	A = 250·1200 µm²
Metal2 - Metal3 Area Capacitance	CAMET2/3	aF/µm²	54	68	82	A.aq	A = 250·1200 µm²
Metal3 - Metal4 Area Capacitance	CAMET3/4	aF/µm²	54	68	82	A.aq	A = 250·1200 µm²
Metal4 - Metal5 Area Capacitance	CAMET4/5	aF/µm²	54	68	82	A.aq	A = 250·1200 µm²
TopMetal1 - Metal5 Area Capacitance	CATOPMET1	aF/µm²	36	42.5	49	A.aq	A = 250·1200 µm²
TopMetal2 - TopMetal1 Area Capacitance	CATOPMET2	aF/µm²	10	13	16	A.aq	A = 250·1200 µm²

https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_process_spec.pdf

Should we Model Inductance?





- Tricky to estimate inductance (entire current loop must be considered)
- Luckily, inductive effects in digital signaling tend to be negligible for
  - Short wires (driver resistance swamps out inductance)
  - Long wires (wire resistance swamps out inductance)
- Inductive effects are most important for the design of clock grids and very wide wires for power supply → Beyond the scope of what we do

Electromigration (EM)

- Unwanted movement of material
- Applies to wires, contacts and vias
- Caused by high current density, momentum transfer from moving electrons to metal ions that make up lattice of interconnect material
- Ions drift in the direction of the electron flow → DC flow is what matters
- Must stay below certain current per wire cross-section, e.g., 1 mA/μm^2 (highly temperature dependent)
- EM has become a substantial showstopper in modern CMOS

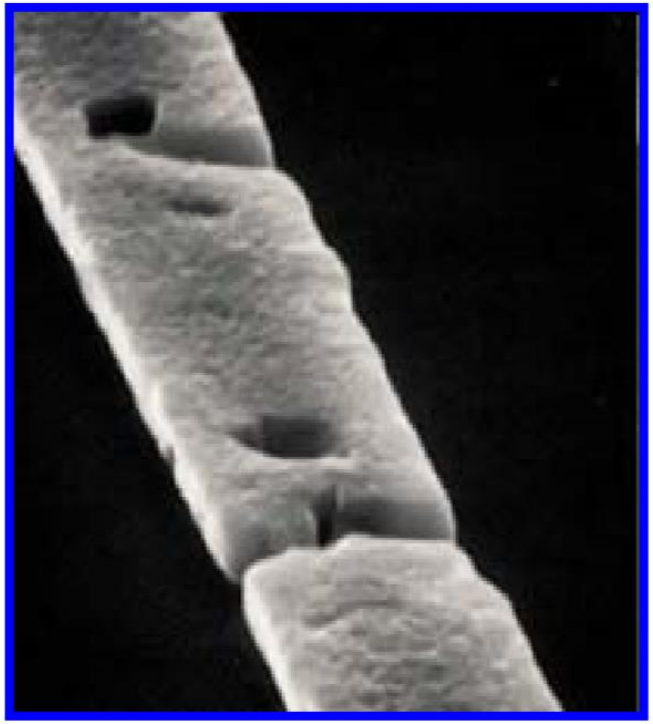


Photo: Sanyo Electronics

2.15 Maximum Current Densities

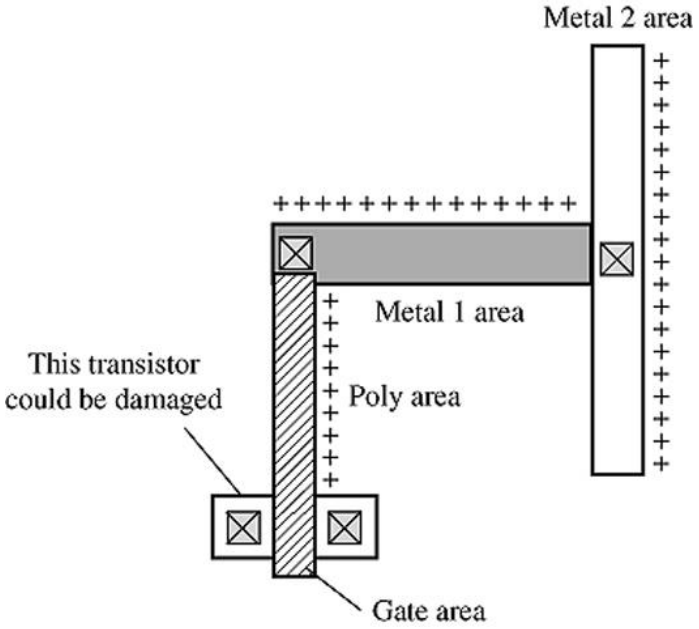
(11 years @105°C)

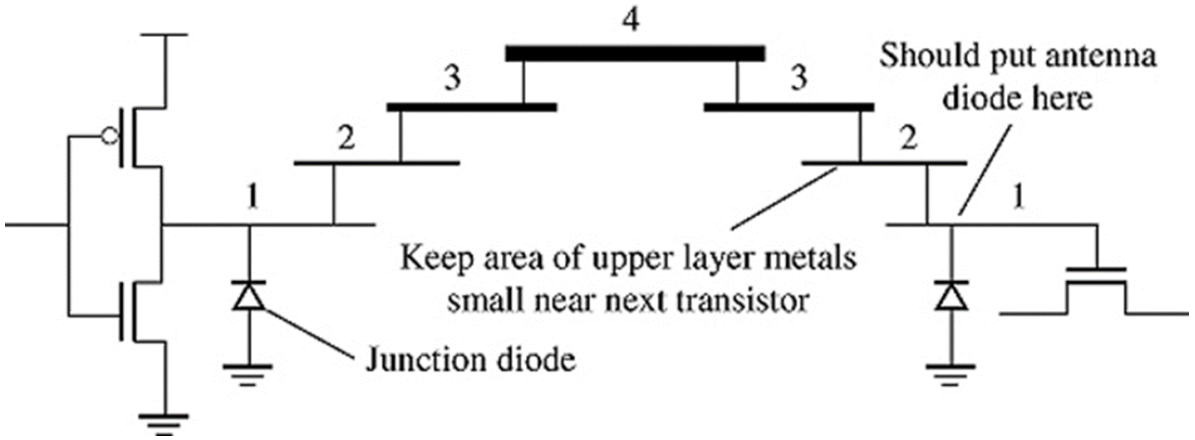
Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Metal1	IMAXM1	mA			0.36	A.v	w = 0.16 ... 0.36 µm
Metal1	JMAXM1	mA/µm			1	A.v	w > 0.36 µm
Metal2	IMAXM2	mA			0.6	A.v	w = 0.2 … 0.3 µm
Metal2	JMAXM2	mA/µm			2	A.v	w > 0.3 µm
Metal3	IMAXM3	mA			0.6	A.v	w = 0.2 … 0.3 µm
Metal3	JMAXM3	mA/µm			2	A.v	w > 0.3 µm
Metal4	IMAXM4	mA			0.6	A.v	w = 0.2 … 0.3 µm
Metal4	JMAXM4	mA/µm			2	A.v	w > 0.3 µm
Metal5	IMAXM5	mA			0.6	A.v	w = 0.2 … 0.3 µm
Metal5	JMAXM5	mA/µm			2	A.v	w > 0.3 µm
TopMetal1	JMAXM6	mA/µm			15	A.v	
TopMetal2	JMAXM7	mA/µm			16	A.v	
Contact	JMAXCNT	mA/Cnt			0.3	A.v	
Via1	JMAXVIA1	mA/Via			0.4	A.v	

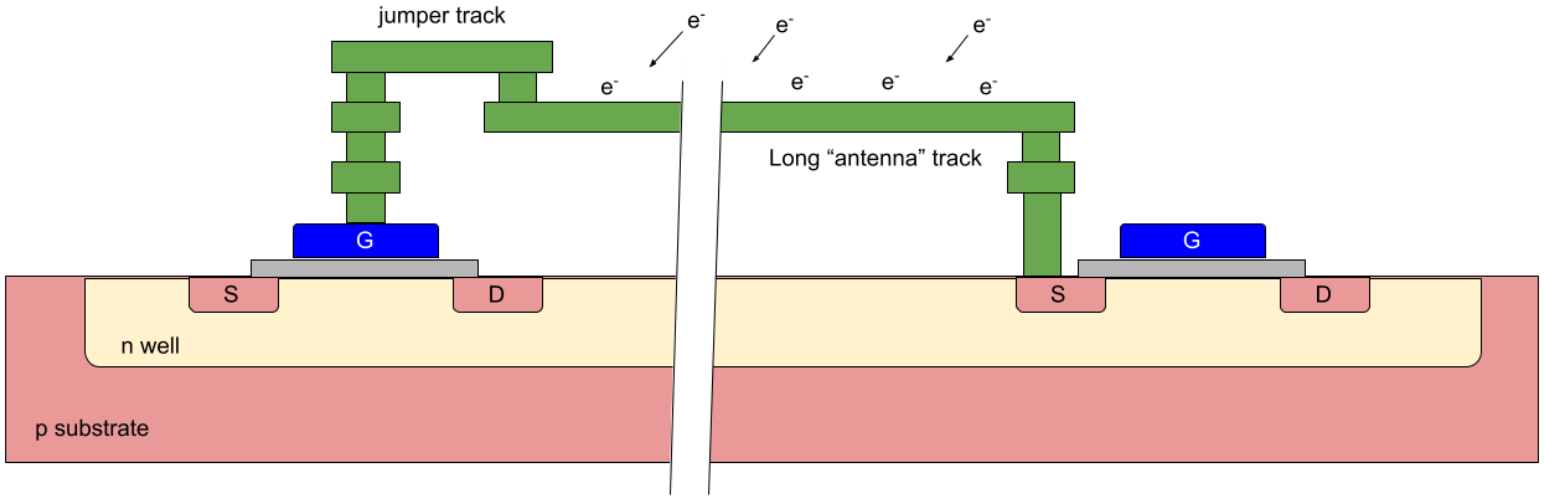
https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_process_spec.pdf

Antenna Effect

- May destroy gate oxide due to charge build-up during plasma etching or CMP (chemical-mechanical polishing)
- Remedy: limit area of low-level metal, add diodes that leak away charge



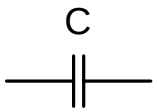




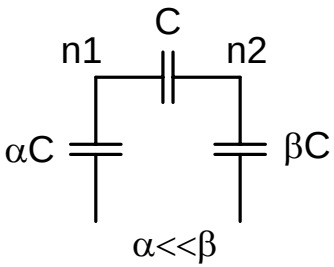
https://www.linkedin.com/pulse/analog-layout-just-transistors-mark-waller/

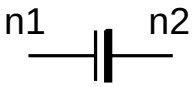
Capacitor Parasitics

Ideal Capacitor

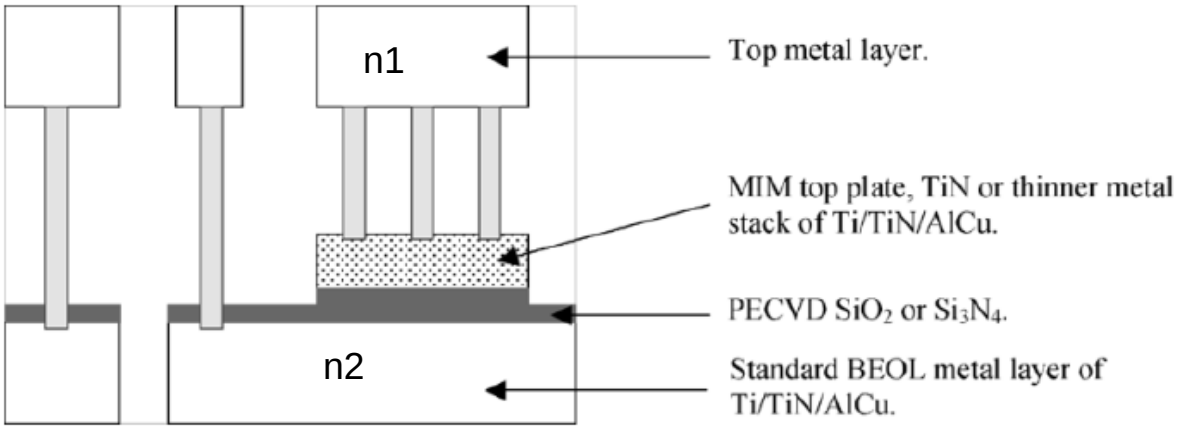


Typical Integrated Circuit Capacitor





E.g., α~1%, β~10% for a MIM capacitor



[Ng, Trans. Electron Dev., 7/2005]

MIM Capacitor

2.12 MIM Capacitor

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Specific Area Capacitance	CMIMA	fF/µm²	**1.35**	**1.5**	**1.65**	A.k	
Specific Capacitance MIM Perimeter	CMIMP	aF/µm		*40*		A.l	
Breakdown Voltage	BVMIM	V	**15**	**23**		A.y	
Voltage Coefficients	VCMIM1 VCMIM2	ppm/V ppm/V²		*-26* *5*		A.ah	
Temperature Coefficient	TCMIM1 TCMIM2	ppm/K ppm/K²		*3.6* *0.002*		A.ad	
Matching Coefficient	KCMIM	nm					

https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_process_spec.pdf

4.3 MIM

Metal-Insulator-Metal (MIM) capacitors are formed by a thin dielectric layer and conductor placed between **TopMetal1** and **Metal5**.

Device recognition: MIM capacitor = **MIM** + **Metal5**

Within **MIM** capacitor layer **Vmim** can be used instead of **TopVia1**.

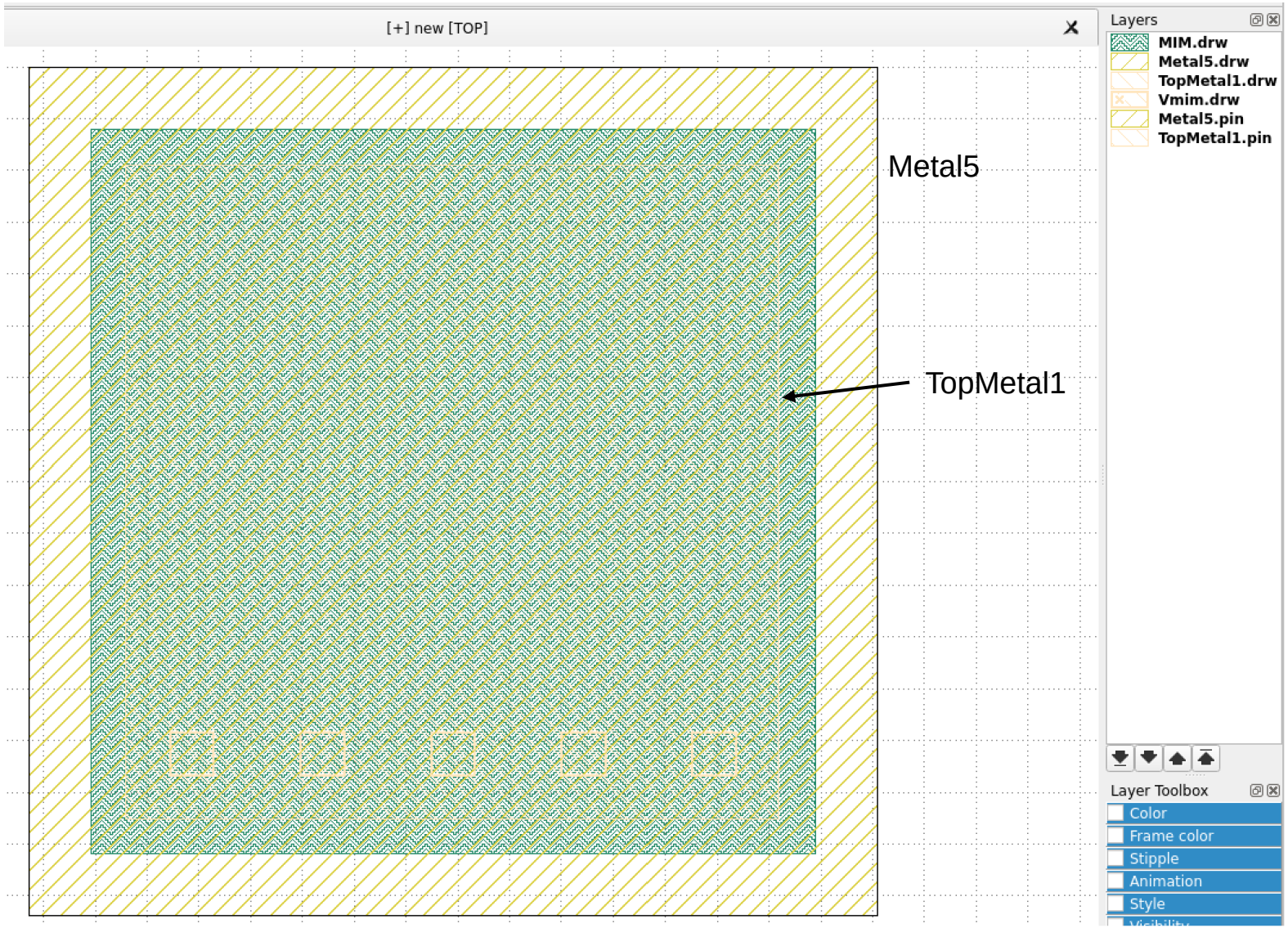
Background: Most EDA tools cannot distinguish between interconnects and electrical components which are formed by the same conductive layers. Within the MIM device, TopVia1 can be replaced with Vmim to prevent false short circuit detection.

Rule	Description	Value
MIM.a	Min. **MIM** width	**1.14**
MIM.b	Min. **MIM** space	**0.6**
MIM.c	Min. **Metal5** enclosure of **MIM**	**0.6**
MIM.d	Min. **MIM** enclosure of **TopVia1**	**0.36**
MIM.e	Min. **TopMetal1** space to **MIM**	**0.6**
MIM.f	Min. **MIM** area per MIM device (µm²)	**1.3**
MIM.g	Max. **MIM** area per MIM device (µm²)	**5625.0**
MIM.gR	Max. recommended total **MIM** area per chip (µm²)	**174800.0**
MIM.h	**TopVia1** must be over **MIM**	
MIM.i	**Via4** under **MIM** is allowed	

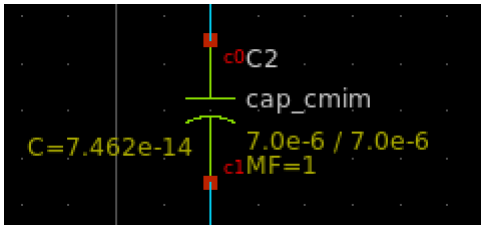
Yield Enhancement Guideline: Wherever MIM-Metal5 is tied to Activ (nSD/pSD), use TopVia1 and Top-Metal1 to perform the connection. See Fig. xx.

https://github.com/IHP-GmbH/IHP-Open-PDK/blob/main/ihp-sg13g2/libs.doc/doc/SG13G2_os_process_spec.pdf

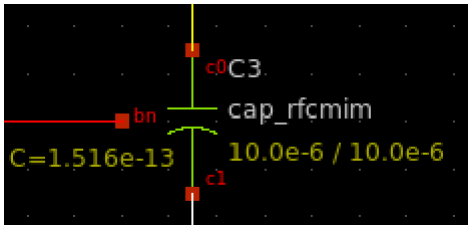
MIM Capacitor Layout



MIM Capacitor Symbols & Spice Models



Basic model, contains only main cap and small series cap. Must use PEX to get top and bottom plate parasitic cap.



RF model, contains complex network and “some” bottom plate parasitic cap (see next slide)

We’ll need to estimate parasitic caps by hand (roughly) and/or use PEX pater…

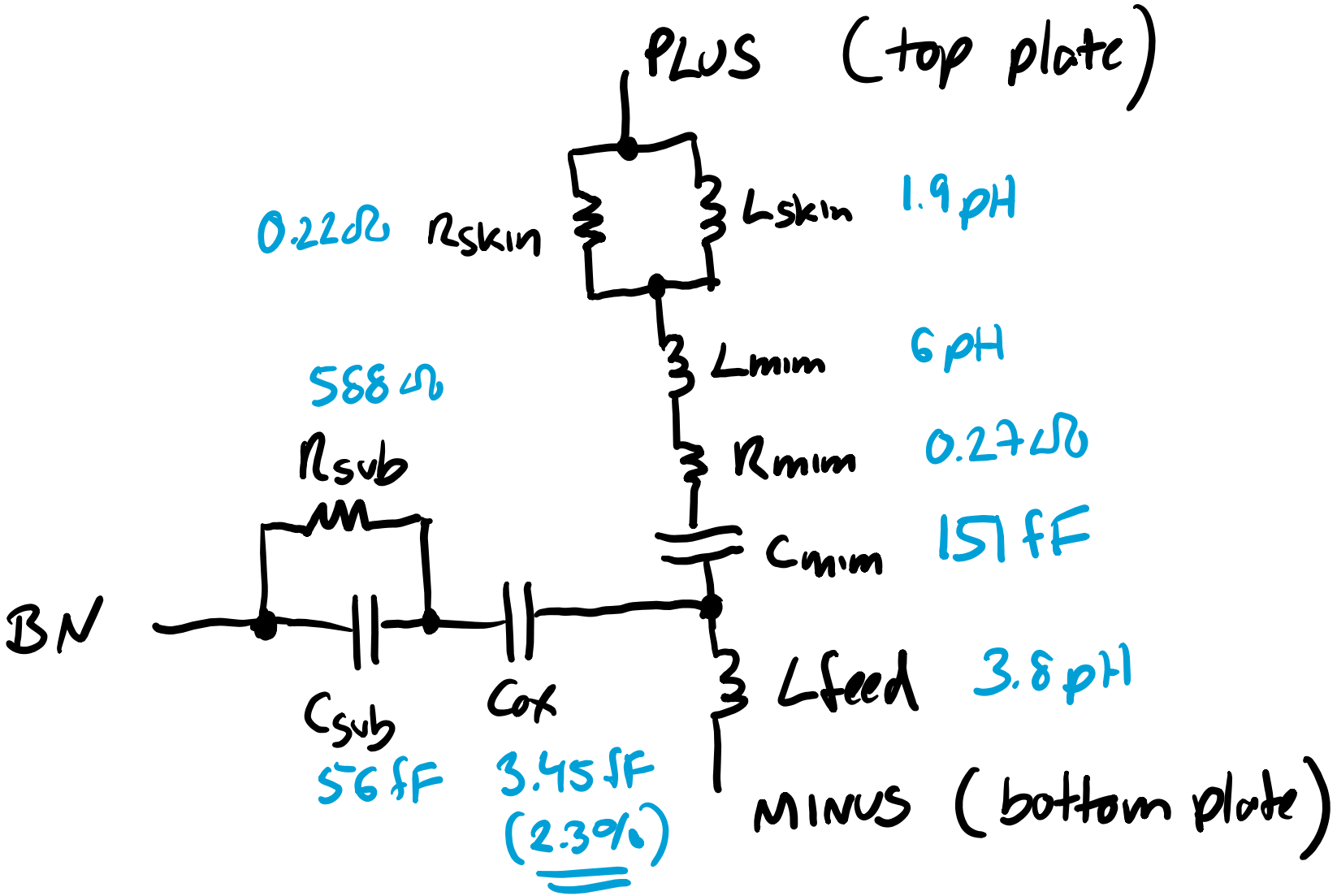
Netlist:

```
XC2 n1 n2 cap_cmim W=7.0e-6 L=7.0e-6 MF=1
XC1 n1 n2 n3 cap_rfcmim W=10.0e-6 L=10.0e-6 wfeed=5.0e-6
```

Spice library to include:

```
.lib /foss/pdks/sg13g2/libs.tech/ngspice/models/cornerCAP.lib cap_typ
```

RF MIM Cap Model



Where to Connect the "Fat Plate" (Large Parasitics)?