# Schematic & Layout Deliberations

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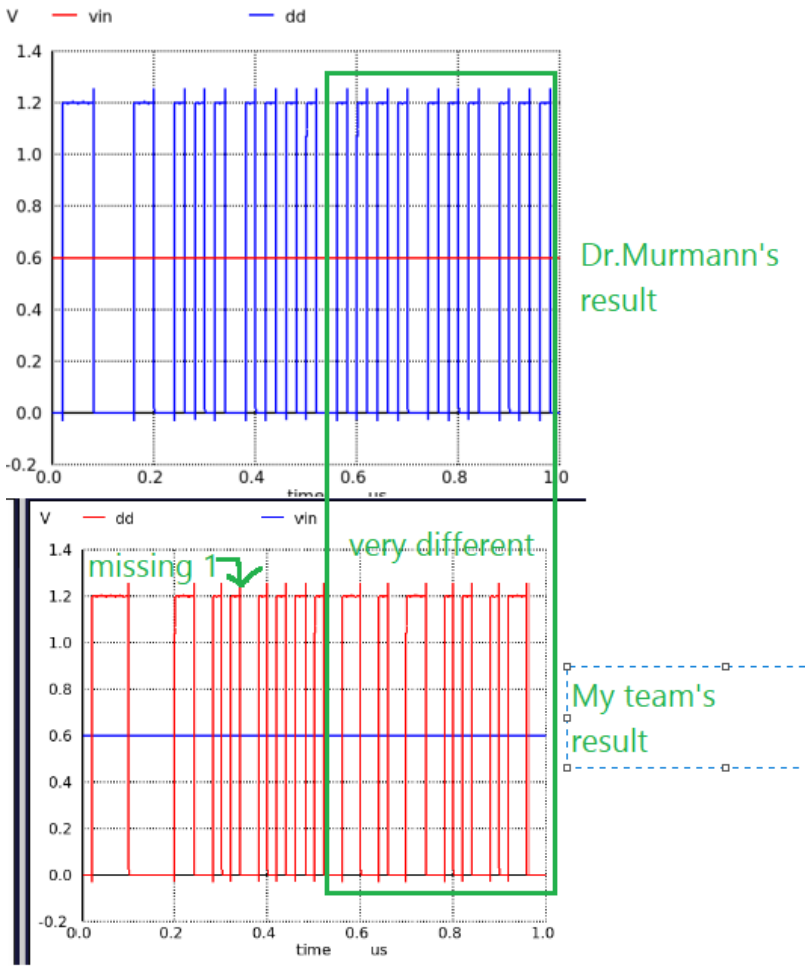
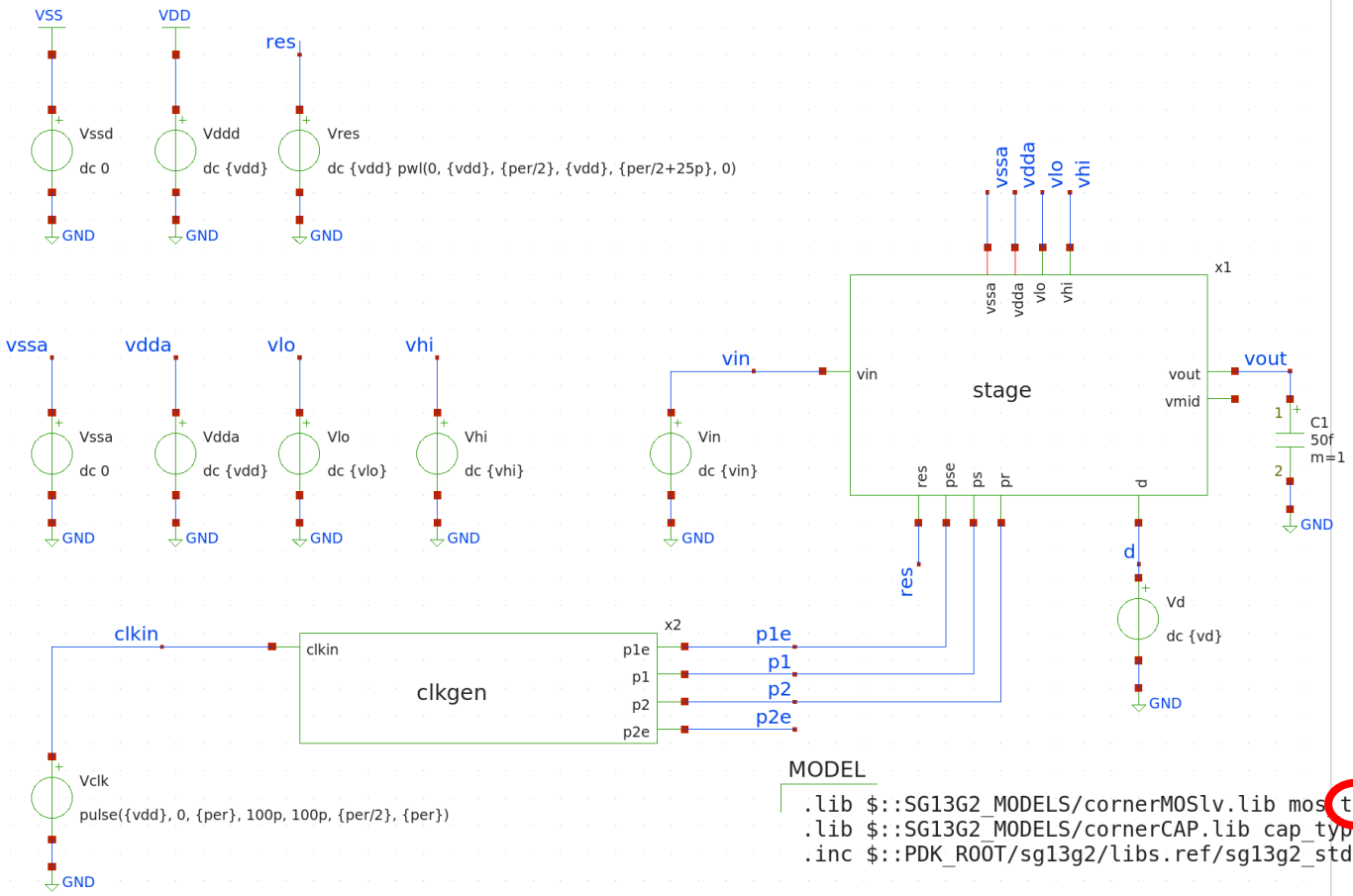
# Output Bitstream

Plots by Wannasa:




- Bit patterns may differ between different computers
- This is not a problem, but somewhat expected
- The bit pattern is very sensitive to initial conditions and small rounding errors
- Two different bit patterns can lead to the same final digital output (after decimation)

# Stage Testbench




NGSPICE

```
.param temp=27 per=20n vdd=1.2
.param vin=0.6 vlo=0.3 vhi=0.9 vd={vdd}
.option method=gear reltol=1e-4

.control
set wr_singlescale
set wr_vecnames
set color0 = white
tran 100p 60n
plot p2e vout
***
wrdata tb_stage_corners_tt.txt p2e vout
***
.endc
```

MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
.lib $::SG13G2_MODELS/cornerCAP.lib cap_typ
.inc $::PDK_ROOT/sg13g2/libs.ref/sg13g2_stdcell/spice/sg13g2_stdcell.spice
```

**tt, ss, ff**

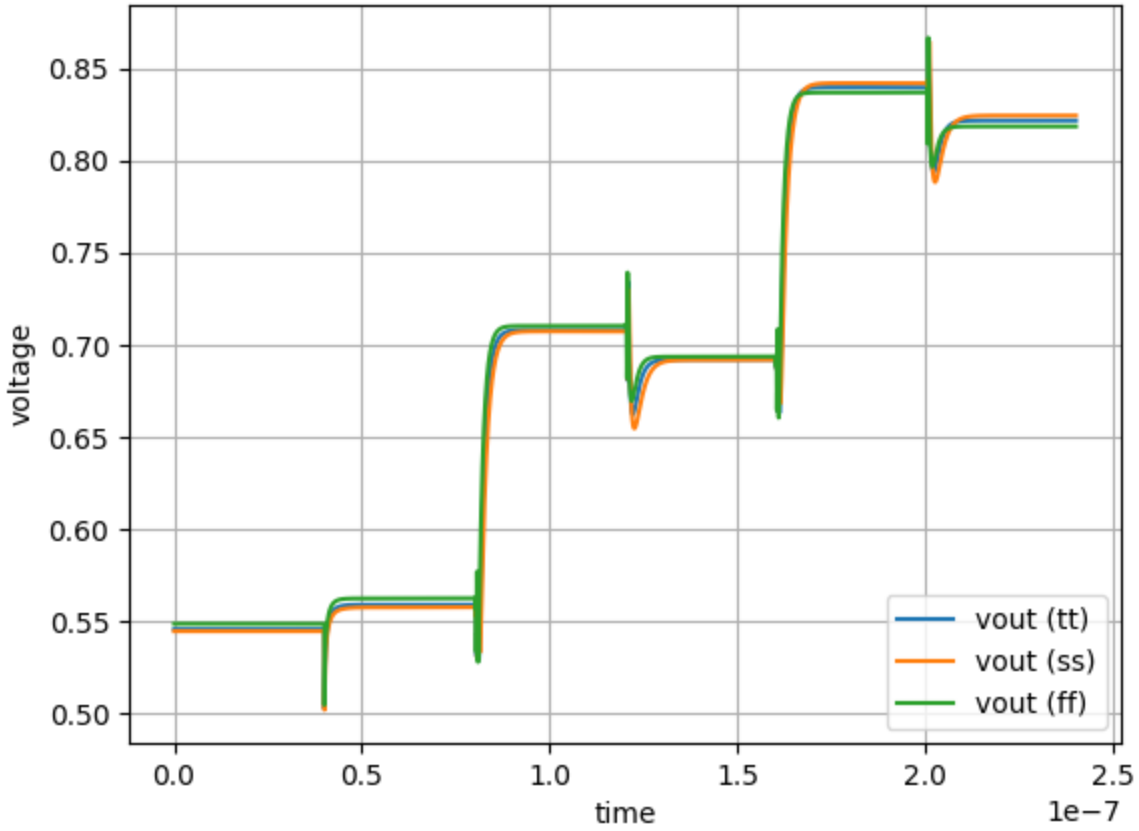
XSCHEM

Boris Murmann 2024-04-03 03:06:35

/foss/designs/tb_stage_corners.sch

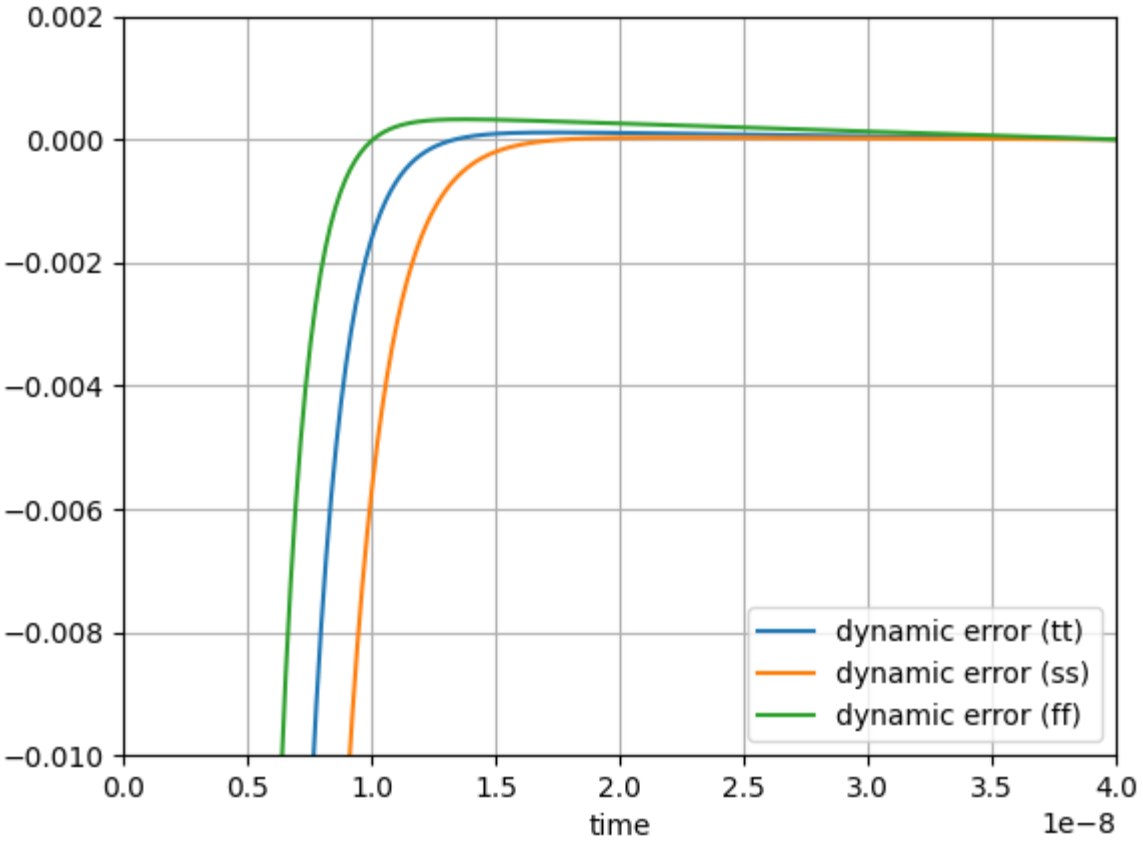
# Output with per = 80ns

https://github.com/bmurmann/EE628/blob/main/5_Design/3_Real_circuits/tb_stage_corners.ipynb



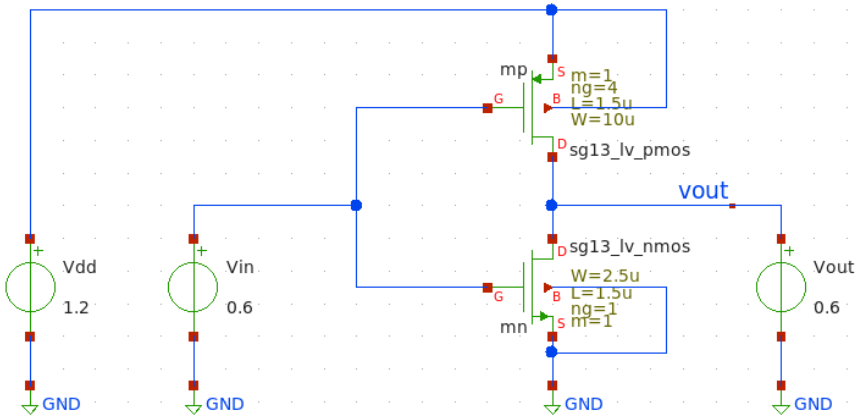
# Dynamic Error

Error = (value(t) – final) / final




Droop due to gate leakage?

# Inverter Gate Leakage Simulation




COMMANDS

```
.param temp=27

.control
dc Vin 0.2 1 1m
set color0 = white
plot i(Vin)
.endc
```

MODEL

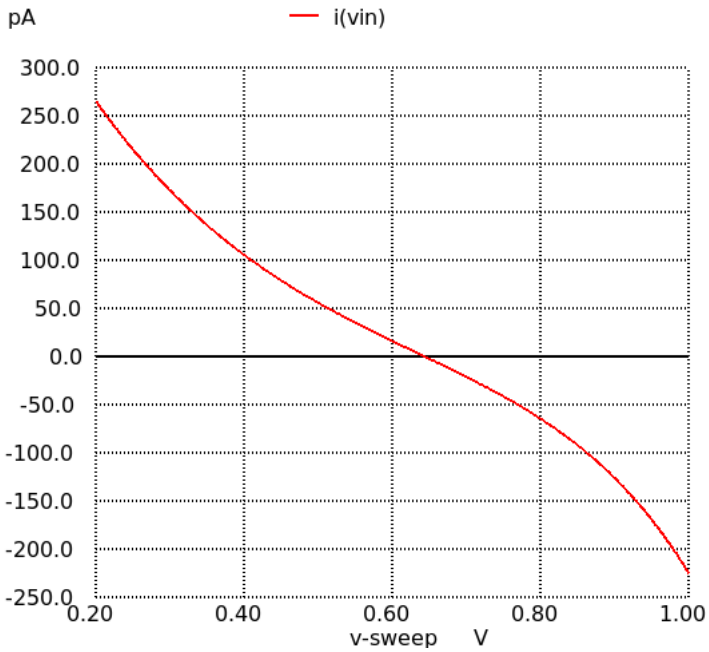
```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
```

XSCHEM

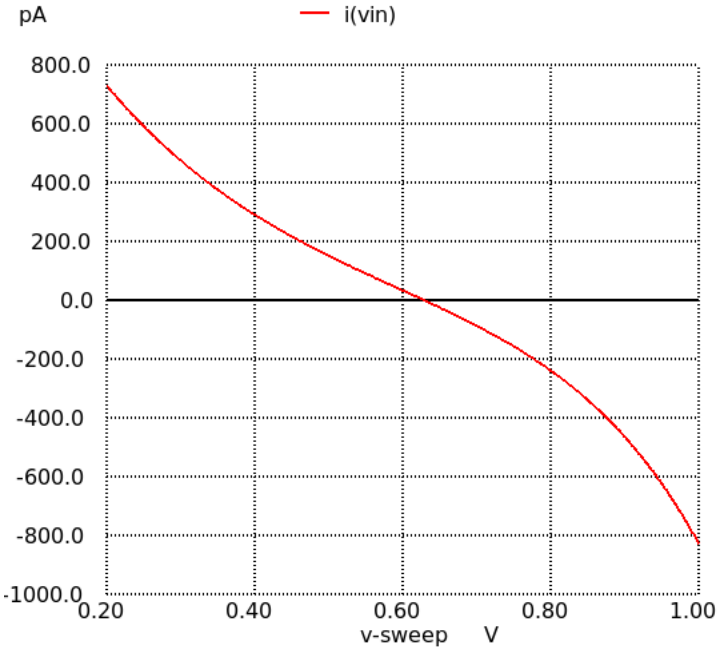
Boris Murmann 2024-04-06 03:47:23

/foss/designs/tb_inv_leak.sch

TT




FF




$$\Delta V = \frac{\Delta t \times I}{C} = \frac{30ns \times 500pA}{100\ fF} = 150\mu V \qquad \frac{150\mu V}{800mV} = 0.0002 = 0.02\%$$

Explains the observed droop

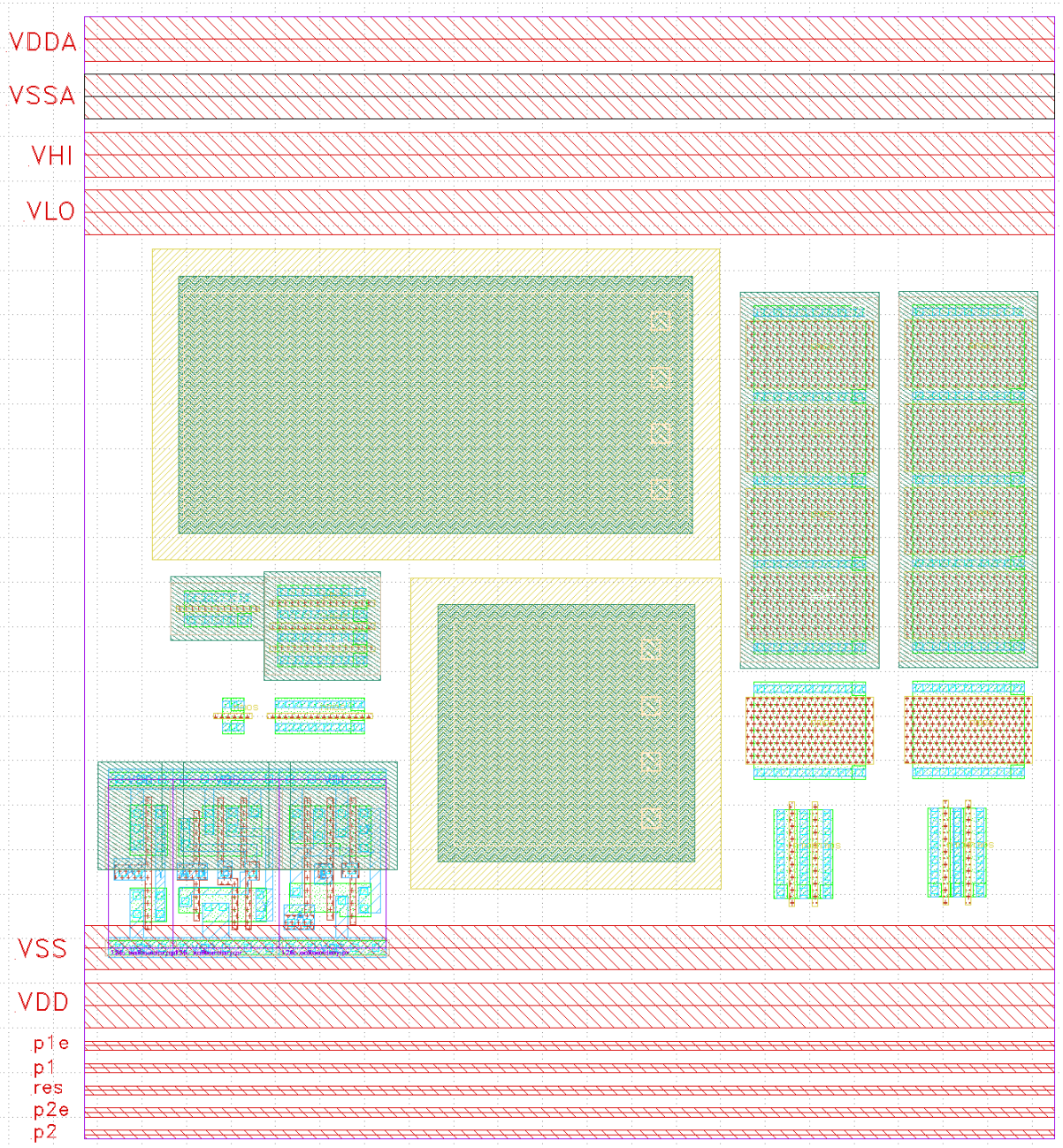
# How Slow Can We Go?

- We will lose the inverter operating point if we drift by voltages on the order of 100mV at the gate (driven by 100fF capacitor)

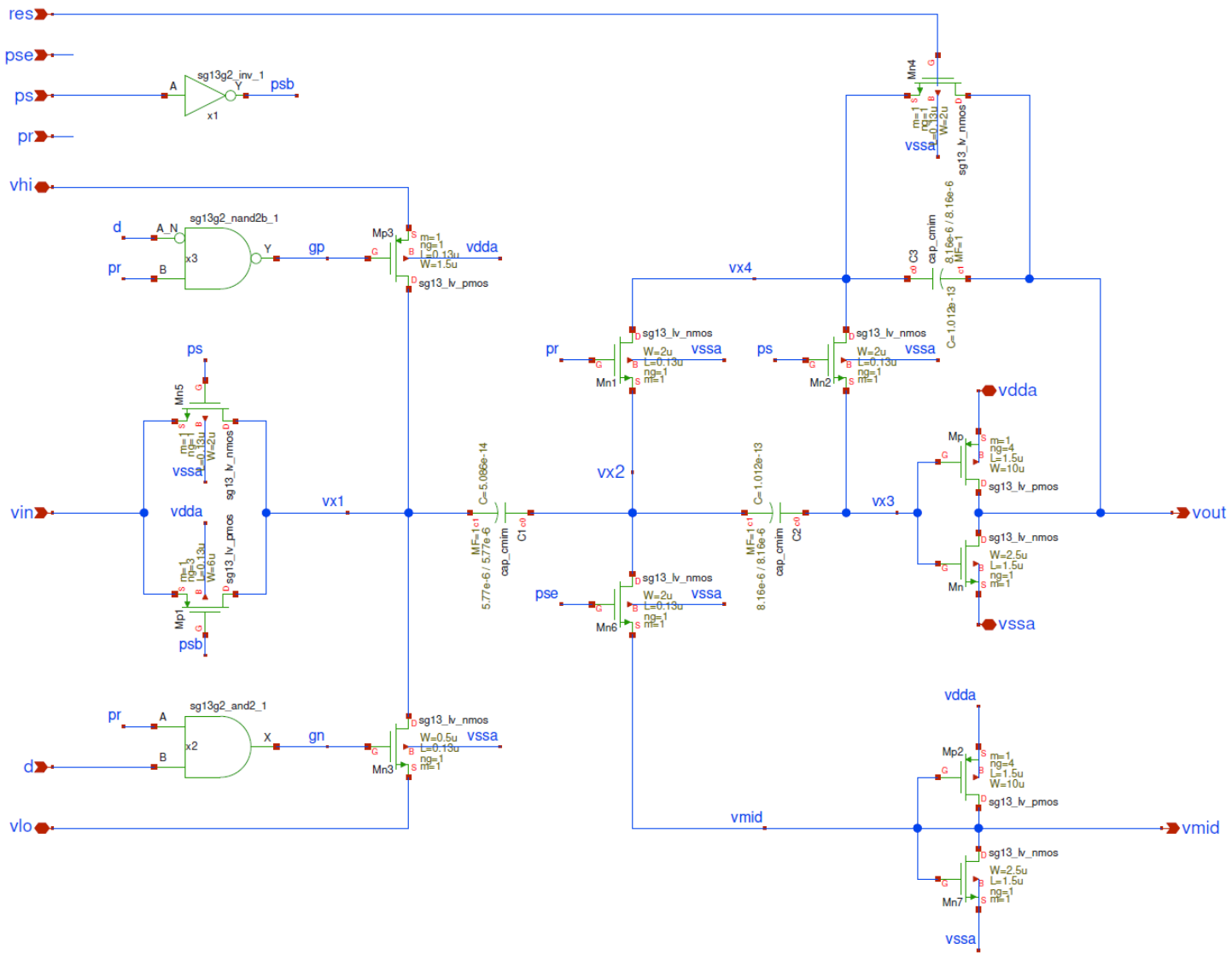
$$\Delta t = \frac{C \times \Delta V}{I} = \frac{100fF \times 100mV}{500pA} = 20\mu s$$

$$f_{clk,min} = \frac{1}{2\Delta t} = 250kHz$$

Sample floorplan for “stage”



# Schematic


res
pse
ps
pr
vhi
vlo
vin
vout
vmid
vdda
vssa
psb
sg13g2_inv_1
x1
sg13g2_nand2b_1
x3
Mp3
gp
sg13_lv_pmos
sg13g2_and2_1
x2
gn
Mn3
sg13_lv_nmos
Mn5
Mp1
vx1
vx2
vx3
vx4
C1
C2
C3
cap_cmim
Mn1
Mn2
Mn4
Mn6
Mn7
Mp
Mp2

# A Few Tips

- Enlarge your drawing grid to simplify placement and routing at larger scales (e.g., as large as 50nm)
- Navigation → Zoom & Pan → On Paste → Don’t Change View
- Use M1 and Poly only for extremely short routes between adjacent devices
- Decide on routing directions for upper metal layers, e.g., M2 vertical, M3 horizontal, etc.
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