# Chip I/O

**Boris Murmann**

**bmurmann@hawaii.edu**

# Grid Issues

**KrzysztofHerman** commented 2 weeks ago — Contributor · · ·

@**bmurmann** thank you for the comment. After some other issues with XOR cross checking of our PyCells against cells generated using commercial tools we also discovered some inconsistencies in the behavior of the tools. We will probably bring back the value of 1nm.

☺

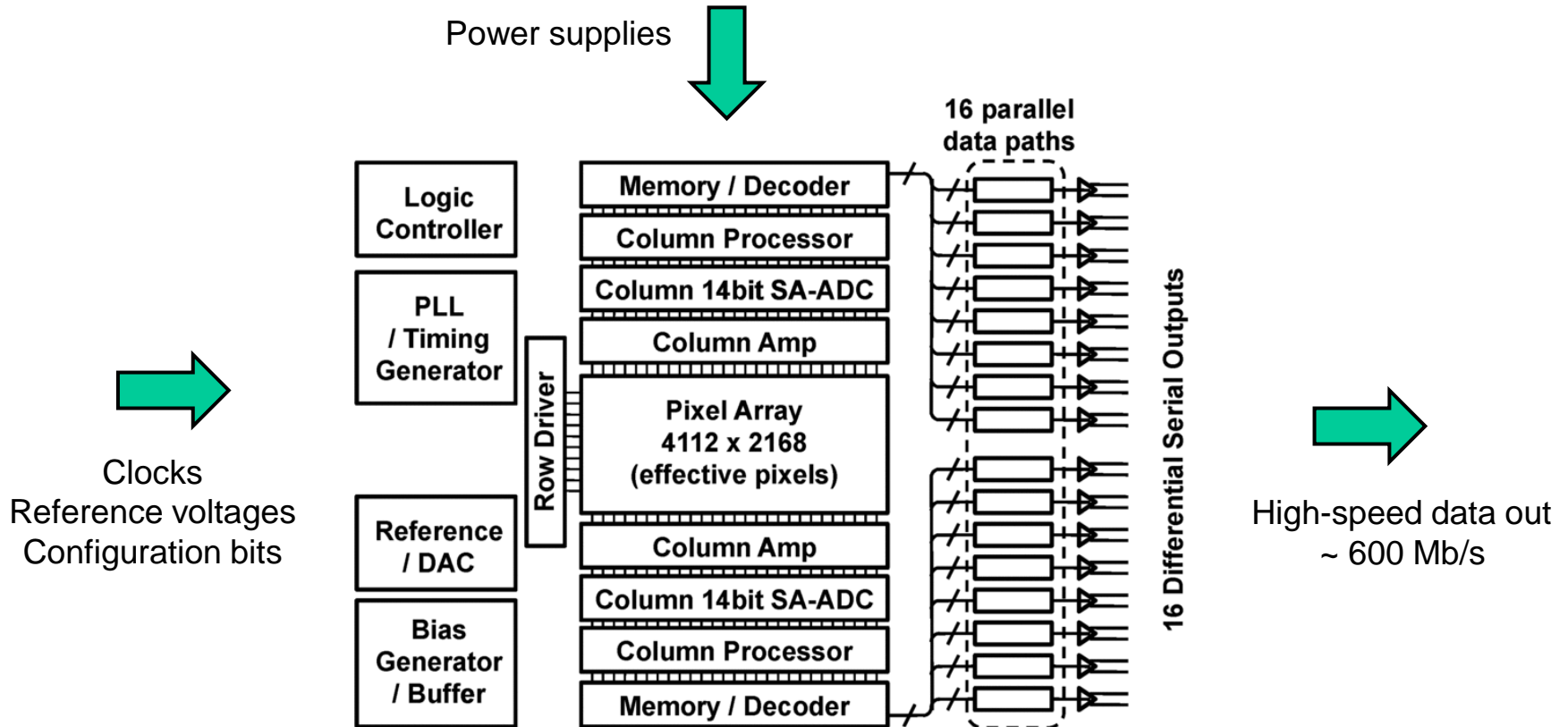**sergeiandreyev** commented last week · edited ▾ — Contributor · · ·

the DBU and grid are different in their purpose and setting, both in commercial PDK and in KLayout, so we decided to rollback the changes (the dbu parameter in KLayout is changed back to 1nm)
regarding the [manufacturing] grid, we still have to understand what is the best way to show/force the users to use 5nm grid when drawing layouts..
and of course, there are several offGrid checks that we have already as part of DRC rule deck - these should find violations and actually enforce the usage of correct grid setting
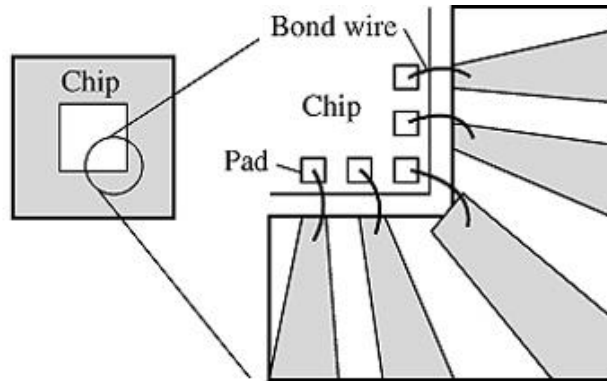
☺

Best bet: Place all your cells on a coarse grid, say 10 nm.

# Chip I/O – Image Sensor Example

Power supplies

16 parallel data paths

Clocks
Reference voltages
Configuration bits

Logic Controller

PLL / Timing Generator

Reference / DAC

Bias Generator / Buffer

Row Driver

Memory / Decoder

Column Processor

Column 14bit SA-ADC

Column Amp

Pixel Array
4112 x 2168
(effective pixels)

Column Amp

Column 14bit SA-ADC

Column Processor

Memory / Decoder

16 Differential Serial Outputs

High-speed data out
~ 600 Mb/s

[Takayanagi, Proc. IEEE, 2013]

# Chip Packaging Options



(a) Dual-inline packaging

Bond wire resistance ~50-100 m$\Omega$/mm

Bond wire inductance ~1 nH/mm
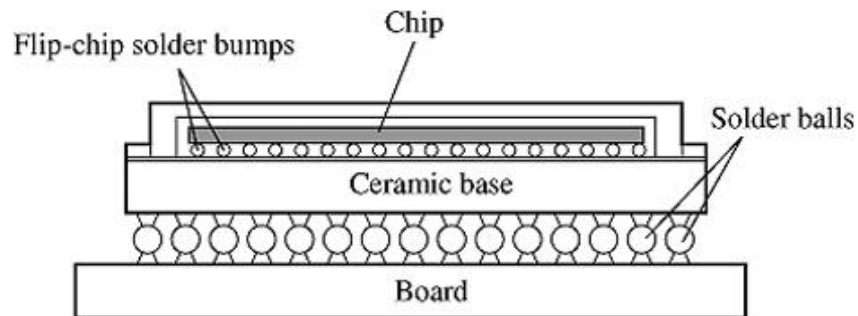


(b) Ball grid array packaging

Solder bump resistance ~2 m$\Omega$

Solder bump inductance ~0.1 nH

# Latest Trend: Chiplets & Advanced Packaging
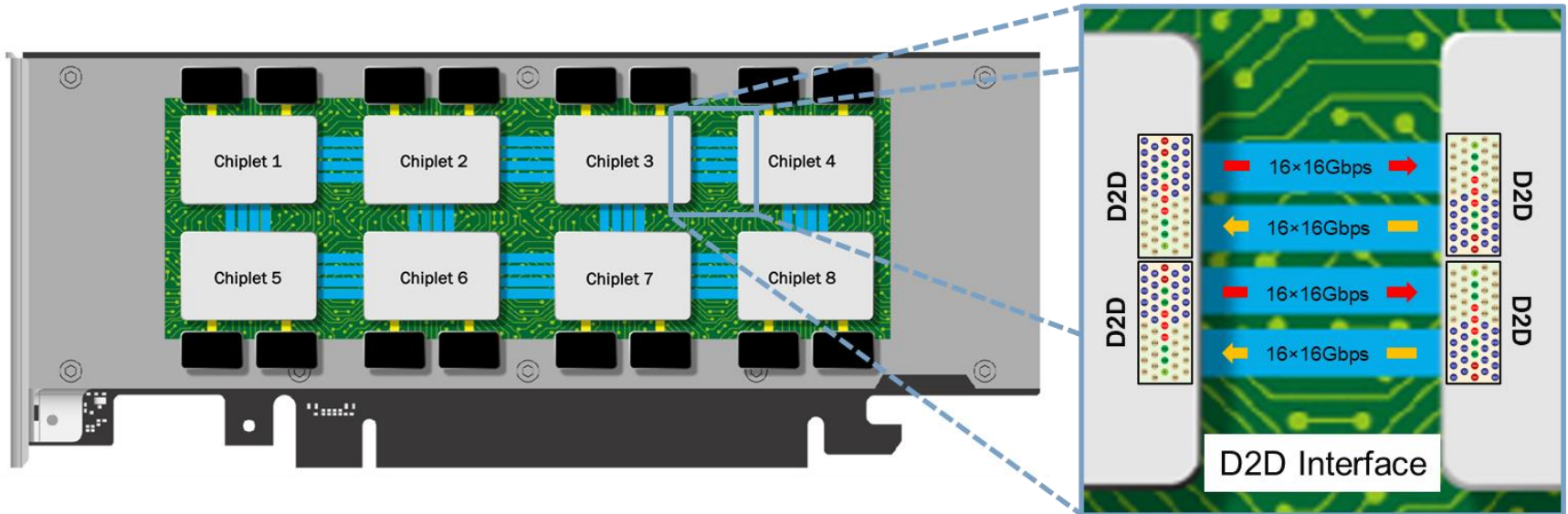


**Beachfront bandwidth:**
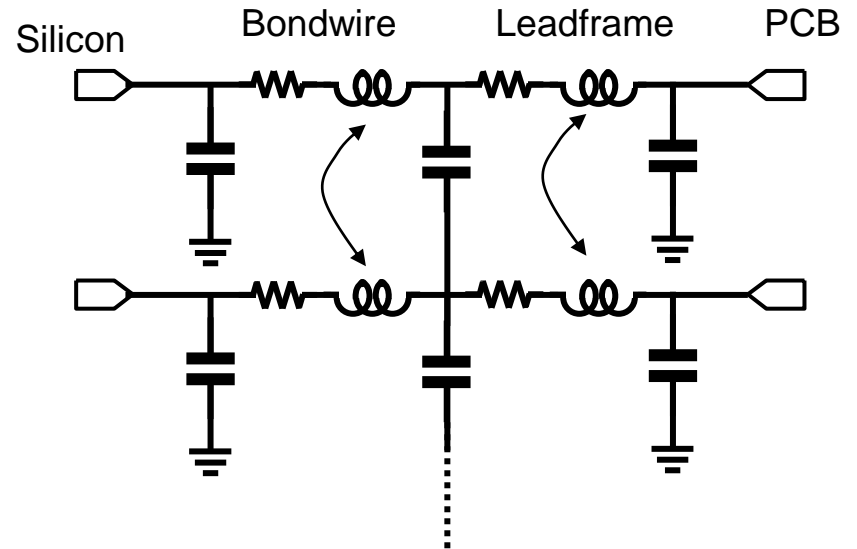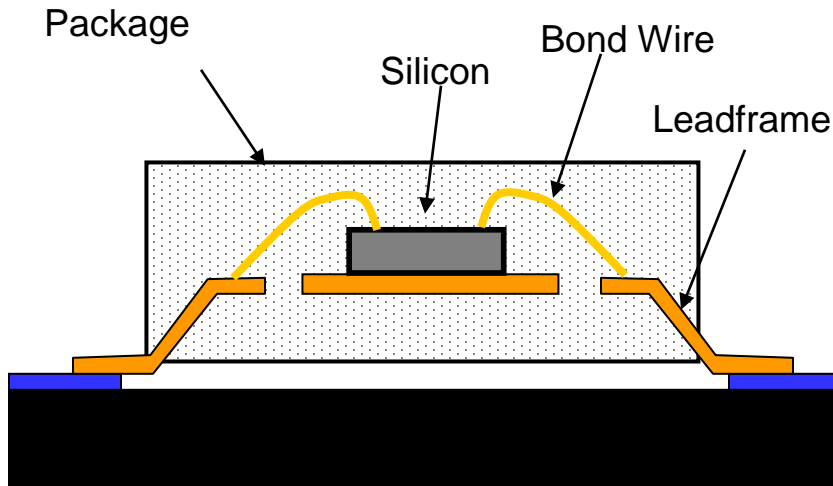0.19 Tbps/mm (single-stack design),
up to 0.75 Tbps/mm (4-stack design)

[Sheth & Liew, Chiplet Summit 2023]

# Routing Approach
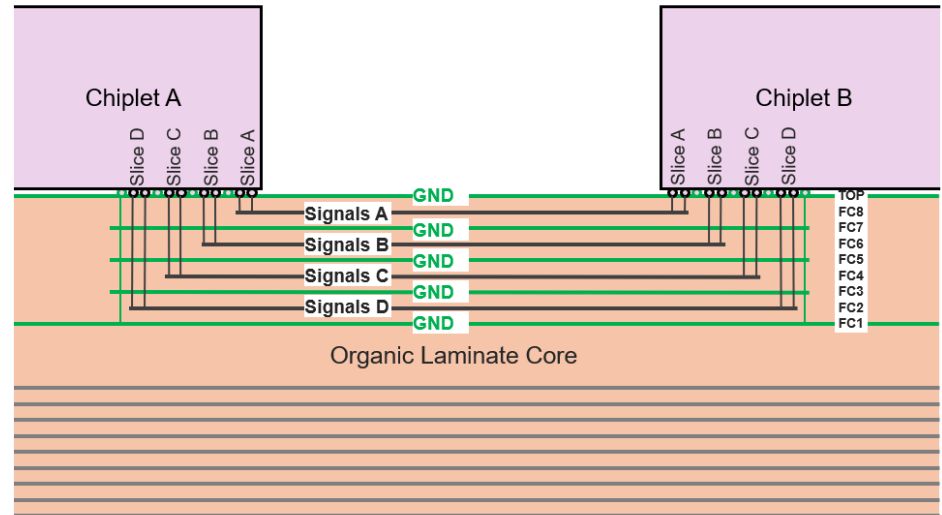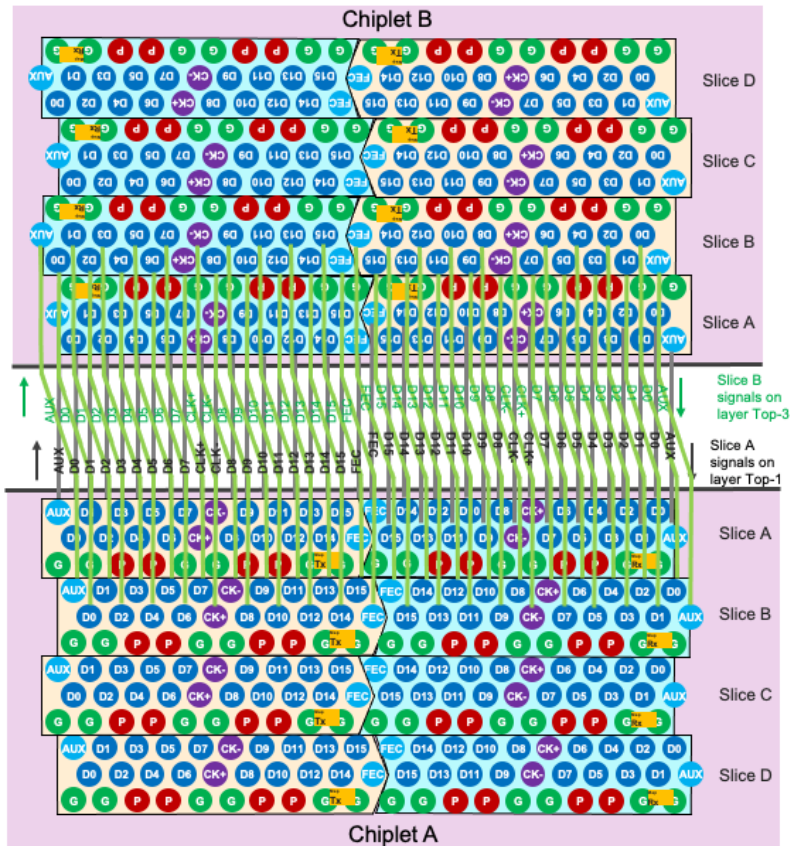


https://opencomputeproject.github.io/ODSA-BoW/bow_specification.html

# Bondwire Packaging: Coupling Issues for Analog



- Sensitive analog signals can suffer from inductive/capacitive coupling

- Must carefully plan pin locations

- Often best to keep sensitive signals on chip (if possible)
  - One may be tempted to bring bias voltages/currents off chip for manual tweaking/tuning

# Supply Bounce Due to CMOS Output Drivers



$$V_g(t) = L\frac{di_g(t)}{dt}$$

Example: $\quad V_P = 5nH\dfrac{50mA}{1ns} = 250mV$
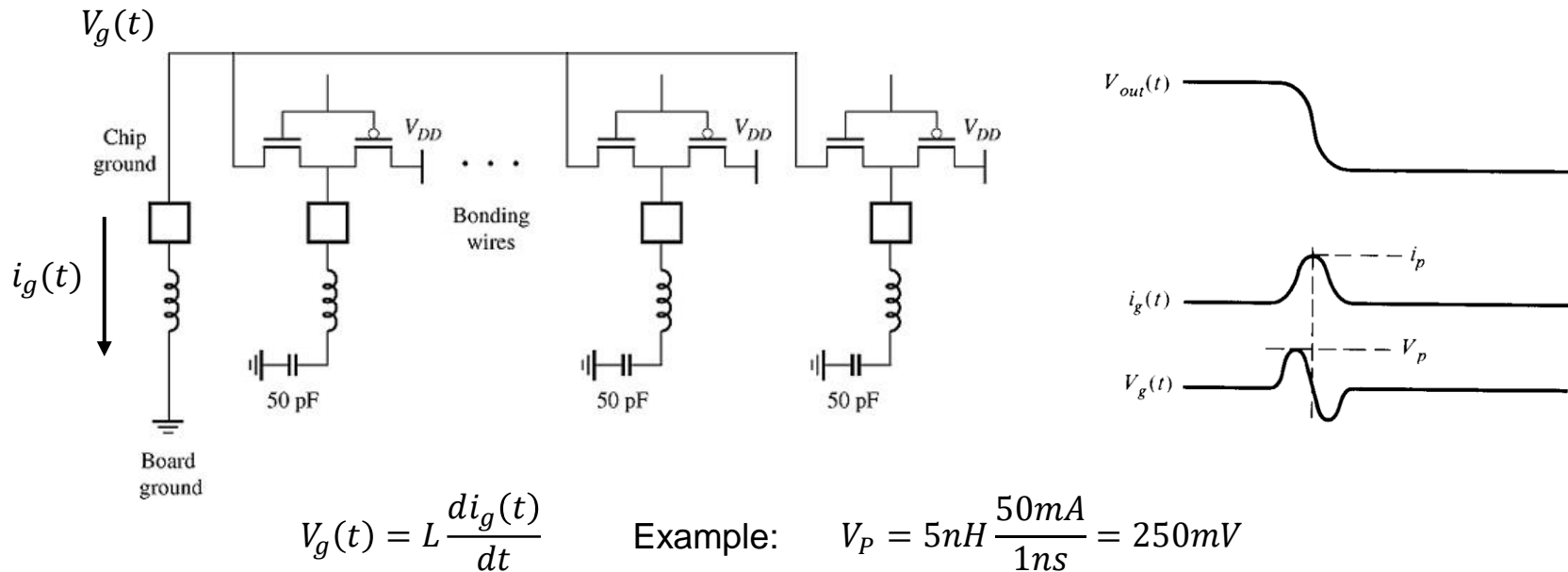
- Minimize inductance in power and ground path

- Reduce off-chip capacitive loads as much as possible

- Design output drivers with deliberately slow rise and fall times

- Separate analog and digital supplies

# Short Circuit Currents in CMOS Output Drivers

$C_L = 10pF$
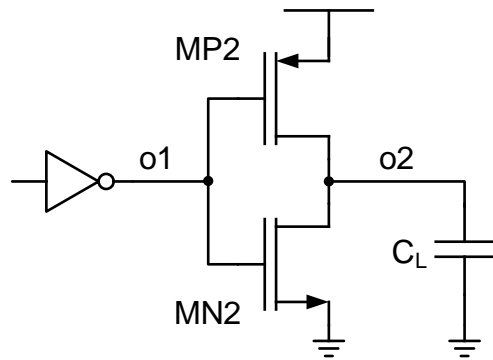
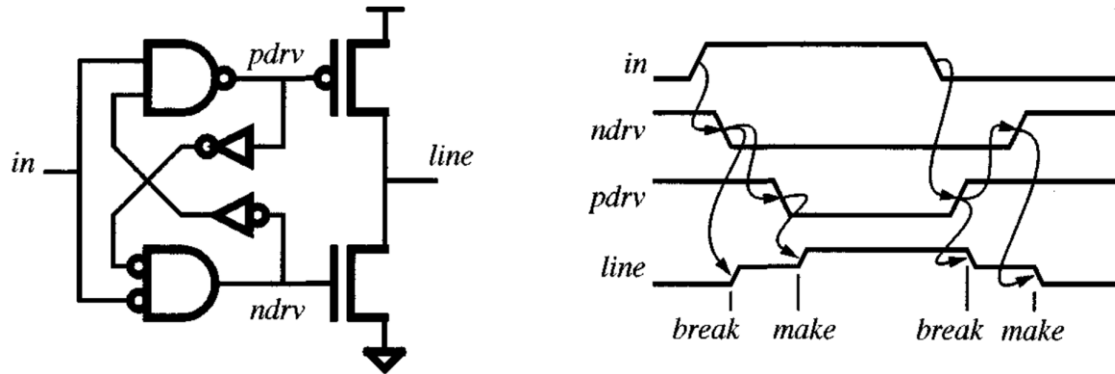- Relatively small short circuit current as long as output falls slower than input rises

# Short Circuit Currents in CMOS Output Drivers



$C_L = 0.5pF$
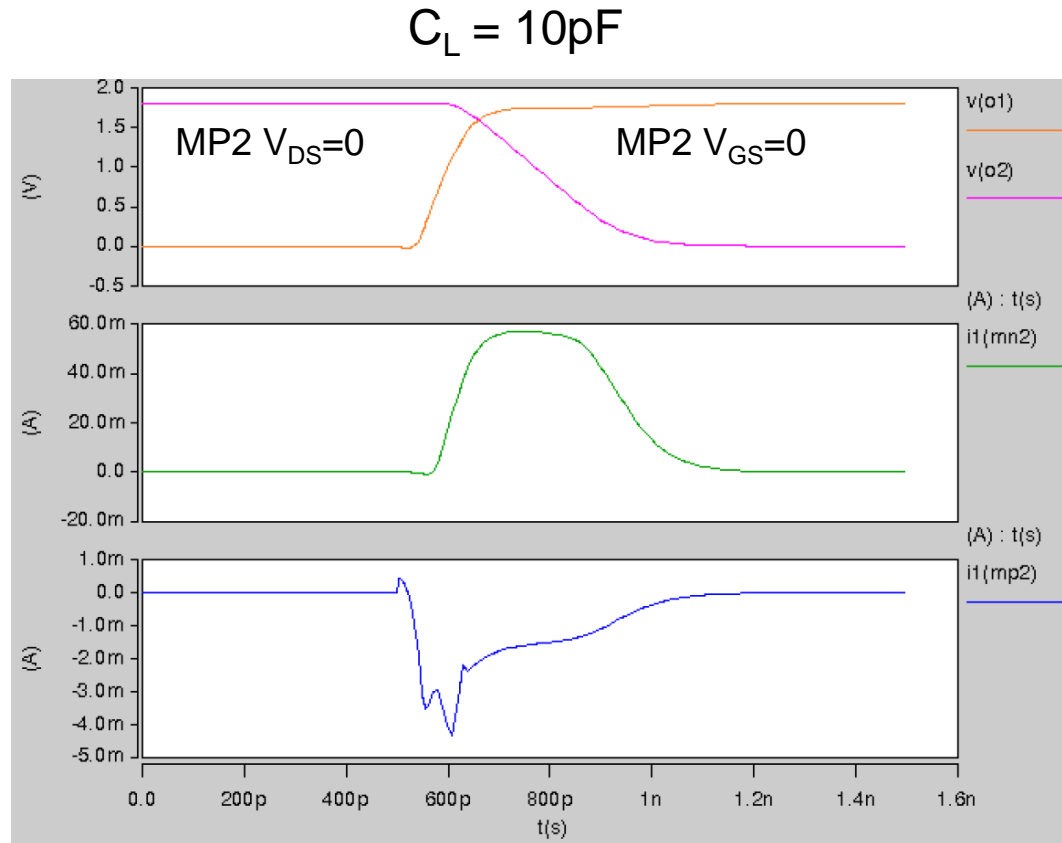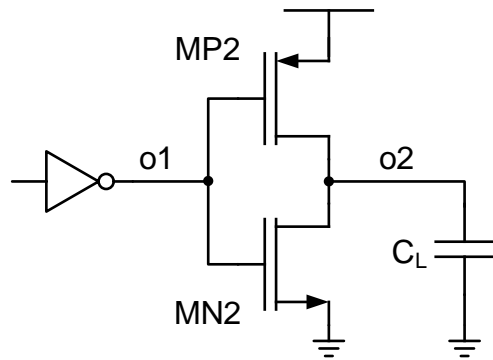
- Short circuit becomes large if output falls faster than input rises
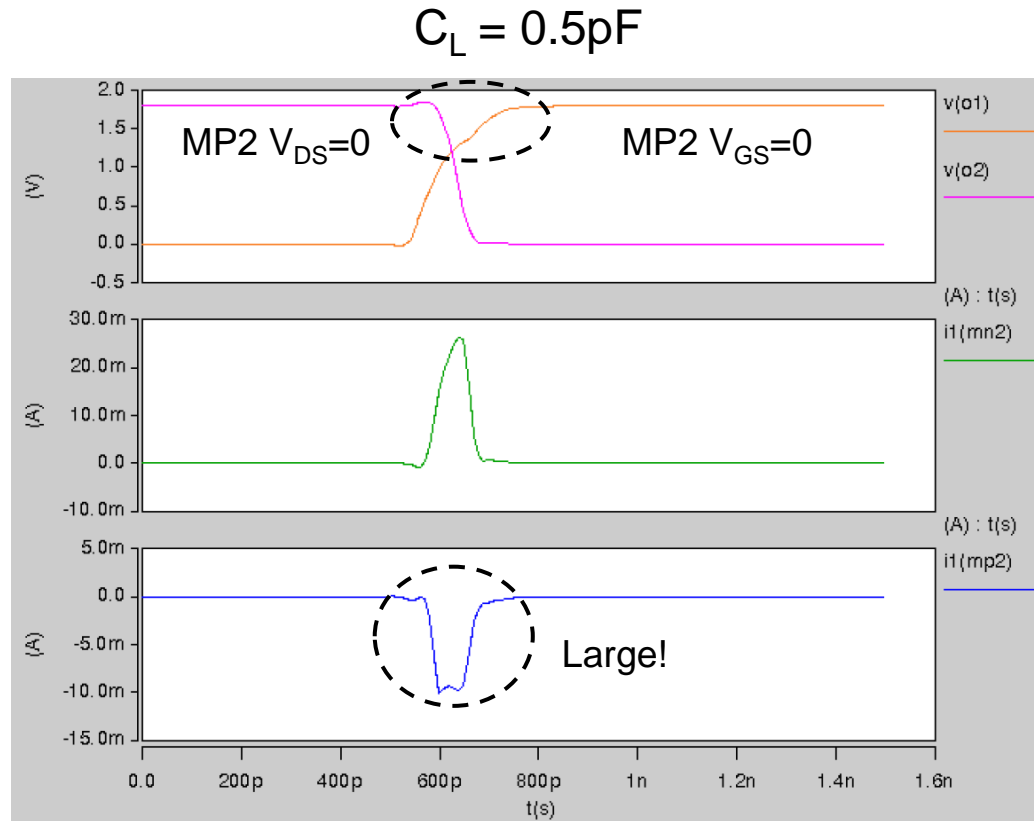
# Eliminating Short Circuit Currents in CMOS Output Drivers

[Dally & Poulton, Digital Systems Engineering, 2012]

- "Break before make" timing
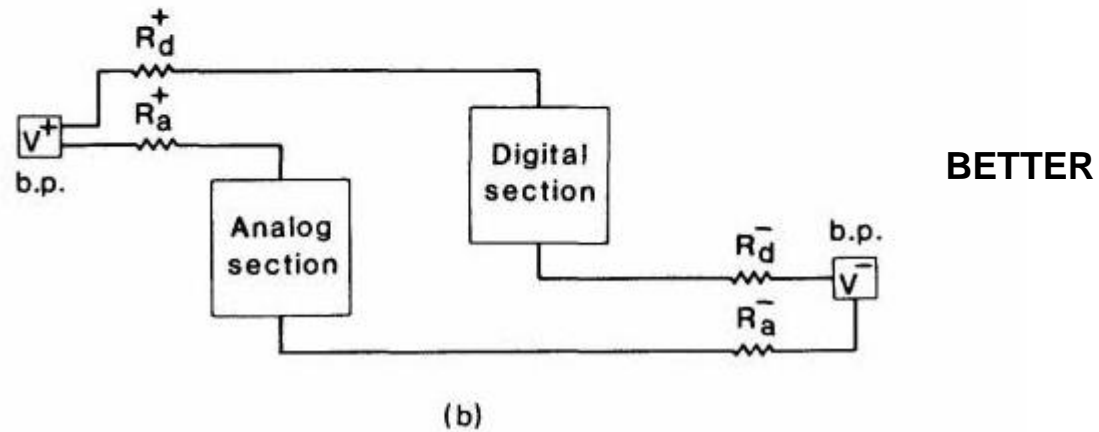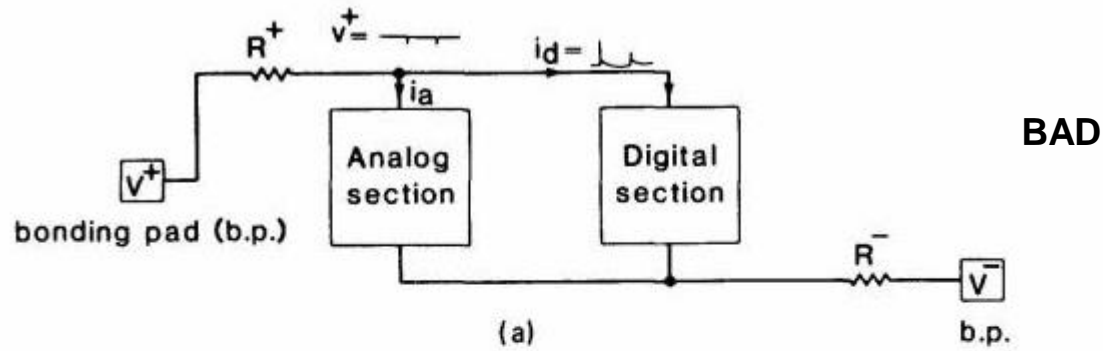  - Turn PMOS off before NMOS turns on (and vice versa)

# Noise Coupling from Digital I/O (Imager Example)
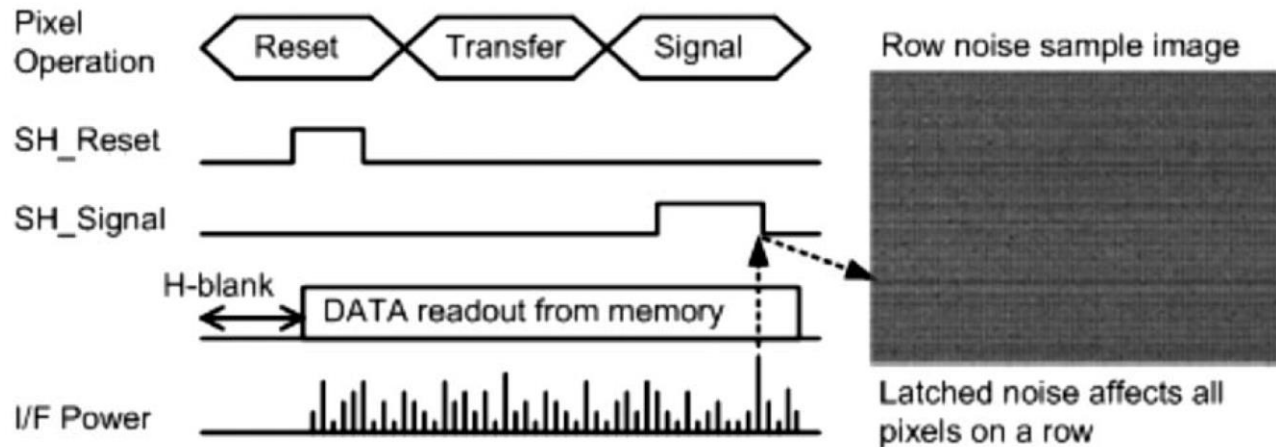


[Takayanagi, Proc. IEEE, 2013]

- Even with the best CMOS output buffer design, some coupling from the output driver to sensitive analog circuitry may occur

# Coupling Mechanism Example



**BAD**

**BETTER**

[Gregorian & Temes, p. 515]

# Proper Ground Separation
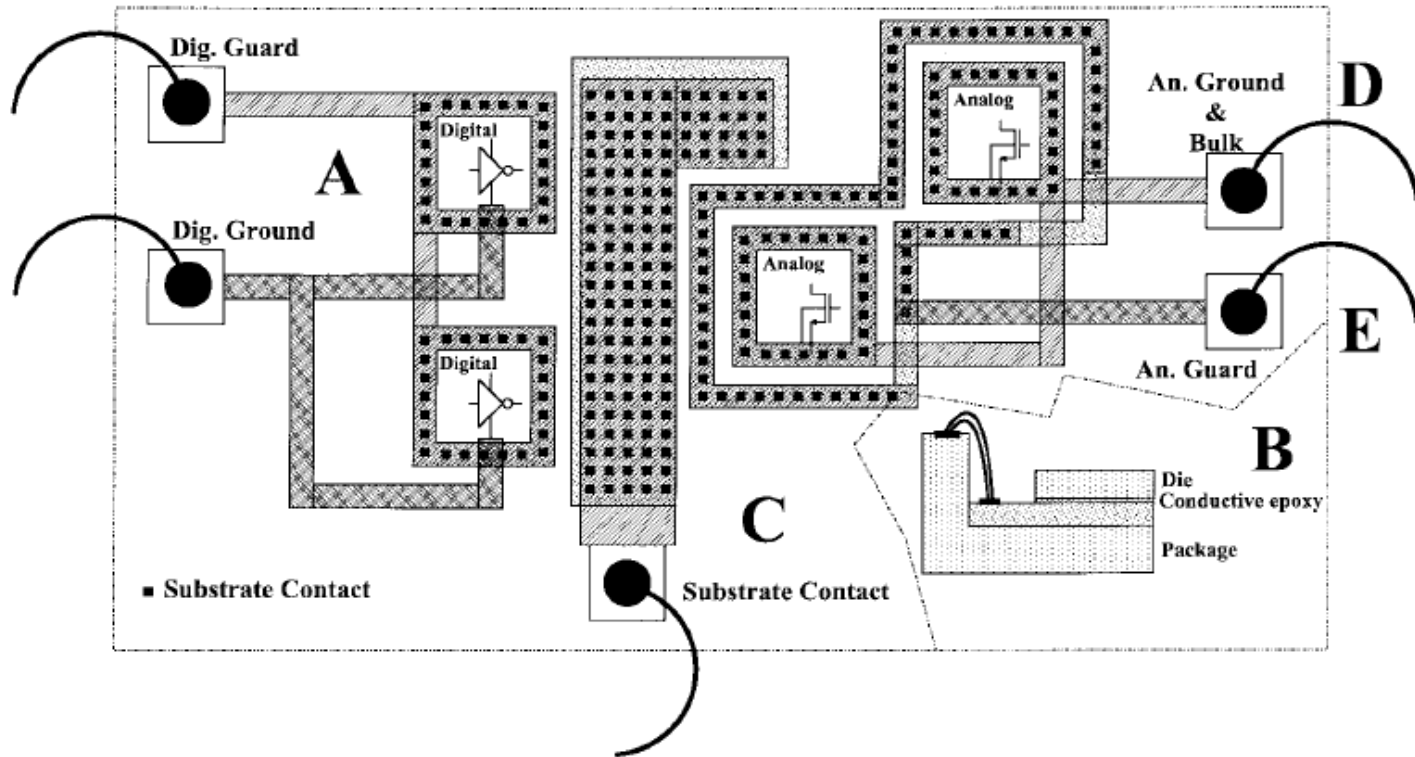


M. Ingels and M.S.J. Steyaert, "Design strategies and decoupling techniques for reducing the effects of electrical interference in mixed-mode IC's," IEEE J. Solid-State Circuits, pp.1136-1141, July 1997.

# Output Buffer Options
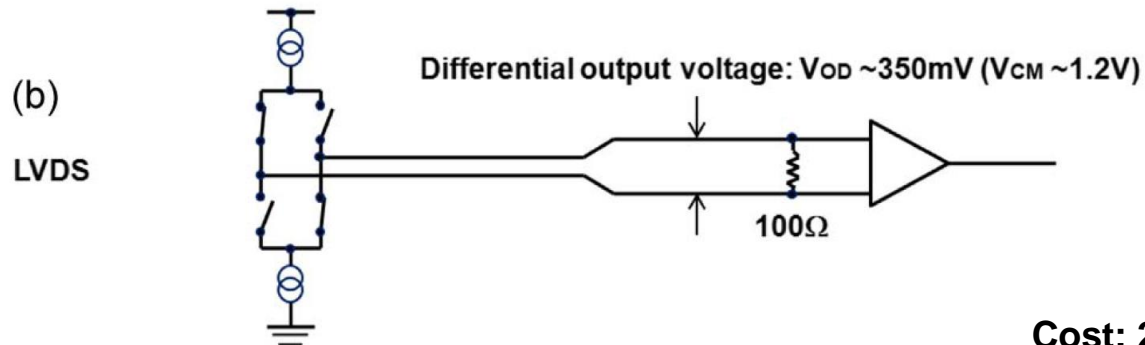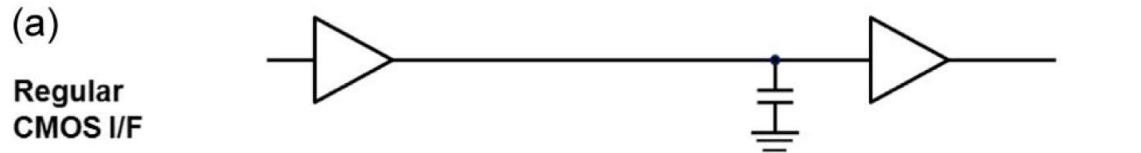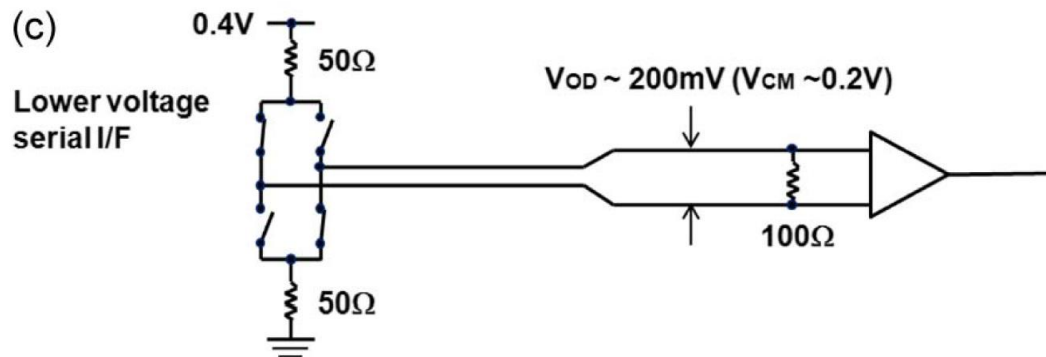


[Takayanagi, Proc. IEEE, 2013]

# LVDS Output Drivers
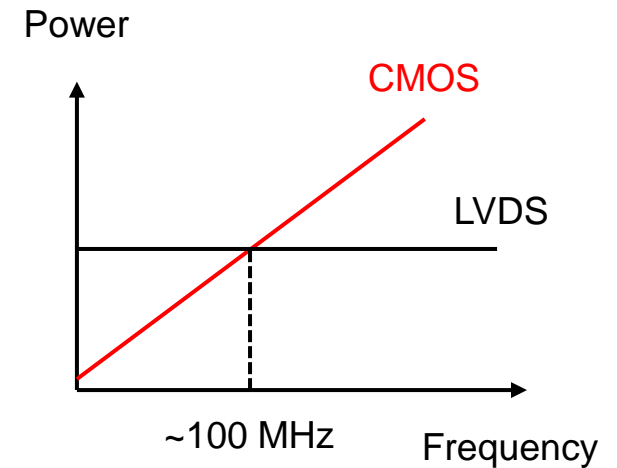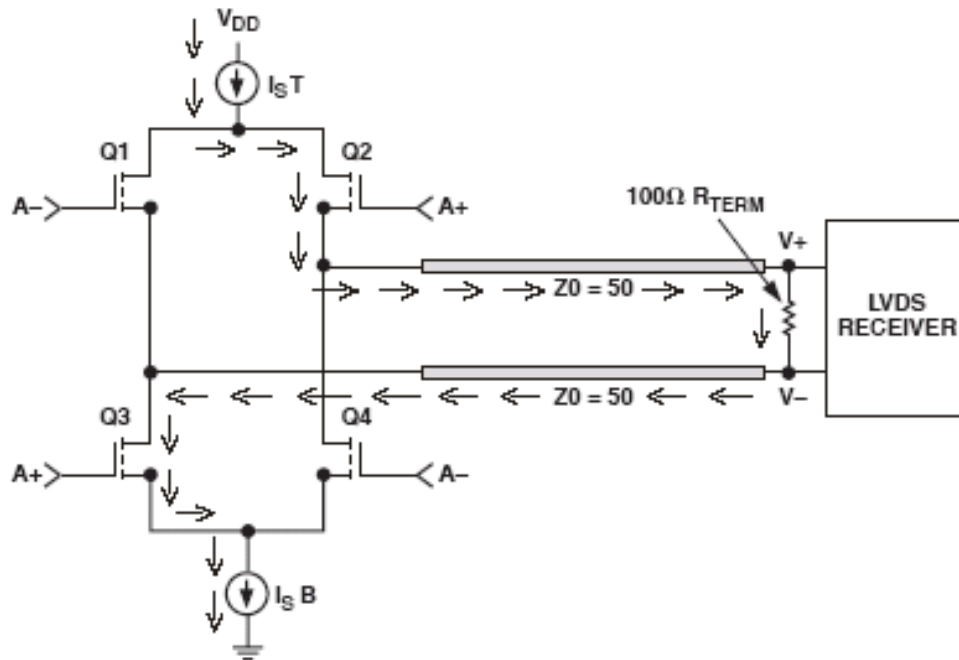


Analog Devices Application Note 586**:** "LVDS Data Outputs for High Speed ADCs"

# Electrostatic Discharge (ESD)

- Example: Charge built up on human body while walking on carpet

- Charged objects near or touching IC pins can discharge through on-chip devices

- Without dedicated protection circuitry, ESD events are destructive
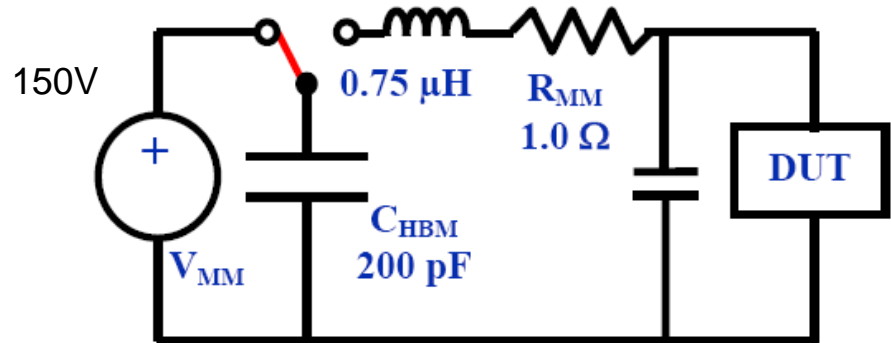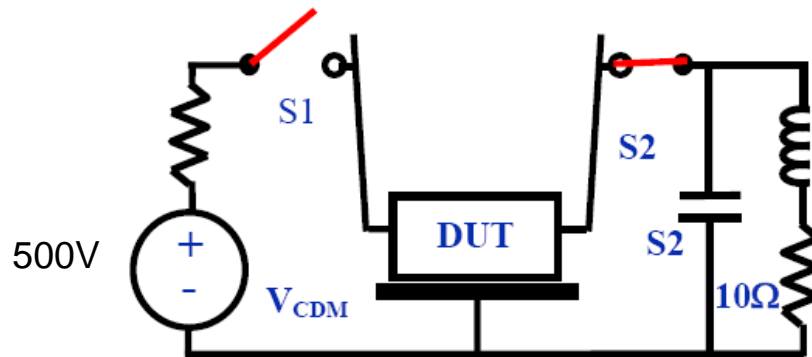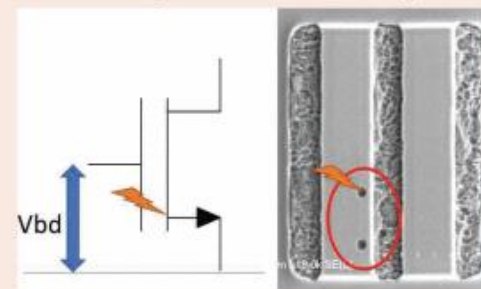
# Models
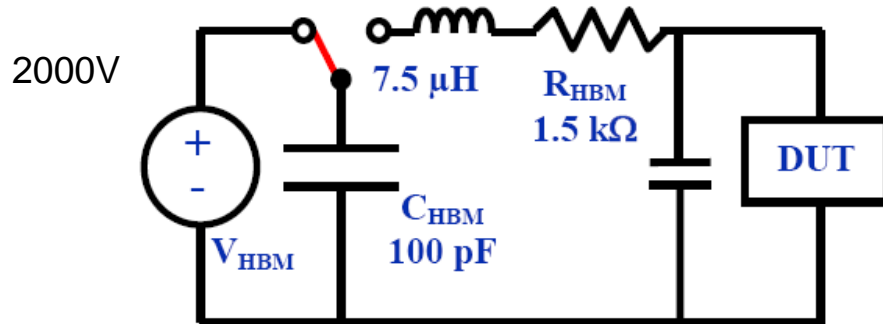


Figure 2.1: Human Body Model (HBM)



Figure 2.2: Machine Model (MM)
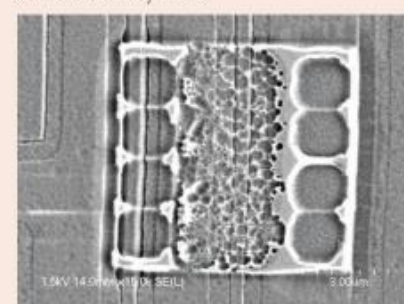


Figure 2.3: Charged Device Model (CDM)

http://www-tcad.stanford.edu/tcad/pubs/theses/chun.pdf

# ESD Current & Damage Examples
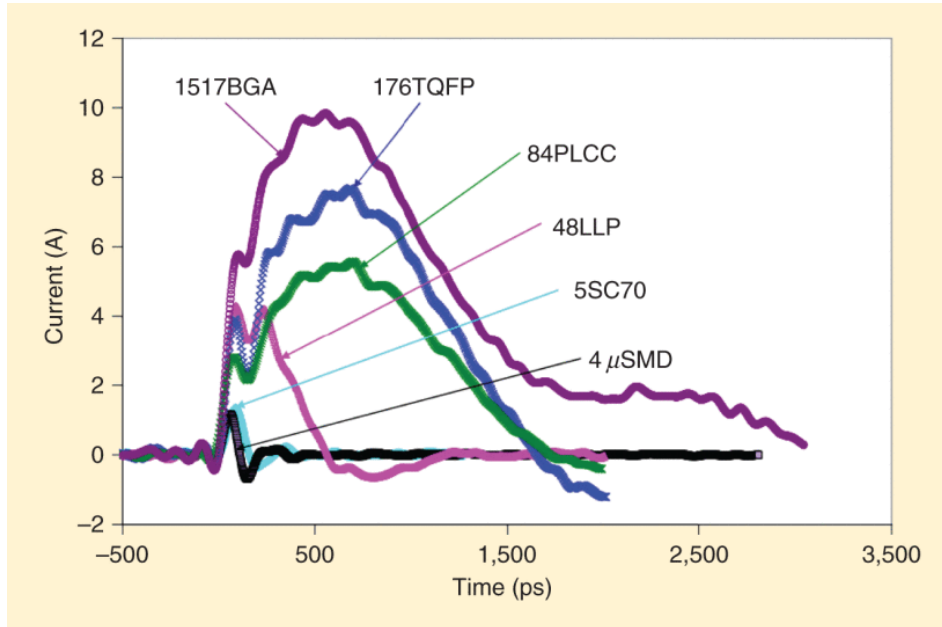


A. Concannon, "Evolution of ESD Robust IC Design: How ESD design and ESD control have changed our industry," in IEEE Solid-State Circuits Magazine, vol. 15, no. 4, pp. 58-63, Fall 2023, https://ieeexplore.ieee.org/document/10320105



| VICTIM | PHYSICAL DAMAGE |
|---|---|
| Gate oxide | Pinhole in the gate oxide at the source edge |
| Parasitic NPN | Junction damage due to NPN snapback |
| Interconnect | Contact via and routing damage due to exceeding current density limits |

# Basic Idea of Protection Circuit
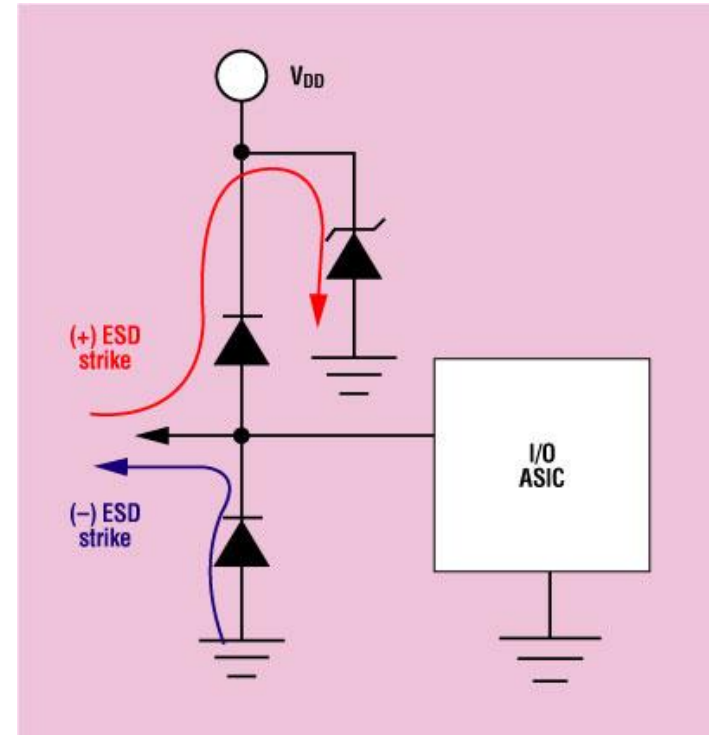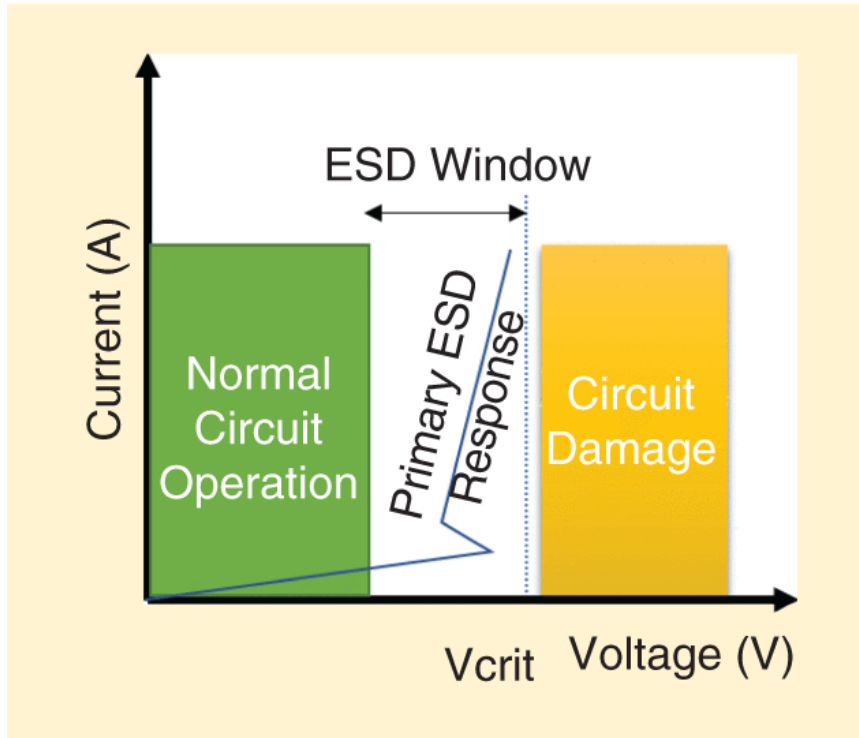
# Complete ESD Protection Scheme
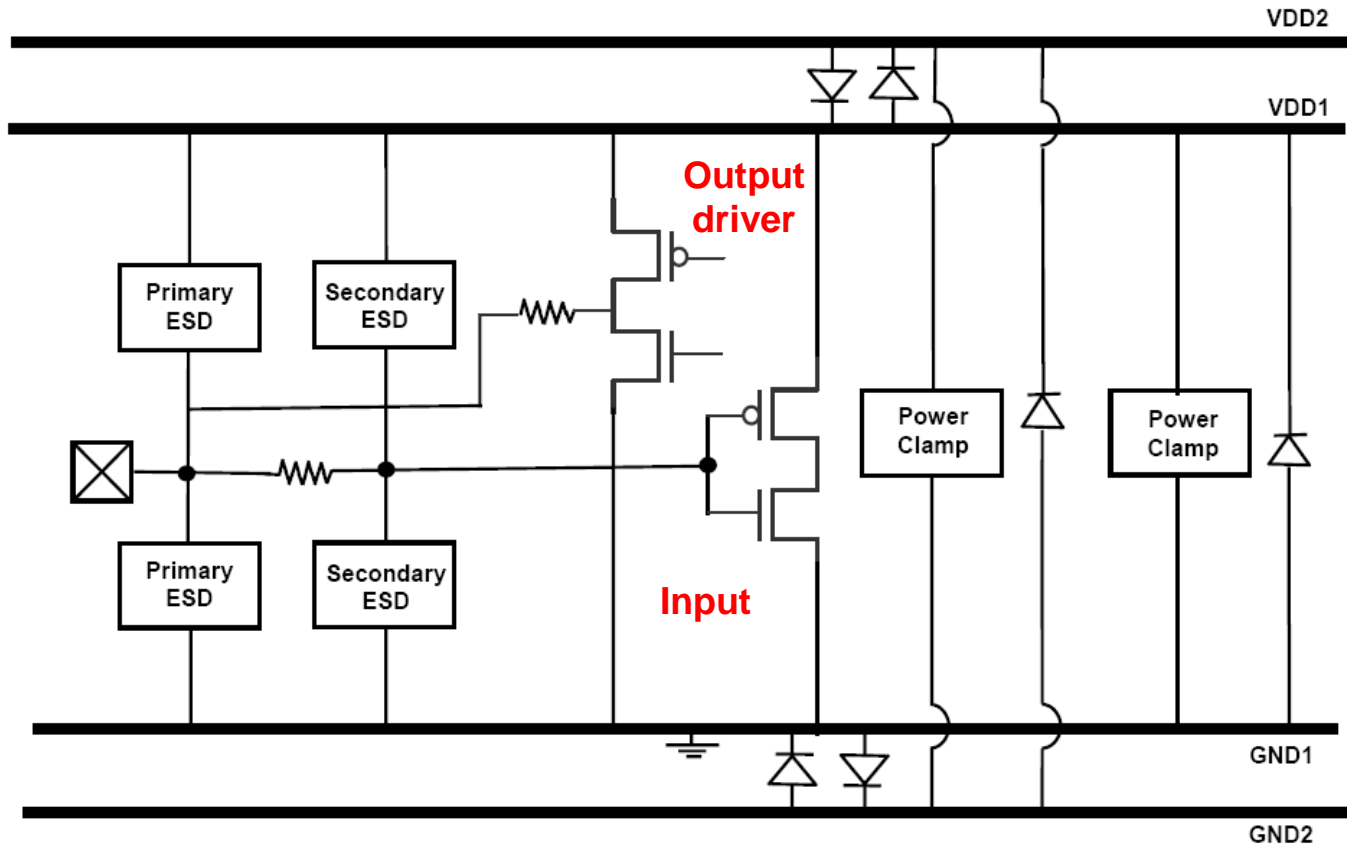


- Gate oxide is most sensitive, requires primary & secondary protection
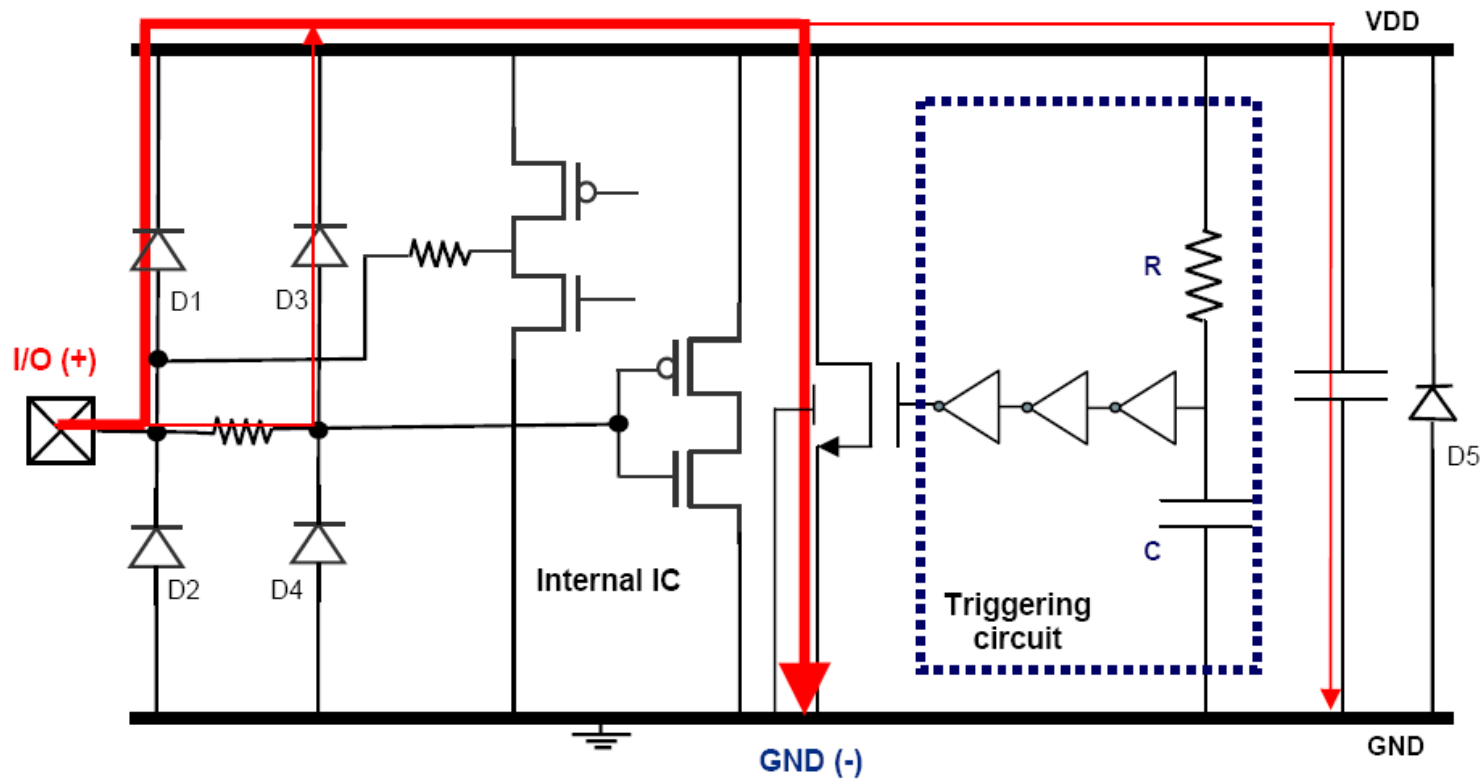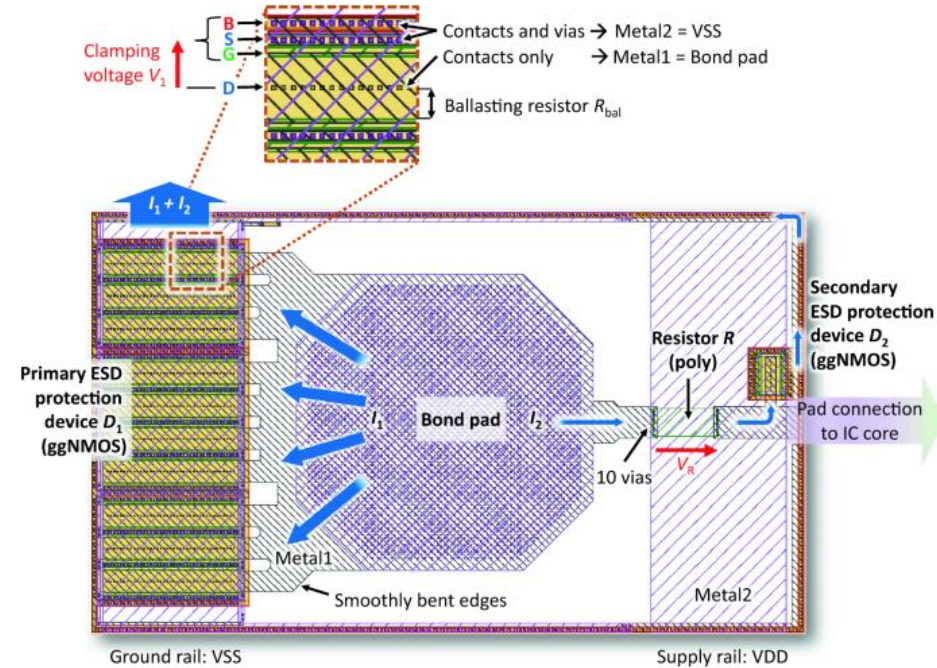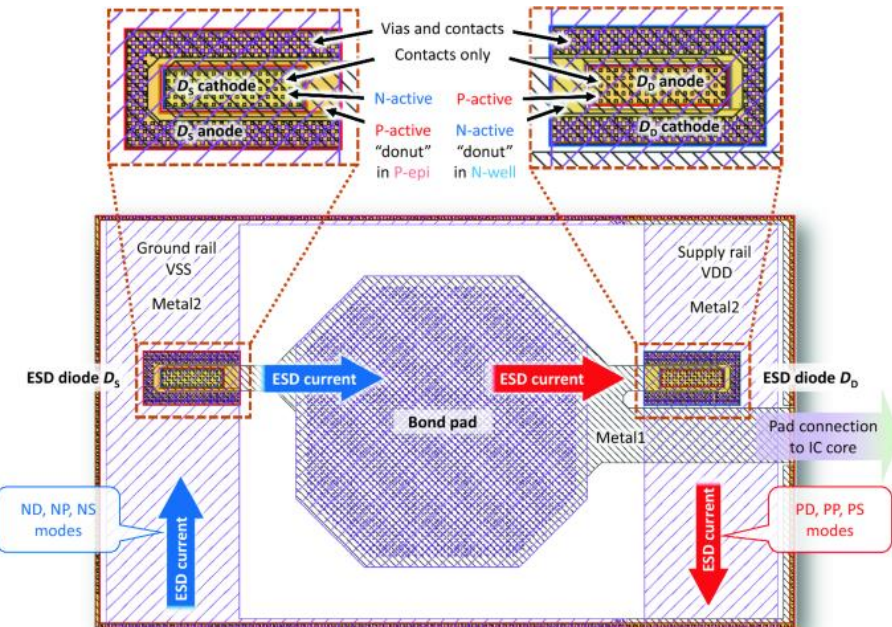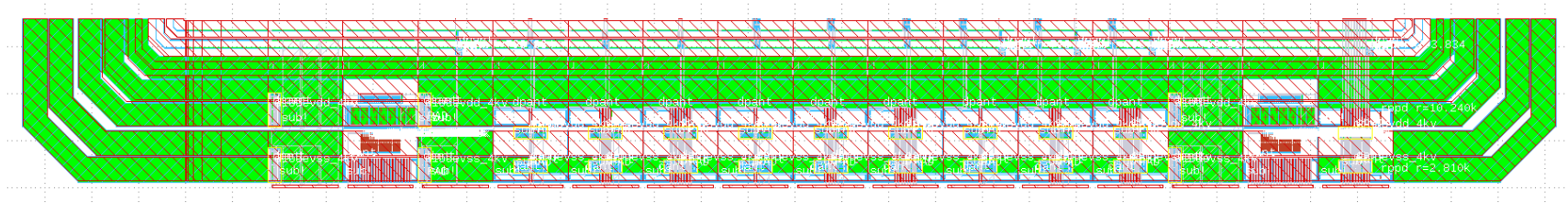
# Power Clamp



Figure 2.9: Concept of rail-based ESD Protection. ESD current is redirected to the $V_{DD}$ power rail and then shunted to GND by a power clamp.

# I/O Cell Examples



https://link.springer.com/chapter/10.1007/978-3-030-39284-0_7

# IHP Pad Ring with I/O Cells



https://github.com/IHP-GmbH/IHP-Open-PDK/tree/dev/ihp-sg13g2/libs.ref/sg13g2_io