Transistorized Integrator

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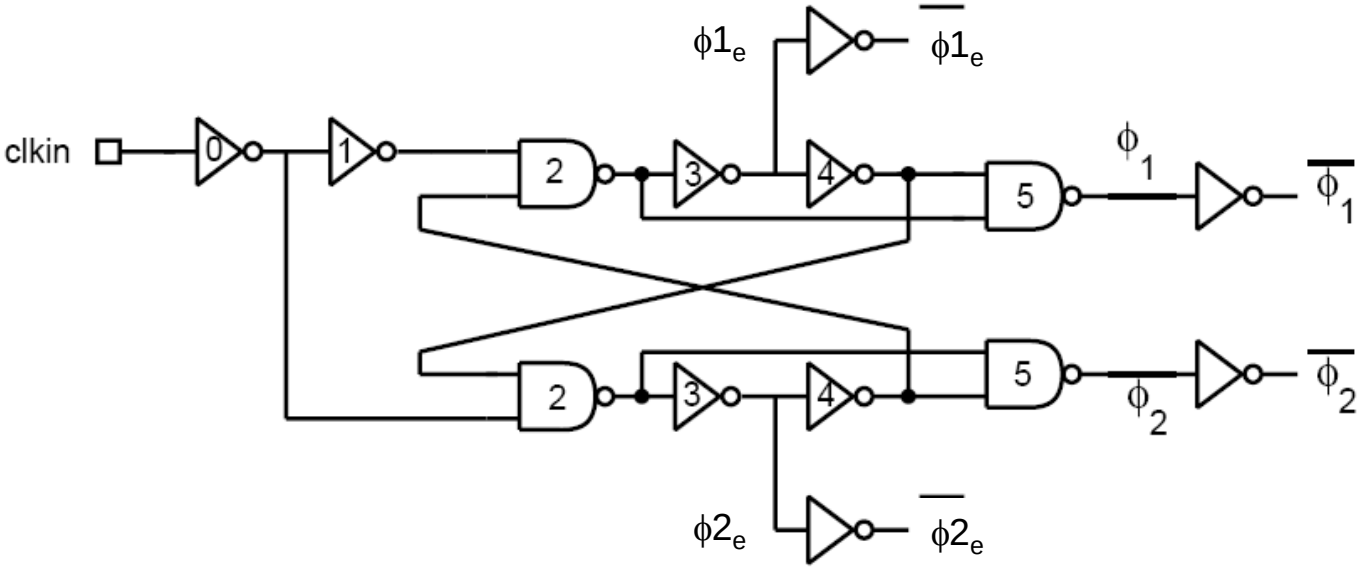
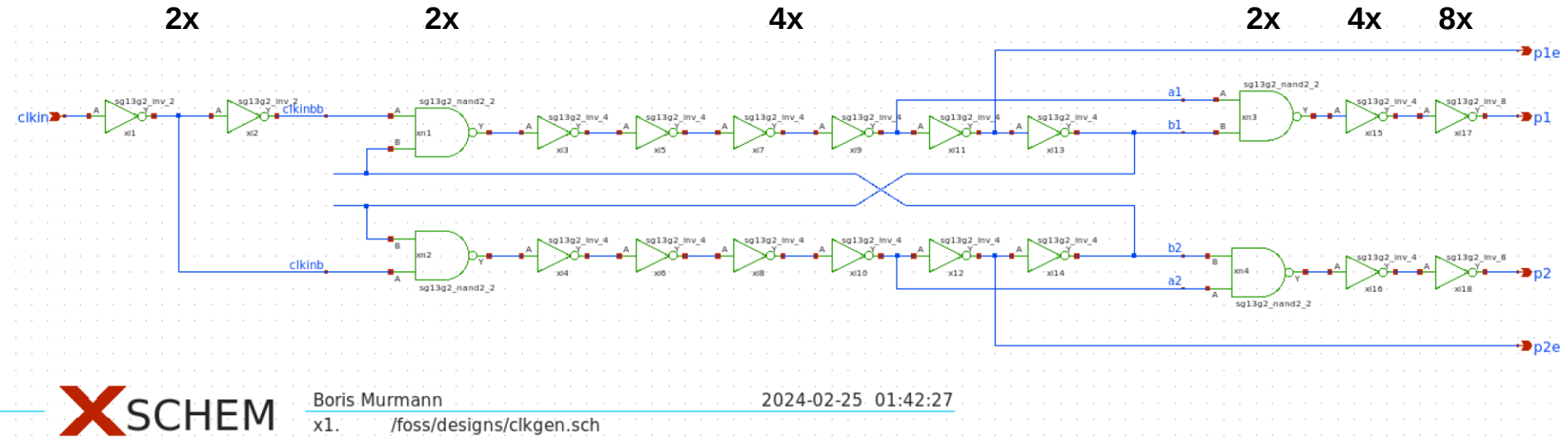
Clock Generation Example



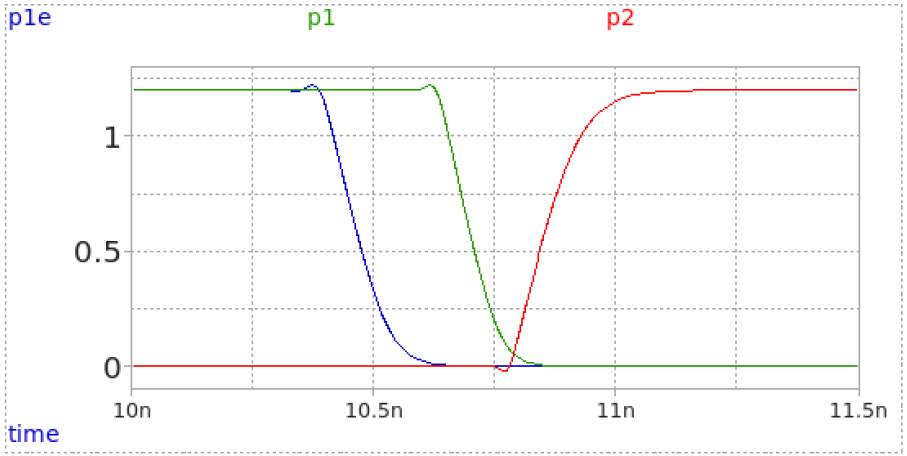
[A. Abo, "Design for Reliability of Low-voltage, Switched-capacitor Circuits," PhD Thesis, UC Berkeley, 1999]

My Design



- Will need to re-visit sizing once we have a good estimate of the load capacitances (including wire parasitics)

Testbench



load waves Ctrl + left click


```
tp1e_p1                =  2.345060e-10
tp1_p2                 =  1.594387e-10
```

NGSPICE

```
.param temp=27 vdd=1.2 per=20n cl=25f
.option method=gear2

.control
save all
tran 10p 15n
meas tran tp1e_p1 TRIG v(p1e) VAL=0.6 FALL=1 TARG v(p1) VAL=0.6 FALL=1
meas tran tp1_p2  TRIG v(p1)  VAL=0.6 FALL=1 TARG v(p2) VAL=0.6 RISE=1
write tb_clkgen.raw
.endc
```

MODEL

```
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
.inc /foss/pdks/sg13g2/libs.ref/sg13g2_stdcell/spice/sg13g2_stdcell.spice
```

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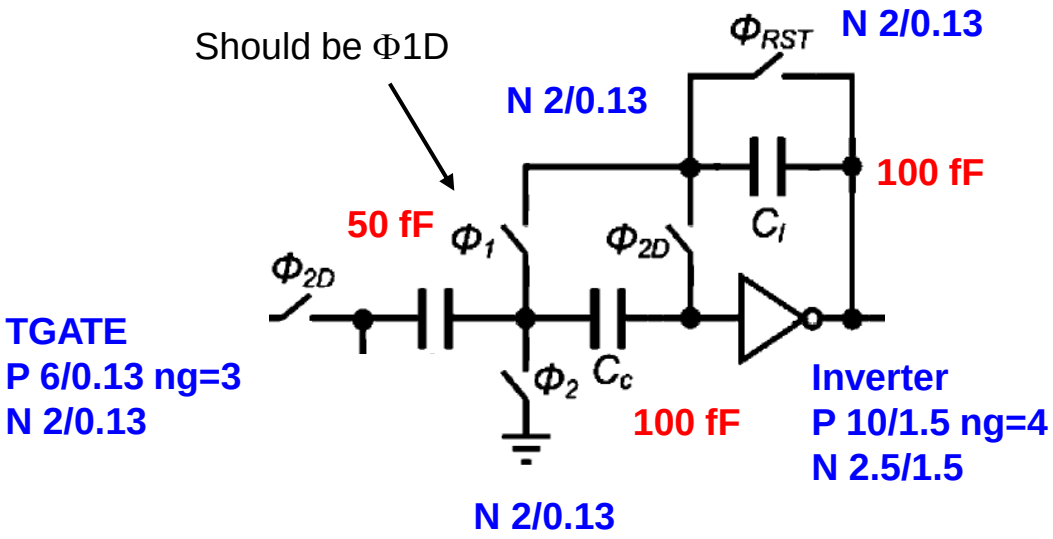
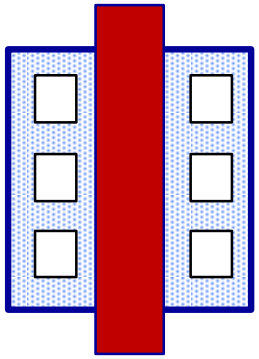
/foss/designs/tb_clkgen.sch

Integrator Prototype

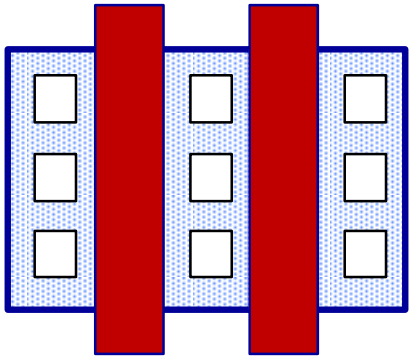


- Sizing based on considerations from lectures 10-13
  - Kept inverter a bit larger to improve settling

Splitting Transistors into Multiple Fingers

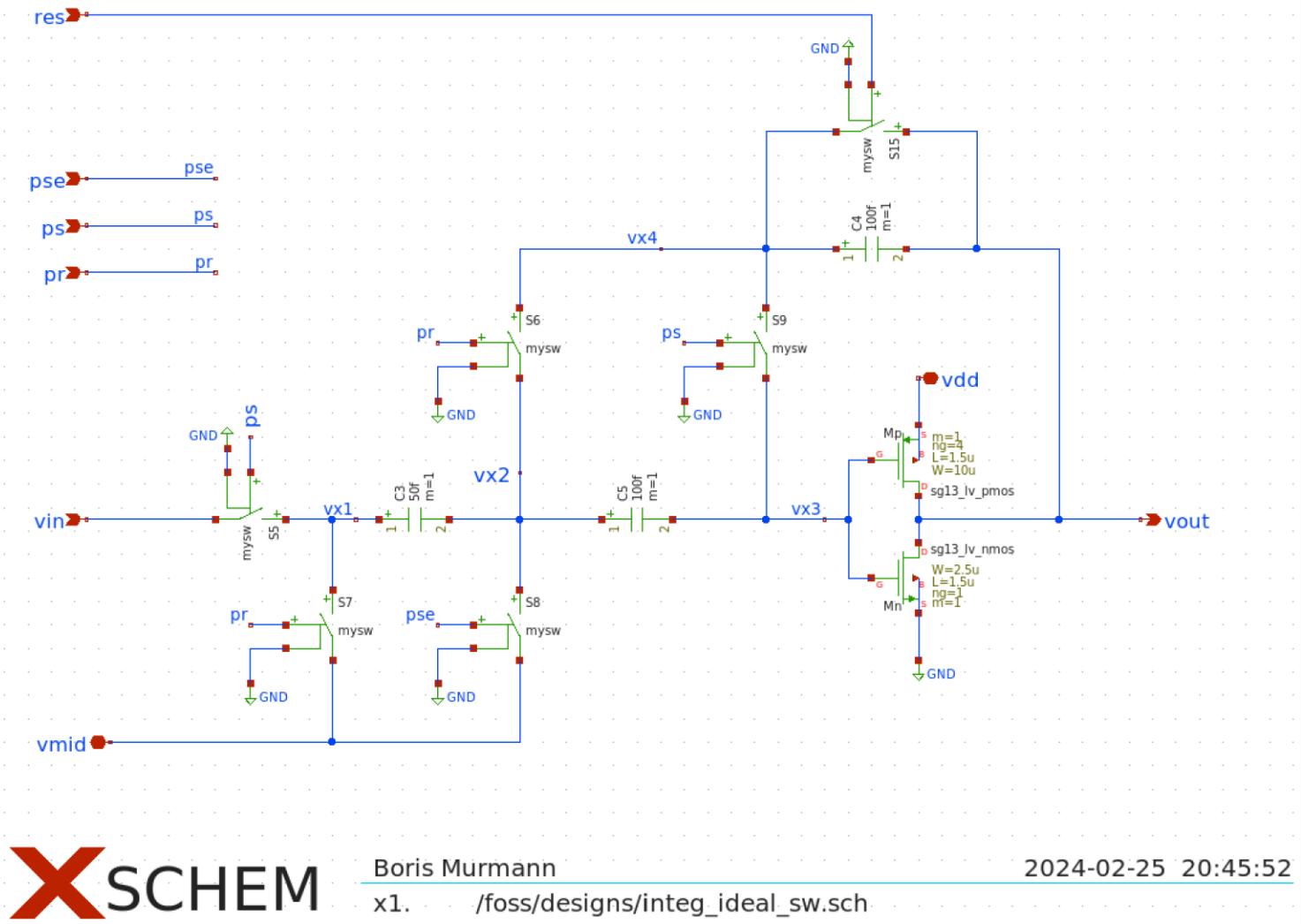


W = 5u
L = 1u
ng = 1

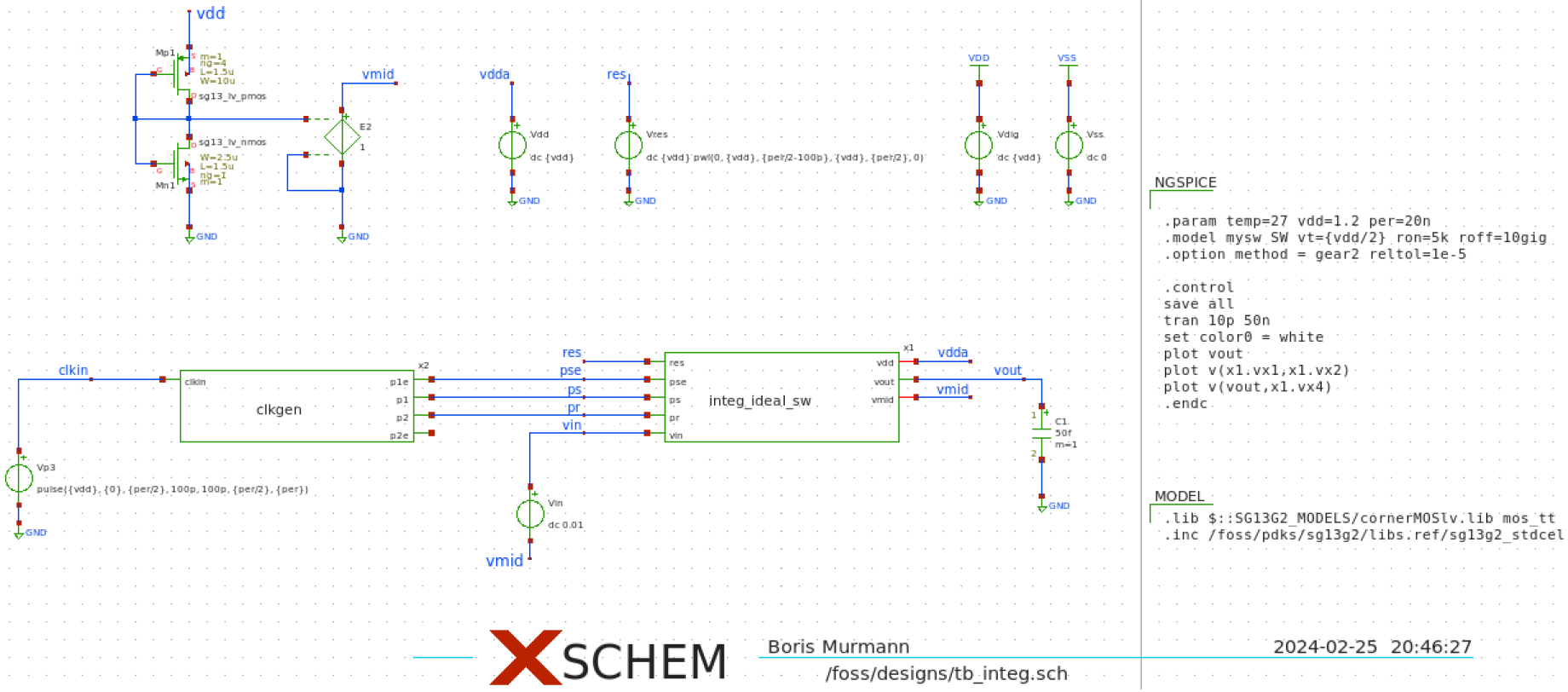


W = 10u
L = 1u
ng = 2

Starting Point With Ideal Switches (R_{on} = 5 kΩ)



Testbench


vdd
Mp1
m=1
ng=4
L=1.5u
W=10u
sg13_lv_pmos
sg13_lv_nmos
W=2.5u
L=1.5u
ng=1
m=1
Mn1
vmid
E2
1
GND
vdda
Vdd
dc {vdd}
res
Vres
dc {vdd} pwl(0, {vdd}, {per/2-100p}, {vdd}, {per/2}, 0)
VDD
Vdig
dc {vdd}
VSS
Vss
dc 0
clkin
clkgen
p1e
p1
p2
p2e
x2
pse
ps
pr
vin
integ_ideal_sw
x1
vout
C1
50f
m=1
Vp3
pulse({vdd}, {0}, {per/2}, 100p, 100p, {per/2}, {per})
Vin
dc 0.01
NGSPICE
.param temp=27 vdd=1.2 per=20n
.model mysw SW vt={vdd/2} ron=5k roff=10gig
.option method = gear2 reltol=1e-5
.control
save all
tran 10p 50n
set color0 = white
plot vout
plot v(x1.vx1,x1.vx2)
plot v(vout,x1.vx4)
.endc
MODEL
.lib $::SG13G2_MODELS/cornerMOSlv.lib mos_tt
.inc /foss/pdks/sg13g2/libs.ref/sg13g2_stdcel
XSCHEM
Boris Murmann
/foss/designs/tb_integ.sch
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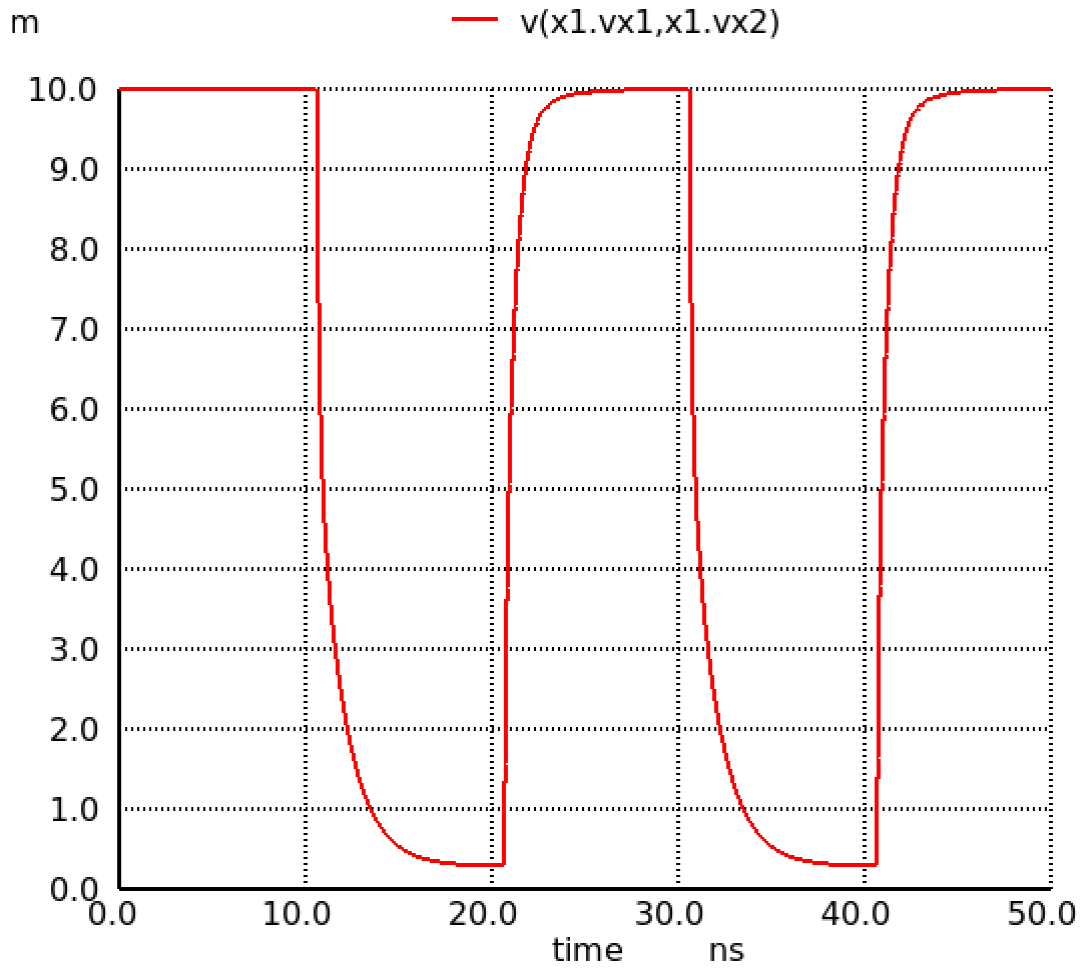
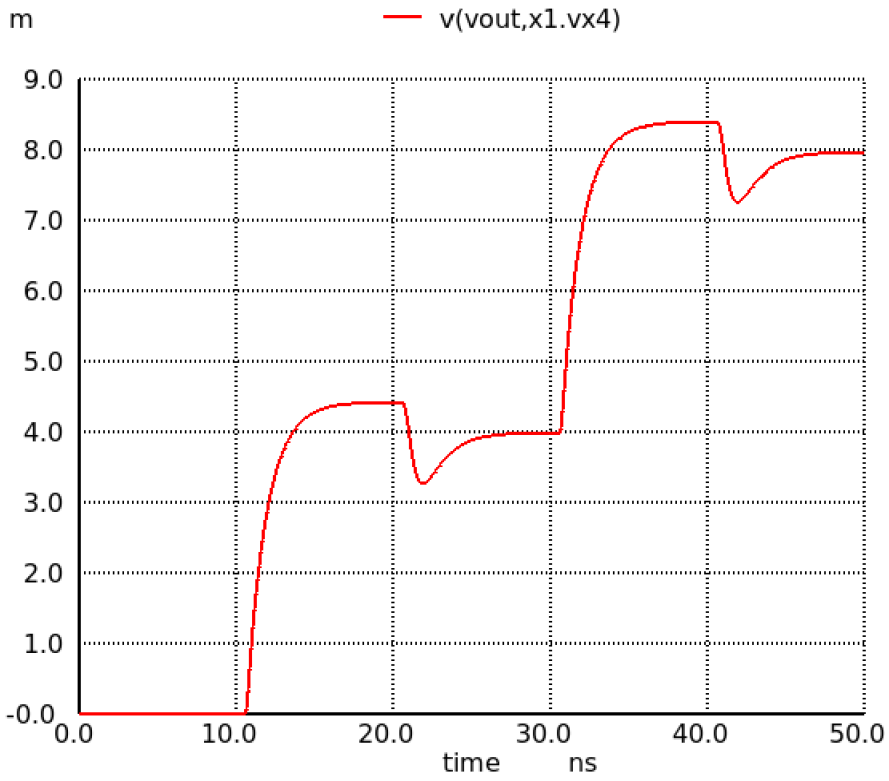
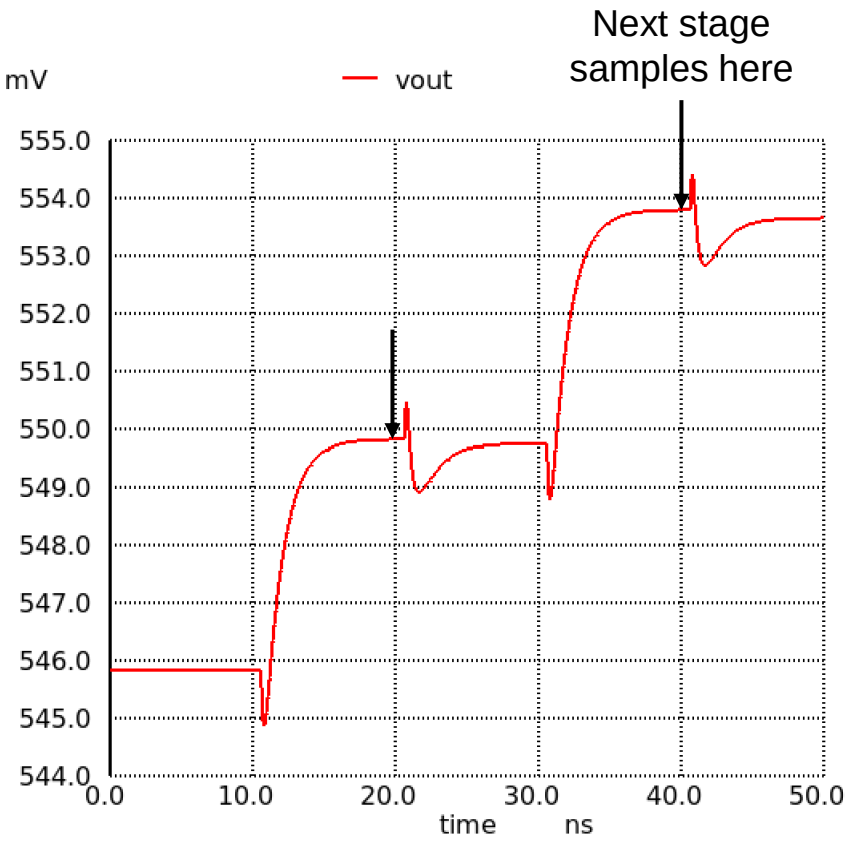
Voltage Across Sampling Capacitor

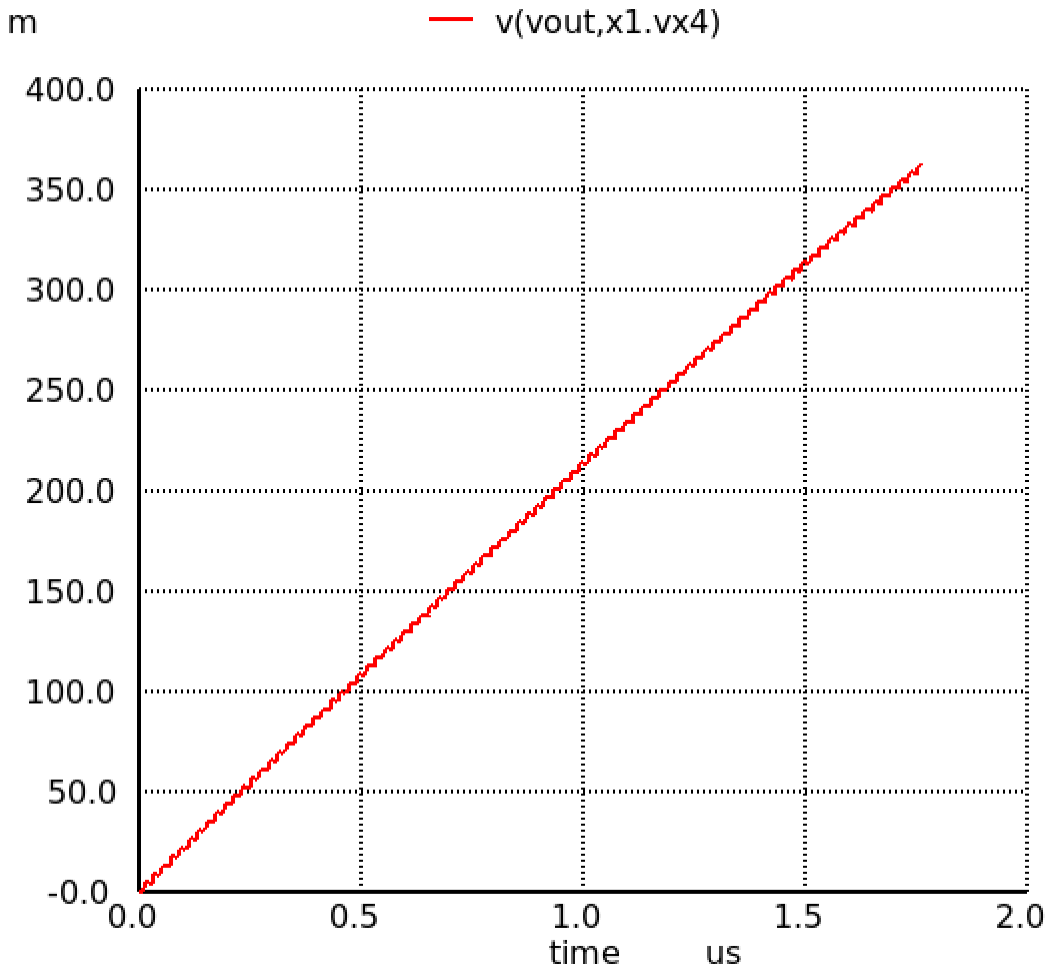


Voltage Across Integration Capacitor & Integrator Output

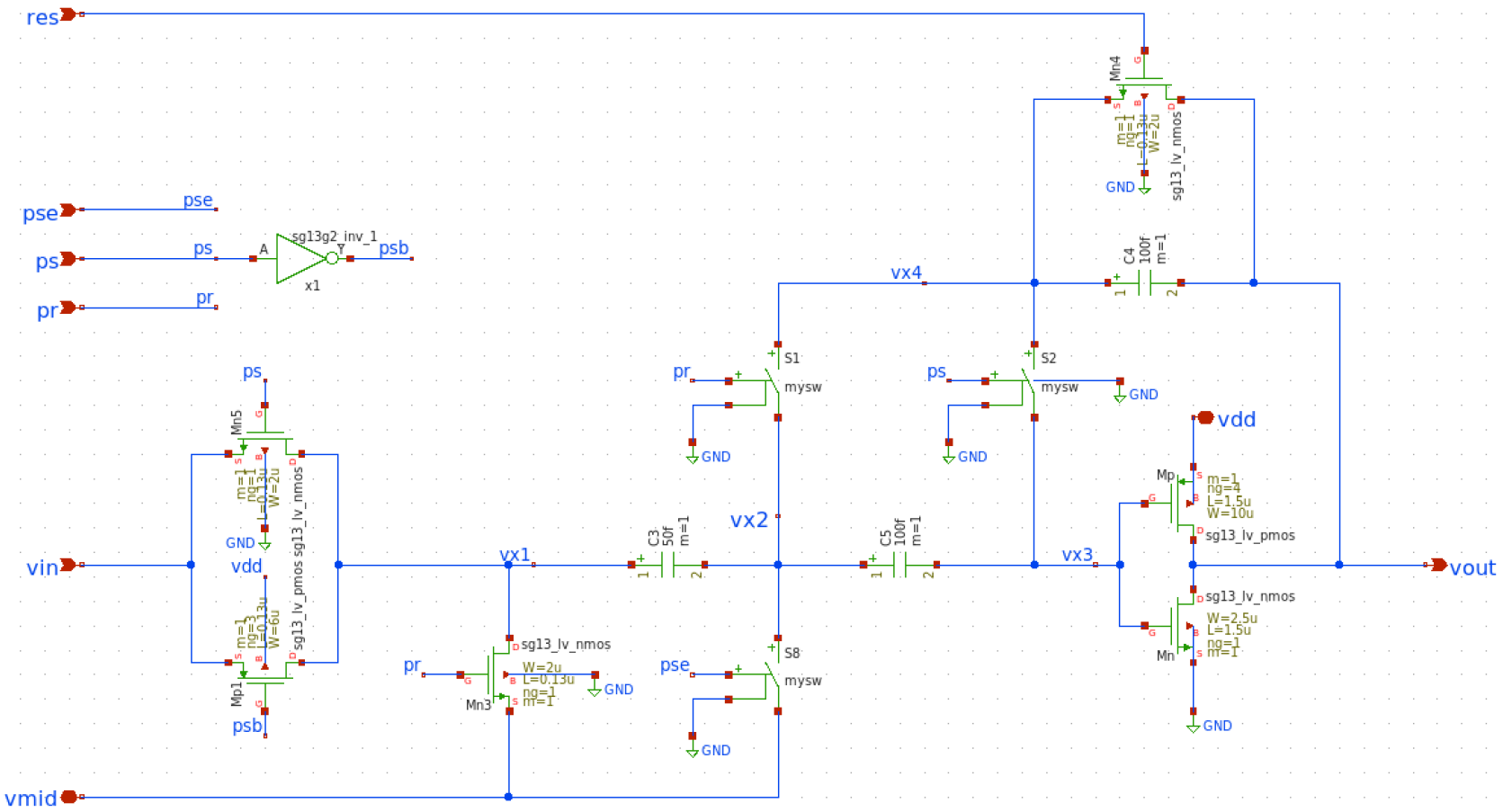




Longer Simulation



Next Step With 3 Ideal Switches



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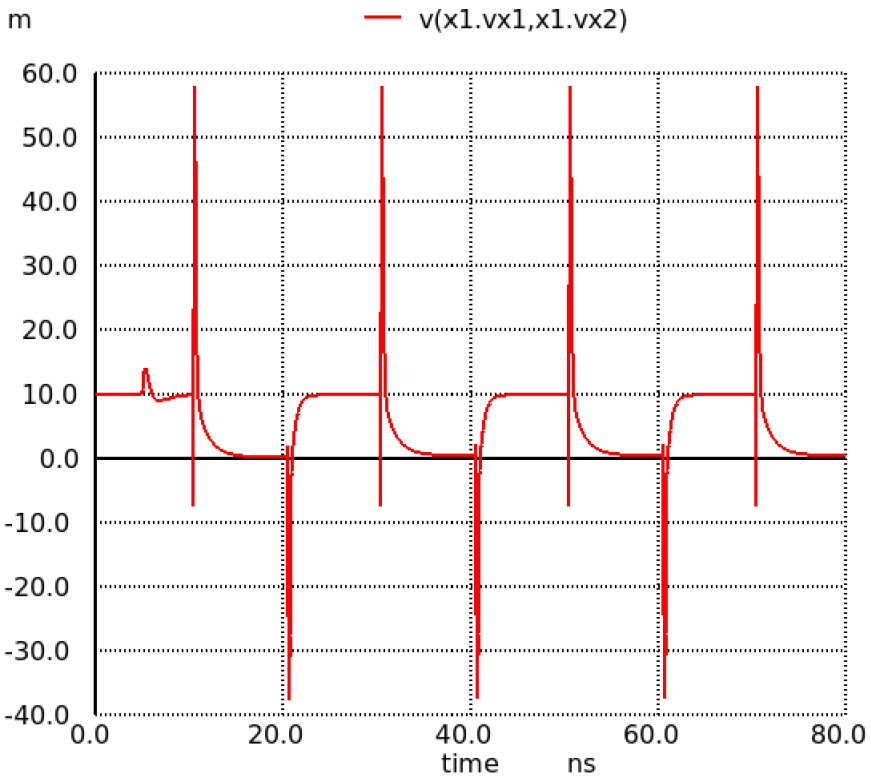
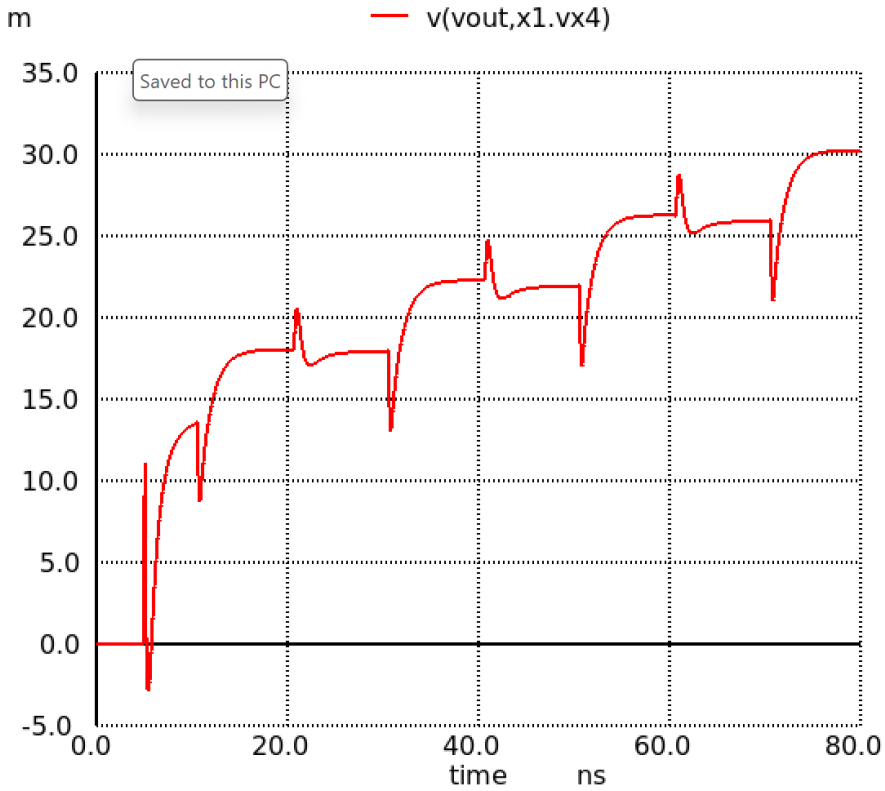
x1. /foss/designs/integ_three_ideal_sw.sch

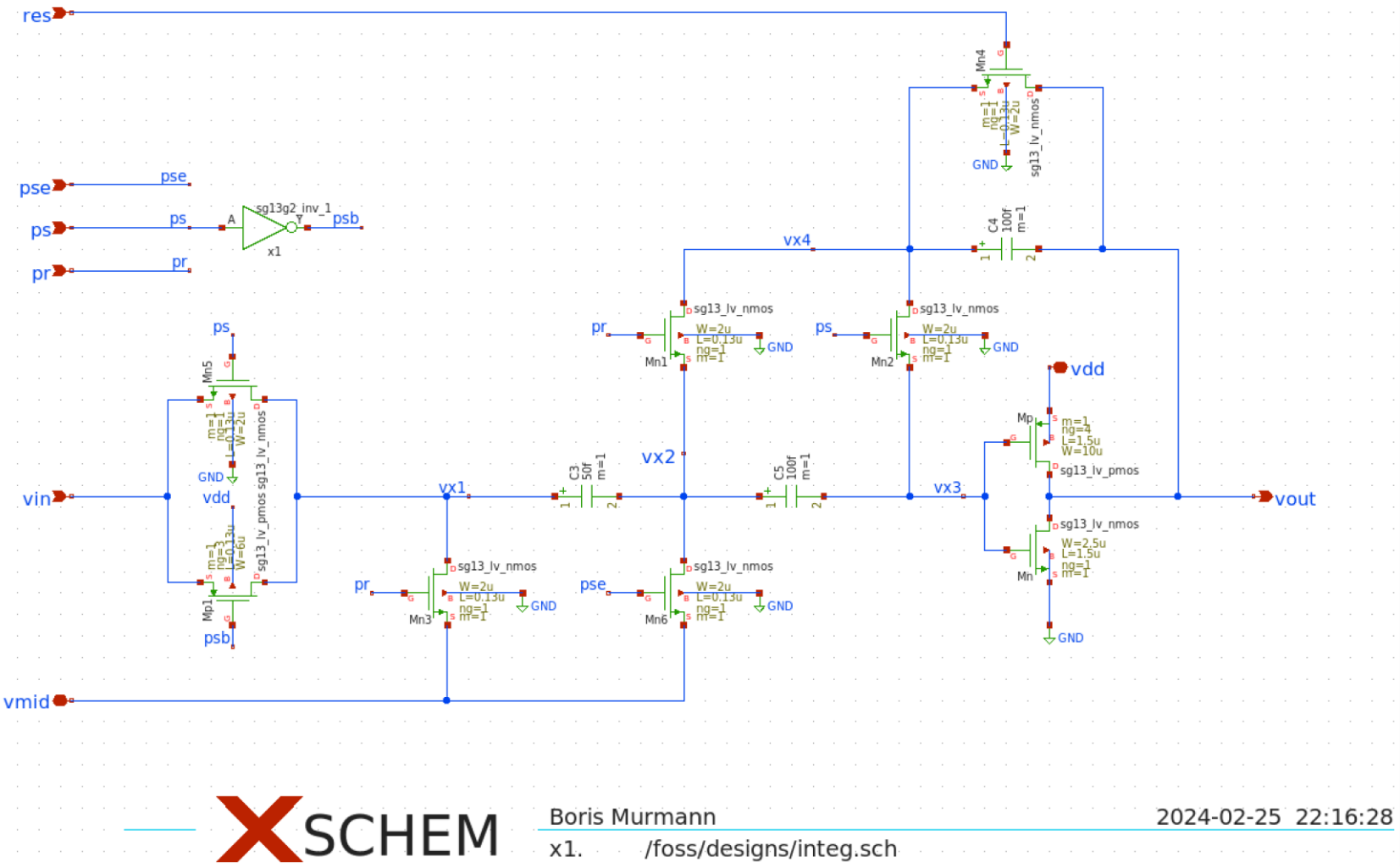
Voltage Across Sampling & Integration Capacitor



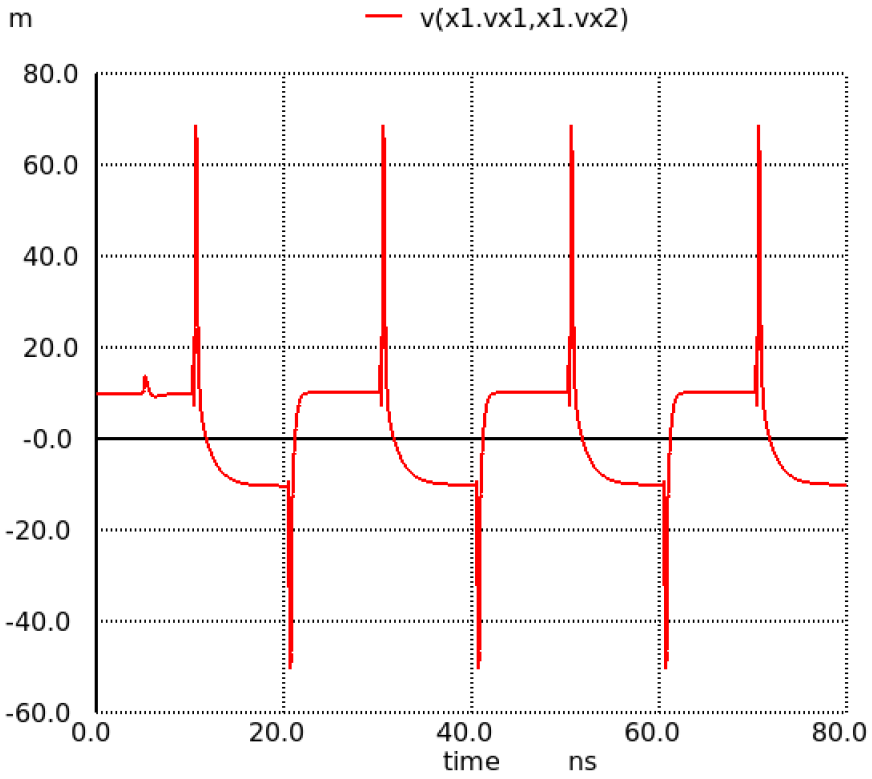


Reset switch
charge injection

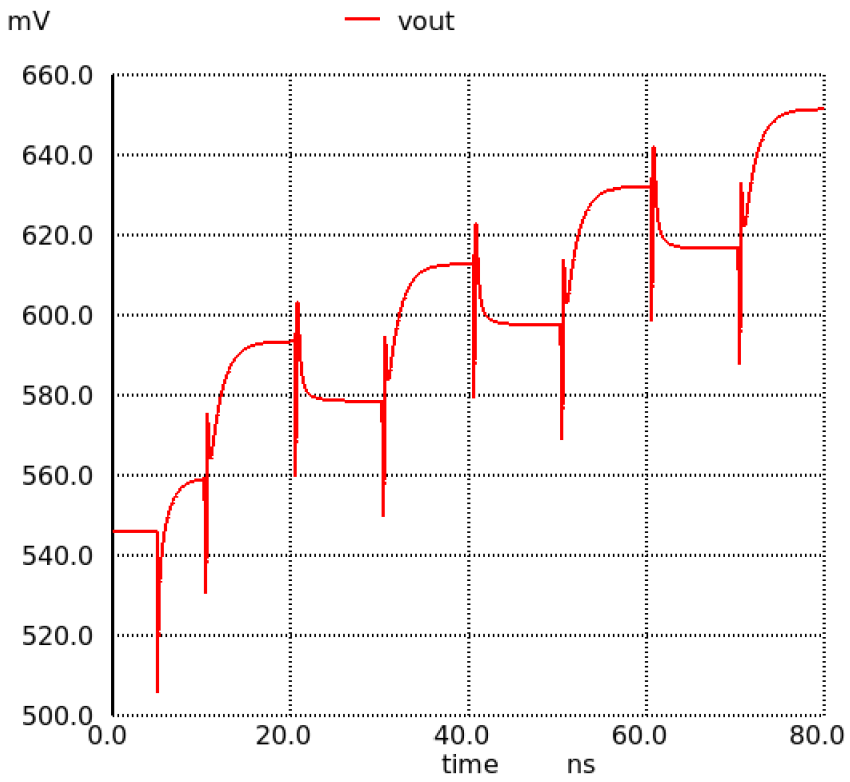
Next Step With Real Switches



Voltage Across Sampling Capacitor & Output Voltage

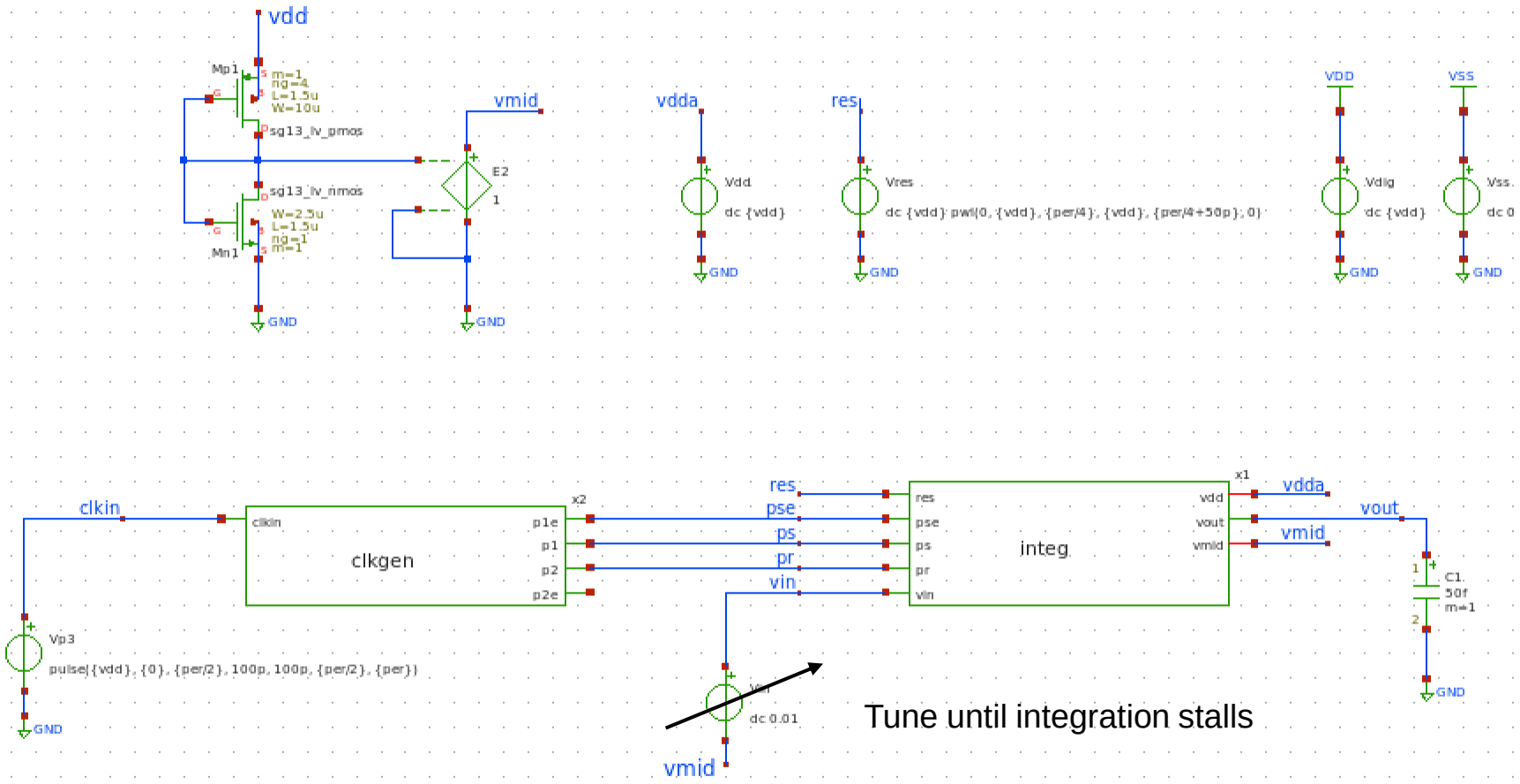


Goes negative due to charge injection

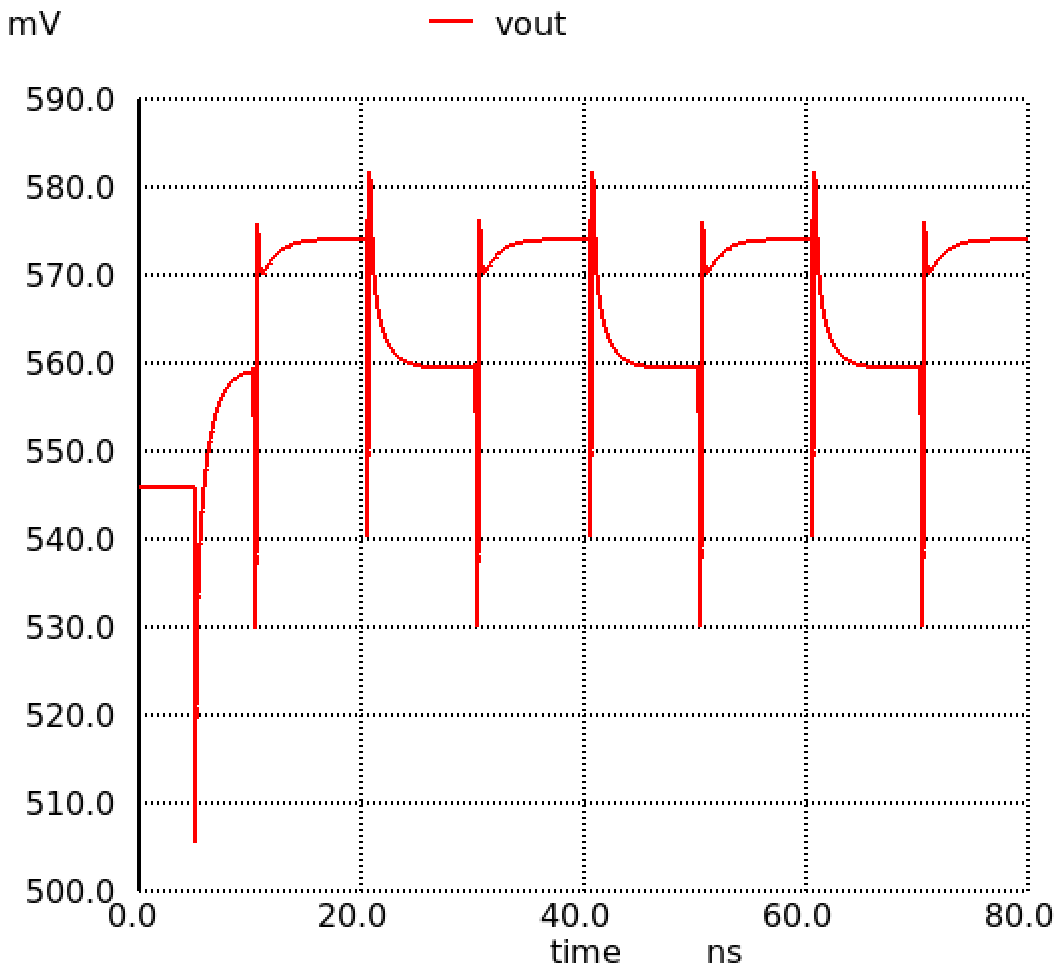


Integration increment larger due to charge injection

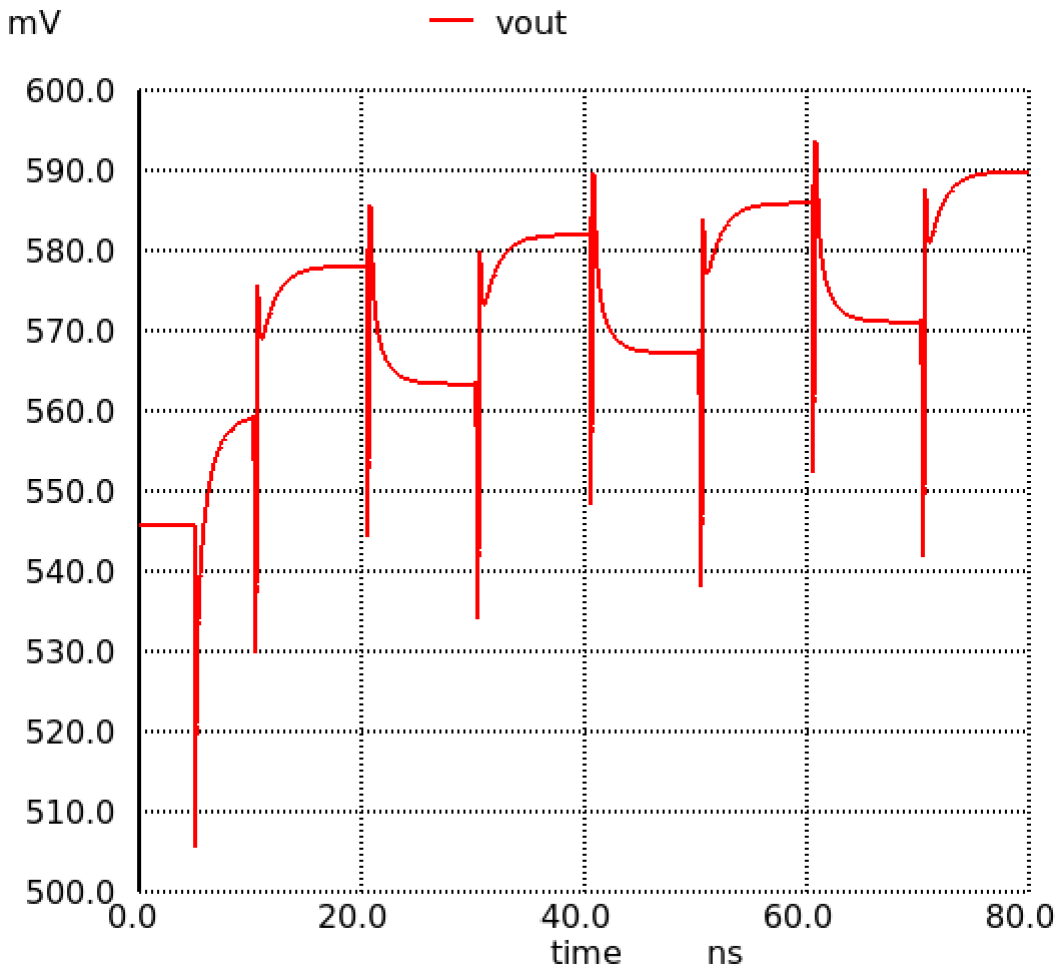
Determining the Input Offset



Output for Vin = -39 mV



Output for Vin = -39+10 mV



Output for Vin = -39+10 mV