Reconfigurable Systems with Xilinx FPGAs

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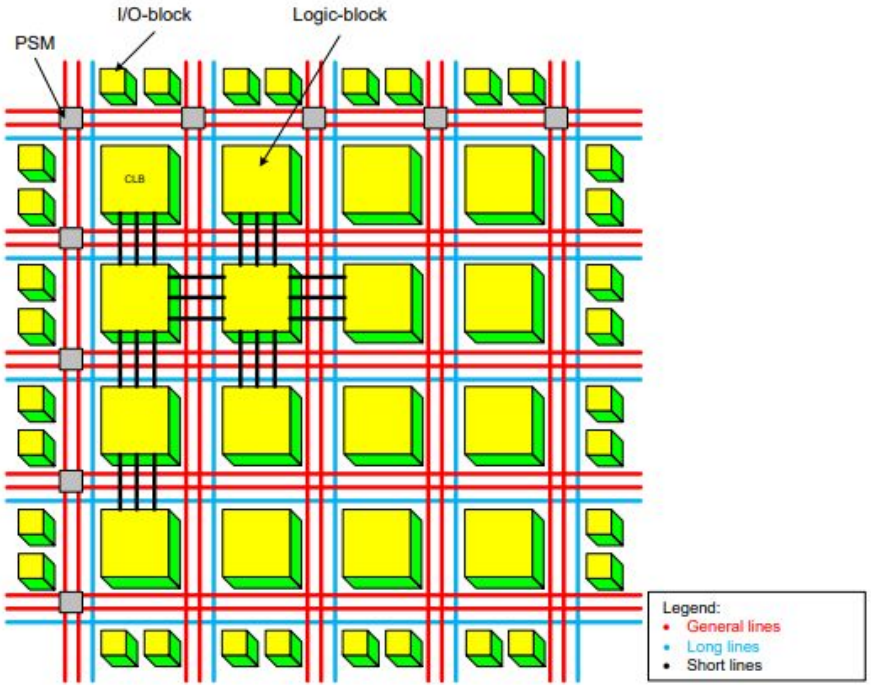
What is a Reconfigurable System?

- System that combines high flexibility of software with high performance of hardware (Wikipedia)
- Use of FPGAs to achieve this
- Configuration or Reconfiguration:
  - Complete
  - Partial
    - Static
    - Dynamic



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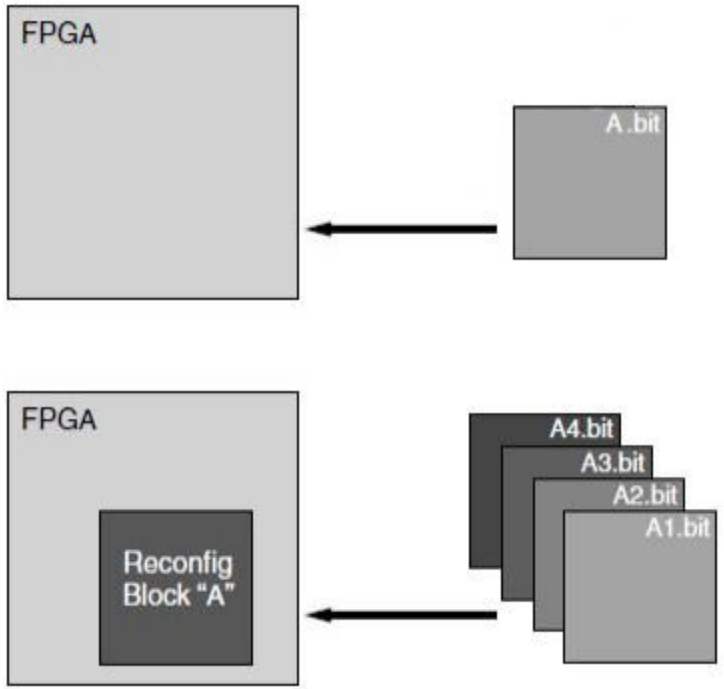
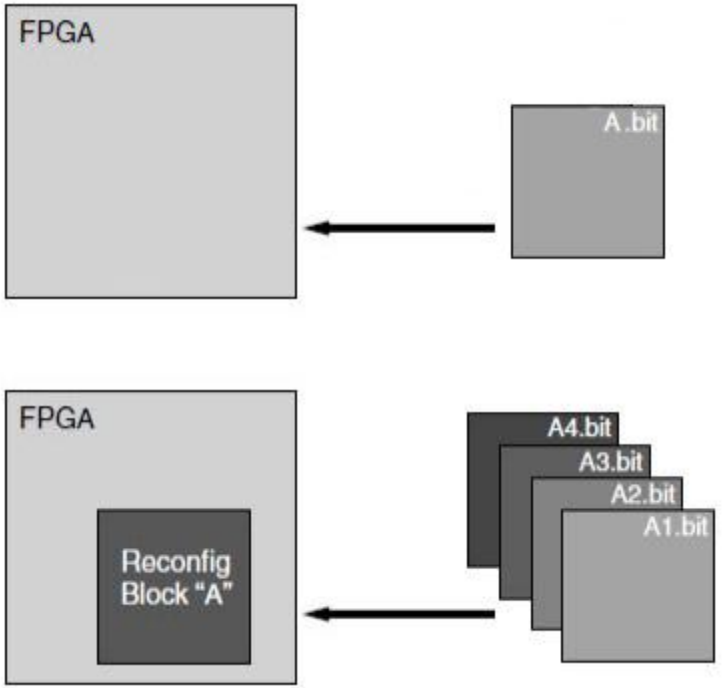
Types of Reconfiguration

- Complete: All the FPGA is loaded with a new configuration
- Partial: Only part of the FPGA is loaded with a new configuration
  - Static: The device stops operating while reconfiguring
  - Dynamic: Only the reconfigured part stops operating while reconfiguring, the rest remains operational
- “Dynamic Function eXchange”



Advantages of Partial Reconfiguration

- Even more flexibility
- Reduction of resource consumption
- Enabling new techniques in design security
- Improving FPGA fault tolerance
- Accelerating configurable computing

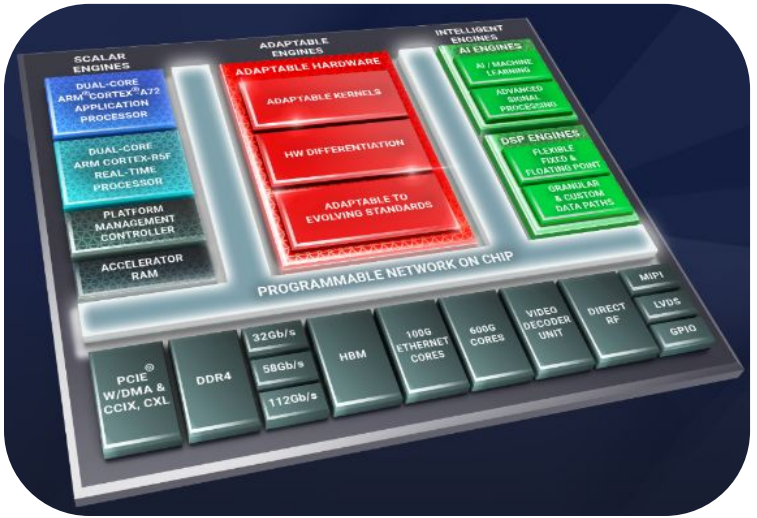


Supported devices

- 7 Series
- Ultrascale
- Ultrascale+
- Versal - Adaptive Compute Acceleration Platform (ACAP)
- Some exceptions, but in general every current device supports

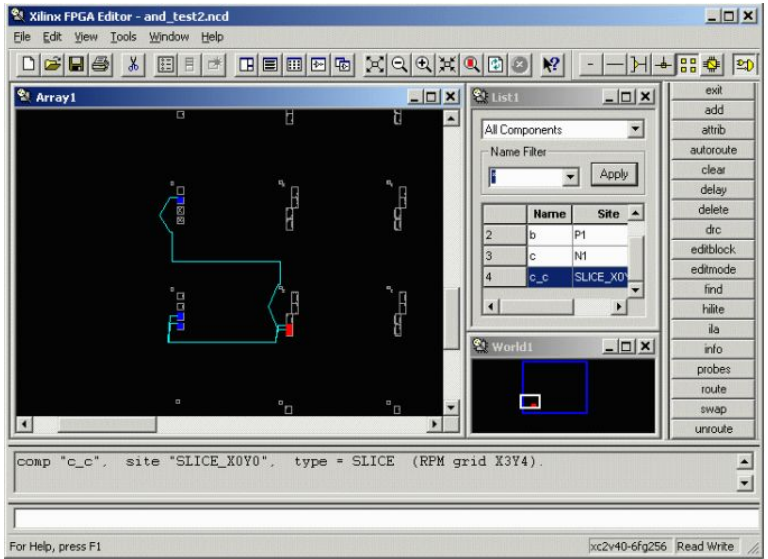
SPARTAN-7 ARTIX-7 KINTEX-7 VIRTEX-7

ARTIX UltraSCALE+ KINTEX UltraSCALE+ VIRTEX UltraSCALE+

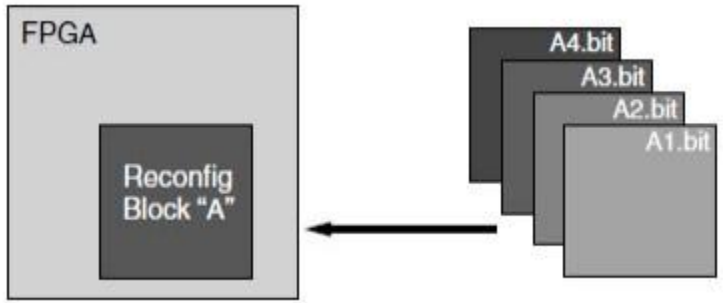


Styles of Partial Reconfiguration

- Difference-Based: small changes, bitstream contained only the differences between old and new design

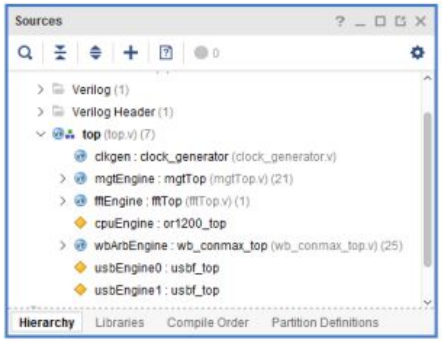


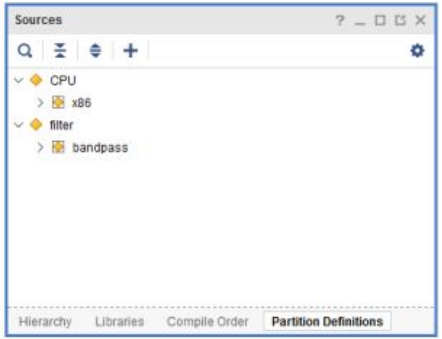
- Module-Based: FPGA is divided in Static and Reprogrammable Regions

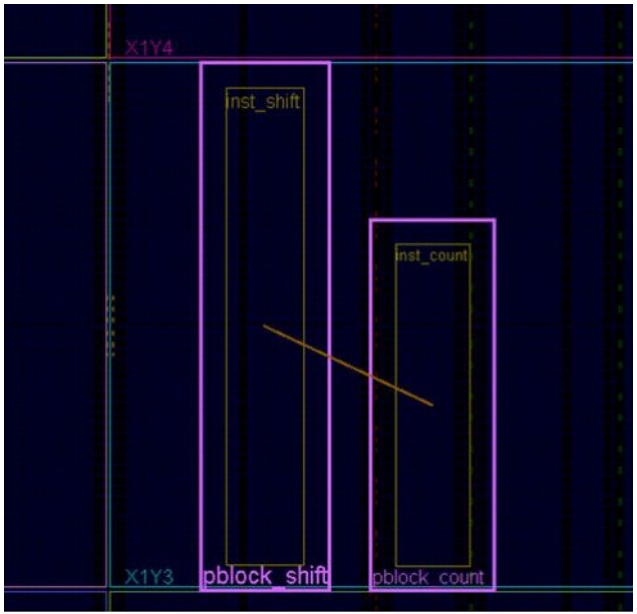


Module-Based project flow

- Enable Partial Reconfiguration (PR)
- Define Reconfigurable Partitions (RPs) and Reconfigurable Modules (RMs)







Module-Based project flow

- Configurations: Combinations of RMs with the Static Region
- Synthesis and Implementation: Out-Of-Context and Bottom-Up. Implements the static region first and reuses it for each configuration
- Bitstreams:
  - Full Configuration Bitstreams: The usual
  - Partial Bitstreams: Delivered after first configuration, self-contained
  - Blanking Bitstreams: Logical black-box
  - Clearing Bitstreams: Specific to Ultrascale devices, shuts down clock region

Configuration modes and ports

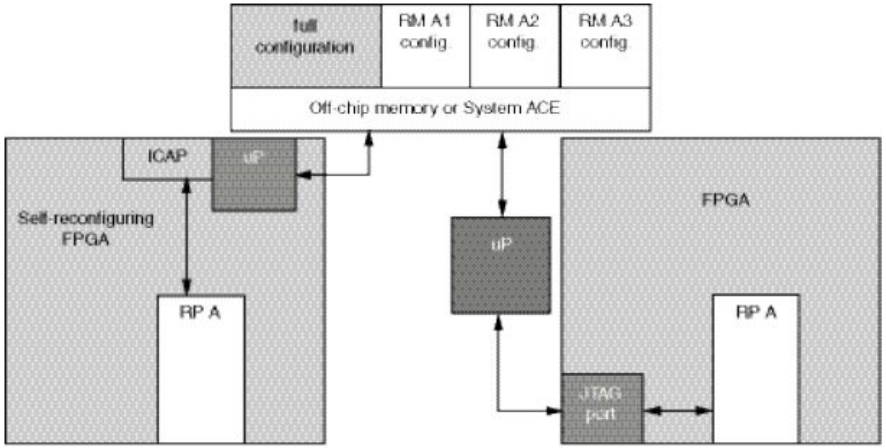
- **ICAP:** Requires the creation of an ICAP controller as well as logic to drive the ICAP interface
- **MCAP:** (UltraScale and UltraScale+ devices only) Provides a dedicated connection to the ICAP from one specific PCIe block per device
- **PCAP:** The primary configuration mechanism only for Zynq-7000 AP SoC and Zynq UltraScale+ designs
- **JTAG:** A good interface for quick testing or debug. Can be driven with the Vivado Logic Analyzer
- **Slave SelectMAP or Slave Serial:** Good choices to perform full configuration and Partial Reconfiguration over the same interface.

Configuration Mode	7 Series	Zynq	UltraScale	UltraScale+	Zynq UltraScale+ MPSoC
JTAG	Yes	Yes	Yes	Yes	Yes
ICAP	Yes	Yes	Yes	Yes	Yes
PCAP	N/A	Yes	N/A	N/A	Yes
MCAP	N/A	N/A	Yes	Yes	Yes
Slave Serial	Yes	N/A	Yes	Yes	N/A
Slave SelectMap	Yes	N/A	Yes	Yes	N/A
SPI (any width)*	No	N/A	No	Yes	N/A
BPI sync mode*	No	N/A	No	Yes	N/A
BPI async mode	Yes	N/A	Yes	Yes	N/A
Master modes	No	N/A	No	No	N/A

Port	Device	Max clock	Data width	Max bandwidth
ICAP	7-Series	100 MHz	32 bit	3.2 GB/s
	Ultrascale	200 MHz	32 bit	6.4 GB/s
MCAP	7-Series	N/A	N/A	N/A
	Ultrascale	200 MHz	32 bit	6.4 GB/s
SelectMAP	7-Series	100 MHz	32 bit	3.2 GB/s
	Ultrascale	125 MHz	32 bit	4.0 GB/s
JTAG	7-Series	66 MHz	1 bit	66 MB/s
	Ultrascale	50 MHz	1 bit	50 MB/s

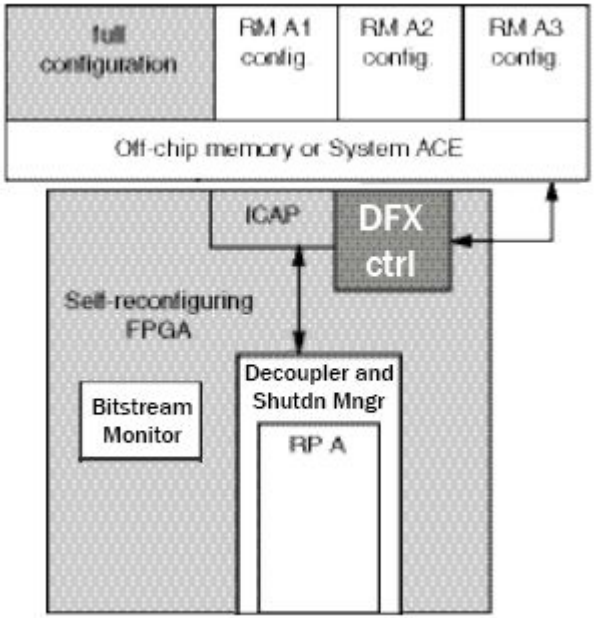
Configuration modes and ports

- **Dynamic Reconfiguration Port (DRP):** Port that exists in only some elements of 7-Series, Ultrascale and Ultrascale+ devices
  - Phase-Locked Loops (PLLs)
  - Mixed-Mode Clock Managers (MMCMs)
  - Serial transceivers (MGTs)
  - And others



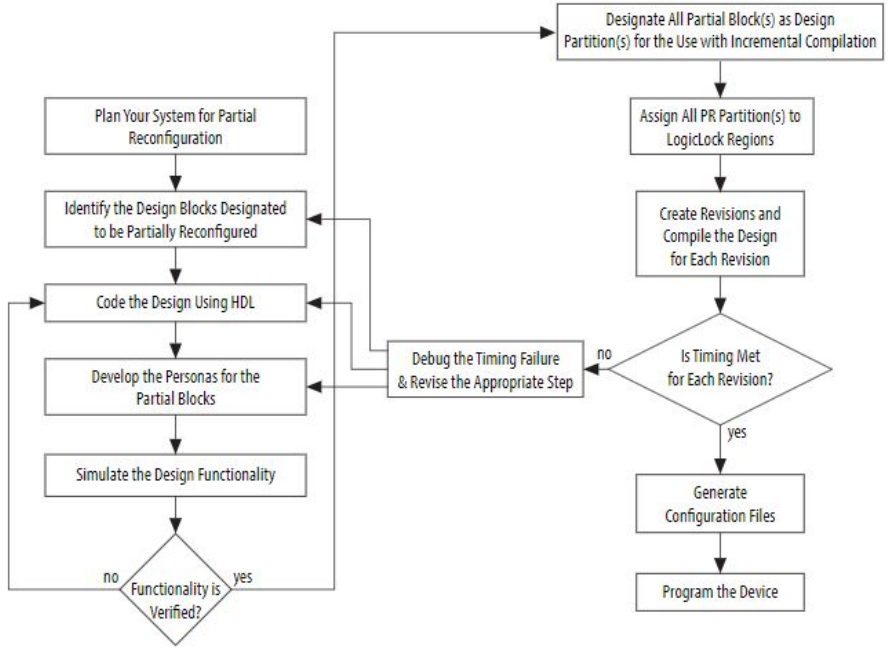
Xilinx' IPs for Partial Reconfiguration

- **DFX Controller:** A controller that manages the partial bitstreams in the FPGA
- **DFX Decoupler:** Provides safe and managed boundaries between static logic and Reconfigurable Partitions during reconfiguration
- **DFX AXI Shutdown Manager:** Similar to the Decoupler, provides safe reconfiguration through AXI interfaces
- **DFX Bitstream Monitor:** Used to identify and track partial bitstream as they flow through the design



Brief mention of Altera

- Also supports PR, mainly in the families of devices Arria and Stratix, using their Quartus Prime software
- Requirements for a controller IP and the pBlocks (here called Logic Lock regions) already exist in non-PR projects



High-level modeling

- Even with all the automation, designing such project is still a difficult task
- Resource management even before simulations
- High-level tools are being developed to aid in this area

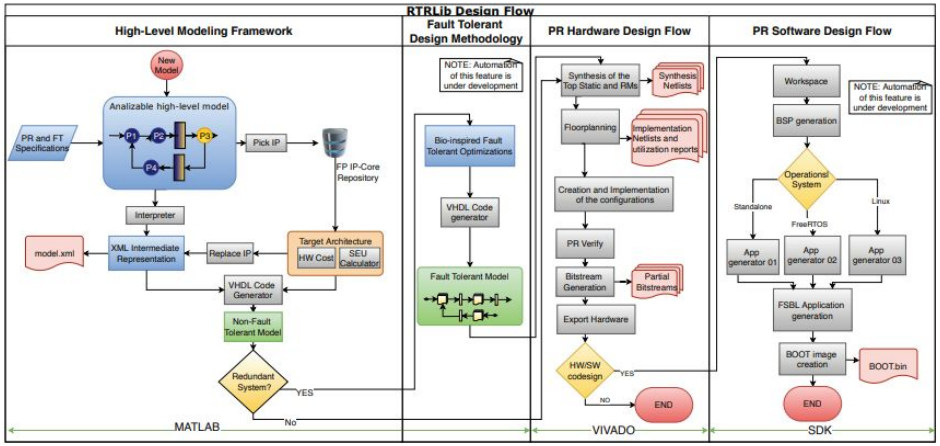


Fig. 1 from *RTRLib: A High-Level Modeling Tool for the Implementation of Dynamically Partial Reconfigurable System-on-Chips* by Daniel M. Muñoz and Regina M. Ivo

Thank you