Microcontrollers & Embeded System Design
CSE 315

Md Awsaf Alam

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Contents

1 8086/8088 Hardware Specifications

1.1 Introduction

$\overline{RD}$
- Whenever this pin goes to logic 0, the data bus becomes receptive to data from the memory or I?O devices connected to the system.
- Floats to high impedence state during a hold acknowledge

READY
- μp enters into **WAIT** state and remains idle if this pin is at logic 0
- No effect on operations of μp, if this pin is at logic 1

INTR
- Used to request a h/w interrupt
- If INTR is held high when $IF = 1$, the μp enters an interrupt acknowledge cycle ($\overline{INTA}$ becomes active) after completion of the current instruction

$\overline{TEST}$
- An input that is tested by the WAIT instruction
- If TEST is logic 0, the WAIT instruction functions as NOP
- If TEST is logic 1, the WAIT instruction waits for **TEST** to become 0

NMI
- Non markable interrupt pin
- Similar to the **INTR** except that NMI does not check IF (whether it is 1)

RESET
- Causes the μp to reset itself if this pin remains high for a minimum of four clocking periods
- whenever the up gets reset , it begins executing instructions at memory location **FFFFOH** and disables future interrupts by clearing IF

CLK
- Provides the base timing signal to the up
- Clock signal must have at least 33% duty cycle (high for the one-third of the clocking period and low for two-third of the period)

VCC
- Power supply input
- Provides +5.0 volt with 10% tolerance to the up

GND
- 2 pins, both must be connected to ground

MN/$\overline{MX}$
- Selects either minimum mode or maximum mode operation of the up

$\overline{BHE}$**/S7**
- Bus high Enable
- Used in 8086 to enable the most signifant data bus bits (D15 - D8) during a read or write operations
- The state of S7 is always a logic 1

1.2 Minimum Mode Pins

IO/$\overline{M}$ or M/$\overline{IO}$
- Selects memory or I/O
- Indicates the $\mu p's$ address bus contains either a memory address or an I/O port address
- High impedence state during a hold acknowledge

$\overline{WR}$
- Indicates that the μp is outputting data to a mem or I/O device
- Data bus contains valid data for memory or I/O during the time $\overline{WR}$ remains 0

$\overline{INTA}$
- A response to the INTR input pin
- Used to gate the interrupt vector number onto the databus in response to an interrupt request.

$\overline{ALE}$
- Address Latch Enable
- Indicates that the $\mu p's$ address/ data bus contains address information
- The address can be a mem address or I/O port number
- [Does **NOT** float during a hold acknowledge]

DT/$\overline{R}$
- Data Transmit or Receive
- Indicates that the $\mu p's$ data bus is transmitting ($DT/\overline{R} = 1$) or receiving ($DT/\overline{R} = 0$) data.
- Used to enable external data bus buffers.

DEN
- Data bus enable
- Activates external data bus buffers.

HOLD
- Requests a direct memory access (DMA)
- If it is a logic 1, μp stops executing S/W and places its address, data and control bus at high impedence state
- If it is a logic 0, the μp executes S/W normally

HLDA
- Hold acknowledge
- Indicates that the μp has entered the hold state

$\overline{SSO}$
- Equivalent to SO pin in maximum mode option of the μp
- It is combined with IO/$\overline{M}$ and DT/$\overline{R}$ to decode function of the current bus cycle

1.3 Tables

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SSO}$	Function
0	0	0	Interrupt acknowledge
0	0	1	Memory read
0	1	0	Memory write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	I/O read
1	1	0	I/O write
1	1	1	Passive inactive

Table 1: Bus cycle status (8088) [Minimum mode]

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Function
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive inactive

Table 2: Bus control functions generated by the bus controller 8288 [Maximum mode]

2 Lecture - 3 (23.04.18)

2.1 Maximum Mode Pins

For using external coprocessors:

$\overline{S2}, \overline{S1} and \overline{S0}$ • Indicate the function of current bus-cycle
- Normally decoded by 8288 bus controllers

$\overline{R1}/\overline{G1} and \overline{R0}/\overline{GT0}$ • Request/grant pins
- Request Direct Memory Access
- Bi-Directional lines
- used to both request and grant a DMA operations

$\overline{LOCK}$ • Used to lock peripherals off the system

$\overline{QS_1} and \overline{QS0}$ • Queue status bits
- Show status of the internal instructions queue
- Accessed by numeric coprocessor (8087)

$\overline{QS_1}$	$\overline{QS_0}$	Function
0	0	Queue is idle
0	1	First byte of opcode
1	0	Queue is empty
1	1	Subsequent byte of opcode

Table 3: Bus control functions generated by the bus controller 8288 [Maximum mode]

2.2 Clock Generator (8284A)

Basic functions • Clock generation
- **RESET** synchronization
- READY synchronization
- TTL-level peripheral clock signal

2.3 Pin Functions

AEN1 and AEN2 (Address enable)

- Qualify the bus ready signals, RDY1 and RDY2 respectively
- wait states are generated by the **READY** pin of μP, which is controlled by $\overline{AEN1} and \overline{AEN2} pins$

RDY1 and RDY2

- Bus ready inputs
- Cause wait states in conjunction with $\overline{AEN1} and \overline{AEN2} pins$

$\overline{ASYNC}$

- Ready synchronization
- Selects either one or two stages of synchronization for RDY1 and RDY2 inputs

READY

- An output pin that connects to the $\mu P's$ READY input
- Synchronized with RDY1 and RDY2 inputs