

Microcontrollers & Embedded System Design
CSE 315

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Chapter 1

8086/8088 Hardware Specifications

1.1 Class Lec 2

1.1.1 Introductory text

This is the **first** CSE 300 class in Jan 2018 term. This is a new **line**. This is a new line. This is a new line. This is a new line. This is a new line.

1.1.2 Introductory text

This is the **first** CSE 300 class in Jan 2018 term. This is a new **line**. This is a new line. This is a new line.

1.1.3 description

\overline{RD} • Whenever this pin goes to logic 0, the data bus becomes receptive to data from the memory or I/O devices connected to the system.
• Floats to high impedance state during a hold acknowledge

READY • uP enters into WAIT state and remains idle if this pin is at logic 0
• No effect on operations of up, if this pin is at logic 1

INTR • Used to request a h/w interrupt
• If INTR is held high when $IF = 1$, the up enters an interrupt acknowledge cycle (INTA becomes active) after completion of the current instruction

TEST • An input that is tested by the WAIT instruction
• If TEST is logic 0, the **WAIT** instruction functions as **NOP**

- If TEST is logic 1, the **WAIT** instruction waits for *blue*TEST to become 0
 - NMI**
 - Non markable interrupt pin
 - Similar to the INTR except that NMI does not check IF (whether it is 1)
 - RESET**
 - Causes the uP to reset itself if this pin remains high for a minimum of four clocking periods
 - whenever the up gets reset , it begins executing instructions at memory location FFFFOH and disables future interrupts by clearing IF
 - CLK**
 - Provides the base timing signal to the up
 - Clock signal must have at least 33% duty cycle (high for the one-third of the clocking period and low for two-third of the period)
 - VCC**
 - Power supply input
 - Provides +5.0 volt with 10% tolerance to the up
 - GND**
 - 2 pins, both must be connected to ground
 - MN/MX**
 - Selects either minimum mode or maximum mode operation of the up
 - BHE/S7**
 - Bus high Enable
 - Used in 8086 to enable the most signifant data bus bits (D15 - D8) during a read or write operations
 - The state of S7 is always a logic 1
- Minimum Mode Pins
- IO/M or M/IO**
 - Selects memory or I/O
 - Indicates

1.2 Figures

Here, we will import figures. Figure 1.1 is our figure.

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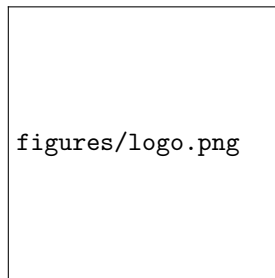


Figure 1.1: BUET Logo

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