Microcontrollers & Embeded System Design
CSE 315

Md Awsaf Alam

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Contents

1 8088 Hardware Specifications

1.1 Maximum Mode Pins

For using external coprocessors:

$\overline{S2}, \overline{S1} and \overline{S0}$ • Indicate the function of current bus-cycle
- Normally decoded by 8288 bus controllers

$\overline{R1}/\overline{G1} and \overline{R0}/\overline{GT0}$ • Request/grant pins
- Request Direct Memory Access
- Bi-Directional lines
- used to both request and grant a DMA operations

$\overline{LOCK}$ • Used to lock peripherals off the system

$\overline{QS_1} and \overline{QS0}$ • Queue status bits
- Show status of the internal instructions queue
- Accessed by numeric coprocessor (8087)

$\overline{QS_1}$	$\overline{QS_0}$	Function
0	0	Queue is idle
0	1	First byte of opcode
1	0	Queue is empty
1	1	Subsequent byte of opcode

Table 1:

2 Clock Generator (8284A)

Basic functions • Clock generation
- **RESET** synchronization
- READY synchronization
- TTL-level peripheral clock signal

2.1 Pin Functions

AEN1 and AEN2
- Qualify the bus ready signals, RDY1 and RDY2 respectively
- wait states are generated by the **READY** pin of μP, which is controlled by $\overline{AEN1}$ and $\overline{AEN2}$ pins

RDY1 and RDY2
- Bus ready inputs
- Cause wait states in conjunction with $\overline{AEN1}$ and $\overline{AEN2}$ pins

$\overline{ASYNC}$
- Ready synchronization
- Selects either one or two stages of synchronization for RDY1 and RDY2 inputs

READY
- An output pin that connects to the $\mu P's$ READY input
- Synchronized with RDY1 and RDY2 inputs