Microcontrollers & Embeded System Design
CSE 315

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Contents

Part I

8086/8088 Hardware Specifications

Chapter 1

Lecture 1

1.1 Differneces between 8086 & 8088

- Virtually no difference between these two μps. Both are packaged in 40-pin dual in-line packages (DIPs)

8086 16 bit μp with a 16-bit data bus ($AD_0 - AD_{15}$)

8088 16 bit μp with a 8-bit data bus ($AD_0 - AD_7$)

8086 : $M/\overline{IO}$; 8088 : $IO/\overline{M}$;
8086 (PIN 34): $\overline{BHE}/S7$; 8088 (PIN 34): SSO;

Power Supply Requirements

- Both : $+5.0V$ with a supply voltage tolerance of ±10%
- Both : $32°F$ to $180°F$
- 8086 : $360mA$; 8088 : $340mA$ (max supply current)
- CMOS version : 80C86 and 80C88 : $10mA$ and $-40°F$ to $225°F$

Pin diagram 8086

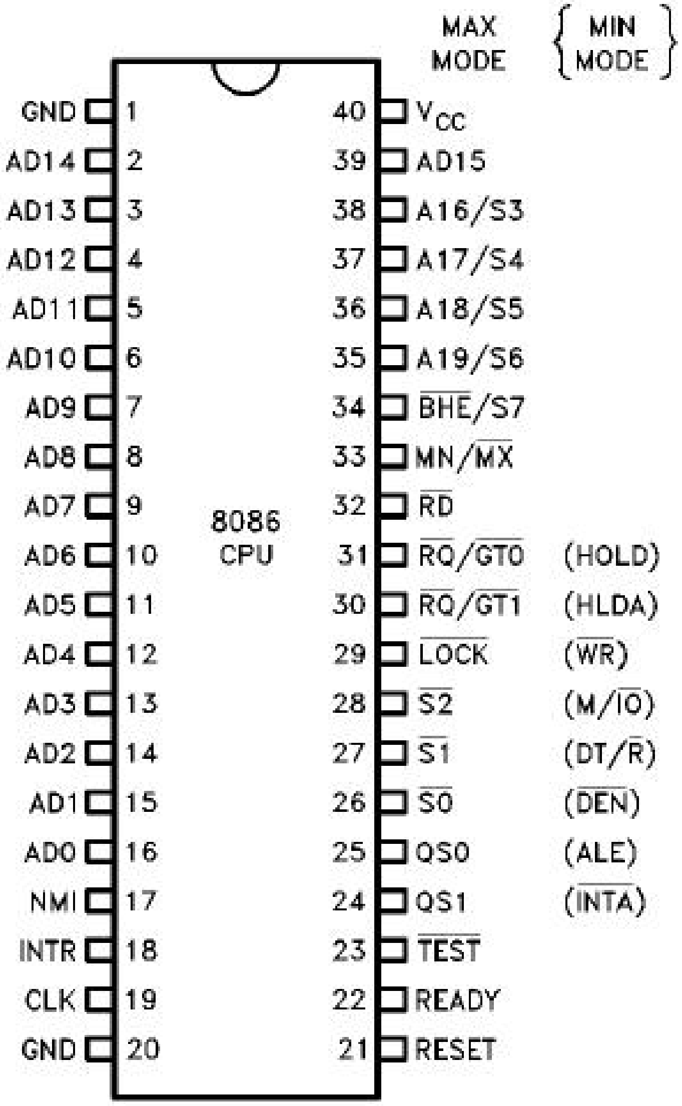
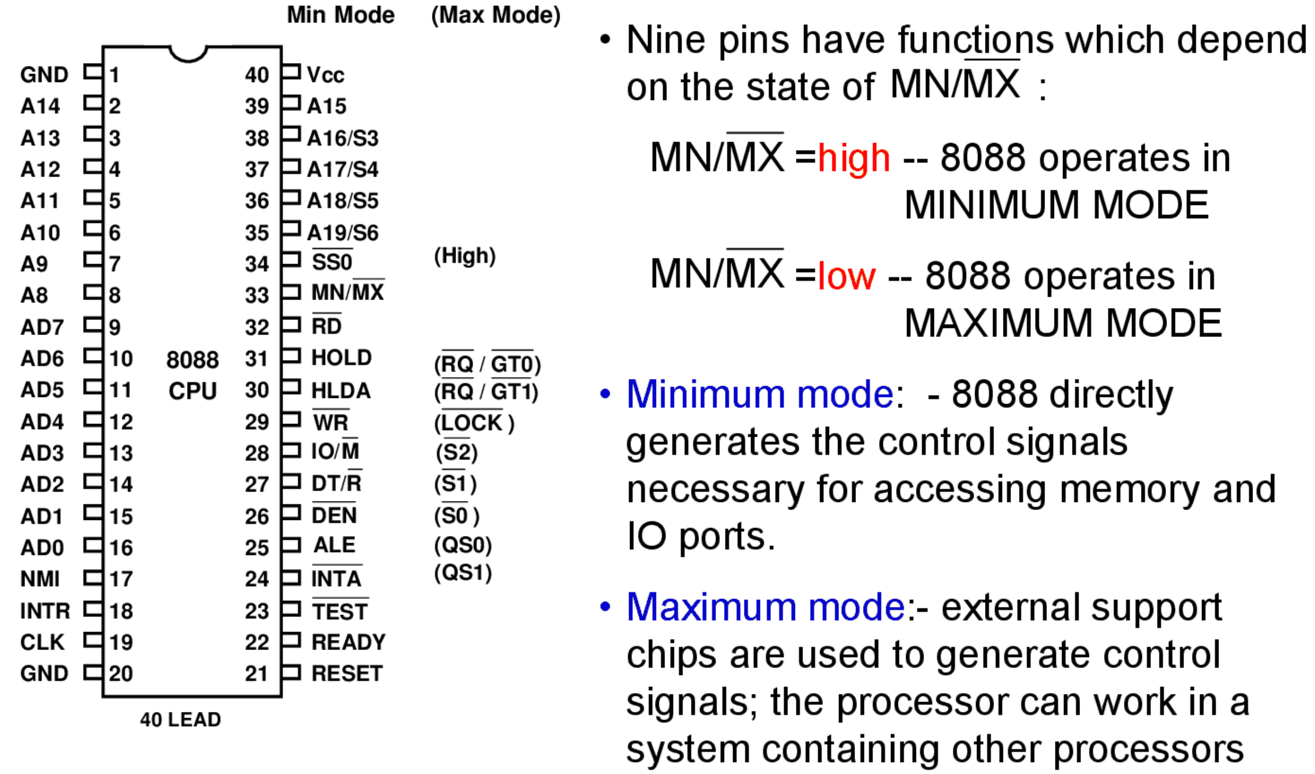


Figure 1.1: Pin Diagram for Intel 8086 Max mode Min Mode


Min Mode
(Max Mode)
GND 1
A14 2
A13 3
A12 4
A11 5
A10 6
A9 7
A8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
8088
CPU
40 Vcc
39 A15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 $\overline{\text{SS0}}$ (High)
33 MN/$\overline{\text{MX}}$
32 $\overline{\text{RD}}$
31 HOLD ($\overline{\text{RQ}}$ / $\overline{\text{GT0}}$)
30 HLDA ($\overline{\text{RQ}}$ / $\overline{\text{GT1}}$)
29 $\overline{\text{WR}}$ ($\overline{\text{LOCK}}$)
28 IO/$\overline{\text{M}}$ ($\overline{\text{S2}}$)
27 DT/$\overline{\text{R}}$ ($\overline{\text{S1}}$)
26 $\overline{\text{DEN}}$ ($\overline{\text{S0}}$)
25 ALE (QS0)
24 $\overline{\text{INTA}}$ (QS1)
23 $\overline{\text{TEST}}$
22 READY
21 RESET
40 LEAD

- Nine pins have functions which depend on the state of MN/$\overline{\text{MX}}$:

  MN/$\overline{\text{MX}}$ =high -- 8088 operates in MINIMUM MODE

  MN/$\overline{\text{MX}}$ =low -- 8088 operates in MAXIMUM MODE

- Minimum mode: - 8088 directly generates the control signals necessary for accessing memory and IO ports.

- Maximum mode:- external support chips are used to generate control signals; the processor can work in a system containing other processors

Figure 1.2: Pin Diagram for Intel 8088 Min mode Max Mode

Pin diagram 8088

1.2 Pin Connections

$AD_7 - AD_0$ • 8088 address / data bus lines

- Multiplexed address data bus
- Rightmost eight bits of the memory address or I/O port no. whenever ALE is active (Logic 1) or data whenever ALE is inactive (Logic 0)
- High impedance state during a hold acknowledge

$A_{15} - A_8$ • 8088 address bus (upper half memory address bits)

- High impedence state during a hold acknowledge.

$AD_{15} - AD_8$ • 8086 address/data bus lines

- Contains address bits $A_{15} - A_8$, when ALE is logic 1

- Enter in high-impedence state whenever a hold acknowledge occurs.

$A_{19}/S_6 - A_{16}/S_3$
- Multiplexed address/ status bus
- Enter in high-impedence during hold acknowledge.

S_6 Always 0

S_5 Indicates the condition of Interrupt flag

S_4, S_3 Indicate segment accessed during current bus cycle

S_4	S_3	Function
0	0	Extra Segment
0	1	Stack Segment
1	0	Code or no segment
1	1	Data Segment

Table 1.1: Segment accessed during current Bus cycle

$\overline{RD}$
- Whenever this pin goes to logic 0, the data bus becomes receptive to data from the memory or I?O devices connected to the system.
- Floats to high impedence state during a hold acknowledge

READY
- μp enters into **WAIT** state and remains idle if this pin is at logic 0
- No effect on operations of μp, if this pin is at logic 1

INTR
- Used to request a h/w interrupt
- If INTR is held high when $IF = 1$, the μp enters an interrupt acknowledge cycle ($\overline{INTA}$ becomes active) after completion of the current instruction

$\overline{TEST}$
- An input that is tested by the WAIT instruction
- If TEST is logic 0, the WAIT instruction functions as NOP
- If TEST is logic 1, the WAIT instruction waits for **TEST** to become 0

NMI
- Non markable interrupt pin
- Similar to the **INTR** except that NMI does not check IF (whether it is 1)

Chapter 2

Lecture 2

2.1 Pin Connections Continued

RESET

- Causes the μp to reset itself if this pin remains high for a minimum of four clocking periods
- whenever the up gets reset , it begins executing instructions at memory location **FFFFOH** and disables future interrupts by clearing IF

CLK

- Provides the base timing signal to the up
- Clock signal must have at least 33% duty cycle (high for the one-third of the clocking period and low for two-third of the period)

VCC

- Power supply input
- Provides +5.0 volt with 10% tolerance to the up

GND

- 2 pins, both must be connected to ground

MN/$\overline{MX}$

- Selects either minimum mode or maximum mode operation of the up

$\overline{BHE}$**/S7**

- Bus high Enable
- Used in 8086 to enable the most signifant data bus bits (D15 - D8) during a read or write operations
- The state of S7 is always a logic 1

2.2 Minimum Mode Pins

IO/$\overline{M}$ **or M/**$\overline{IO}$

- Selects memory or I/O
- Indicates the $\mu p's$ address bus contains either a memory address or an I/O port address

- High impedence state during a hold acknowledge

$\overline{WR}$

- Indicates that the μp is outputting data to a mem or I/O device
- Data bus contains valid data for memory or I/O during the time $\overline{WR}$ remains 0

$\overline{INTA}$

- A response to the INTR input pin
- Used to gate the interrupt vector number onto the databus in response to an interrupt request.

$\overline{ALE}$

- Address Latch Enable
- Indicates that the $\mu p's$ address/ data bus contains address information
- The address can be a mem address or I/O port number
- [Does **NOT** float during a hold acknowledge]

DT/$\overline{R}$

- Data Transmit or Receive
- Indicates that the $\mu p's$ data bus is transmitting ($DT/\overline{R} = 1$) or receiving ($DT/\overline{R} = 0$) data.
- Used to enable external data bus buffers.

DEN

- Data bus enable
- Activates external data bus buffers.

HOLD

- Requests a direct memory access (DMA)
- If it is a logic 1, μp stops executing S/W and places its address, data and control bus at high impedence state
- If it is a logic 0, the μp executes S/W normally

HLDA

- Hold acknowledge
- Indicates that the μp has entered the hold state

$\overline{SSO}$

- Equivalent to SO pin in maximum mode option of the μp
- It is combined with IO/$\overline{M}$ and DT/$\overline{R}$ to decode function of the current bus cycle

2.3 Bus Control functions

IO/$\overline{M}$	DT/$\overline{R}$	$\overline{SSO}$	Function
0	0	0	Interrupt acknowledge
0	0	1	Memory read
0	1	0	Memory write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	I/O read
1	1	0	I/O write
1	1	1	Passive inactive

Table 2.1: Bus cycle status (8088) [Minimum mode]

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Function
0	0	0	Interrupt acknowledge
0	0	1	I/O read
0	1	0	I/O write
0	1	1	Halt
1	0	0	Opcode fetch
1	0	1	Memory read
1	1	0	Memory write
1	1	1	Passive inactive

Table 2.2: Bus control functions generated by the bus controller 8288 [Maximum mode]

Chapter 3

Lecture 3

3.1 Maximum Mode Pins

For using external coprocessors:

$\overline{S2}, \overline{S1} and \overline{S0}$
- Indicate the function of current bus-cycle
- Normally decoded by 8288 bus controllers

$\overline{R1}/\overline{G1} and \overline{R0}/\overline{GT0}$
- Request/grant pins
- Request Direct Memory Access
- Bi-Directional lines
- used to both request and grant a DMA operations

$\overline{LOCK}$
- Used to lock peripherals off the system

$\overline{QS_1} and \overline{QS0}$
- Queue status bits
- Show status of the internal instructions queue
- Accessed by numeric coprocessor (8087)

$\overline{QS_1}$	$\overline{QS_0}$	Function
0	0	Queue is idle
0	1	First byte of opcode
1	0	Queue is empty
1	1	Subsequent byte of opcode

Table 3.1:

3.2 Clock Generator (8284A)

Basic functions

- Clock generation
- **RESET** synchronization
- READY synchronization
- TTL-level peripheral clock signal

3.2.1 Pin diagram

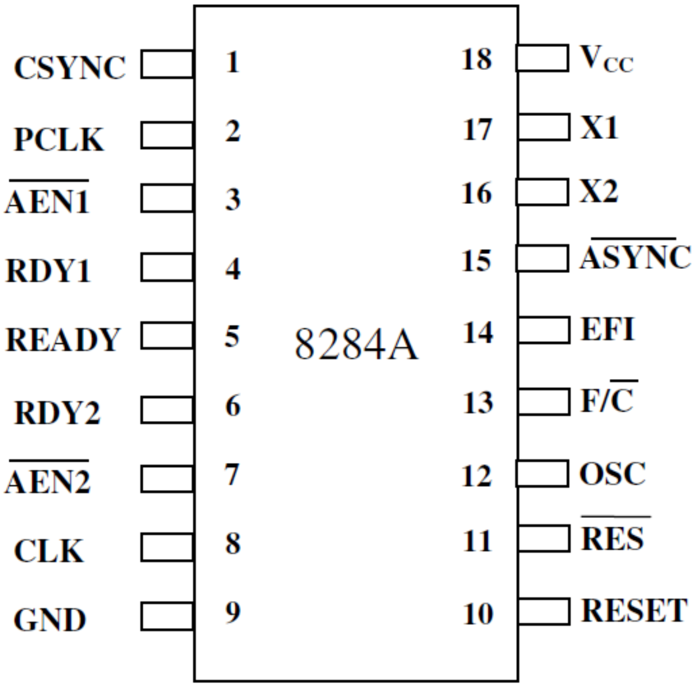


Figure 3.1: Pin Diagram for Intel 8284A

3.2.2 Pin Functions

AEN1 and AEN2
- Qualify the bus ready signals, RDY1 and RDY2 respectively
- wait states are generated by the **READY** pin of μP, which is controlled by $\overline{AEN1}$ and $\overline{AEN2}$ pins

RDY1 and RDY2
- Bus ready inputs
- Cause wait states in conjunction with $\overline{AEN1}$ and $\overline{AEN2}$ pins

$\overline{ASYNC}$
- Ready synchronization
- Selects either one or two stages of synchronization for RDY1 and RDY2 inputs

READY
- An output pin that connects to the $\mu P's$ READY input
- Synchronized with RDY1 and RDY2 inputs

X1 and X2
- Crystal oscillator Pins
- Connect to an external crystal, which is used as the timing source for rhe clock generator and all its functions

F/$\overline{C}$
- Frequrncy/ crystal select input
- Chooses the clocking source
- If it is held high, and external clock is provided to the EFI pin.
- If it is held low, the internal crystal oscillator provides the timing signal.

EFI
- External frequency input
- Supplies timing whenever $F/\overline{C}$ pin is held high

CLK
- Clock output pin, which provides clock input tp μP and other components
- Output signal and **one-third** of the crystal or EFI input frequency and has a duty cycle of 33% (as required by 8086/8088)

PCLK
- Peripheral clock
- One sixth of the crystal of EFI input frequency, and has a 50% duty cycle.

OSC
- Oscillator output
- At the same frequency as the crystal or EFI input
- Provides an EFI input to the other 8284A in a multiprocessor system.

$\overline{RES}$
- Reset input
- Often connected to an *RC network* that provides power on resetting

RESET
- Reset output
- connected to the $\mu P'$s RESET input pin

CSYNC
- Clock synchronization
- Used whenever the EFI input provides synchronization in a multiprocessor system
- If the *internal oscillator* is used , this pin must be grounded.

3.3 Internal Block Diagram of 8284A Clock Generator

- If a crystal is attached to X1 and X2, the oscillator generates a square wave signal at the same frequenct as the crystal
- $CLK = \frac{frequency}{3}$; $PCLK = \frac{frequency}{6}$;

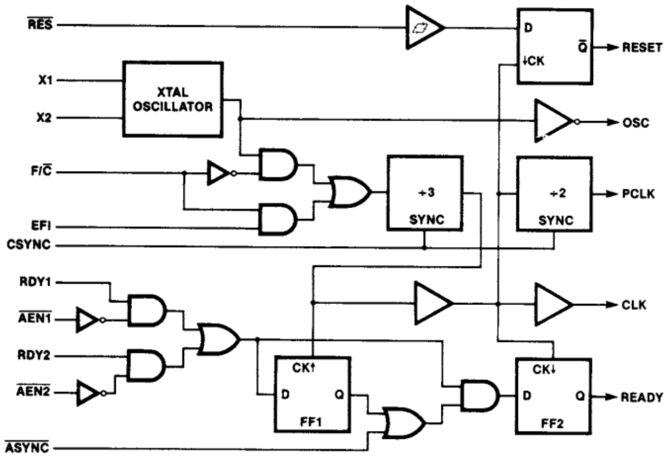


Figure 3.2: Internal Block Diagram of 8284A Clock Generator

3.3.1 Operation of the RESET selection

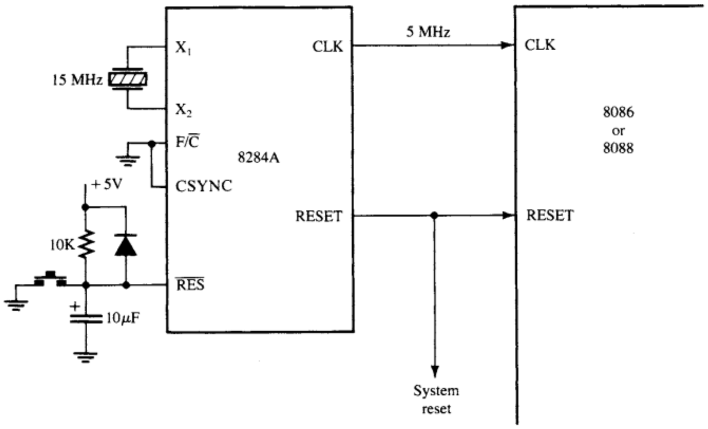


Figure 3.3: The clock generator (8284A) and the 8086 and 8088 microprocessors illustrating the connection for the clock and reset signals. A 15 MHz crystal provides the 5 MHz clock for the microprocessor

- $\overline{RES}$ goes through a **Schmitt Trigger** and a D-type flip-flop, which ensures meeting timing requirements of the $\mu P's$ RESET input.
- The circuit applies RESET to the μP at tghe negative edge ($1 \longrightarrow 0$),and the μP samples the RESET signal at the positive edge ($0 \longrightarrow 1$)

- When power is first applied to the system, the RC circuit provides a **logic 0** to the $\overline{RES}$
- After a short time, $\overline{RES}$ becomes **logic 1**, as the capacitor charges to the $+5V$ through the resistor
- The push allows the μP to be reset by an operator
- Correct RESET timing requires the RESET input to become a **logic 1** no later then 4 clock cycles after the power is applied, and held high for atleast $50\mu s$
- RESET goes high in 4 clock cycles: by FF
- RESET stays high for $50\mu s$: by RC time constant.

Chapter 4

Lecture 4

4.1 Bus Buffering and Latching

- The address / data bus on the μP is multiplexed (shared) to reduce the number of pins, which on the other hand, burdens with the task of extracting or *demultiplexing* info from these pins
- **Why not leave the buses multiplexed?**
  - Memory and I/O require that the address remains valid and stable throughout a read or write cycle. If the busses are multiplexed, the address can get changed causing read or write in wrong locations.
- All computer systems have three types of buses:
  1. **Address bus**: Provides memory address or I/O port numbers
  2. **Data bus**: Transfers data between μP and the memory I/O
  3. **Control bus**: Provides control signals to memory and I/O

4.2 Basic of Demultiplexing

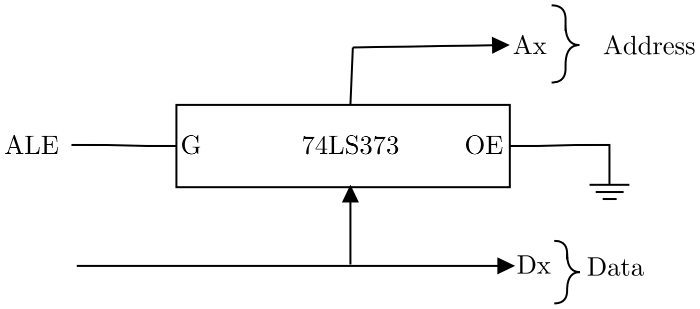


Figure 4.1: Using the 74LS373

4.2.1 Demultiplexing 8088

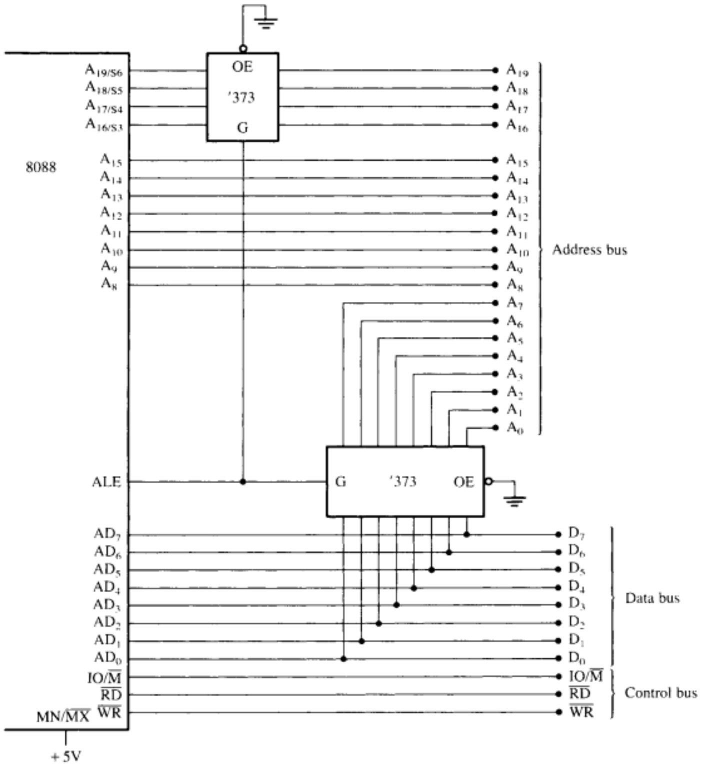


Figure 4.2: The 8088 microprocessor shown with a demultiplexed address bus. This is the model used to build many 8088-based systems.

- **74LS373** latches (OE for output enable and G or LE for latch enable inside) are used to demultiplex address/data bus connections and the address/status bus connections.

- **74LS373** passes inputs to outputs like wires when **ALE** is logic 1; when **ALE** is logic 0, the latches remember the inputs at the time of the change to logic 0.

4.2.2 Demultiplexing 8086

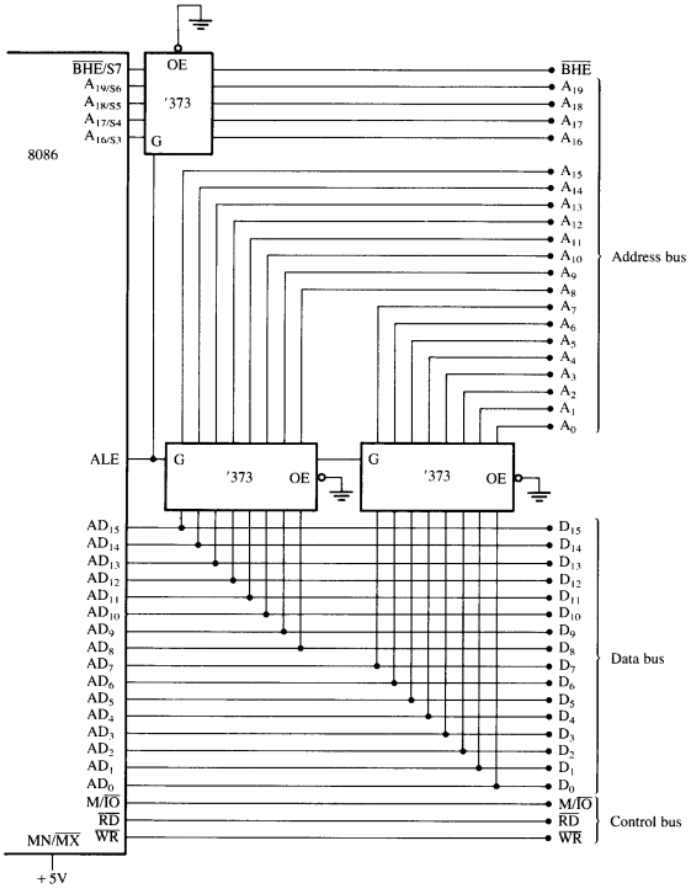


Figure 4.3: The 8086 microprocessor shown with a demultiplexed address bus. This is the model used to build many 8086-based systems.

- Difference from 8088 AD15 - AD8 and $\overline{BHE}/S7$ is that $\overline{BHE}$ selects a high-order memory bank in a 16-bit memory system in 8086.

4.3 Buffered System

- If more than 10 unit loads are attached to any bus pin, the entire μP system must be buffered (Buffer provides amplification in a digital circuit to drive output loads enabling more TTL unit loads to be driven)
- The *demultiplexed* pins are already buffered by the **74LS373** latches.
- A fully buffered signal will introduce a timing delay, which causes no difficulty unless memory or I/O devices are used that function at near the maximum speed of the bus.

4.3.1 Fully Buffered 8088

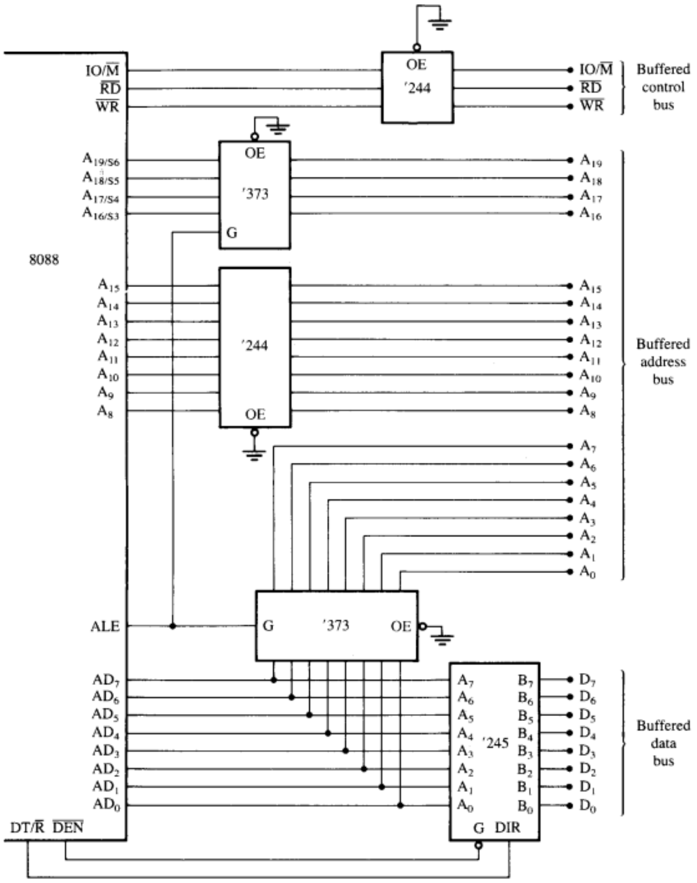


Figure 4.4: A fully buffered 8088 microprocessor.

- **74LS244**: Octal buffer
- **74LS245**: Octal bidirectional buffer

4.3.2 Fully Buffered 8086

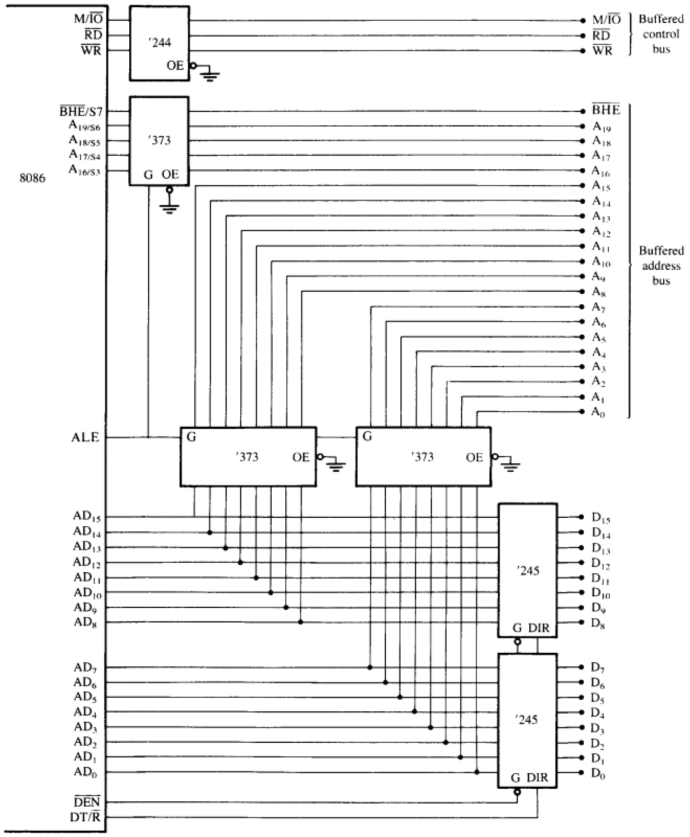


Figure 4.5: A fully buffered 8086 microprocessor.

4.3.3 Number of chips required for fully buffered microprocessor

μP	**74LS244** (Octal buffer)	**74LS245** (Octal bidirectional buffer)	**74LS373**
8088	2	1	2
8086	1	2	3

Table 4.1: Number of chips required for fully buffered microprocessor

Part II

Memory Interface

Chapter 5

Lecture 5

5.1 Memory Interface

- Four common types of memory:
  1. Read Only Memory (ROM)
  2. Flash memory (EEPROM)
  3. Static Random Access Memory (SRAM)
  4. Dynamic Random Access Memory (DRAM)
- Pin connections common to all memory devices :
  1. address inputs
  2. data outputs (inputs/outputs)
  3. some type of selection input
  4. Atleast one control input used to select a read or write operations
- Control connections:
  1. **ROM** $\longrightarrow$ Only one control input ($\overline{OE}$[Output Enable] or $\overline{G}$[Gate])
  2. **RAM** $\longrightarrow$ Only one($R/\overline{W}$) or two ($\overline{WE}/\overline{W}$ and $\overline{OE}/\overline{G}$) control input. [$\overline{WE}/\overline{W}$ and $\overline{OE}/\overline{G}$ do not get actualed at the same time]

5.1.1 ROM Memory (nonvolatile memory)

- Permanently stores programs that are resident to the system and must **not** change when power supply is disconnected (permanently programmed) for example BIOS.
- **EPROM** (Erasable Programmable ROM): Programmed using a device called EPROM programmer; erasable if exposed to high-intensity UV light for about 20 minutes or less.

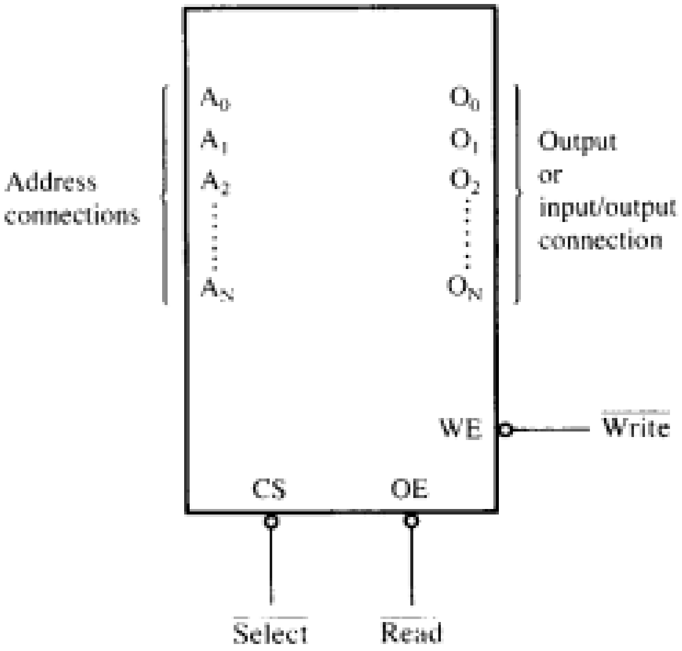


Figure 5.1: A pseudo-memory component illustrating the address, data, and control connections.

- **PROM** (Programmable ROM): Programmed by burning open tiny NI-Chrome or Silicon Oxide fuses; Once programmed, it cannot be erased

- **Read Mostly Memory**(RMM) or **Flash memory** or **EEPROM**(Electrically Erasable Programmable ROM) or **EAROM**(Electrically Alterable ROM) or **NOVRAM**(Non volatile RAM) : Electrically erasable however, needs more time to erase than a normal RAM.

5.1.2 Delays in operation od an EPROM

t_{acc1} : Address to output delay
t_{OH} : Address to output hold
t_{CO} : Chip Select to Output delay
t_{DF} : Chip Deselect to Output float

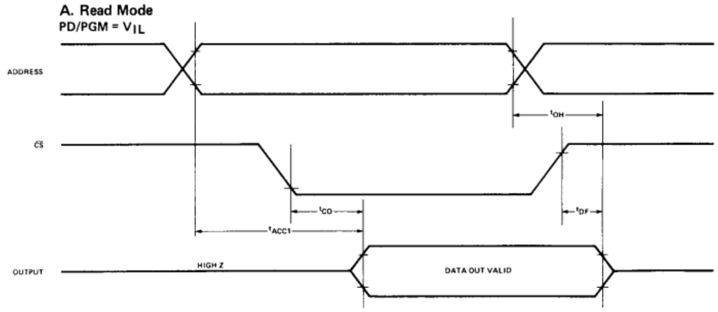


Figure 5.2: The timing diagram of AC characteristics of the 2716 EPROM.

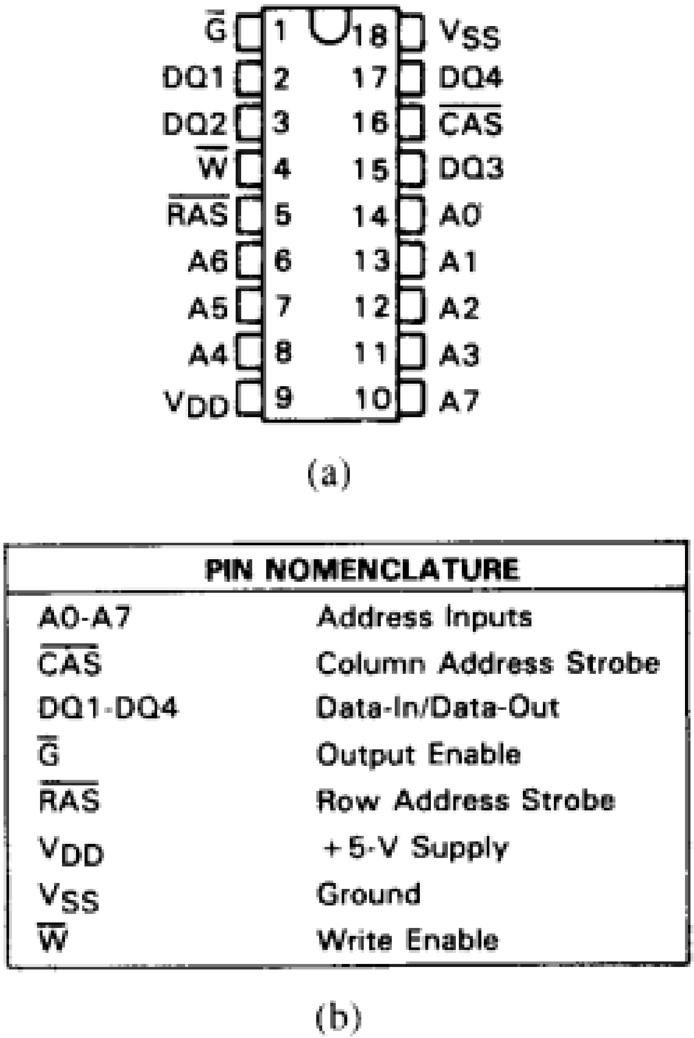
5.1.3 Static memory or static RAM(SRAM) or Volatile memory

- Retain data as long as DC power is applied (no data without power)
- Difference between ROM and RAM :
  - **RAM** ⟶ written under normal operation
  - **ROM** ⟶ programmed outside the computer and is normally read.

5.1.4 Dynamic Ram (DRAM)

- DRAM is essentially same as SRAM, except that it retains data for only 2 or 4ms on an integrated capacitor
- After 2 or 4 ms, the contents of DRAM must be completely rewritten (refreshed) because the capacitors (which store Logic 1/0) lose their charges.
- Refreshing also occurs during a write, a read, or during a special refresh cycle.
- Have much larger sizes compared to SRAM. Its obvious disadvantage is requirement of many address pins. To reduce the number of address pins, the address inputs are multiplexed.

Example of multiplexed address pins : 64K x 4 DRAM Here, for 64K, 16



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column Address Strobe
DQ1-DQ4	Data-In/Data-Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row Address Strobe
V_{DD}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

Figure 5.3: The pin-out of the TMS4464, 64K x 4 dynamic RAM (DRAM).

address pins are required. However, 8 address pins are used through multiplexing.

- At first, A0 - A7 are stored in internal row latch as row address through enabling $\overline{RAS}$
- Next, A8-A5 are stored in internal column latch as column address through enabling $\overline{CAS}$

Address multiplexer of 64K x 4

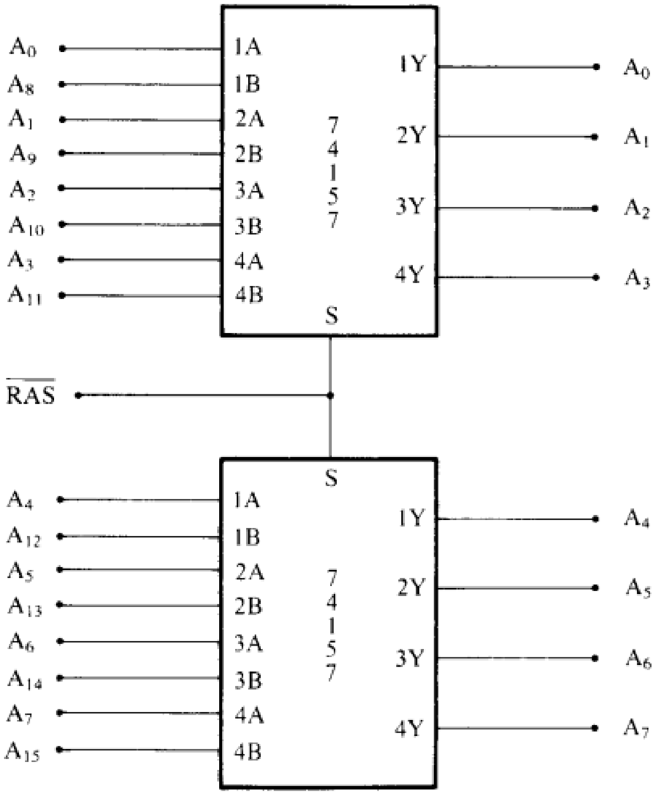


Figure 5.4: Address multiplexer for the TMS4464 DRAM.

- If $\overline{RAS}$ is 0, then A pins get connected and A0-A7 are stored in the internal Row Address latch
- *Internal Row Address Latch* is edge triggered, and therefore the row address gets captured into the latch before the address changes to column address.
- If $\overline{RAS}$ is 1, the the 8 pins get connected and A8-A15 are stored in *Internal Column Address Latch*

Chapter 6

Lecture 6

6.1 Address Decoding

- Decoding address sent from μP is necessary, as without it, only one memory device can be connected to a μP
- Another reason of decoding is possible mismatch (or difference) between the numbr of connections in μP and memory.

Example: a 2K x 8 EPROM (2716) has 11 address pins, whereas the μP 8088 has 20 address pins.

6.1.1 Simple NAND Gate Decoder

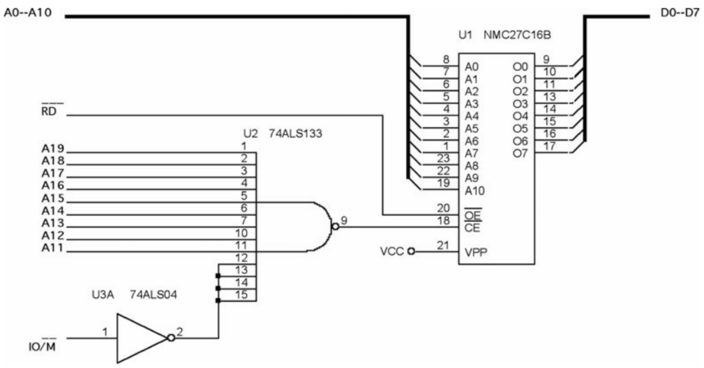
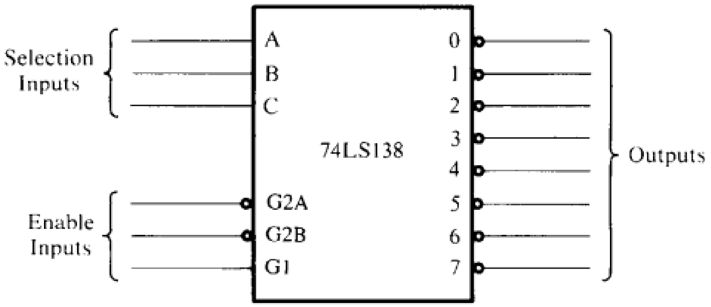


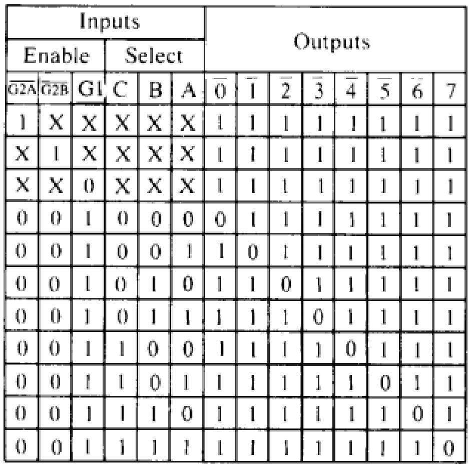
Figure 6.1: A simple NAND gate decoder that selects a 2716 EPROM for memory location FF800H–FFFFFH

- Here, the 2K EPROM is decoded at memory address locations **FF899H - FFFFFH**.(The FF8 corresponds to 1's in left nine positions)

- In such a decoding, one NAND gate decoder selects one 2K EPROM out of many 2K EPROMs that appear in 1M address space.
- The obvious disadvantage is that each EPROM needs one NAND gate decoder

6.1.2 3-to-8 Line Decoder(74LS138)





Inputs						Outputs							
Enable			Select										
$\overline{G2A}$	$\overline{G2B}$	G1	C	B	A	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	7
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

Figure 6.2: The 74LS138 3-to-8 line decoder and function table.

- **Input**: Enable = 001 and Selection(ABC) = n
- **Input**: $n^{th} output = 0$; all reset are 1
- **Input**: $Enable \neq 001$

- **Input**: All outputs are 1

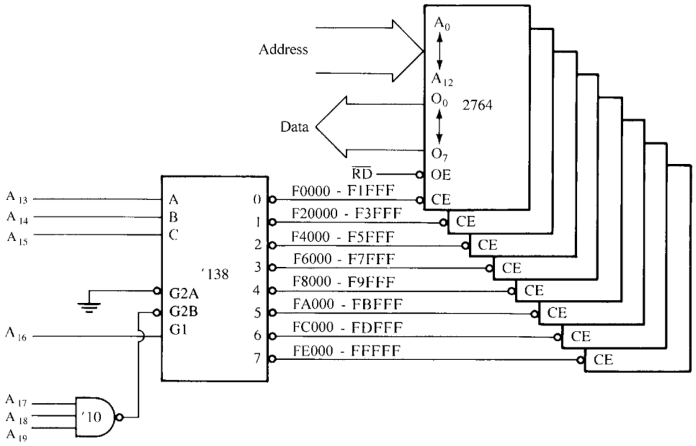


Figure 6.3: A circuit that uses eight 2764 EPROMs for a 64K x 8 section of memory in an 8088 microprocessor-based system. The addresses selected in this circuit are **F0000H-FFFFFH**

- A16-A19 must have 1 for activating 74LS138. Therefore, all addresses begin with "1111" at the left.

- Eight 2764 EPROMs (each 8K x 8, having 13 pins) are decoded over address space **F0000H-FFFFFH**(64K x 8)

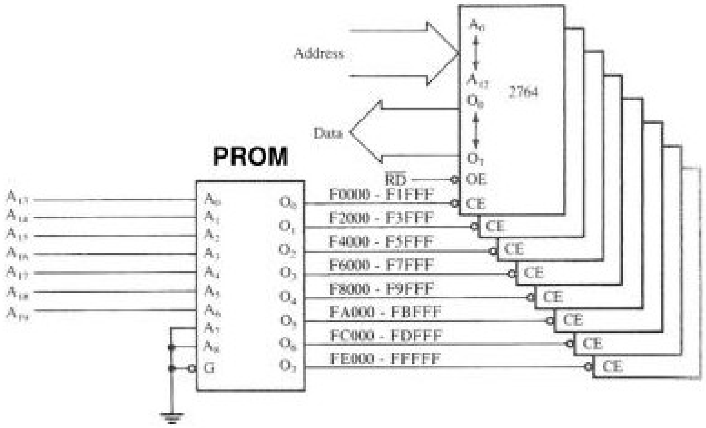
6.2 PROM Address Decoder

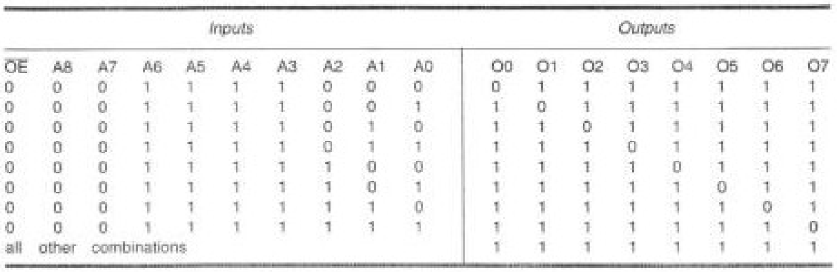
Bipolar PROM is used because of its larger number of input connections, which reduces the number of other circuits required in the decoding system.
Example: 82S147 (512 x 8) PROM has 10 input connections and 8 output connections. Among the input connections, 9 are used for memory addressing (of PROM) with 1 control (G) input.

Here, the control input ($\overline{G}$ or $\overline{CE}$) must be grounded, as if this PROM's outputs float to their high-impedence state, one or more of the PROMs might be selected by noise impulse of the system.

- Main advantage of using PROM is that address map can be easily changed.

- As the PROM comes with all the locationa programmed as logic 1, only eight of the 512 locations must be programmed.





Inputs										*Outputs*							
$\overline{OE}$	A8	A7	A6	A5	A4	A3	A2	A1	A0	O0	O1	O2	O3	O4	O5	O6	O7
0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	1	1	0	0	1	1	0	1	1	1	1	1	1
0	0	0	1	1	1	1	0	1	0	1	1	0	1	1	1	1	1
0	0	0	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1
0	0	0	1	1	1	1	1	0	0	1	1	1	1	0	1	1	1
0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	0	1	1
0	0	0	1	1	1	1	1	1	0	1	1	1	1	1	1	0	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
all other combinations										1	1	1	1	1	1	1	1

6.3 PLD programmable Decoders

There are three **Programmable Logic Devices**(PLDs) that function in the same manner:

1. PLA (Programmable Logic Array)
2. PAL (Programmable Array Logic)
3. GAL (Gated Array Logic)

- These devices can be programmed by blowing fumes to establish connections.
- The decoding circuit using a PLD is similar as that with a PROM, where the PROM gets replaced by the PLD (programmed with the logic representing the input-output pattern realized by PROM, as shown in a table in the last decoding)
- No control or selection logic is required hence.

Chapter 7

Lecture 7

7.1 8088 and 80188 (8-bit memory interface)

Examples presented here pertain to the minimum mode. The microprocessor has 20 address pins, 8 data pins and 3 control signals containing $IO/\overline{M}$, $\overline{RD}$, $and\,\overline{WR}$.

7.1.1 Interfacing EPROM to the 8088

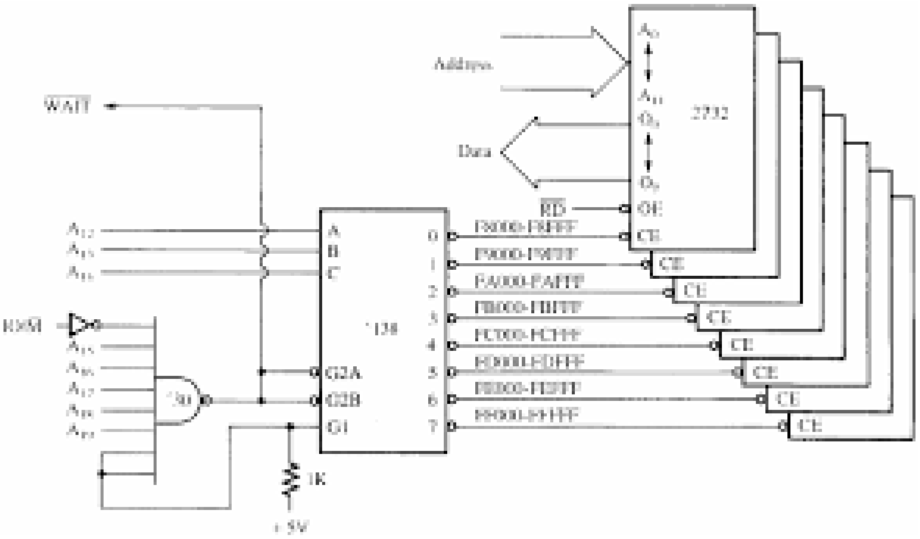


Figure 7.1: Interfacing EPROM 2732 to the 8088

- EPROM 2732 has a memory access time of 450 ms. 8-8 aperates with 5 MHz clock allowing 460ns for the memory to access data. However, as decoders added time delay is 12ms, it is impossible for the memory to function with the 40ns delay. Therefore, generating a signal for inserting **WAIT** states is required.

- Each extra wait state adds 200ns (1 clock cycle) making a total of 660ns for the EPROM to access data.
- The address space (F8000H - FFFFFH) includes the upper 32K bytes of memory containing FFFF0H, where 8088 starts executing instructions after a hardware reset. FFFF0H location is often called the "cold start" location. S/W stored at the FFFF0H location would contain a JMP instruction at FFFF0H that jumps to F8000H so the remainder of the program can execute.

7.1.2 Interfacing RAM to the 8088

- Most RAMs **do not** require wait states
- Interrupt vectors (often modified by S/W packages) reside in RAMs.

In the Figure 7.2, 16 *62256*(32K x 8) static RAMs are interfaced to 8088 beginning at memory location 00000H to 7FFFFH(512K x 8). Here, two decoders select from 1 different RAM components and a third to select the other decodes for appropriate memory selection.

- U4 selects the other two decoders. U3 selects sddresses beginning with 00 and U9 selects addresses beginning with 01. Extra pins of U4 remain for future extension.
- All address, data and control ($\overline{RD}$ and $\overline{WR}$) are buffered. Buffering is important when many devices appear in a single system. Excessive load without buffering can cause logic 0 output to rise above 0.V, maximum allowed in a system.

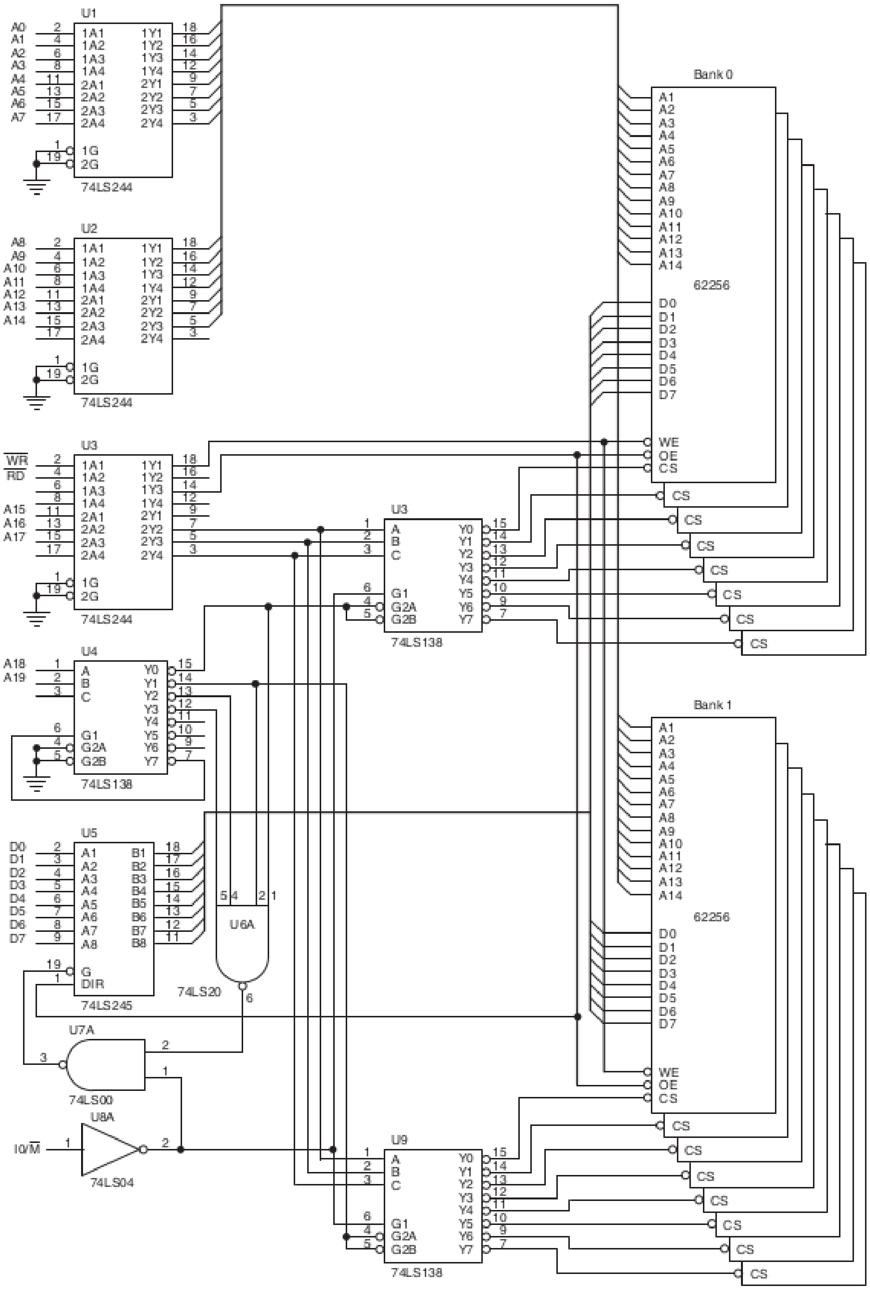


Figure 7.2: A 512K-byte static memory system using 16 62255 SRAMs.

Chapter 8

Lecture 8

8.1 Interfacing Flash Memory

Flash Memory requires a 12V programming voltage to erase or write new data. The 12V can be available either at the power supplyor through 5V-to-12V converter.

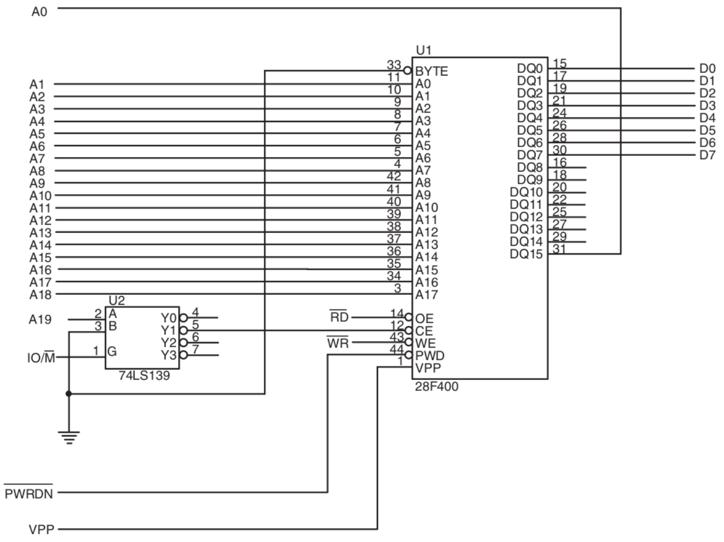


Figure 8.1: The 28F400 flash memory device interfaced to the 8088 microprocessor.

- **28F400** can be used either as a 512K x 8 or as a 512K x 16 memory device. For interfacing with 8088, it is used as a 512K x 8
- New pins in flash memory compared to SRAM :

1. VPP, which is connected to 12V for erasing and programming
2. $\overline{PWD}$, which selects power down mode when a logic 0 is applied and also used for programming.
3. BYTE, which selects byte(0) or word(1) operation.

- Pin **DQ15** functions as the least-signifcant address input when operated in byte mode
- Flash memory is much slower than SRAM (can need around $10^7 times$ more time).
- The single decoder (**74LS139**) uses address connection A19 and $IO/\overline{M}$ as inputs (location in the example : **80000H-FFFFFH**)

8.2 Parity for memory error detection

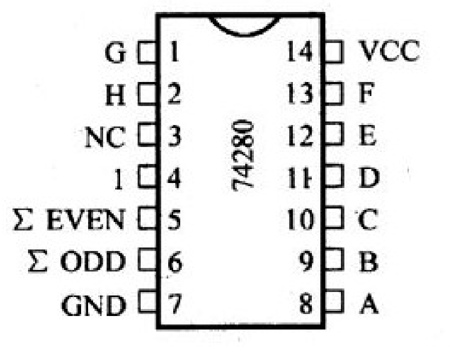
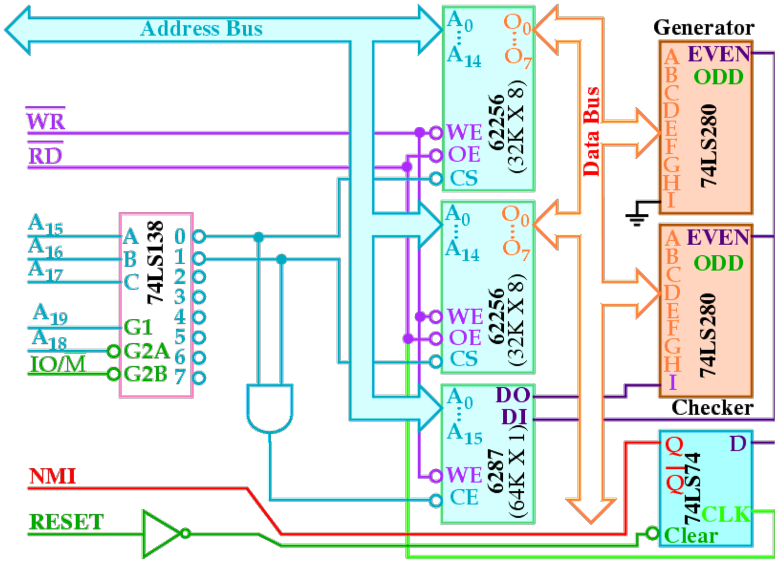


Figure 8.2: 9-bit parity generator/decoder

Input: Number of Logic 1's in A-I (9 pins)	Outputs	
	$\sum Even$	$\sum Odd$
0,2,4,6,8	H	L
1,3,5,7,9	L	H

Table 8.1: Number of chips required for fully buffered microprocessor

Example below shows 64K x 8 statis RAM using two 62556 (32K x 8) SRAMs having a parity bit stored in 6287 (64k x 1) SRAM generated by 74AS280 Decoded memory space is at **80000H-8FFFFH**. In Figure 8.2 as I of first **74LS280** is grounded, a 1 is stored in the parity RAM **6287**. If an even number of 1's appear in the data bus (connected to A-H). Thus, including the stored parity bit, an odd parity is stored for each byte.



- **Parity SRAM**: No $\overline{OE}$ connection for $\overline{RD}$. It reads data from output pin when selected ($\overline{CE}$ is enabled) and writes data when selected with $\overline{WE} = 0$.

- If overall parity is odd (everything is okay), the even parity output of second **74LS280** will become logic 1. The parity output is connected to 8088's NMI.

- Dataread from the memory are settled to the final state before an NMI input (error detection) occurs through being timed by a D flip-flop

- The DFF latches output of the parity checker **74LS280** at the end of an $\overline{RD}$ cycle on the memory.

8.3 Error correction

- **74LS636** : An -bit error correction and detection circuit that corrects any single bit memory read error and flags any 2-bit error.

- Corrects error by storing five parity bits with each byte of memory data.
- If more than two bits are in error(rare), the circuit ,may **not** detect it.
- Whenever a memory component fails completely, its bits are all high or all low. In this case, the circuit flags the processor with a multi-bit error detection.
- 8 data pins, 5 check bit pins, 2 control pins(S0 and S1), and 2 error outputs (**Single Error Flag**(SEF) and **Double Error Flag**(DEF))

S_0	S_1	Function	SEF	DEF
0	0	Write check word	0	0
0	1	Correct data word	*	*
1	0	Read data	0	0
1	1	Latch data	*	*

Table 8.2: Control inputs for 74LS636

* **:** ***These levels are determined by the type of error***

- When a single error is detected, the **74LS636** goes through an error correction cycle:
  It places 01 on S0 and S1 by causing a wait and then read following error correction.
- Difference in connection in memory components :
  $\overline{S}$ is grounded, which enable data to be accessed from memory before $\overline{RD}$ goes low.
- On the next negative edge of the clock after an $\overline{RD}$, the 74LS636 checks **SEF**. If a single bit error is detected, a correction cycle causes the single-bit error to be corrected. If a double-bit error is detected, **DEF** generates an NMI.

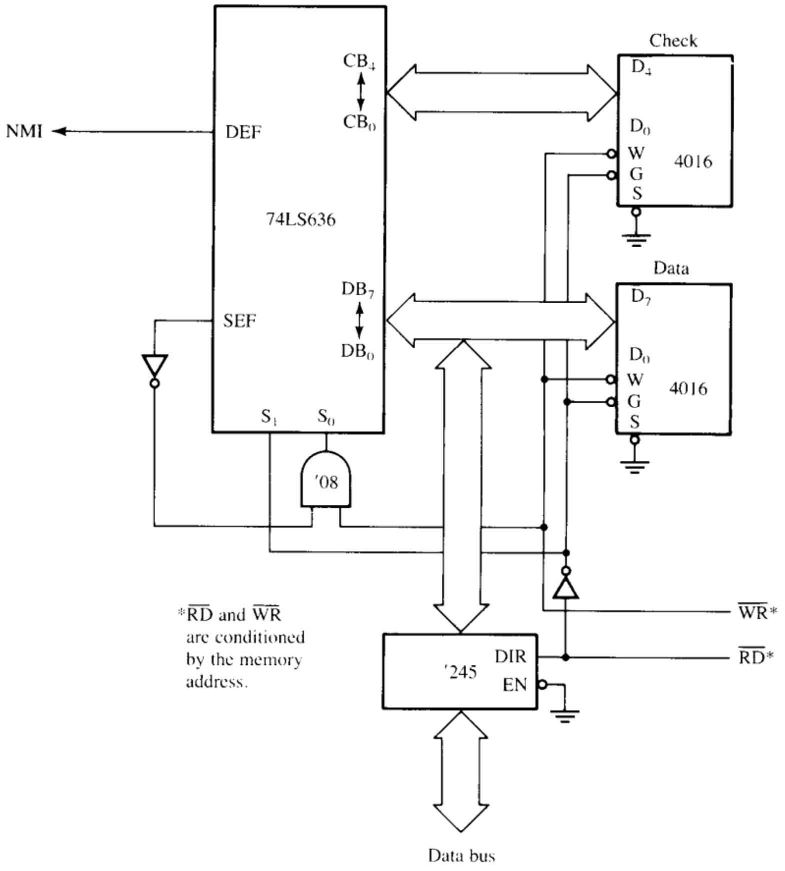


Figure 8.3: An error detection and correction circuit using the 74LS636.

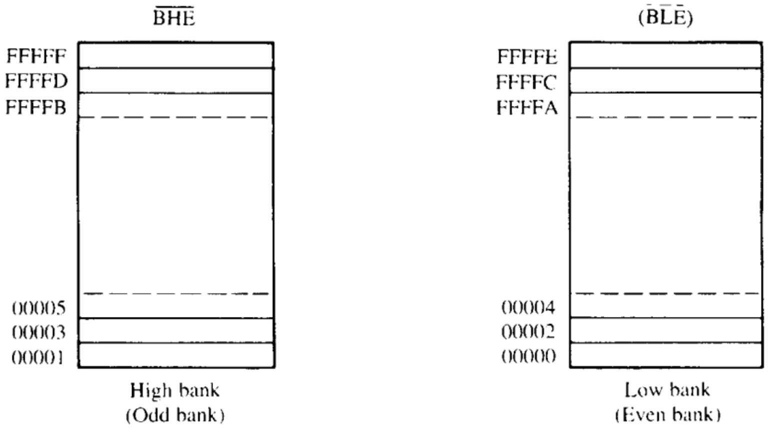
Chapter 9

Lecture 9

9.1 8086, 80186,80286,8038 (16-bit) memory interface

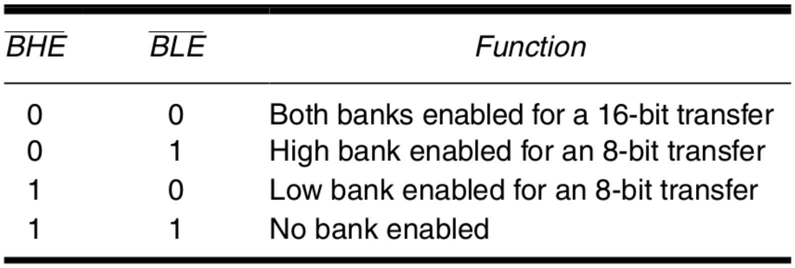
- **80286/80386**: 24-bit address bus. $\overline{MRDC}$ and $\overline{MWTC}$ instead of $\overline{RD}$ and $\overline{WR}$.

- These μPs must be able to write data to any 16-bit or 8-bit location. Therefore, the 16-bit data bus must be divided into two separate sections (banks), which are 8-bit wide.



Note: A_0 is labeled $\overline{BLE}$ (Bus low enable) on the 80386SX.

Figure 9.1: The high (odd) and low (even) 8-bit memory banks of the 8086/80286/80386SX microprocessors.



$\overline{BHE}$	$\overline{BLE}$	Function
0	0	Both banks enabled for a 16-bit transfer
0	1	High bank enabled for an 8-bit transfer
1	0	Low bank enabled for an 8-bit transfer
1	1	No bank enabled

Figure 9.2: Memory bank selection using $\overline{BHE}$ and $\overline{BLE}$ (A_0).

Bank selection is accomplished in two ways:

1. A separate write signal is developed to select a write to each bank (least costly)

2. Separate decoders are used for each bank

- Two 74LS138 decoders are used to select 64K RAM for 80386 μP (24-bit address)

- An enable pin (G2A) of U3[First 74LS138] is enabled by $\overline{BHE}$ and of U2[Second 74LS138] is enabled by $\overline{BLE}$ (A_0).

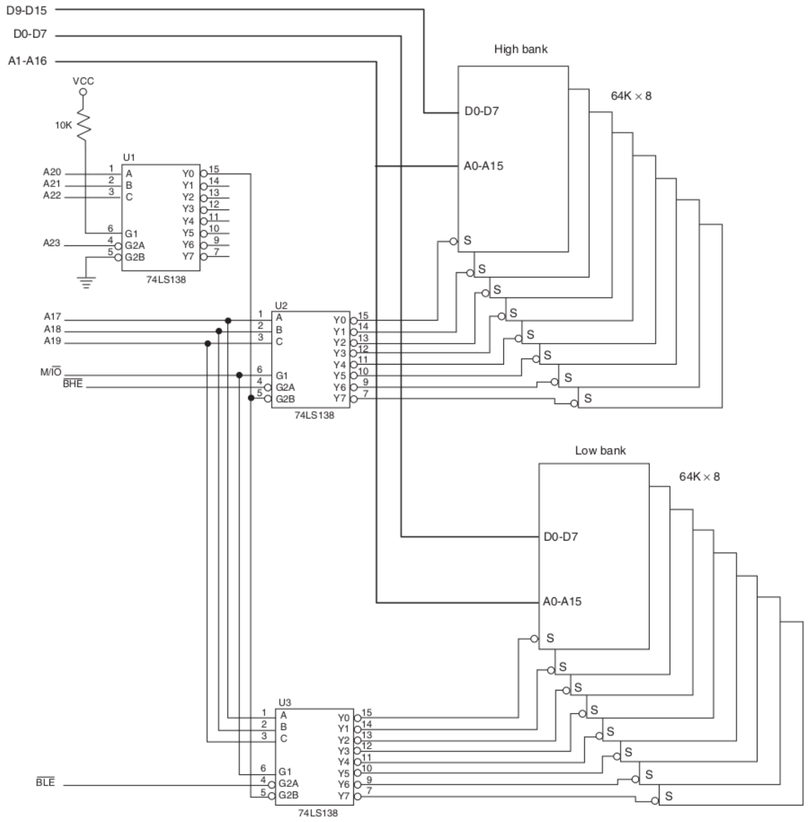


Figure 9.3: Separate bank decoders.

- U3 controls enabling the high bank, and U2 controls enabling the low bank.
- Decoded memory location range is **000000H-0FFFFFH**(1M).
- A_0 (or $\overline{BLE}$) is **not** connected to the memory to ensure having separate memory address (odd or even) in separate banks. If it would be connected to the memory address pin, the half of the memory will be wasted.
  [A_0 is **NOT** even a pin in 80386 μP]

9.2 8086 (16-bit) memory interface

Separate bank write strobes for memory: $\overline{WR}$ combines with A_0 for low bank selection ($\overline{LWR}$), and $\overline{BHE}$ for high bank selection ($\overline{HWR}$)
For 80286 and 80386: $\overline{MWTC}$ is used instead of $\overline{WR}$

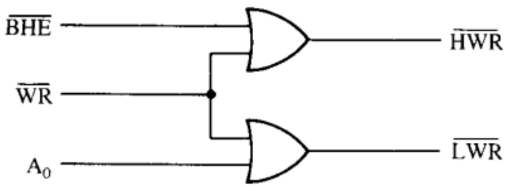


Figure 9.4: The memory bank write selection input signals: $\overline{HWR}$ (high bank write) and $\overline{LWR}$ (low bank write).

Why not also generate read strobe for each memory bank ?

- It is usually unnecessary as 086, 80286, 80386 μPs read only the byte of data they need at any given time ignoring the other parts without causing any problem.
- **Example**: 16-bit memory stored at locations 060000H-06FFFFH for 80286 or 80386 μP using PAL
- PAL logics:
  1. $\overline{CS} = \overline{A23} \cdot \overline{A22} \cdot \overline{A21} \cdot \overline{A20} \cdot \overline{A19} \cdot \overline{A18} \cdot \overline{A17} \cdot \overline{A16}$
  2. $\overline{LWR} = \overline{MWTC} \cdot \overline{A_0}$
  3. $\overline{HWR} = \overline{MWTC} \cdot \overline{BHE}$

Extend this concept of separate banking for all subsequent design (32, 64, ... bits) * SELF STUDY *****

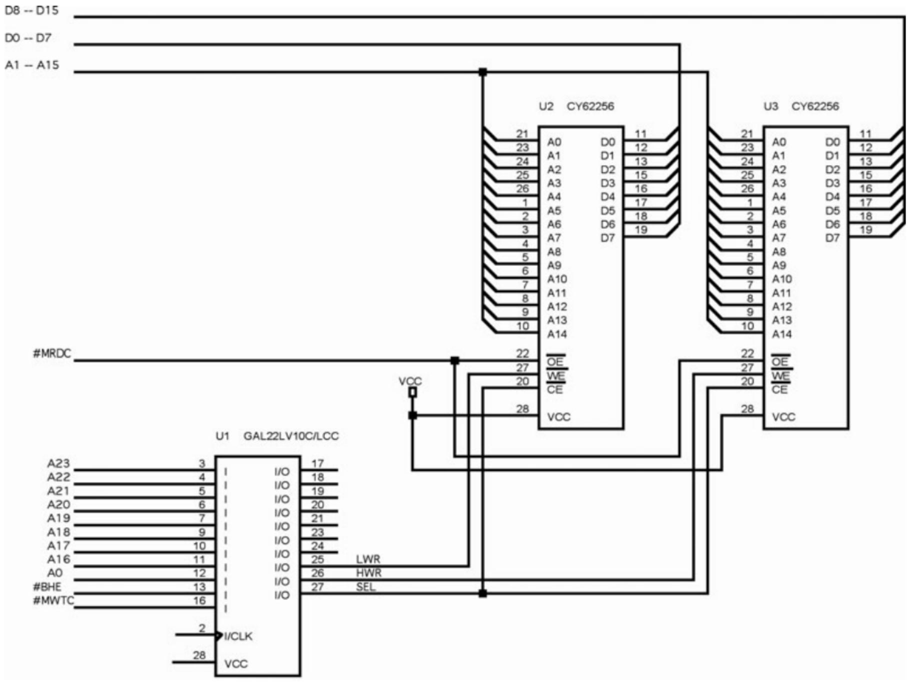


Figure 9.5: A 16-bit-wide memory interfaced at memory locations 06000H–06FFFH.

Example: A memory system for 8086 containing 64K byte EPROM and 128K byte SRAM.

- $\overline{RD}$ is connected to all $\overline{OE}$ inputs (enabling all 16-bits while reading).
- $\overline{LWR}$ and $\overline{HWR}$ are connected to different banks of RAM. Here, both $\overline{LWR}$ and $\overline{HWR}$ go low. For 8-bit eriting, either of them goes low. Such writing is **not** needed for EPROM
- A 74LS139 (dual 2-to-4 decoder) is used to select EPROM with one half and RAM with the other half. It decodes memory as 1-bit wide (not 8-bit).
- EPROM's decoder signal is sent to 8086 wait state generator.

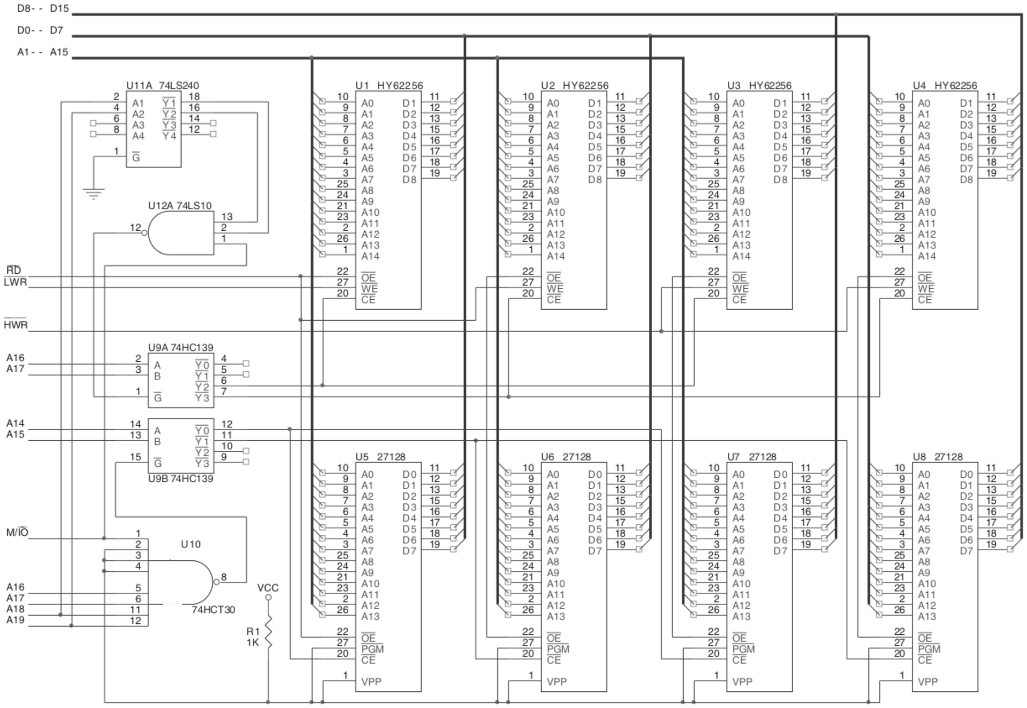


Figure 9.6: A memory system for the 8086 that contains a 64K-byte EPROM and a 128K-byte SRAM.

Chapter 10

Lecture 10

10.1 DRAM