

1. What are the GPIO control registers that the lab mentions? Briefly describe each of their functions.

MODER / Mode Register: GPIO port mode register. Set the mode of the pin. Input, general purpose, etc.

OTYPER / Output TYpe Register: GPIO port output type register. Sets the output to push push or open drain.

OSPEEDR / GPIO port output speed register: GPIO speed register. Sets the speed of the GPIO pin. Low, medium, or high speed.

PUPDR / GPIO port pull-up/pull-down register: Sets the GPIO to pull up, pull down, etc.

IDR / GPIO port input data register: Outputs the value of the GPIO port.

2. What values would you want to write to the bits controlling a pin in the GPIOx_MODER register in order to set it to analog mode?

The two bits controlling the pin would need to be set to 11.

3. Examine the bit descriptions in GPIOx_BSRR register: which bit would you want to set to clear the fourth bit in the ODR?

You would set bit 20 of the BSRR in order to reset the fourth bit in the ODR.

4. Perform the following bitwise operations:

- $0xAD \mid 0xC7 = 10101101 \mid 11000111 = 11101111$
- $0xAD \& 0xC7 = 10101101 \& 11000111 = 10000101$
- $0xAD \& \sim(0xC7) = 10101101 \& 00111000 = 00101000$
- $0xAD \wedge 0xC7 = 10101101 \wedge 11000111 = 01101010$

5. How would you clear the 5th and 6th bits in a register while leaving the other's alone?

Register = $\sim((1 \ll 5) \mid (1 \ll 6));$

6. What is the maximum speed the STM32F072R8 GPIO pins can handle in the lowest speed setting?

Lowest bit on the OSPEEDR should be 0 second bit can be whatever value. If V_{DDIOX} is less than 2V then the max frequency at the low setting is 1MHz othersize the max frequency is 2MHz.

V_{DDIOX} is the I/O supply voltage.

7. What RCC register would you manipulate to enable the following peripherals: (use the comments next to the bit defines for better peripheral descriptions)

- TIM1 (TIMER1): APB peripheral clock enable register 2 (RCC_APB2ENR) Bit 11
- DMA1: AHB peripheral clock enable register (RCC_AHBENR) Bit 0
- I2C1: APB peripheral clock enable register 1 (RCC_APB1ENR) Bit 21