Why can’t you use both pins PA0 and PC0 for external interrupts at the same time?
PA0 and PC0 both go to the MUX that drives EXTI0 so you can’t use them both together.
What software priority level gives the highest priority? What level gives the lowest?
Priority 0 is the highest and priority 4 is the lowest.
How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt (including non-implemented bits)? Which bits in the group are implemented?
The IPR registers provide an 8-bit priority field for each interrupt. These registers are only word-accessible. Each register holds four priority fields. The processor implements only bits[7:6] of each field, bits[5:0] read as zero and ignore writes.
What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer? Make sure to include a screenshot in the post-lab submission.
About 35ms between button press and LED change. (Images on GitHub repo)
Why do you need to clear status flag bits in peripherals when servicing their interrupts?
You need to clear the status flag to show that the interrupt has been handled. Otherwise it will keep calling the interrupt handler.