RTL8029AS

Realtek PCI Full-Duplex Ethernet Controller with built-in SRAM

ADVANCE INFORMATION

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1. FEATURES

- 100-pin PQFP
- ❋ **Pin-to-pin compatible with RTL8029**
- ❋ **16K byte SRAM built in**
- ❋ **Compliance to PCI V2.1**
- ❋ **Programmable PCI Vendor ID and Sub Vendor ID**
- PCI local bus single-chip Ethernet controller
- Compliant to Ethernet II and IEEE802.3 10Base5, 10Base2, 10BaseT
- Supports Full-Duplex Ethernet function to double channel bandwidth
- ❋ **Support Flow Control(802.3x) to improve network performance in full-duplex mode**
- Supports three level power down modes:

  - Sleep

  - Power down with internal clock running

  - Power down with internal clock halted

- Built-in data prefetch function to improve performance
- Built-in 10BaseT transceiver
- Provides auto-detect capability between integrated 10BaseT transceiver and Attachment Unit Interface (AUI)
- Supports auto polarity correction for 10BaseT
- Supports Boot ROM function for PCI bus
- Supports 8K, 16K and 32K Boot ROM size
- Use 9346 (64*16-bit EEPROM) to store resource configurations and ID parameters
- Capable of programming blank 9346 on board for manufacturing convenience
- Supports 4 diagnostic LED pins with programmable outputs

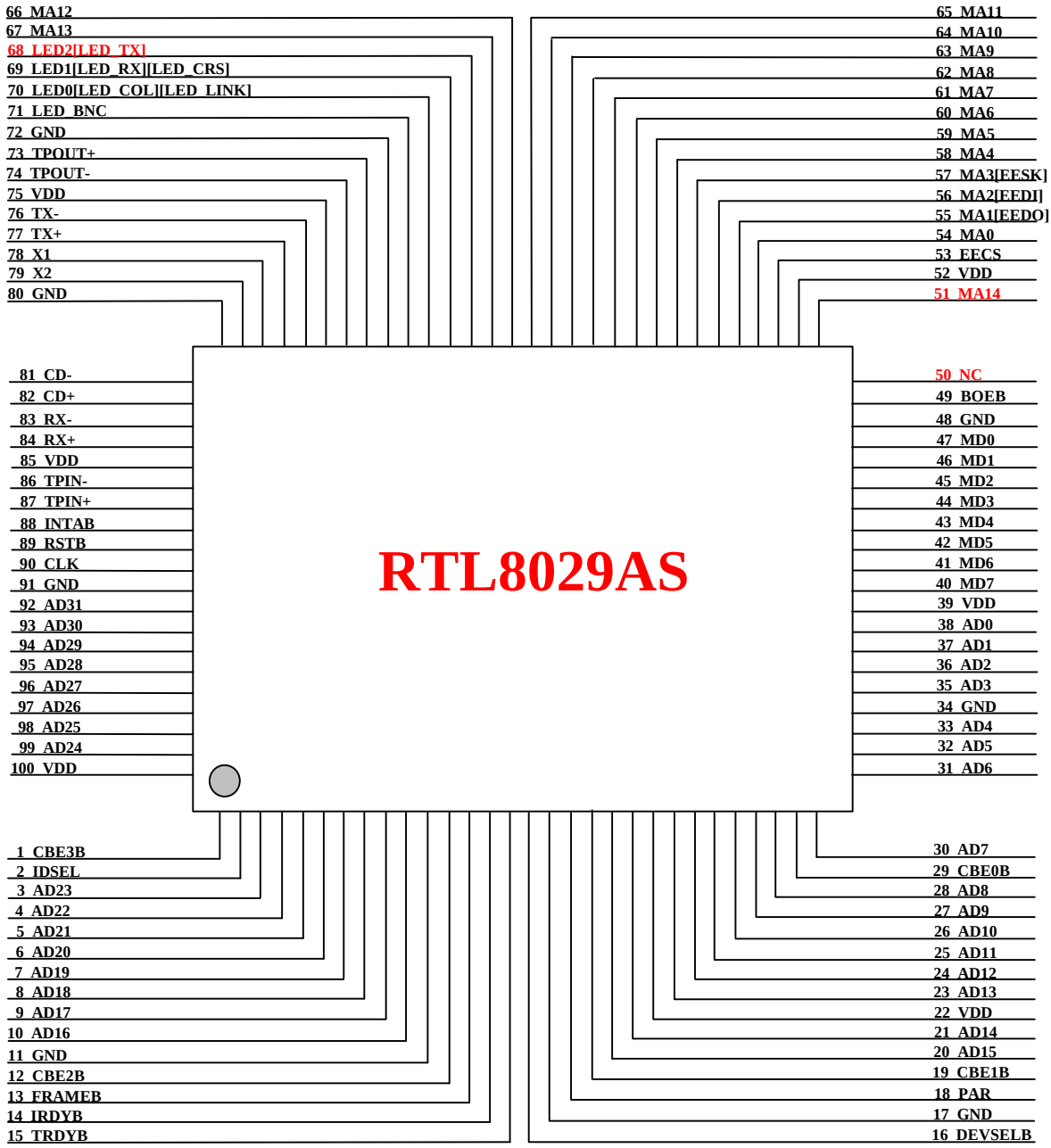
P.S. "❋" denotes new feature of RTL8029AS

2. GENERAL DESCRIPTION

The RTL8029AS controller is an NE2000 compatible Ethernet Controller for PCI interface. Taking the benefit of PCI's high throughput rate, the RTL8029AS controller offers a 32-bit data path to highly improve the data transfer rate compared with traditional Ethernet card on ISA, EISA and MCA bus. Due to the additional benefits of PCI, the RTL8029AS controller provides a low maintaining cost network environment without usage barriers. The Auto-configuration function of PCI can relieve the users from pains of taking care the system resource conflict. The RTL8029AS controller also supports full-duplex and power down features. With three levels power down control features, the RTL8029AS controller is made to be an ideal choice of the network device for a GREEN PCI PC system. The full-duplex function enables simultaneously transmission and reception on the twisted-pair link to a full-duplex Ethernet switching hub. This feature not only increases the channel bandwidth from 10 to 20 Mbps but also avoids the performance degrading problem due to the channel contention characteristics of the Ethernet CSMA/CD protocol.

The RTL8029AS controller requires no glue logic and integrates with Manchester Encoder/Decoder and 10BaseT transceiver on chip. The built-in 10BaseT transceiver can automatically correct the polarity error on its receiving pair. The RTL8029AS controller also has the capability of auto-sensing for 10Base2 or 10BaseT connection. Four diagnostic LEDs supported by RTL8029AS controller simplify the troubleshooting procedure in a network. Furthermore, The RTL8029AS controller supports 8K, 16K & 32K byte Boot ROM. It can be applied in a workstation without disk to improve the network security and management convenience. Data prefetch function in RTL8029AS controller can enhance the data transmission and highly uplift the network performance without extra fee.

3. PIN CONFIGURATION



4. PIN DESCRIPTIONS

4.1. Signal Type Definition

P Power pins include VDD and GND.

I Input is a standard input-only signal.

O It indicates output signal.

T/S Tri-State is a bi-directional, tri-state input/output pin.

S/T/S Sustained Tri-State is an active low tri-state signal owned and driven by one and only one agent at a time. The agent that drives an S/T/S pin low must drive it high for at least one clock before letting it float.

O/D Open Drain allowed multiple device to share as a wire-OR.

4.2. Power Pins

No.	Name	Type	Description
22, 39, 52, 75, 85, 100	VDD	P	+5V DC power
11, 17, 34, 48, 72, 80, 91	GND	P	Ground

4.3. PCI Bus Interface Pins

No.	Name	Type	Descriptions
90	CLK	I	Bus Clock provides timing for all transactions on PCI and is an input pin to every PCI device. All bus signals are sampled on the rising edge of CLK and all parameters are defined with respect to this edge.
92-99, 3-10, 20, 21, 23-28, 30-33, 35-38	AD31-0	T/S	Address/Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. The address phase is the clock cycle in which FRAMEB is asserted. During data phase AD7-0 contain the least significant byte(lsb) and AD31-24 contain the most significant byte(msb). Write data is stable and valid when IRDYB is asserted and read data is stable and valid when TRDYB is asserted.
1, 12, 19, 29	CBE3-0B	T/S	Bus Command/Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, CBE3-0B define the Bus Command. During the data phase CBE3-0B are used as Byte Enables. The Byte Enables define which physical byte lanes carry meaning data. CBE0B applies to byte 0(lsb) and CBE3B applies to byte 3(msb).

18	PAR	T/S	Parity is even parity across AD31-0 and CBE3-0B. PAR is stable and valid one clock after the address phase. For data phases PAR is stable and valid one clock after either IRDYB is asserted on a write transaction or TRDYB is asserted on a read transaction.
13	FRAMEB	S/T/S	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAMEB is asserted to indicate a bus transaction is beginning. While FRAMEB is asserted, data transfers continue. When FRAMEB is deasserted, the transaction is in the final data phase.
14	IRDYB	S/T/S	Initiator Ready indicates the initiating agent's ability to complete the current data phase of the transaction. IRDYB is used in conjunction with TRDYB. A data phase is completed on any clock when both IRDYB and TRDYB are asserted. During a write, IRDYB indicates that valid data is present on AD31-0. During a read, it indicates the master is prepare to accept data. Wait cycles are inserted until both IRDYB and TRDYB are asserted simultaneously.
15	TRDYB	S/T/S	Target Ready indicates the target's agent's ability to complete the current data phase of the transaction. TRDYB is used in conjunction with IRDYB. A data phase is completed on any clock when both TRDYB and IRDYB are asserted. During a read, TRDYB indicates that valid data is present on AD31-0. During a write, it indicates the target is prepare to accept data. Wait cycles are inserted until both IRDYB and TRDYB are asserted simultaneously.
16	DEVSELB	S/T/S	Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, DEVSELB indicates whether any device on the bus has been selected.
2	IDSEL	I	Initialization Device Select is used as a chip select for RTL8029AS controller during configuration read and write transaction.
89	RSTB	I	When RSTB is asserted low, the RTL8029AS performs an internal system hardware reset. RSTB must be held for a minimum of 120 ns periods. RSTB may be asynchronous to CLK when asserted or deasserted. It is recommended that the deassertion be synchronous to guarantee clean and bounce free edge.
88	INTAB	O/D	Interrupt A is an asynchronous attention signal which is used to request an interrupt.

4.4. Memory Interface Pins (including BROM, EEPROM)

No.	Name	Type	Description
49	BOEB	O	Boot ROM chip select. Active low signal, asserted when Boot ROM is read.
50	NC	-	Unused
53	EECS	O	9346 chip select. Active high signal, asserted when 9346 is read/write.
51, 67-54	MA14-0	O	Boot ROM address bus
[57]	[EESK]	O	9346 serial data clock

[56]	[EEDI]	O	9346 serial data input
[55]	[EEDO]	I	9346 serial data output
40-47	MD7-0	I/O	Boot ROM data bus

4.5. Medium Interface Pins

No.	Name	Type	Description
82, 81	CD+,CD-	I	This AUI collision input pair carries the differential collision input signal from the MAU.
84, 83	RX+,RX-	I	This AUI receive input pair carries the differential receive input signal from the MAU.
77, 76	TX+,TX-	O	This AUI transmit output pair contains differential line drivers which send Manchester encoded data to the MAU. These outputs are source followers and require 270 ohm pull-down resistors to GND.
87, 86	TPIN+,TPIN-	I	This TP input pair receives the 10 Mbits/s differential Manchester encoded data from the twisted-pair wire.
73, 74	TPOUT+,TPOUT-	O	This pair carries the differential TP transmit output. The output Manchester encoded signals have been pre-distorted to prevent overcharge on the twisted-pair media and thus reduce jitters.
78	X1	I	20Mhz crystal or external oscillator input.
79	X2	O	Crystal feedback output. This output is used in crystal connection only. It must be left open when X1 is driven with an external oscillator.

4.6. LED Output Pins

No.	Name	Type	Description
71	LED_BNC	O	This pin goes high when RTL8029AS's medium type is set to 10Base2 mode or auto-detect mode with link test failure. Otherwise, this pin is low. This pin can be used to control the power of the DC converter for CX MAU and connected to an LED to indicate the used medium type.
70	LED0	O	When LEDS0 bit (in CONFIG3 register of RTL8029AS Page3) is 0, this pin acts as LED_COL. When LEDS0=1, it acts as LED_LINK.
69, 68	LED1,LED2	O	When LEDS1 bit (in CONFIG3 register of RTL8029AS Page3) is 0, these 2 pins act as LED_RX & LED_TX respectively. When LEDS1=1, these pins act as LED_CRS & MCSB. Please refer to section 6.5 for details of the lightening behavior of all LEDs.

5. REGISTER DESCRIPTIONS

The registers in RTL8029AS controller can be roughly divided into two groups by their address and functions -- one for NE2000, the other for PCI Configuration Space.

5.1. Group 1: NE2000 Registers

This group includes 4 pages of registers which are selected by bit PS0 & PS1 in the CR register. Each page contains 16 registers. Besides those registers compatible with NE2000, the RTL8029AS controller defines some registers for software configuration and feature enhancement.

5.1.1. Register Table

No (Hex)	Page0		Page1	Page2	Page3	
	[R]	[W]	[R/W]	[R]	[R]	[W]
00	CR	CR	CR	CR	CR	CR
01	CLDA0	PSTART	PAR0	PSTART	***9346CR***	***9346CR***
02	CLDA1	PSTOP	PAR1	PSTOP	-	-
03	BNRY	BNRY	PAR2	-	***CONFIG0***	-
04	TSR	TPSR	PAR3	TPSR	-	-
05	NCR	TBCR0	PAR4	-	***CONFIG2***	***CONFIG2***
06	FIFO	TBCR1	PAR5	-	***CONFIG3***	***CONFIG3***
07	ISR	ISR	CURR	-	-	-
08	CRDA0	RSAR0	MAR0	-	-	-
09	CRDA1	RSAR1	MAR1	-	-	***HLTCLK***
0A	***8029ID0***	RBCR0	MAR2	-	-	-
0B	***8029ID1***	RBCR1	MAR3	-	-	-
0C	RSR	RCR	MAR4	RCR	-	-
0D	CNTR0	TCR	MAR5	TCR	-	-
0E	CNTR1	DCR	MAR6	DCR	***8029ASID0***	-
0F	CNTR2	IMR	MAR7	IMR	***8029ASID1***	-
10-17	Remote DMA Port					
18-1F	Reset Port					

Notes: "-" denotes reserved. Registers with names typed in ***bold italic*** format are RTL8029AS defined registers and are not supported in a standard NE2000 adapter.

Page 0 (PS1=0, PS0=0)

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	CR	R/W	PS1	PS0	RD2	RD1	RD0	TXP	STA	STP
01H	CLDA0	R	A7	A6	A5	A4	A3	A2	A1	A0
	PSTART	W	A15	A14	A13	A12	A11	A10	A9	A8
02H	CLDA1	R	A15	A14	A13	A12	A11	A10	A9	A8
	PSTOP	W	A15	A14	A13	A12	A11	A10	A9	A8
03H	BNRY	R/W	A15	A14	A13	A12	A11	A10	A9	A8
04H	TSR	R	OWC	CDH	0	CRS	ABT	COL	-	PTX
	TPSR	W	A15	A14	A13	A12	A11	A10	A9	A8
05H	NCR	R	0	0	0	0	NC3	NC2	NC1	NC0
	TBCR0	W	TBC7	TBC6	TBC5	TBC4	TBC3	TBC2	TBC1	TBC0
06H	FIFO	R	D7	D6	D5	D4	D3	D2	D1	D0
	TBCR1	W	TBC15	TBC14	TBC13	TBC12	TBC11	TBC10	TBC9	TBC8
07H	ISR	R/W	RST	RDC	CNT	OVW	TXE	RXE	PTX	PRX
08H	CRDA0	R	A7	A6	A5	A4	A3	A2	A1	A0
	RSAR0	W	A7	A6	A5	A4	A3	A2	A1	A0
09H	CRDA1	R	A15	A14	A13	A12	A11	A10	A9	A8
	RSAR1	W	A15	A14	A13	A12	A11	A10	A9	A8
0AH	8029ID0	R	0	1	0	1	0	0	0	0
	RBCR0	W	RBC7	RBC6	RBC5	RBC4	RBC3	RBC2	RBC1	RBC0
0BH	8029ID1	R	0	1	0	0	0	0	1	1
	RBCR1	W	RBC15	RBC14	RBC13	RBC12	RBC11	RBC10	RBC9	RBC8
0CH	RSR	R	DFR	DIS	PHY	MPA	0	FAE	CRC	PRX
	RCR	W	-	-	MON	PRO	AM	AB	AR	SEP
0DH	CNTR0	R	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
	TCR	W	-	-	-	OFST	ATD	LB1	LB0	CRC
0EH	CNTR1	R	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
	DCR	W	-	FT1	FT0	ARM	LS	LAS	BOS	WTS
0FH	CNTR2	R	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
	IMR	W	-	RDCE	CNTE	OVWE	TXEE	RXEE	PTXE	PRXE

Page 1 (PS1=0, PS0=1)

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	CR	R/W	PS1	PS0	RD2	RD1	RD0	TXP	STA	STP
01H	PAR0	R/W	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
02H	PAR1	R/W	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
03H	PAR2	R/W	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
04H	PAR3	R/W	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
05H	PAR4	R/W	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
06H	PAR5	R/W	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40
07H	CURR	R/W	A15	A14	A13	A12	A11	A10	A9	A8
08H	MAR0	R/W	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
09H	MAR1	R/W	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
0AH	MAR2	R/W	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
0BH	MAR3	R/W	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
0CH	MAR4	R/W	FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32
0DH	MAR5	R/W	FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40
0EH	MAR6	R/W	FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48
0FH	MAR7	R/W	FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56

Page 2(PS1=1, PS0=0)

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	CR	R/W	PS1	PS0	RD2	RD1	RD0	TXP	STA	STP
01H	PSTART	R	A15	A14	A13	A12	A11	A10	A9	A8
02H	PSTOP	R	A15	A14	A13	A12	A11	A10	A9	A8
03H	-									
04H	TPSR	R	A15	A14	A13	A12	A11	A10	A9	A8
05H | 0BH	-									
0CH	RCR	R	-	-	MON	PRO	AM	AB	AR	SEP
0DH	TCR	R	-	-	-	OFST	ATD	LB1	LB0	CRC
0EH	DCR	R	-	FT1	FT0	ARM	LS	LAS	BOS	WTS
0FH	IMR	R	-	RDCE	CNTE	OVWE	TXEE	RXEE	PTXE	PRXE

Page 3(PS1=1, PS0=1)

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	CR	R/W	PS1	PS0	RD2	RD1	RD0	TXP	STA	STP
01H	9346CR	R	EEM1	EEM0	-	-	EECS	EESK	EEDI	EEDO
		W	EEM1	EEM0	-	-	EECS	EESK	EEDI	-
02H	-									
03H	CONFIG0	R	-	-	-	-	-	BNC	0	0
04H	-									
05H	CONFIG2	R	PL1	PL0	***FCE**	***PF**	-	-	BS1	BS0
		W*	PL1	PL0	***FCE**	-	-	-	-	-
06H	CONFIG3	R	-	FUDUP	LEDS1	LEDS0	-	SLEEP	PWRDN	-
		W*	-	***FUDUP**	-	-	-	SLEEP	PWRDN	-
07H	TEST1	-	Reserved							
08H	-	-	Unused							
09H	HLTCLK	W	HLT7	HLT6	HLT5	HLT4	HLT3	HLT2	HLT1	HLT0
0AH	TEST2	-	Reserved							
0B-0DH	-	-	Unused							
***0EH**	**8029ASID0**	**R**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**
***0FH**	**8029ASID1**	**R**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Notes: The registers marked with type='W*' can be written only if bits EEM1=EEM0=1.

Notes: "*" denotes the bits or registers which are RTL8029AS defined bits or registers and are not supported in RTL8029.

5.1.2. Register Functions

5.1.2.1. NE2000 Compatible Registers

CR: Command Register (00H; Type=R/W)

This register is used to select register pages, enable or disable remote DMA operation and issue commands.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7, 6</td><td>PS1, PS0</td><td>
<table>
<tr><th>PS1</th><th>PS0</th><th>Register Page</th><th>Remark</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>NE2000 compatible</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>NE2000 compatible</td></tr>
<tr><td>1</td><td>0</td><td>2</td><td>NE2000 compatible</td></tr>
<tr><td>1</td><td>1</td><td>3</td><td>RTL8029AS Configuration</td></tr>
</table>
</td></tr>
<tr><td>5-3</td><td>RD2-0</td><td>
<table>
<tr><th>RD2</th><th>RD1</th><th>RD0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Not allowed</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Remote Read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Remote Write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Send Packet</td></tr>
<tr><td>1</td><td>*</td><td>*</td><td>Abort/Complete remote DMA</td></tr>
</table>
</td></tr>
<tr><td>2</td><td>TXP</td><td>This bit must be set to transmit a packet. It is internally reset either after the transmission is completed or aborted. Writing a 0 has no effect.</td></tr>
<tr><td>1</td><td>STA</td><td>The STA bit controls nothing. It only reflects the value written to this bit. POWER UP=0.</td></tr>
<tr><td>0</td><td>STP</td><td>This bit is the STOP command. When it is set, no packets will be received or transmitted. POWER UP=1.
<table>
<tr><th>STA</th><th>STP</th><th>Function</th></tr>
<tr><td>1</td><td>0</td><td>Start Command</td></tr>
<tr><td>0</td><td>1</td><td>Stop Command</td></tr>
</table>
</td></tr>
</table>

ISR: Interrupt Status Register (07H; Type=R/W in Page0)

This register reflects the NIC status. The host reads it to determine the cause of an interrupt. Individual bits are cleared by writing a "1" into the corresponding bit. It must be cleared after power up.

Bit	Symbol	Description
7	RST	This bit is set when NIC enters reset state and is cleared when a start command is issued to the CR. It is also set when receive buffer overflows and is cleared when one or more packets have been read from the buffer.
6	RDC	Set when remote DMA operation has been completed.
5	CNT	Set when MSB of one or more of the network tally counters has been set.
4	OVW	This bit is set when the receive buffer has been exhausted.
3	TXE	Transmit error bit is set when a packet transmission is aborted due to excessive collisions.
2	RXE	This bit is set when a packet received with one or more of the following errors: - CRC error - Frame alignment error - Missed packet
1	PTX	This bit indicates packet transmitted with no errors.
0	PRX	This bit indicates packet received with no errors.

IMR: Interrupt Mask Register (0FH; Type=W in Page0, Type=R in Page2)

All bits correspond to the bits in the ISR register. POWER UP=all 0s. Setting individual bits will enable the corresponding interrupts.

DCR: Data Configuration Register (0EH; Type=W in Page0, Type=R in Page2)

Bit	Symbol	Description
7	-	Always 1
6, 5	FT1, FT0	FIFO threshold select bit 1 and 0.
4	ARM	Auto-initialize Remote 0: Send Packet Command not executed. 1: Send Packet Command executed.
3	LS	Loopback Select 0: Loopback mode selected. Bits 1 and 2 of the TCR must also be programmed for Loopback operation. 1: Normal Operation
2	LAS	This bit must be set to zero. NIC only supports dual 16-bit DMA mode. POWER UP =1
1	BOS	Byte Order Select 0: MS byte placed on MD15-8 and LS byte on MD7-0. (32xxx,80x86) 1: MS byte placed on MD7-0 and LS byte on MD15-8. (680x0)
0	WTS	Word Transfer Select 0: byte-wide DMA transfer 1: word-wide DMA transfer

TCR: Transmit Configuration Register (0DH; Type=W in Page0, Type=R in Page2)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7-5</td><td>-</td><td>Always 1.</td></tr>
<tr><td>4</td><td>OFST</td><td>Collision Offset Enable.</td></tr>
<tr><td>3</td><td>ATD</td><td>Auto Transmit Disable.
0: normal operation
1: reception of multicast address hashing to bit 62 disables transmitter, reception of multicast address hashing to bit 63 enables transmitter.</td></tr>
<tr><td>2, 1</td><td>LB1, LB0</td><td>
<table>
<tr><th>LB1</th><th>LB0</th><th>Mode</th><th>Remark</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Normal Operation</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Internal Loopback</td></tr>
<tr><td>1</td><td>0</td><td>2</td><td>External Loopback</td></tr>
<tr><td>1</td><td>1</td><td>3</td><td>External Loopback</td></tr>
</table>
</td></tr>
<tr><td>0</td><td>CRC</td><td>The NIC CRC logic comprises a CRC generator for transmitter and a CRC checker for receiver. This bit controls the activity of the CRC logic. If this bit set, CRC is inhibited by transmitter. Otherwise CRC is appended by transmitter.
<table>
<tr><th colspan="2">Conditions</th><th colspan="2">CRC Logic Activities</th></tr>
<tr><th>CRC Bit</th><th>Mode</th><th>CRC Generator</th><th>CRC Checker</th></tr>
<tr><td>0</td><td>normal</td><td>enabled</td><td>enabled</td></tr>
<tr><td>1</td><td>normal</td><td>disabled</td><td>enabled</td></tr>
<tr><td>0</td><td>loopback</td><td>enabled</td><td>disabled</td></tr>
<tr><td>1</td><td>loopback</td><td>disabled</td><td>enabled</td></tr>
</table>
</td></tr>
</table>

TSR: Transmit Status Register (04H; Type=R in Page0)

This register indicates the status of a packet transmission.

Bit	Symbol	Description
7	OWC	Out of Window Collision. It is set when a collision is detected after a slot time (51.2us). Transmissions are rescheduled as in normal collisions.
6	CDH	CD Heartbeat. The NIC watches for a collision signal (i.e., CD Heartbeat signal) during the first 6.4us of the interframe gap following a transmission. This bit is set if the transceiver fails to send this signal.
5	-	Always 0.
4	CRS	Carrier Sense lost bit is set when the carrier is lost during transmitting a packet.
3	ABT	It indicates the NIC aborted the transmission because of excessive collisions.
2	COL	It indicates the transmission collided with some other station on the network.
1	-	Always 1.
0	PTX	This bit indicates the transmission completes with no errors.

RCR: Receive Configuration Register (0CH; Type=W in Page0, Type=R in Page2)

Bit	Symbol	Description
7, 6	-	Always 1.
5	MON	When monitor mode bit is set, received packets are checked for address match, good CRC and frame alignment but not buffered to memory. Otherwise, packets will be buffered to memory.
4	PRO	If PRO=1, all packets with physical destination address accepted. If PRO=0, physical destination address must match the node address programmed in PAR0-5.
3	AM	If AM=1, packets with multicast destination address are accepted. If AM=0, packets with multicast destination address are rejected.
2	AB	If AB=1, packets with broadcast destination address are accepted. If AB=0, packets with broadcast destination address are rejected.
1	AR	If AR=1, packets with length fewer than 64 bytes are accepted. If AR=0, packets with length fewer than 64 bytes are rejected.
0	SEP	If SEP=1, packets with receive errors are accepted. If SEP=0, packets with receive errors are rejected.

RSR: Receive Status Register (0CH; Type=R in Page0)

Bit	Symbol	Description
7	DFR	Deferring. Set when a carrier or a collision is detected.
6	DIS	Receiver Disabled. When the NIC enters the monitor mode, this bit is set and receiver is disabled. Reset when receiver is enabled after leaving the monitor mode.
5	PHY	PHY bit is set when the received packet has a multicast or broadcast destination address. It is reset when the received packet has a physical destination address.
4	MPA	Missed Packet bit is set when the incoming packet can not be accepted by NIC because of a lack of receive buffer or if NIC is in monitor mode. Increment CNTR2 tally counter.
3	-	Always 0.
2	FAE	Frame Alignment Error bit reflects the incoming packet didn't end on a byte boundary and CRC did not match at last byte boundary. Increment CNTR0 tally counter.

1	CRC	CRC error bit reflects packet received with CRC error. This bit will also be set for FAE errors. Increment CNTR1 tally counter.
0	PRX	This bit indicates packet received with no errors.

CLDA0,1: Current Local DMA Registers (01H & 02H; Type=R in Page0)

These two registers can be read to get the current local DMA address.

PSTART: Page Start Register (01H; Type=W in Page0, Type=R in Page 2)

The Page Start register sets the start page address of the receive buffer ring.

PSTOP: Page Stop Register (02H; Type=W in Page0, Type=R in Page2)

The Page Stop register sets the stop page address of the receive buffer ring.

BNRY: Boundary Register (03H; Type=R/W in Page0)

This register is used to prevent overwrite of the receive buffer ring. It is typically used as a pointer indicating the last receive buffer page the host has read.

TPSR: Transmit Page Start Register (04H; Type=W in Page0)

This register sets the start page address of the packet to the transmitted.

TBCR0,1: Transmit Byte Count Registers (05H & 06H; Type=W in Page0)

These two registers set the byte counts of the packet to be transmitted.

NCR: Number of Collisions Register (05H; Type=R in Page0)

The register records the number of collisions a node experiences during a packet transmission.

FIFO: First In First Out Register (06H; Type=R in Page0)

This register allows the host to examine the contents of the FIFO after loopback.

CRDA0,1: Current Remote DMA Address registers (08H & 09H; Type=R in Page0)

These two registers contain the current address of remote DMA.

RSAR0,1: Remote Start Address Registers (08H & 09H; Type=W in Page0)

These two registers set the start address of remote DMA.

RBCR0,1: Remote Byte Count Registers (0AH & 0BH; Type=W in Page0)

These two registers set the data byte counts of remote DMA.

CNTR0: Frame Alignment Error Tally Counter Register (0DH; Type=R in Page0)

CNTR1: CRC Error Tally Counter Register (0EH; Type=R in Page0)

CNTR2: Missed Packet Tally Counter Register (0FH; Type=R in Page0)

PAR0-5: Physical Address Registers (01H - 06H; Type=R/W in Page1)

These registers contain my Ethernet node address and are used to compare the destination address of incoming packets for acceptation or rejection.

CURR: Current Page Register (07H; Type=R/W in Page1)

This register points to the page address of the first receive buffer page to be used for a packet reception.

MAR0-7: Multicast Address Register (08H - 0FH; Type=R/W in Page1)

These registers provide filtering bits of multicast addresses hashed by the CRC logic.

5.1.2.2. RTL8029AS Defined Registers

Page 0 (PS1=0, PS0=0)

Two registers are defined to contain the RTL8029AS chip ID and Read Sequence Command is NO LONGER supported in RTL8029AS.

No.	Name	Type	Bit7-0
0AH	8029ID0	R	50H (ASCII code of "P")
0BH	8029ID1	R	43H (ASCII code of "C")

Page 3(PS1=1, PS0=1)

Page3 Power Up Values before loading 9346 contents

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	CR	R/W	0	0	1	0	0	0	0	1
01H	9346CR	R/W	0	0	-	-	*	*	*	*
02H	-									
03H	CONFIG0	R	-	-	-	-	-	*	0	0
04H	-									
05H	CONFIG2	R/W*	*	*	**0**	**0**	-	-	*	*
06H	CONFIG3	R/W*	-	*	*	*	-	0	0	-
07H	-									
08H	-									
09H	HLTCLK	W	1	1	1	1	1	1	1	1
0AH	-									
0BH	-									
0CH	-									
0DH	-									
0EH	**8029ASID0**	**R**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**
0FH	**8029ASID1**	**R**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Page3 Content Descriptions

9346CR: 9346 Command Register (01H; Type=R/W except Bit0=R)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>7-6</td><td>EEM1-0</td><td>These 2 bits select the RTL8029AS operating mode.
<table>
<tr><th>EEM1</th><th>EEM0</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal (DP8390 compatible)</td></tr>
<tr><td>0</td><td>1</td><td>Auto-load:
Entering this mode will make the RTL8029AS load the contents of 9346 like when the RSTB signal is asserted.
This auto-load operation will take about 2ms. After it is completed, the RTL8029AS goes back to the normal mode automatically (EEM1=EEM0 =0) and the CR register is reset to 21H.</td></tr>
<tr><td>1</td><td>0</td><td>9346 programming:
In this mode, both the local & remote DMA operations of 8390 are disabled. The 9346 can be directly accessed via bit3-0 which now reflect the states of EECS, EESK, EEDI, & EEDO pins respectively.</td></tr>
<tr><td>1</td><td>1</td><td>Config register write enable:
Before writing to the Page3 CONFIG2,3 registers, the RTL8029AS must be placed in this mode. This will prevent RTL8029AS's configurations from accidental change.</td></tr>
</table></td></tr>
<tr><td>5-4</td><td>-</td><td>Not used.</td></tr>
<tr><td>3</td><td>EECS</td><td rowspan="4">These bits reflect the state of EECS, EESK, EEDI & EEDO pins in auto-load or 9346 programming mode.</td></tr>
<tr><td>2</td><td>EESK</td></tr>
<tr><td>1</td><td>EEDI</td></tr>
<tr><td>0</td><td>EEDO</td></tr>
</table>

CONFIG0: RTL8029AS Configuration Register 0 (03H; Type=R)

Bit	Symbol	Description
7-3	-	Not used
2	BNC	When set, this bit indicates that the RTL8029AS is using the 10Base2 thin cable as its networking medium. This bit will be set in the following 2 cases: (1) PL1=PL0=0 (auto-detect) and link test fails (2) PL1=PL0=1 (10 Base 2)
1-0	-	Always 0s.

CONFIG1: Reserved

CONFIG2: RTL8029AS Configuration Register 2 (05H; Type=R except Bit[7:5]=R/W)

Bit	Symbol	Description
7-6	PL1-0	Select network medium types.

		<table><tr><th>PL1</th><th>PL0</th><th>Medium Type</th></tr><tr><td>0</td><td>0</td><td>TP/CX auto-detect (10BaseT link test is enabled)</td></tr><tr><td>0</td><td>1</td><td>10BaseT with link test disabled</td></tr><tr><td>1</td><td>0</td><td>10Base5</td></tr><tr><td>1</td><td>1</td><td>10Base2</td></tr></table>
5	**FCE**	**Flow Control Enable: The flow control is enabled in full-duplex mode only.**
4	**PF**	**Pause Flag: Set when RTL8029AS is in backoff state because a pause packet is received.**
3-2	-	Not used
1-0	BS1-0	Select Boot ROM size <table><tr><th>BS1</th><th>BS0</th><th>BROM size</th></tr><tr><td>0</td><td>0</td><td>No Boot ROM</td></tr><tr><td>0</td><td>1</td><td>8K Boot ROM</td></tr><tr><td>1</td><td>0</td><td>16K Boot ROM</td></tr><tr><td>1</td><td>1</td><td>32K Boot ROM</td></tr></table>

CONFIG3: RTL8029AS Configuration Register 3 (06H; Type=R except Bit[6,2:1]=R/W)

Bit	Symbol	Description
7	-	Unused
6	FUDUP	When this bit is set, RTL8029AS is set to the full-duplex mode which enables simultaneously transmission and reception on the twisted-pair link to a full-duplex Ethernet switching hub. This feature not only increases the channel bandwidth from 10 to 20 Mbps but also avoids the performance degrading problem due to the channel contention characteristics of the Ethernet CSMA/CD protocol.
5-4	LEDS1-0	These two bits select the outputs to LED2-0 pins. <table><tr><th>LEDS0</th><th>LED0 Pin</th></tr><tr><td>0</td><td>LED_COL</td></tr><tr><td>1</td><td>LED_LINK</td></tr></table> <table><tr><th>LEDS1</th><th>LED1 Pin</th><th>LED2 Pin</th></tr><tr><td>0</td><td>LED_RX</td><td>LED_TX</td></tr><tr><td>1</td><td>LED_CRS</td><td>MCSB</td></tr></table> Please refer to section 6.4 for the behavior of LEDs. The MCSB signal is defined to put the local buffer SRAM into standby mode while DMA is not in progress and thus saves powers.
3	-	Reserved. **Must not** write a 1 to this bit.
2	SLEEP	This bit, when set, puts RTL8029AS into sleep mode. In sleep mode, all LED signals (P.S. MCSB is not an LED signal) except LED_BNC are forced high to turn off the LEDs. The RTL8029AS still handles the network transmission and reception like in normal mode. The LED_BNC is not affected by this bit. This bit's power-up initial value is 0 and can be modified by software when EEM1=EEM0=1.

1	PWRDN	This bit, when set, puts RTL8029AS into power down mode. RTL8029AS supports two kinds of power down modes, which is selected by the contents of the HLTCLK register: (1) mode 1: power down with clock running (2) mode 2: power down with clock halted In both power down modes, the RTL8029AS's serial network interface and transceiver are turned off. All network activities are ignored. All LED signals except LED_BNC are forced high. The LED_BNC is forced low to disable the DC converter for coaxial transceiver. In power down mode 2, the RTL8029AS stops its internal clock for minimal power consumption. Registers except HLTCLK are typically not accessible in this mode. This bit's initial value comes from 9346 and can be modified if EEM1=EEM0=1 in 9346CR register.
0	-	Unused

HLTCLK: Halt Clock Register (09H; Type=W)

This is the only active one of Group1 registers when RTL8029AS is inactivated. Writing to this register is invalid if RTL8029AS is not in power down mode. (i.e., If PWRDN bit in CONFIG3 register is zero.) The data written to this register determines the RTL8029AS's power down mode.

Data	Power Down Mode
52H (ASCII code of 'R')	Mode 1 - clock **R**unning
48H (ASCII code of 'H')	Mode 2 - clock **H**alted
Other values	Ignored

8029ASID0,1: RTL8029AS ID = 8029H (0E,0FH; Type=R)

5.2. Group 2: PCI Configuration Space Registers

5.2.1. PCI Configuration Space Table

No.	Name	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	VID	R	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
01H		R	VID15	VID14	VID13	VID12	VID11	VID10	VID9	VID8
02H	DID	R	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
03H		R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
04H	Command	R	0	0	0	0	0	0	MEMEN	IOEN
		W	-	-	-	-	-	-	MEMEN	IOEN
05H		R	0	0	0	0	0	0	0	0
		W	-	-	-	-	-	-	-	-
06H	Status	R	0	0	0	0	0	0	0	0
07H		R	0	0	0	0	0	DST1	DST0	0
08H	RID	R	0	0	0	0	0	0	0	0
09H	PIFR	R	0	0	0	0	0	0	0	0
0AH	SCR	R	0	0	0	0	0	0	0	0
0BH	BCR	R	0	0	0	0	0	0	1	0
0CH	-		Reserved							

0DH	LTR	R	0	0	0	0	0	0	0	0
0EH	HTR	R	0	0	0	0	0	0	0	0
0FH	-		Reserved							
10H	BAR	R	BAR7	BAR6	BAR5	0	0	0	0	IOIN
		W	BAR7	BAR6	BAR5	-	-	-	-	-
11H		R/W	BAR15	BAR14	BAR13	BAR12	BAR11	BAR10	BAR9	BAR8
12H		R/W	BAR23	BAR22	BAR21	BAR20	BAR19	BAR18	BAR17	BAR16
13H		R/W	BAR31	BAR30	BAR29	BAR28	BAR27	BAR26	BAR25	BAR24
14H | 2BH	-		Reserved							
2CH	**SVID**	**R**	**SVID7**	**SVID6**	**SVID5**	**SVID4**	**SVID3**	**SVID2**	**SVID1**	**SVID0**
2DH		**R**	**SVID15**	**SVID14**	**SVID13**	**SVID12**	**SVID11**	**SVID10**	**SVID9**	**SVID8**
2EH	**SID**	**R**	**SID7**	**SID6**	**SID5**	**SID4**	**SID3**	**SID2**	**SID1**	**SID0**
2FH		**R**	**SID15**	**SID14**	**SID13**	**SID12**	**SID11**	**SID10**	**SID9**	**SID8**
30H	BROMBAR	R	0	0	0	0	0	0	0	BROMEN
		W	-	-	-	-	-	-	-	BROMEN
31H		R	BMR15	BMR14	BMR13	BMR12	BMR11	0	0	0
		W	BMR15	BMR14	BMR13	BMR12	BMR11	-	-	-
32H		R/W	BMR23	BMR22	BMR21	BMR20	BMR19	BMR18	BMR17	BMR16
33H		R/W	BMR31	BMR30	BMR29	BMR28	BMR27	BMR26	BMR25	BMR24
34H | 3BH	-		Reserved							
3CH	ILR	R	-	-	-	-	ILR3	ILR2	ILR1	ILR0
		W	-	-	-	-	ILR3	ILR2	ILR1	ILR0
3DH	IPR	R	0	0	0	0	0	0	0	1
3EH | FFH	-		Reserved							

5.2.2. PCI Configuration Space functions

The PCI configuration space is intended for configuration, initialization, and catastrophic error handling functions. The functions of RTL8029AS's configuration space are described below.

VID: Vendor ID Register (01-00H; Type=R)

The Vendor ID register is a 16-bit register that identifies the manufacturer of the RTL8029AS controller. Realtek Vendor ID = 10ECH(default value)

DID: Device ID Register (03-02H; Type=R)

The Device ID register is a 16-bit register that shows the device ID of the RTL8029AS controller. RTL8029AS Device ID = 8029H(default value)

Command: Command Register (05-04H; Type=R except Bit1, 0=R/W)

The Command register is a 16-bit register used to provide coarse control over a device's ability to generate and respond to PCI cycles.

Bit	Symbol	Description
15-10	-	Reserved area. Read as 0, write operation has no effect.
9	FBTBEN	Fast Back-To-Back ENable. Read as 0, write operation has no effect. The RTL8029AS will not generate Fast Back-to-Back cycles.
8	SERREN	SERR ENable. Read as 0, write operation has no effect.
7	ADSTEP	Address/Data STEPping. Read as 0, write operation has no effect. The RTL8029AS never do address/data stepping.
6	PERREN	This bit controls the device's response to parity errors. When the value of this bit is 0, the device must ignore any parity errors that it detects and continues normal operation. Read as 0, write operation has no effect.
5	VGASNOOP	VGA palette SNOOP. Read as 0, write operation has no effect.
4	MWIEN	Memory Write and Invalidate cycle ENable. Read as 0, write operation has no effect.
3	SCYCEN	Special CYCle ENable. Read as 0, write operation has no effect. The RTL8029AS ignores all special cycle operation.
2	BMEN	Bus Master ENable. Read as 0, write operation has no effect.
1	MEMEN	Controls a device's response to memory space accesses. 0 : Disable the device response 1 : Enable the device response
0	IOEN	Controls a device's response to I/O space accesses. 0 : Disable the device response 1 : Enable the device response

Status: Status Register (07-06H; Type=R)

The Status register is a 16-bit register used to record status information for PCI bus related events. Reads to this register behave normally. Writes are slightly different in that bits can be reset, but not set.

Bit	Symbol	Description
15	DPE	Detected Parity Error. Read as 0, write operation has no effect.
14	SSE	Signaled System Error. Read as 0, write operation has no effect.
13	RMA	Received Master Abort. Read as 0, write operation has no effect.
12	RTA	Received Target Abort. Read as 0, write operation has no effect.
11	STA	Signaled Target Abort. Read as 0, write operation has no effect.
10-9	DST1-0	These bits encode the timing of DEVSELB. They are set to 01b (medium), indicating the RTL8029AS controller will assert DEVSELB two clocks after FRAMEB is asserted.
8	DPD	Data Parity Detected. Read as 0, write operation has no effect.
7	FBBC	Fast Back-to-Back Capable. Read as 0, write operation has no effect.
6-0	-	Reserved area. Read as 0, write operation has no effect.

RID: Revision ID Register (08H; Type=R)

The Revision ID register is an 8-bit register that specifies the RTL8029AS controller revision number. Revision ID = 00H

PIFR: Programming InterFace Register (09H; Type=R)

The Programming interface register is an 8-bit register that identifies the programming interface of RTL8029AS controller. PCI doesn't define any other specific register level programming interface for network devices. So PIFR = 00H.

SCR: Sub-Class Register (0AH; Type=R)

The Sub-class register is an 8-bit register that identifies specially the function of the RTL8029AS controller. SCR = 00H indicates that the RTL8029AS controller is an Ethernet controller.

BCR: Base-Class Register (0BH; Type=R)

The Base-class register is an 8-bit register that broadly classifies the function of the RTL8029AS controller. BCR = 02H indicates that the RTL8029AS controller is a network controller.

HTR: Header Type Register (0EH; Type=R)

The header type register is an 8-bit register that describes the layout of bytes 10H through 3FH in configuration space and also whether or not the device contains multiple functions. HTR = 00H

Bit	Symbol	Description
7	FUNC	single/multi FUNCtion. Read as 0, write operation has no effect. 0 : single function device 1: multiple functions device The RTL8029AS controller is a single function device
6-0	LAYOUT	PCI configuration space layout. These bits specify the layout of bytes 10H through 3FH. One encoding, 00H is defined and specifies the layout show in section 5.2.1. Read as 0, write operation has no effect.

LTR: Latency Timer Register (0DH; Type=R)

This register is an 8-bit register. LTR = 00H indicates when the RTL8029AS controller is preempted, it will release the bus immediately after finishing the current data transfer.

BAR: Base Address Register (13-10H; Type=R/W except Bit4-0=R)

The Base Address register is a 32-bit register that determines the I/O space mapping of the RTL8029AS controller.

Bit	Symbol	Description
31-5	BAR31-5	These bits are used to set I/O base address for I/O operation.
4-2	IOSIZE	These bits indicate how many I/O spaces to be used. Read as 0, write operation has no effect.
1	-	Reserved area. Read as 0, write operation has no effect.
0	IOIN	I/O space INdicator. Read as 1, write operation has no effect. Indicating that the base address is an I/O base address.

SVID: Subsystem Vendor ID Register (2C-2DH; Type=R)

The Subsystem Vendor ID register is a 16-bit register that uniquely identifies the add-in board or subsystem where the PCI device resides. The default value is **10EC**H.

SID: Subsystem ID Register (2E-2FH; Type=R)

The Subsystem ID register is a 16-bit register that are vendor specific. The default value is **8029**H.

BROMBAR: Boot ROM Base Address Register (33-30H; Type=R/W except Bit12-1=R)

The Base Boot ROM Address register is a 32-bit register that determines the Boot ROM space mapping of the RTL8029AS controller.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th></tr>
<tr><td>31-15</td><td>BMR31-15</td><td>These bits are used to set Boot ROM base address for Boot ROM access.</td></tr>
<tr><td>14-11</td><td>BROMSIZE</td><td>These bits indicate how many Boot ROM spaces to be supported.
<table>
<tr><th>BS1</th><th>BS0</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>No BROM : BROMEN=0(R)
BMR11,12=0,0(R)</td></tr>
<tr><td>0</td><td>1</td><td>8K BROM : BROMEN=0(R/W)
BMR11,12=0,0(R)
BMR13=0(R/W)
BMR14=0(R/W)</td></tr>
<tr><td>1</td><td>0</td><td>16K BROM : BROMEN=0(R/W)
BMR11,12=0,0(R)
BMR13=0(R)
BMR14=0(R/W)</td></tr>
<tr><td>1</td><td>1</td><td>32K BROM : BROMEN=0(R/W)
BMR11,12=0,0(R)
BMR13=0(R)
BMR14=0(R)</td></tr>
</table></td></tr>
<tr><td>10-1</td><td>-</td><td>Reserved area. Read as 0, write operation has no effect.</td></tr>
<tr><td>0</td><td>BROMEN</td><td>BROM ENable bit.
0 : disable
1 : enable</td></tr>
</table>

ILR: Interrupt Line Register (3CH; Type=R/W)

The Interrupt Line register is an 8-bit register used to communicate with the routing of the interrupt. It is written by the POST software to set interrupt line for the RTL8029AS controller. ILR = 00-0FH

IPR: Interrupt Pin Register (3DH; Type=R)

The Interrupt Pin register is an 8-bit register indicating the interrupt pin used by the RTL8029AS controller. The RTL8029AS controller uses the INTA interrupt pin. IPR = 01H

6. FUNCTION DESCRIPTION

6.1. RTL8029AS Configuration Process

The RTL8029AS controller supports PCI configuration operation. In PCI system, the initial process is completed by the system BIOS software. The system BIOS has to find where the system resources are available, such as I/O base address, BROM memory base address, and interrupt request line, and assigns the resources to the required devices. At the same time the RTL8029AS controller performs a series of EEPROM read operation after power-up to set Ethernet ID, media type, operation mode¡K, etc. The RTL8029AS's resource configuration information is stored in the PCI configuration space as well as CONFIG registers in Group1 Page3. The CONFIG registers power-up default values always come from the contents of 9346 and the values can be modified by software. The update configuration is only valid temporarily and will be lost after an auto-load command, an active RSTB, or PC power off. Permanent changes of configuration must be done by changing the contents of 9346. Note that the BROM size can not be modified temporarily.

6.2. 9346 Contents

The 9346 is a 1K-bit EEPROM. Although it is actually addressed by words, we list its contents by bytes below for convenience.

Bytes		Contents	Comments
00H - 01H	**(2 bytes)**		**Power-up initial value of Page3**
	00H	CONFIG2	Board Configurations
	01H	CONFIG3	
02H - 0FH	**(14 bytes)**		**NE2000 ID PROM**
	02H - 07H	Ethernet ID 0-5	Ethernet node address
	08H - 0FH	Product ID 0-7	Assigned by card makers; negligible
10H - 17H	**(8 bytes)**		**Flow Control**
	10H - 11H	Pause Type 0-1	
	12H - 17H	Pause Multicast ID0-5	
18H-75H		**Unused**	
76H-77H	**(2 bytes)**	**8029ASID**	**The value is 8029H which is programmed by PG8029.**
78H-7FH	**(8 bytes)**	**PCI ID**	**PCI VID, DID, SVID and SID**
	78H-79H	VID0-1	
	7AH-7BH	DID0-1	
	7CH-7DH	SVID0-1	
	7EH-7FH	SID0-1	

6.2.1 Detail values of 9346 CONFIG2-3 & 8029ASID0-1 bytes

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONFIG2	PL1	PL0	**FCE**	*	*	*	BS1	BS0
CONFIG3	*	FUDUP	LEDS1	LEDS0	*	*	PWRDN	*
8029ASID0	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**
8029ASID1	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

P.S. '*' denotes don't care.

Note: RTL8029AS checks the 8029ASID word in 9346 when power up. If the value matches "8029h", the RTL8029AS works in RTL8029AS mode. You can use all new features defined by RTL8029AS, such as Flow Control, Programmable Vendor ID … etc. If the value doesn't match, the RTL8029AS works like RTL8029. All enhanced functions and registers are not available. Also the PCI IDs in 9346 are ignored and the RTL8029's ID(10ECh, 8029h) will be used instead.

6.2.2 ID PROM Contents

The RTL8029AS emulates the ID PROM of NE2000 internally. After 9346 is loaded, the contents of ID PROM are as follows.

offset	Bit7-0
00H	Ethernet ID0
01H	Ethernet ID1
02H	Ethernet ID2
03H	Ethernet ID3
04H	Ethernet ID4
05H	Ethernet ID5
06H	PID0
07H	PID1
08H	PID2
09H	PID3
0AH	PID4
0BH	PID5
0CH	PID6
0DH	PID7
0EH	57 (ASCII Code of "W")
0FH	57 (ASCII Code of "W")
10H	Ethernet ID0
11H	Ethernet ID1
12H	Ethernet ID2
13H	Ethernet ID3
14H	Ethernet ID4
15H	Ethernet ID5
16H	PID0
17H	PID1
18H	PID2
19H	PID3
1AH	PID4
1BH	PID5
1CH	PID6
1DH	PID7
1EH	42 (ASCII Code of "B")
1FH	42 (ASCII Code of "B")

6.3. Local Memory Bus Control

The local memory bus of RTL8029AS is shared by the BROM & 9346 EEPROM.The following diagram demonstrates their connection relationship.

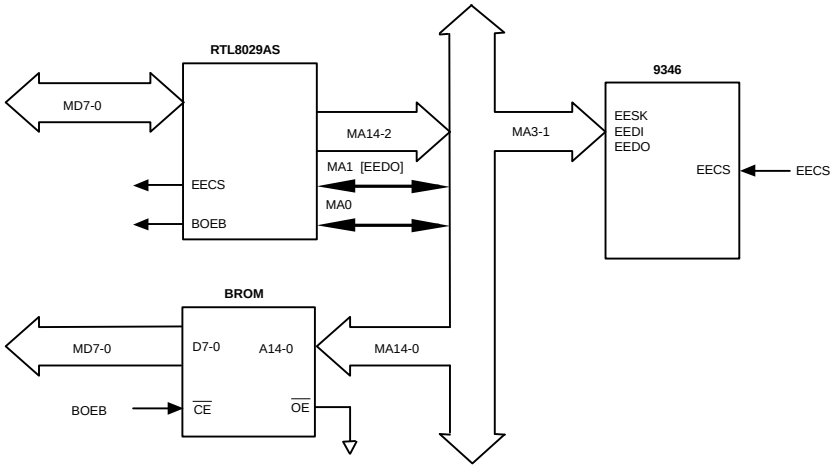


Figure 1. Local Memory Bus Block Diagram

6.4. Flow Control

The RTL8029AS supports IEEE802.3X flow control to improve performance in full-duplex mode. It detects PAUSE packet to achieve flow control task.

6.4.1. Control Frame Transmission

When RTL8029AS detects its free receive buffer less than 3K bytes, it sends a **PAUSE packet with pause_time(=FFFFh)** to inform the source station to stop transmission for the specified period of time. After the driver has processed the packets in the receive buffer and updated the boundary pointer, the RTL8029AS sends the other **PAUSE packet with pause_time(=0000h)** to wake up the source station to restart transmission.

6.4.2. Control Frame Reception

RTL8029AS enters backoff state for the specified period of time when it receives a valid **PAUSE packet with pause_time(=n)**. If the PAUSE packet is received while RTL8029AS is transmitting, RTL8029AS starts to backoff after current transmission completes. RTL8029AS frees to transmit next packets again when it receives a valid **PAUSE packet with pause_time(=0000h)** or the **backoff timer(=n*51.2us)** elapses.

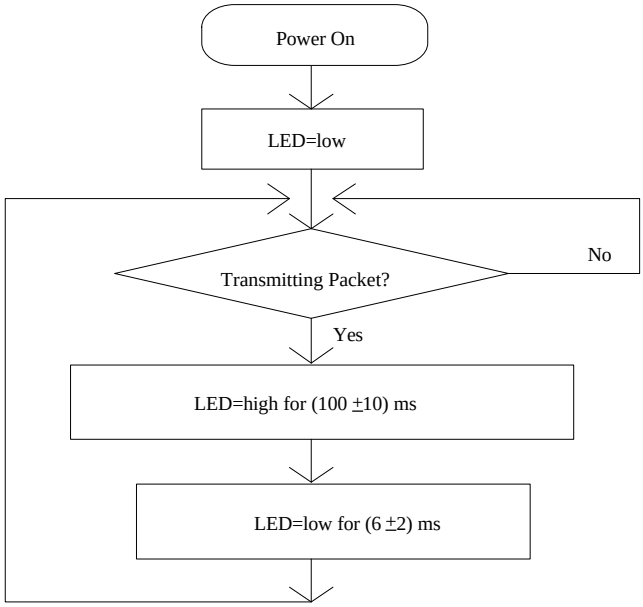
Note: The PAUSE operation cannot be used to inhibit transmission of MAC Control frames (e.g. PAUSE packet).

6.5. LED Behaviors

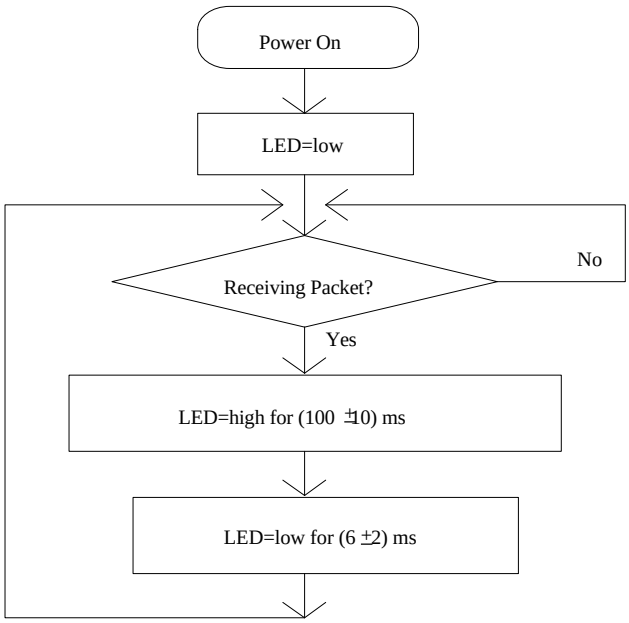
This section describes the lighting behaviors of the LED output signals which may be selected by LEDS1 and LEDS0 bits in the Page3 CONFIG3 register.

P.S. It is assumed that the LED is on when the signal goes low.

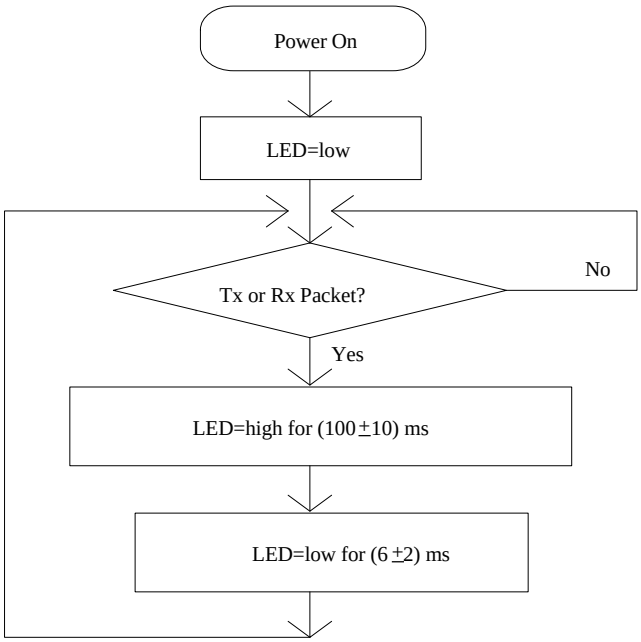
6.5.1 LED_TX: Tx LED



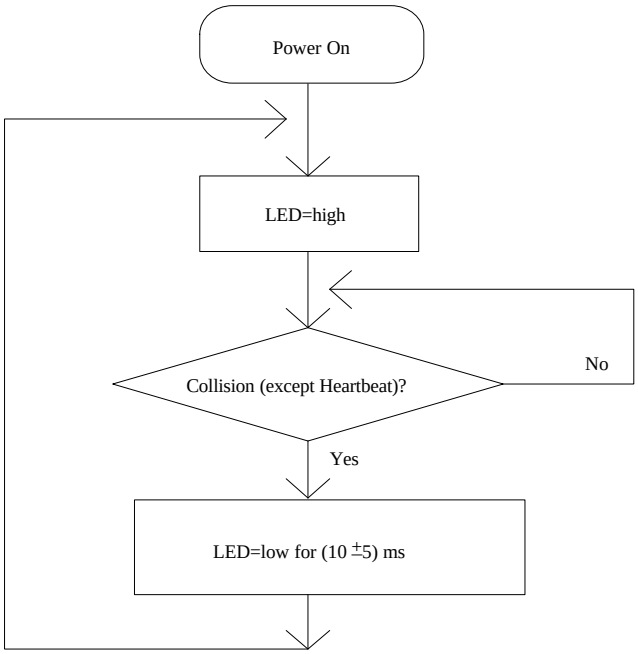
6.5.2 LED_RX: Rx LED



6.5.3 LED_CRS=LED_TX+LED_RX: Carrier Sense LED



6.5.4 LED_COL: Collision LED



6.5.5 LED Output States in Power Down Modes

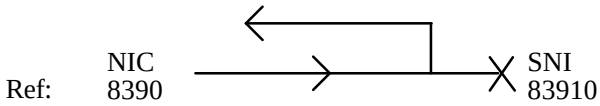
LED Output	Normal Mode / Idle	Sleep Mode	Power Down Mode
LED_BNC	-	-	Low
LED_LINK	-	High	High
LED_COL	High	High	High
LED_TX	Low	High	High
LED_RX	Low	High	High
LED_CRS	Low	High	High

6.6. Loopback Diagnostic Operation

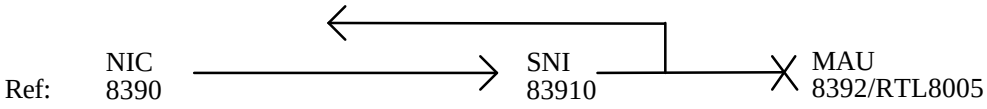
6.6.1. Loopback operation

The RTL8029AS provides 3 loopback modes. By loopback test, we can verify the integrity of data path, CRC logic, address recognition logic and cable connection status.

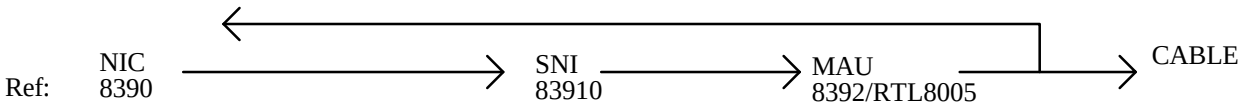
Mode 1: Loopback through the NIC (LB1=0, LB0=1 in TCR).
The NRZ data is not transmitted to the SNI but instead it's loopbacked to the NIC's Rx deserializer. The traffic on the cable is ignored.



Mode 2: Loopback through the SNI (LB1=1, LB0=0 in TCR)
The Manchester encoded data is not transmitted to the MAU. It's loopbacked through the SNI to NIC. The traffic on the cable is ignored.



Mode 3: Loopback through the cable (LB1=1, LB0=1 in TCR)
The packets are transmitted via the MAU onto the network and RTL8029AS receives all incoming packets (not only the MAU-loopbacked Tx data) in the meantime.



❑ Alignment of the Reception FIFO

The reception FIFO is an 8-byte ring structure. The first received byte is put at location zero. When the location pointer goes to the end of the FIFO, it wraps to the beginning of the FIFO and overwrites the previous data. At the end of the packet reception, the FIFO contents are in the "order" (from the ring structure's view) as shown below.

(1) CRC enabled (CRC bit in TCR=0)

- 1-byte received packet data
- 4-byte CRC
- 1-byte lower byte count
- 1-byte upper byte count
- 1-byte upper byte count

(2) CRC disabled (CRC bit in TCR=1)

- 5-byte received packet data
- 1-byte lower byte count
- 1-byte upper byte count
- 1-byte upper byte count

6.6.2. To Implement Loopback Test

(1) To verify the integrity of data path

- set RCR=00H to accept physical packet
- set PAR0-5 to accept packet
- set DCR=43H
- set TCR=02H, 04H, 06H to do loopback test 1, 2, 3 respectively
- set CRC enabled (CRC=00H in TCR)
- clear ISR
- Tx a packet and check ISR
- check FIFO after loopback

Notes: Loopback mode 3 is sensitive to the network traffic, so the values of FIFO may be not correct.

(2) To verify CRC logic

❑ Select a loopback mode (e.g. mode 2) to test

A. To test CRC generator

- set RCR=00H to accept physical packet
- set PAR0-5 to accept packet
- set TCR=04H (CRC enabled)
- set DCR=43H
- clear ISR
- Tx a packet
- check CRC bytes in FIFO after loopback

B. To test CRC checker

- set RCR=00H to accept physical packet
- set PAR0-5 to accept packet
- set TCR=05H (CRC disabled)
- set DCR=43H
- clear ISR
- Tx a packet with good or bad CRC appended by program
- check FIFO, ISR & RSR after loopback

  For bad CRC, expected: ISR=06H, RSR=02H (Tx:OK, Rx:CRC error)
  For good CRC, expected: ISR=02H, RSR=01H (Tx:OK, Rx:OK)

Notes: In loopback mode, the received packets are not stored to SRAM, so PRX bit in ISR isn't set.

(3) To verify the address recognition function

❑ Select a loopback mode (e.g. mode 2) to test

A. Right physical destination address

- set RCR=00H to accept physical packet
- set PAR0-5 to accept packet
- set TCR=04H (CRC enabled)
- set DCR=43H
- clear ISR
- Tx a packet
- check ISR after loopback

  Expected: ISR=06H (packets accepted, Rx CRC error)

B. Wrong physical destination address

- set RCR=00H to accept physical packet
- set PAR0-5 to reject packet
- set TCR=04H (CRC enabled)
- set DCR=43H
- clear ISR
- Tx a packet
- check ISR after loopback

  Expected: ISR=02H (packets rejected, Rx no response)

(4) To Test Cable Connection

❑ There are four physical medium types in RTL8029AS.

We perform loopback mode 3 to test the cable connection status.

- set RCR=00H to accept physical packet
- set PAR0-5 to accept packet
- set TCR=06H (CRC enabled)
- set DCR=43H
- clear ISR
- Tx a packet
- check TSR after loopback

A. 10Base2

If cable OK, get TSR=01H (Tx OK).
If cable FAIL, get TSR=0CH (Collision and Tx aborted).

B. 10Base5

If cable OK, get TSR=01H (Tx OK).
If MAU connected but cable FAIL, get TSR=0CH (Tx collision and Tx aborted).
If MAU not connected, get TSR=51H (Carrier sense is lost during transmission and CD heartbeat fails.).

C. 10BaseT with link test disabled

RTL8029AS disables link test in this case, so cable OK or FAIL doesn't affect TSR; get TSR=01H.

D. Auto-detection (10BaseT with link test enabled)

RTL8029AS automatically switches from 10BaseT to 10Base2 if the twisted-pair wire is not connected (10BaseT link test fails).

If twisted-pair wire OK, get TSR=01H (Tx OK) & BNC=0 in CONFIG2.
If twisted-pair wire FAIL but coaxial cable OK, get TSR=01H (Tx OK) & BNC=1 in CONFIG2.
Otherwise, get TSR=0CH (same as 10Base2 connection fail).

7. ELECTRICAL SPECIFICATIONS AND TIMINGS

7.1. Absolute Maximum Ratings

Operating Temperature ..... 0¢J to 70¢J
Storage Temperature ..... -65 ¢J to 140¢J
All Outputs and Supply Voltages, with respect to Ground ..... -0.5V to 7V
Power Dissipation .....

Warning:
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only.
Functionality at or above these limits is not recommended and extended exposure to "Absolute Maximum Ratings" may affect device reliability.

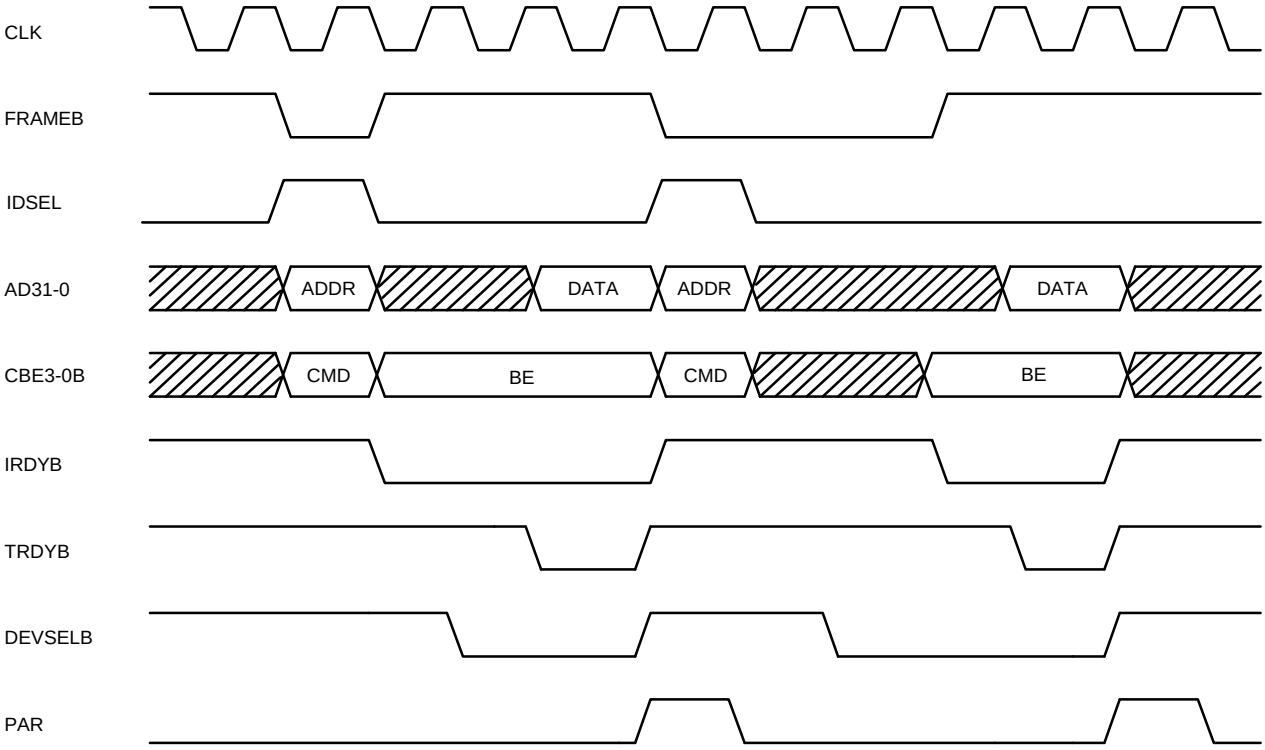
7.2. D.C. Characteristics (Tc=0 ¢J to 70 ¢J, Vcc=5V±5%)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Vil	Input Low Voltage			0.8	V	
Vih	Input High Voltage	2.0		5.5	V	
Vol	Low-level output voltage			0.55	V	Io=3mA, 6mA
Voh	High-level output voltage	2.4				Ioh=-2mA
II	Input Leakage Current			10	µA	V=GND to VDD

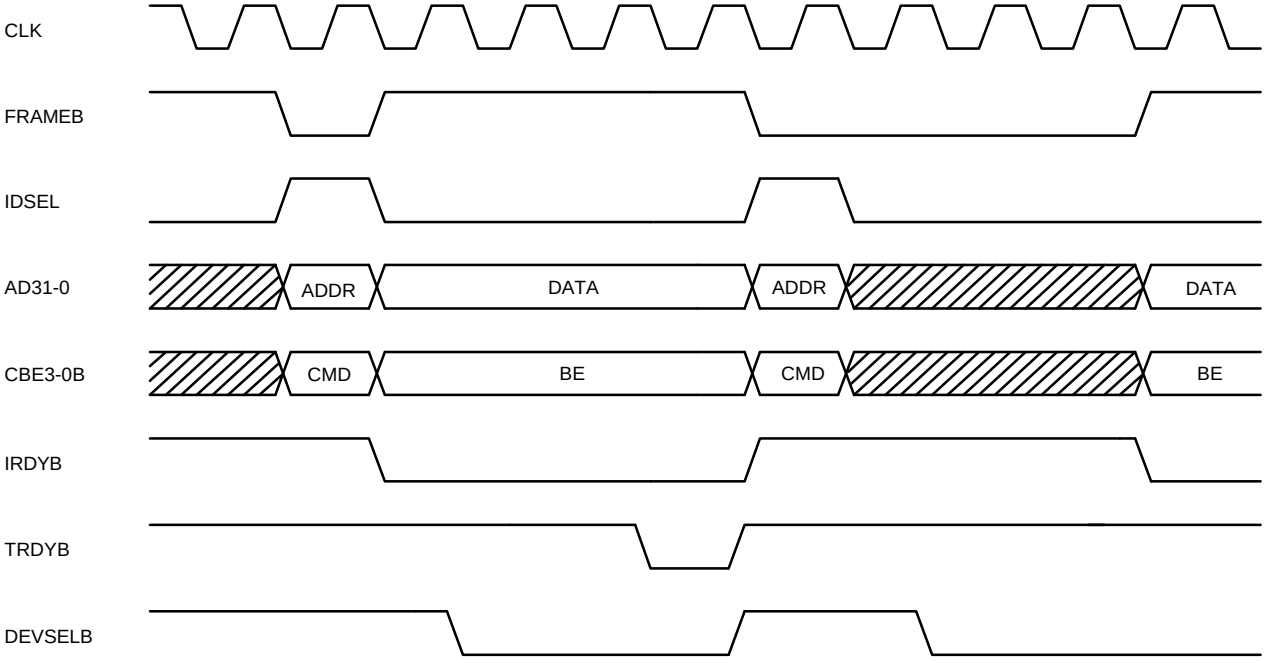
7.3. A.C. Timing Characteristics

7.3.1. PCI Configuration Read/Write

7.3.1.1. Configuration Read

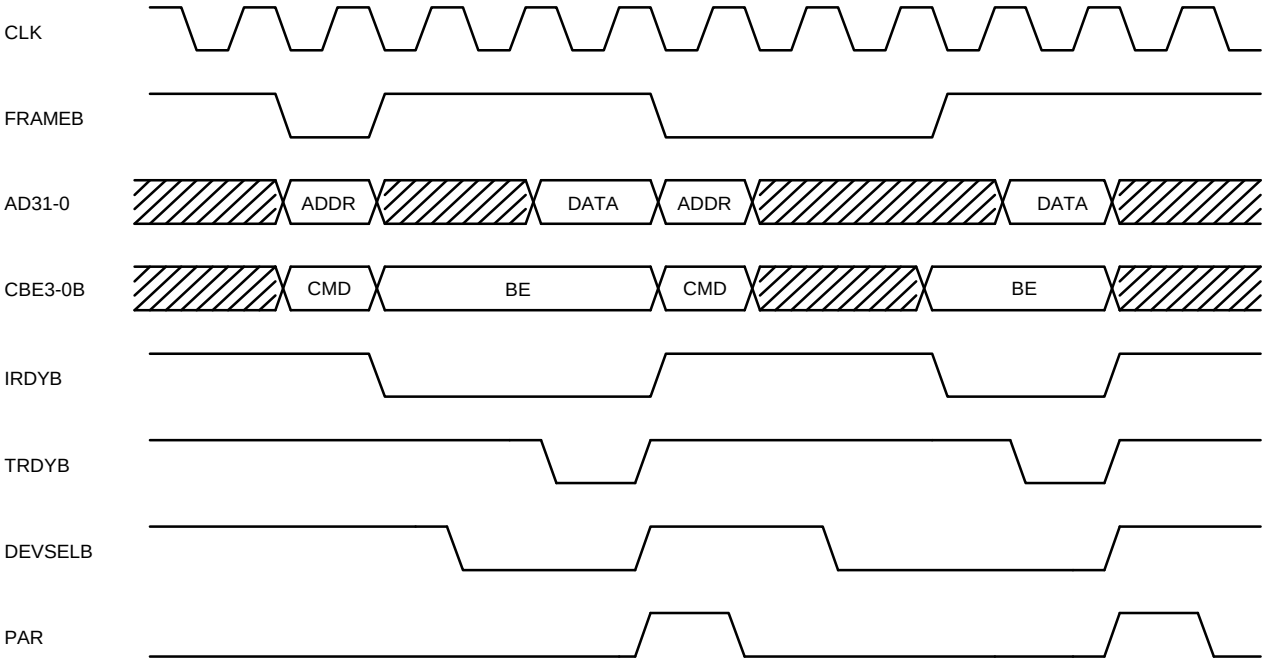


7.3.1.2. Configuration Write

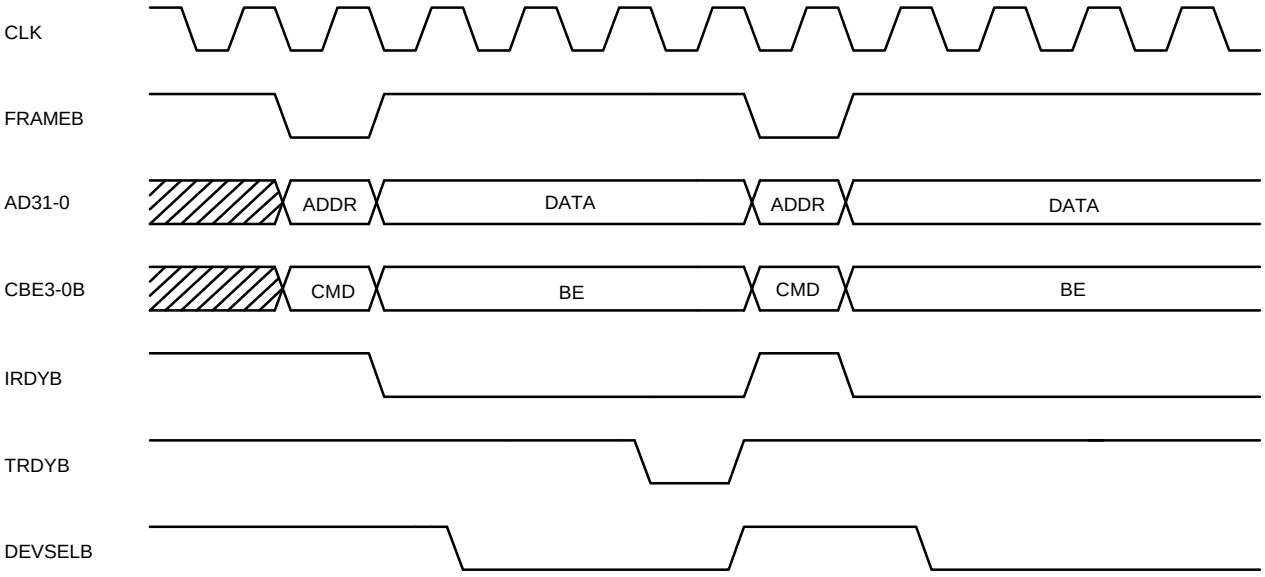


7.3.2. PCI I/O Read/Write

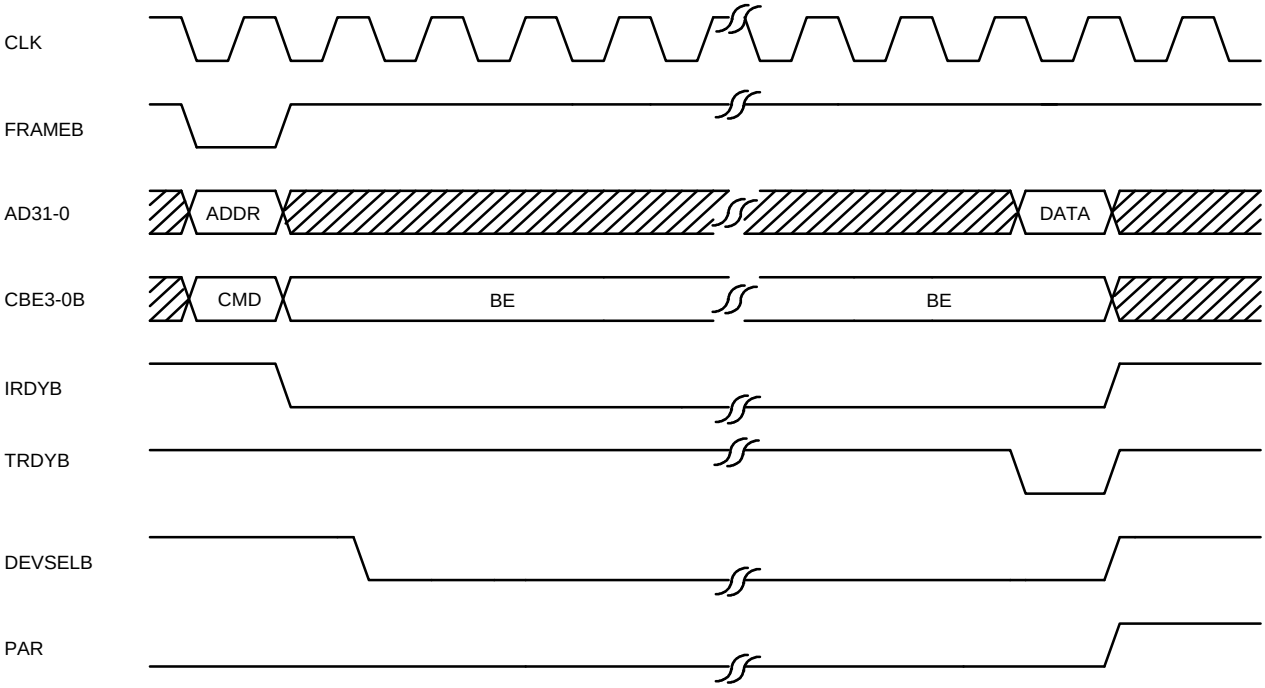
7.3.2.1. PCI I/O Read



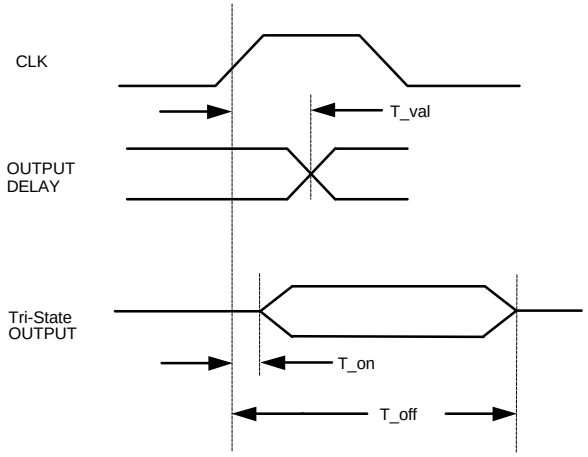
7.3.2.2. PCI I/O Write



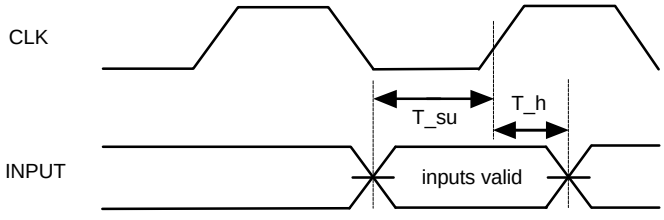
7.3.3. BROM Read



7.3.4. Output Timing for PCI Interface

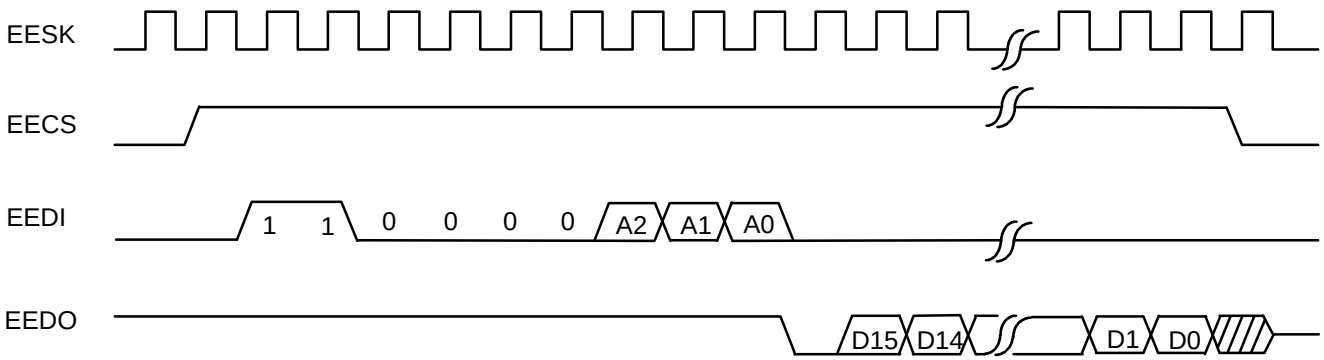


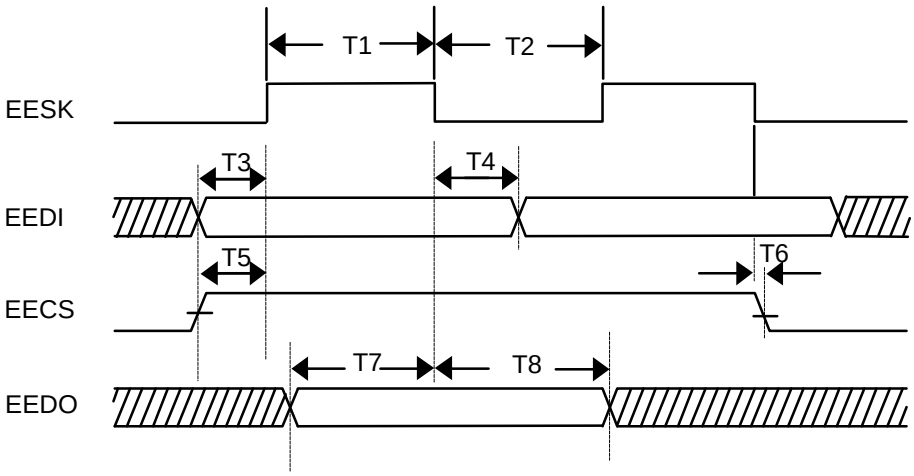
7.3.5. Input Timing for PCI Interface



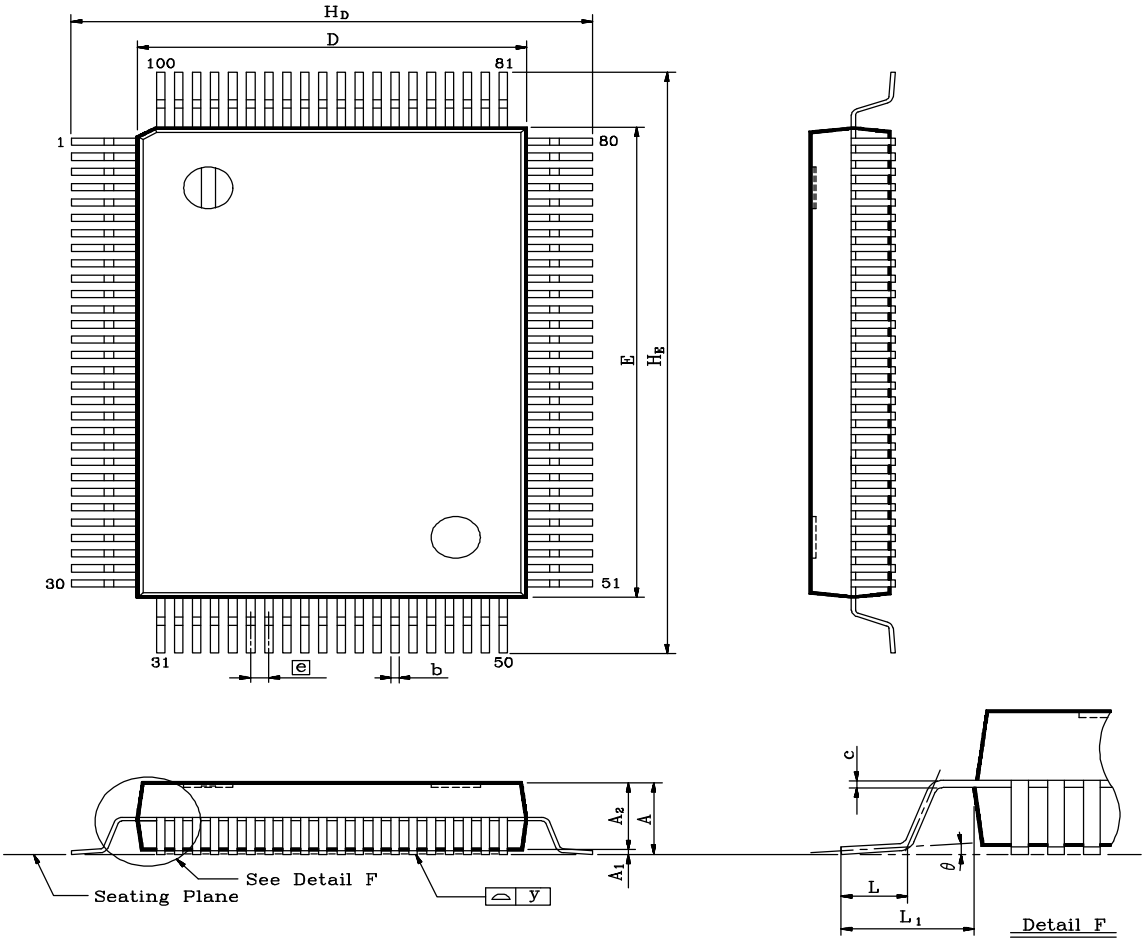
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{val}	CLK to Signal Valid Delay-bussed signals	2		11	ns
t_{on}	Float to Active Delay			11	ns
t_{off}	Active to Float Delay			11	ns
t_{su}	Input Set up Time to CLK-bussed signals	7			ns
t_h	Input Hold Time from CLK	0			ns

7.3.6. Serial EEPROM (9346) Auto-load





Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	EESK high width		3.2		ns
T2	EESK low width		3.2		ns
T3	EEDI setup to EESK rising edge	3.0			ns
T4	EEDI hold from EESK falling edge	3.0			ns
T5	EECS goes high to EESK rising edge	3.0			ns
T6	EECS goes low from EESK falling edge				ns
T7	EEDO setup to EESK falling edge	20			ns
T8	EEDO hold from EESK falling edge	10			ns



Note:

1.Dimension D & E do not include interlead flash.
2.Dimension b does not include dambar protrusion/intrusion.
3.Controlling dimension: Millimeter
4.General appearance spec. should be based on final visual inspection spec.

Symbol	Dimension in mil			Dimension in mm		
	Min	Typ	Max	Min	Typ	Max
A	106.3	118.1	129.9	2.70	**3.00**	3.30
A1	4.3	20.1	35.8	0.11	**0.51**	0.91
A2	102.4	112.2	122.0	2.60	**2.85**	3.10
b	7.1	11.8	16.5	0.18	**0.30**	0.42
c	1.6	5.9	10.2	0.04	**0.15**	0.26
D	541.3	551.2	561.0	13.75	**14.00**	14.25
E	777.6	787.4	797.2	19.75	**20.00**	20.25
e	19.7	25.6	31.5	0.50	**0.65**	0.80
HD	726.4	740.2	753.9	18.45	**18.80**	19.15
HE	962.6	976.4	990.2	24.45	**24.80**	25.15
L	39.4	47.2	55.1	1.00	**1.20**	1.40
L1	88.6	94.5	104.3	2.25	**2.40**	2.65
y	¡Ð	¡Ð	3.9	¡Ð	¡Ð	0.10
£c	0¢X	¡Ð	12¢X	0¢X	¡Ð	12¢X

TITLE : 100L QFP (14x20 mm**2) FOOTPRINT 4.8 mm PACKAGE OUTLINE DRAWING			
LEADFRAME MATERIAL:			
APPROVE		DWG NO.	
		REV NO.	
		SCALE	
CHECK	Ricardo Chen	DATE	
		SHT NO.	1 OF
REALTEK SEMI-CONDUCTOR CO., LTD			