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P. Leader	Check by	Design by

Project Code & Schematics Subject: M610 PVT Main Board      PCB P/N: 黃田 1P-0072100-8010  
翰宇博德 1P-0072500-8010

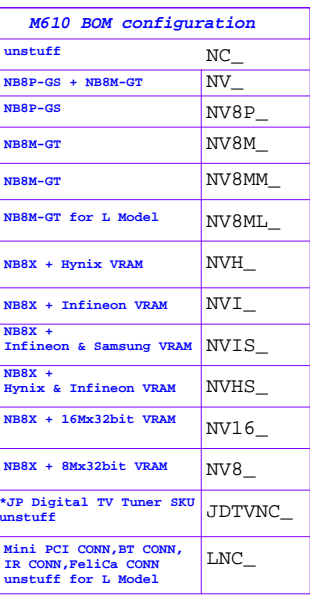
FOXCONN HON HAI PRECISION IND. CO., LTD.  
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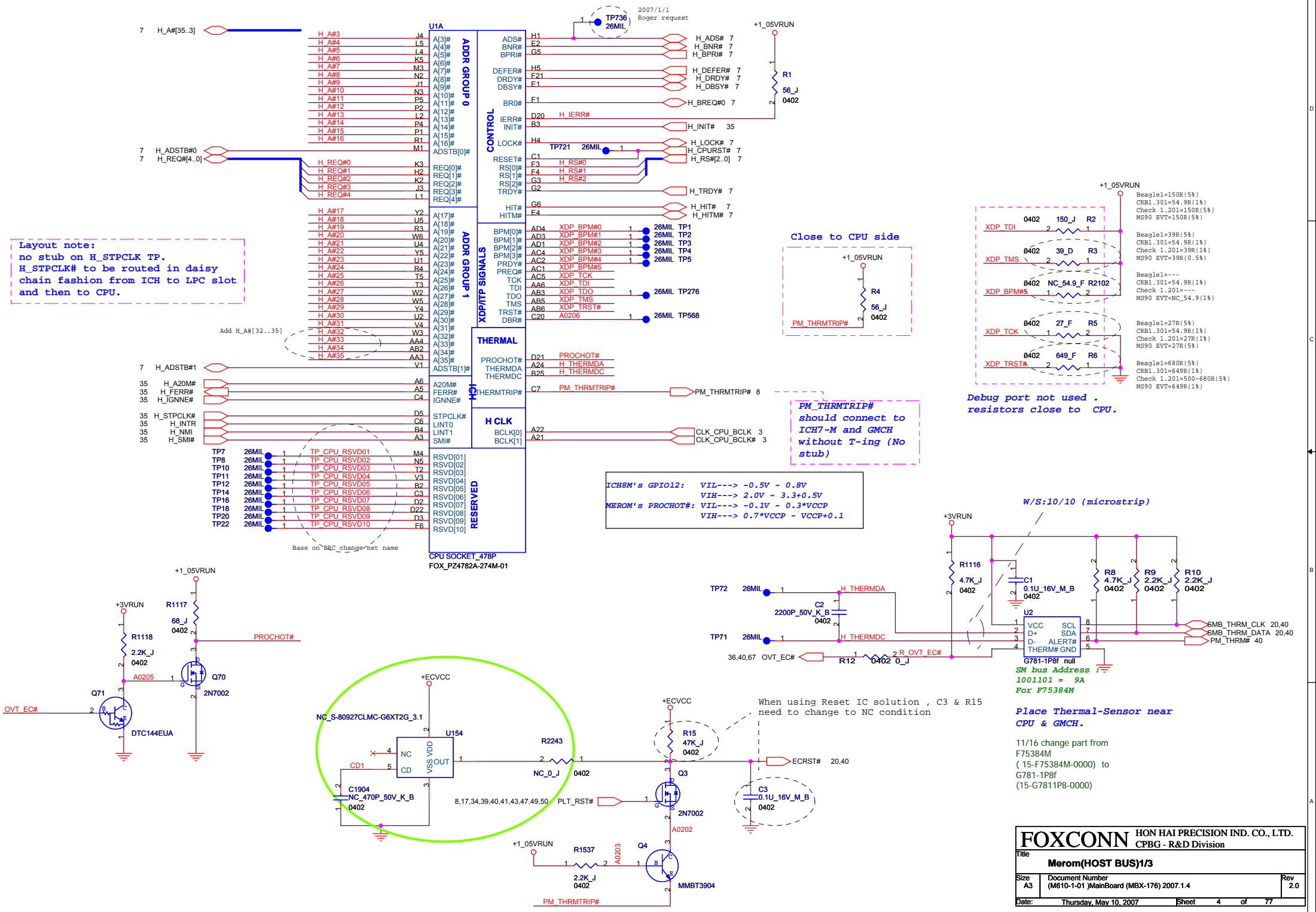
Size A3    Document Number (M610-1-01 )MainBoard (MBX-176) 2007.1.4    Rev 2.0

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Red texts:  
New modified



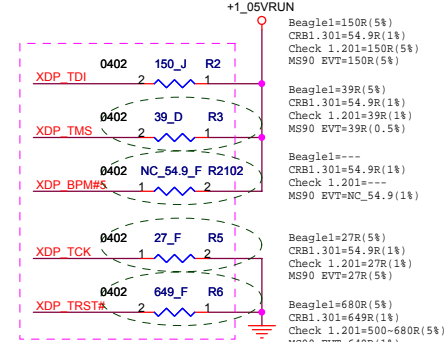




Layout note:  
no stub on H\_STPCLK TP.  
H\_STPCLK# to be routed in daisy chain fashion from ICH to LPC slot and then to CPU.

Close to CPU side

PM\_THRMTRIP# should connect to ICH7-M and GMCH without T-ing (No stub)



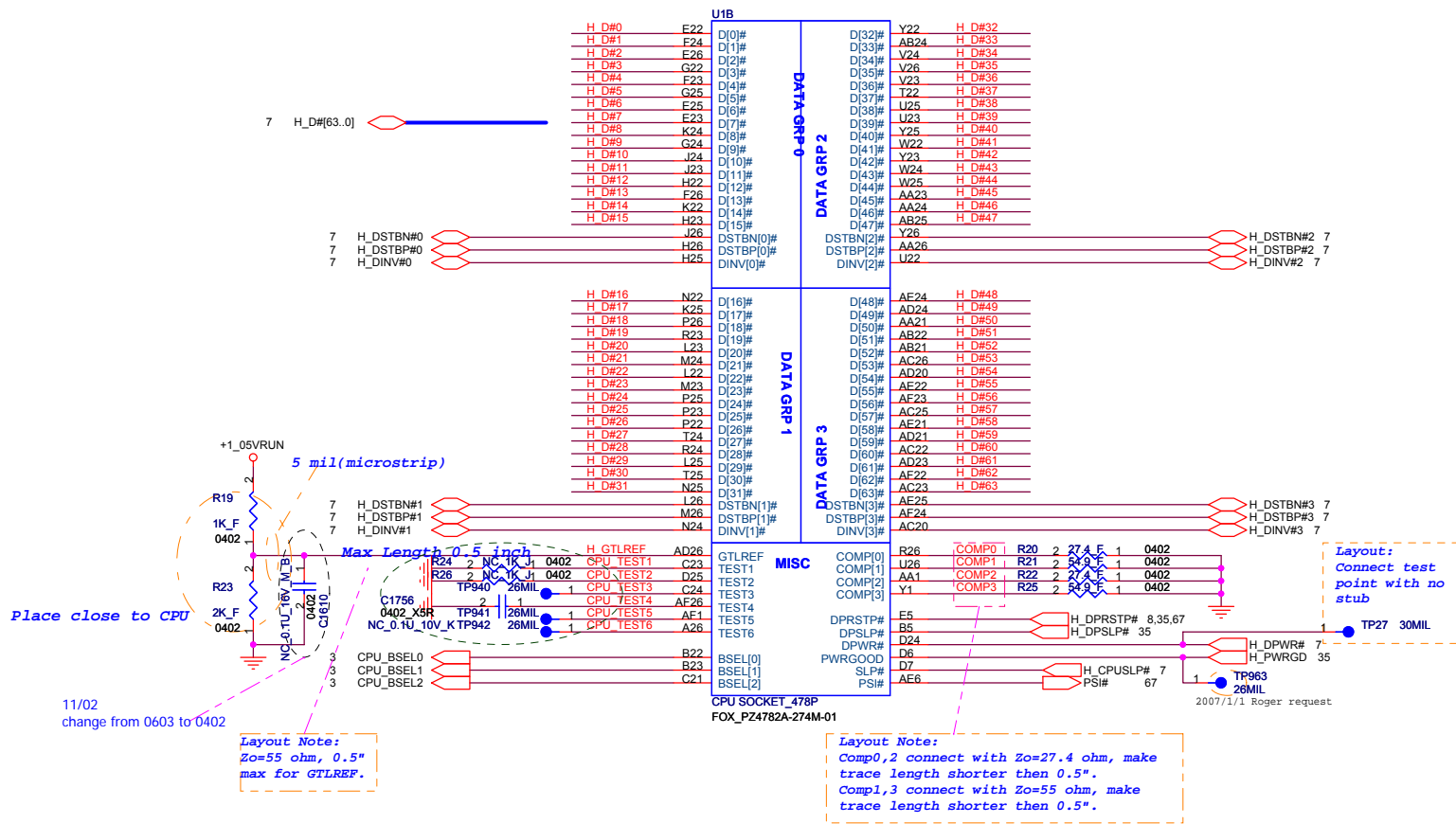
Debug port not used . resistors close to CPU.

ICH8M's GPIO12: VIL----> -0.5V ~ 0.8V  
VIH----> 2.0V ~ 3.3+0.5V  
MEROM's PROCHOT#: VIL----> -0.1V ~ 0.3\*VCCP  
VIH----> 0.7\*VCCP ~ VCCP+0.1

W/S:10/10 (microstrip)

Place Thermal-Sensor near CPU & GMCH.

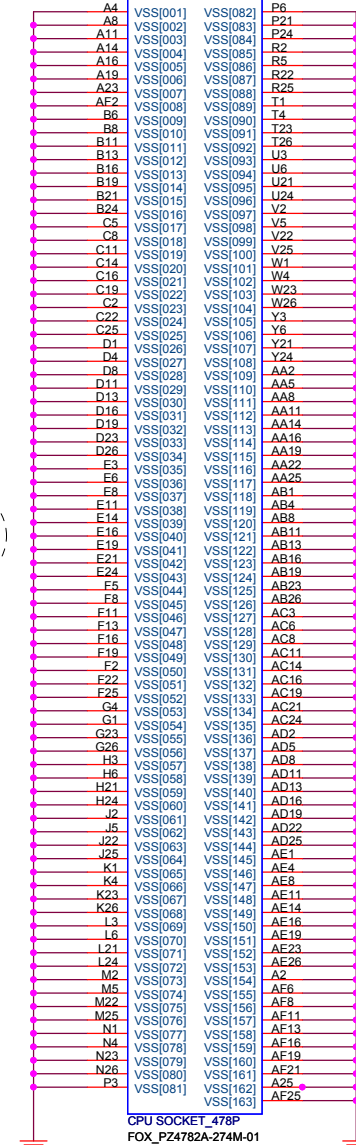
11/16 change part from F75384M (15-F75384M-0000) to G781-1P8f (15-G7811P8-0000)



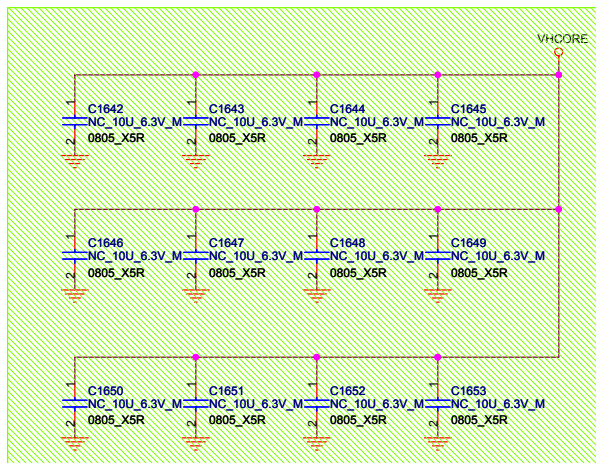
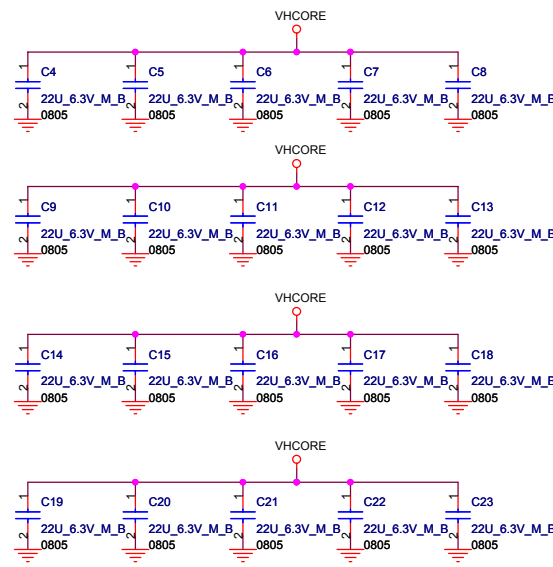
CPU\_VCCA----->130mA  
CPU\_VCCP----->4.5A  
CPU\_VCC----->44A

MS90 check

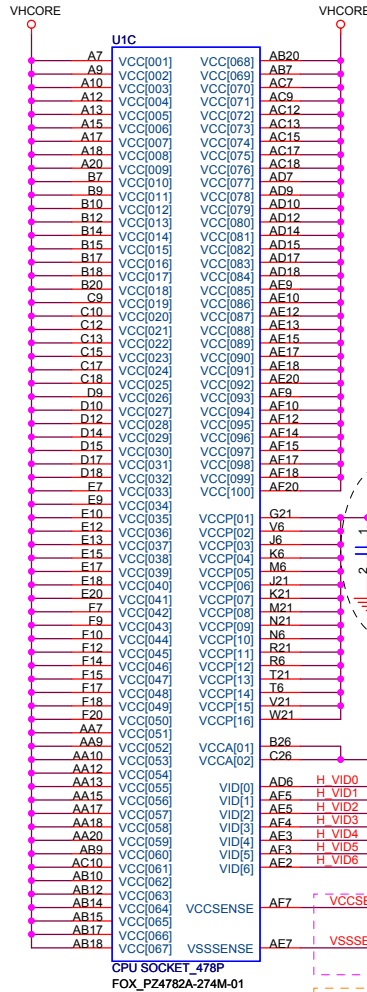
U1D



CPU SOCKET\_478P  
FOX\_PZ4782A-274M-01

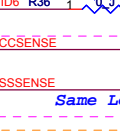
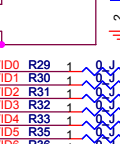
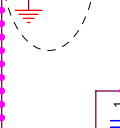


Backup 10uF capacitors for 22uF shortage.



CPU SOCKET\_478P  
FOX\_PZ4782A-274M-01

Beagle1=10U  
CRB1.301=NO  
2HwC=1.201=NO  
MS90 RV=NO



Layout Note: Route  
VCCSENSE traces at 27.4  
Ohms with 50 mil spacing.  
Place PU and PD within 1  
inch of cpu.  
  
width=18 mil  
spacing=7 mil

(Design check 1.301) 2006.9.3  
No Stuff 27.4 ± 1% pull-down to GND  
near Intel MVP 6 controller for testing purposes.

100 mil

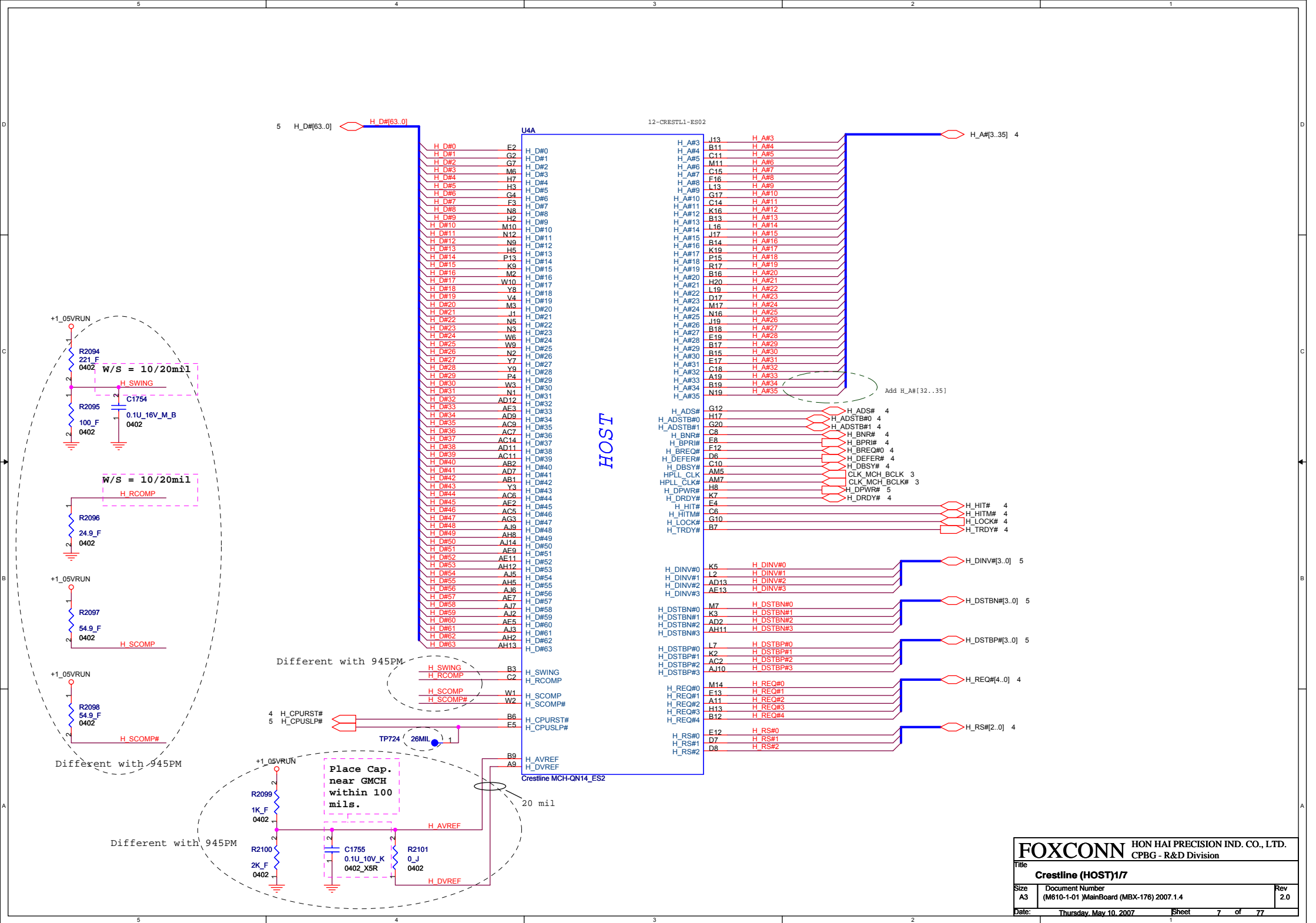
1.5VRUN

- 20 mil

LAYOUT NOTE:  
Place 0.01uF  
near PIN B26

CAP7 move from pagell  
fix PAD location, but change  
CAP val from NC\_47U to 330U

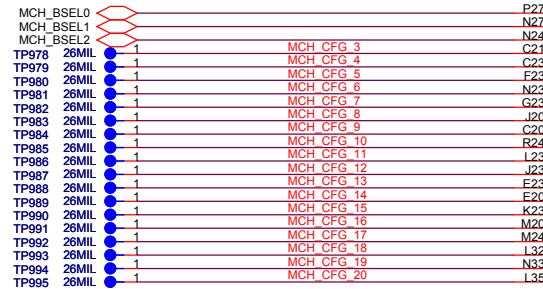




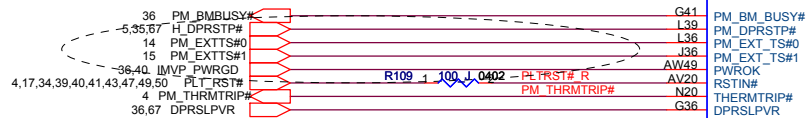
CFG[2:0]  
010 = FSB 800 MHz  
011 = FSB 667 MHz

MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane operation High = Normal operation
---	---

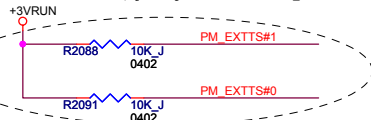
For layout convenience



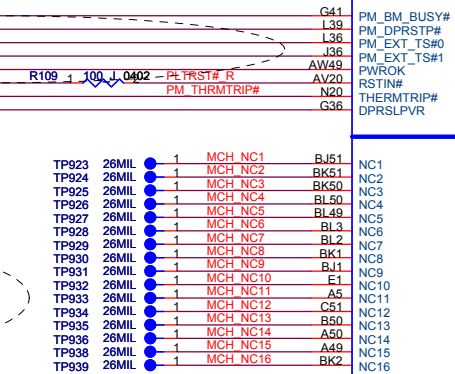
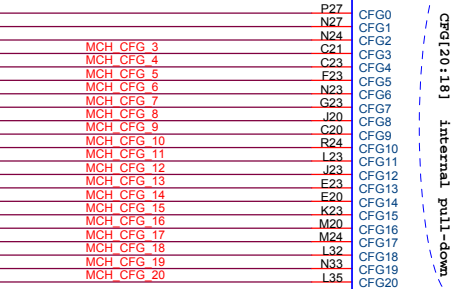
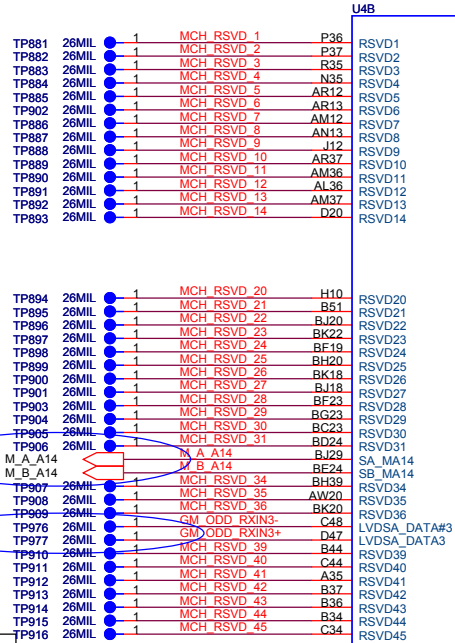
Wait to confirm with Page 13 / CRB



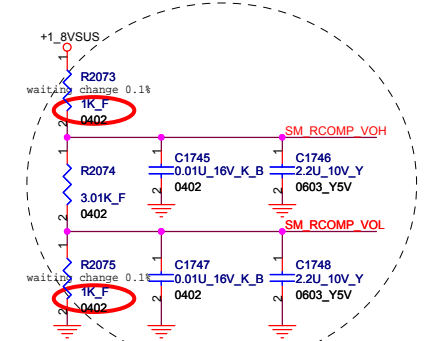
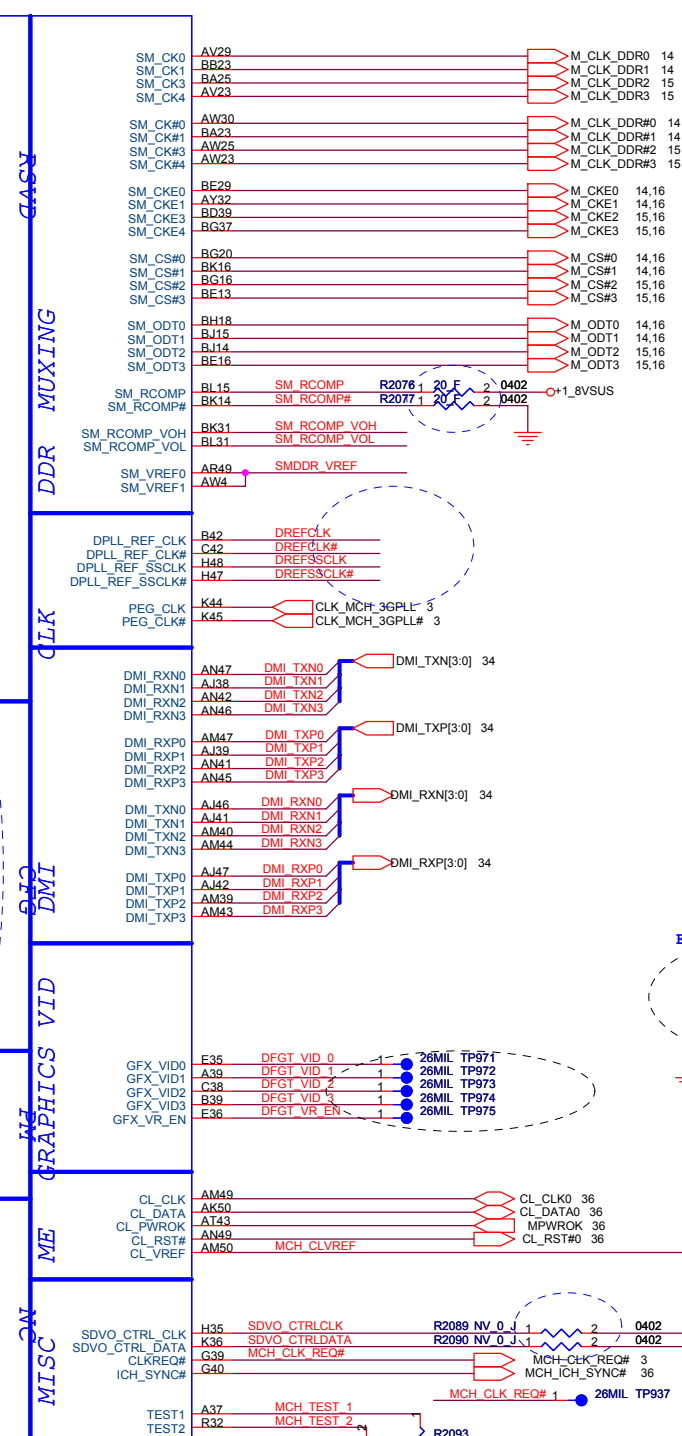
Design check 1.201  
DDR2 Connect to PM\_EXT\_TS#0/1 pins  
of GMCH, pull up with 10K to Vcc3\_3



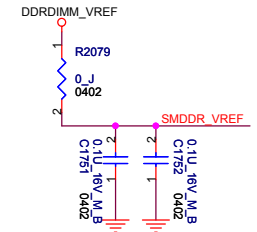
20.40 DDR\_ALERT#  
Form (U8)thermal sanser & (EC) 0402



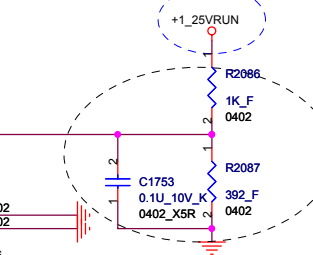
Crestline MCH-QN14\_ES2



Note: If the voltage regulator for the system memory interface already supplies a VREF output and meets the voltage tolerance and current requirements for these pins, then a voltage divider would not be needed.

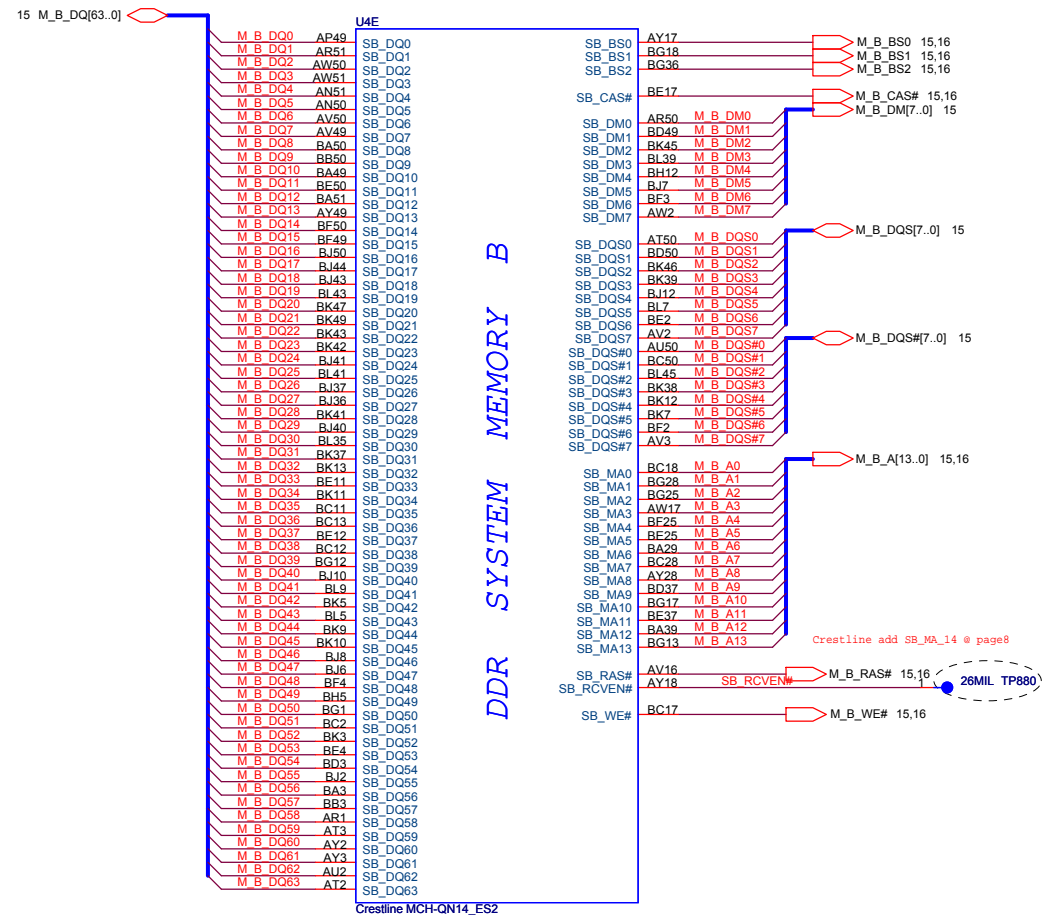
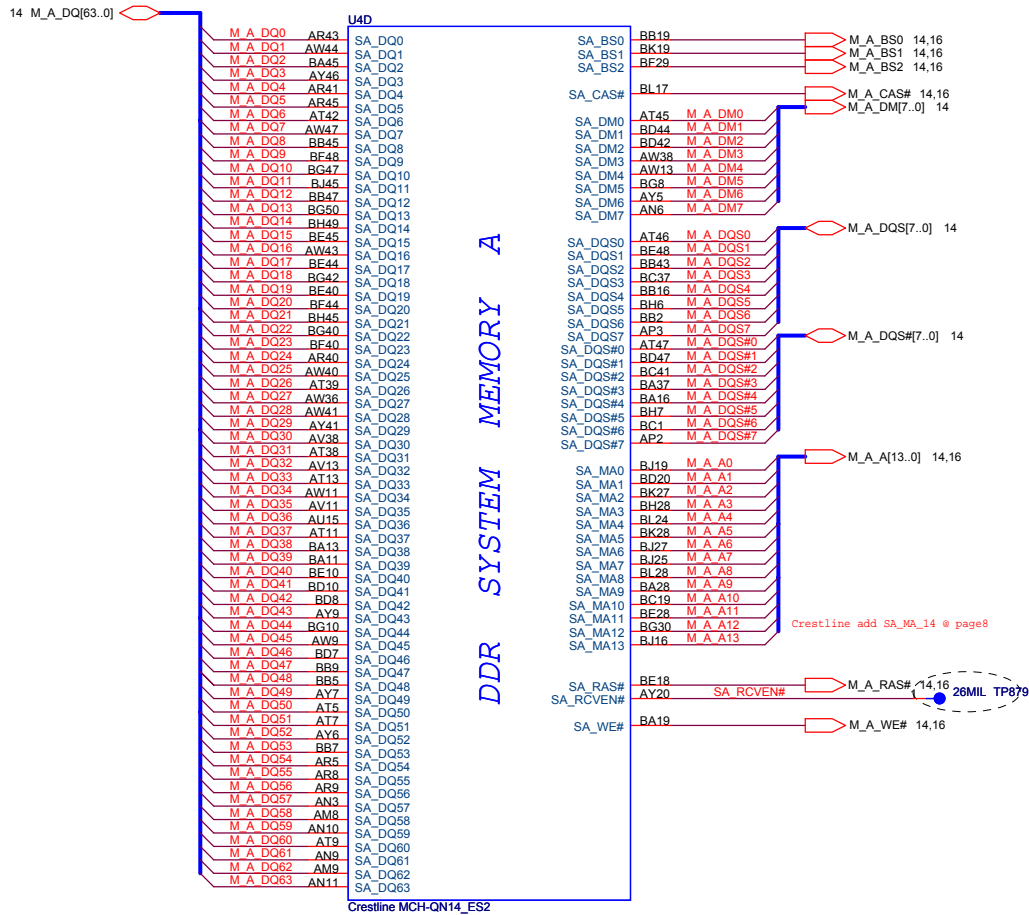


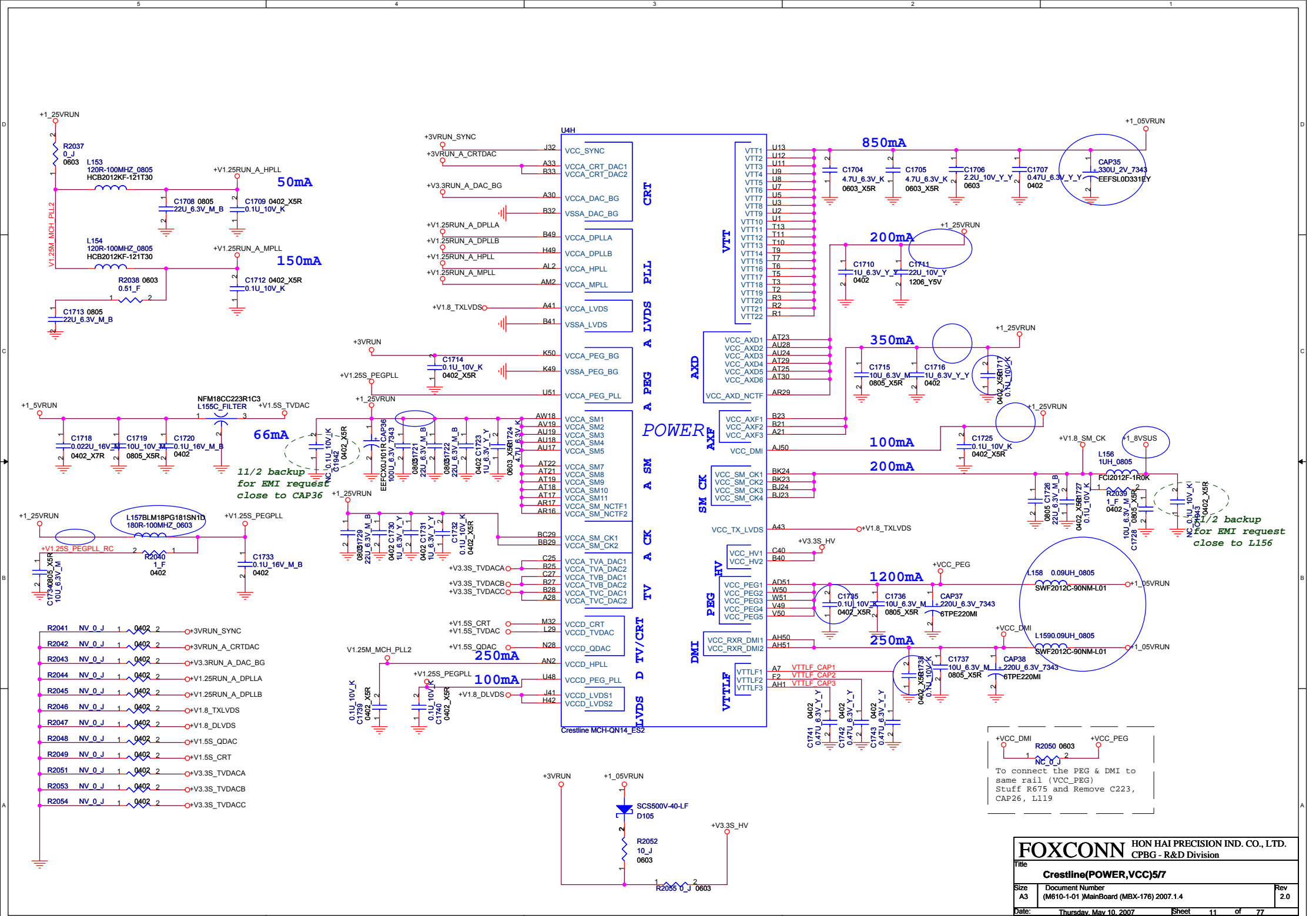
External Graphics (GMCH CRT/TVOUT Disable)

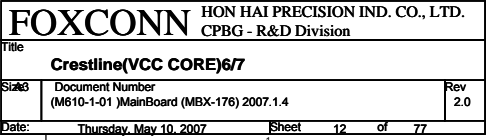


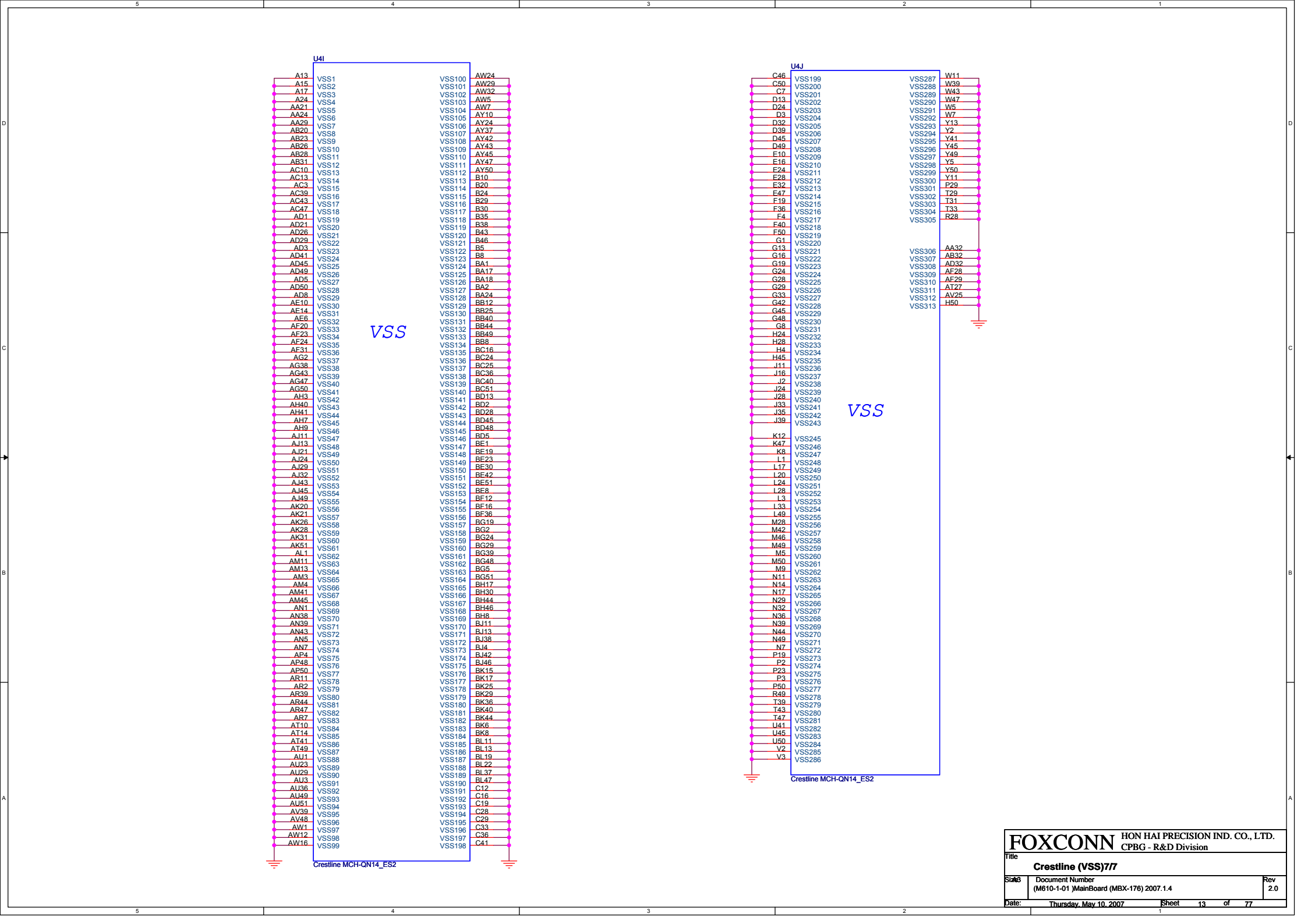








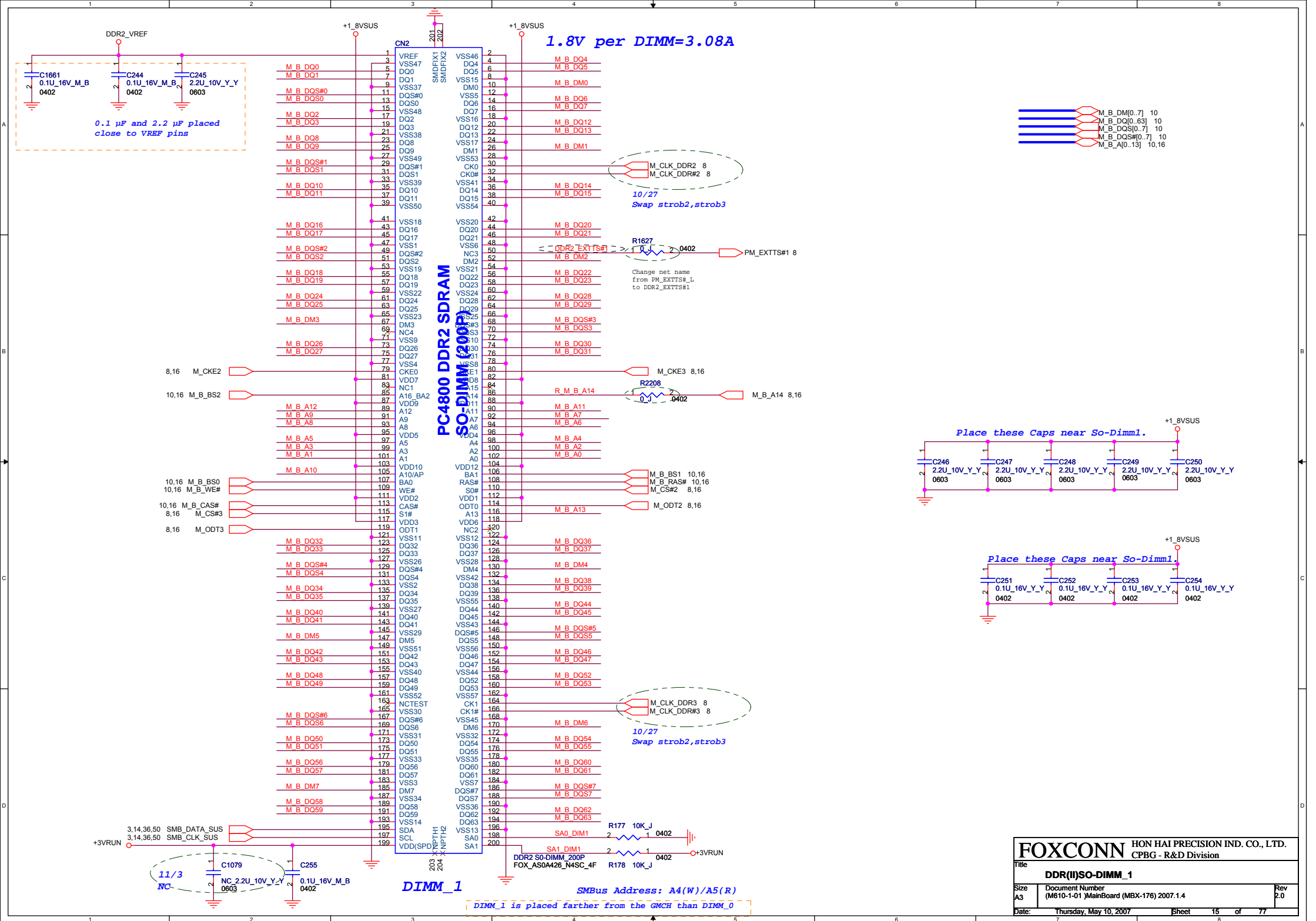


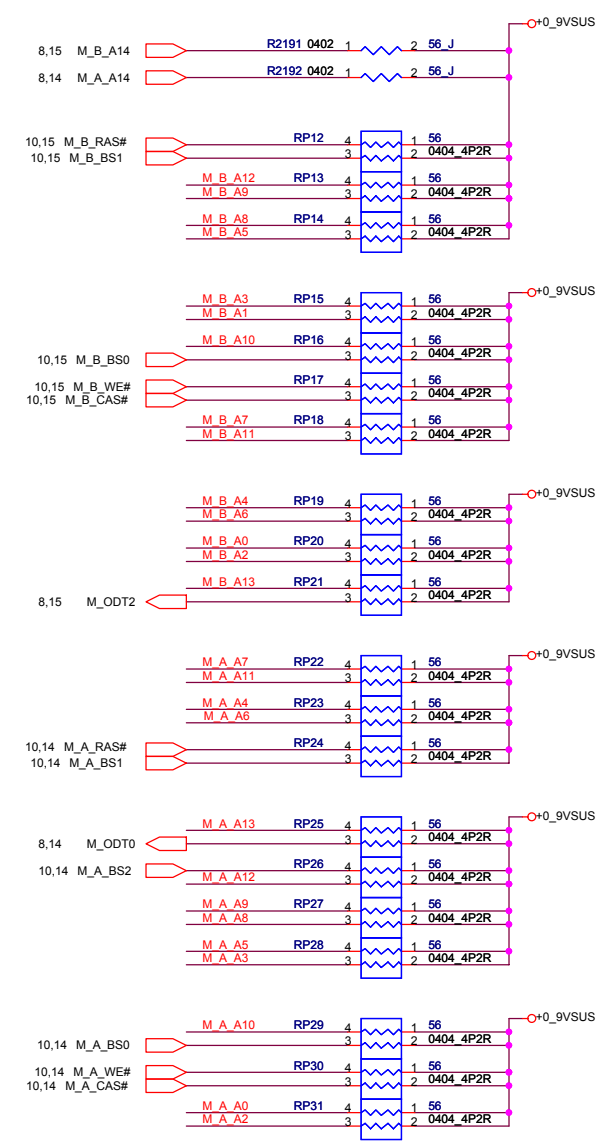
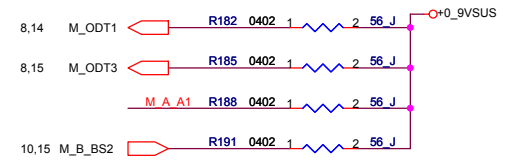
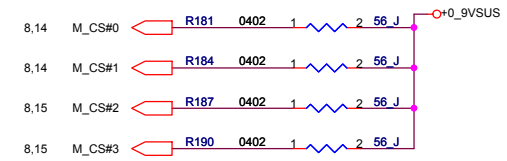
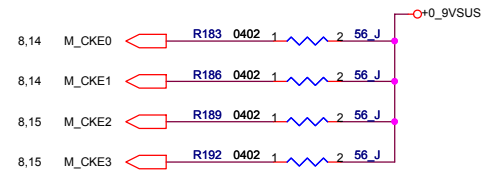
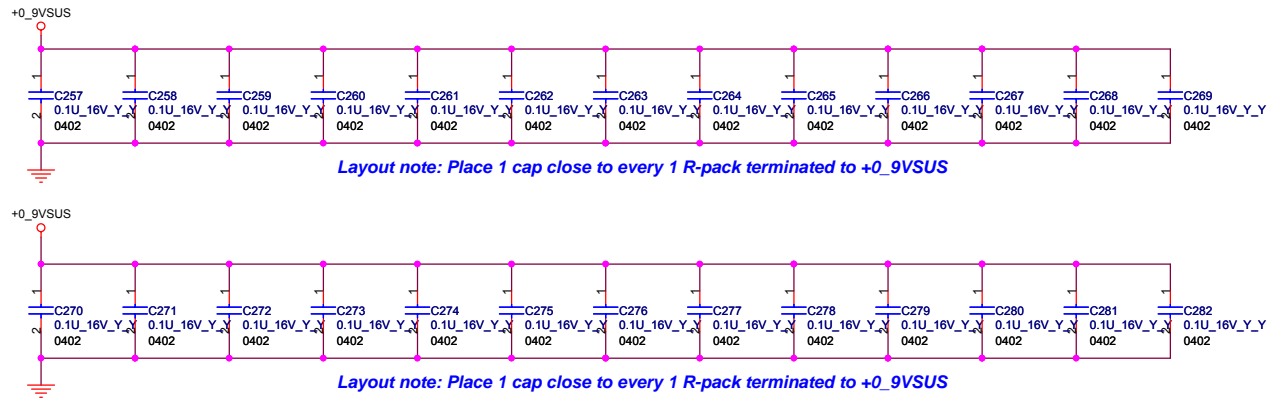


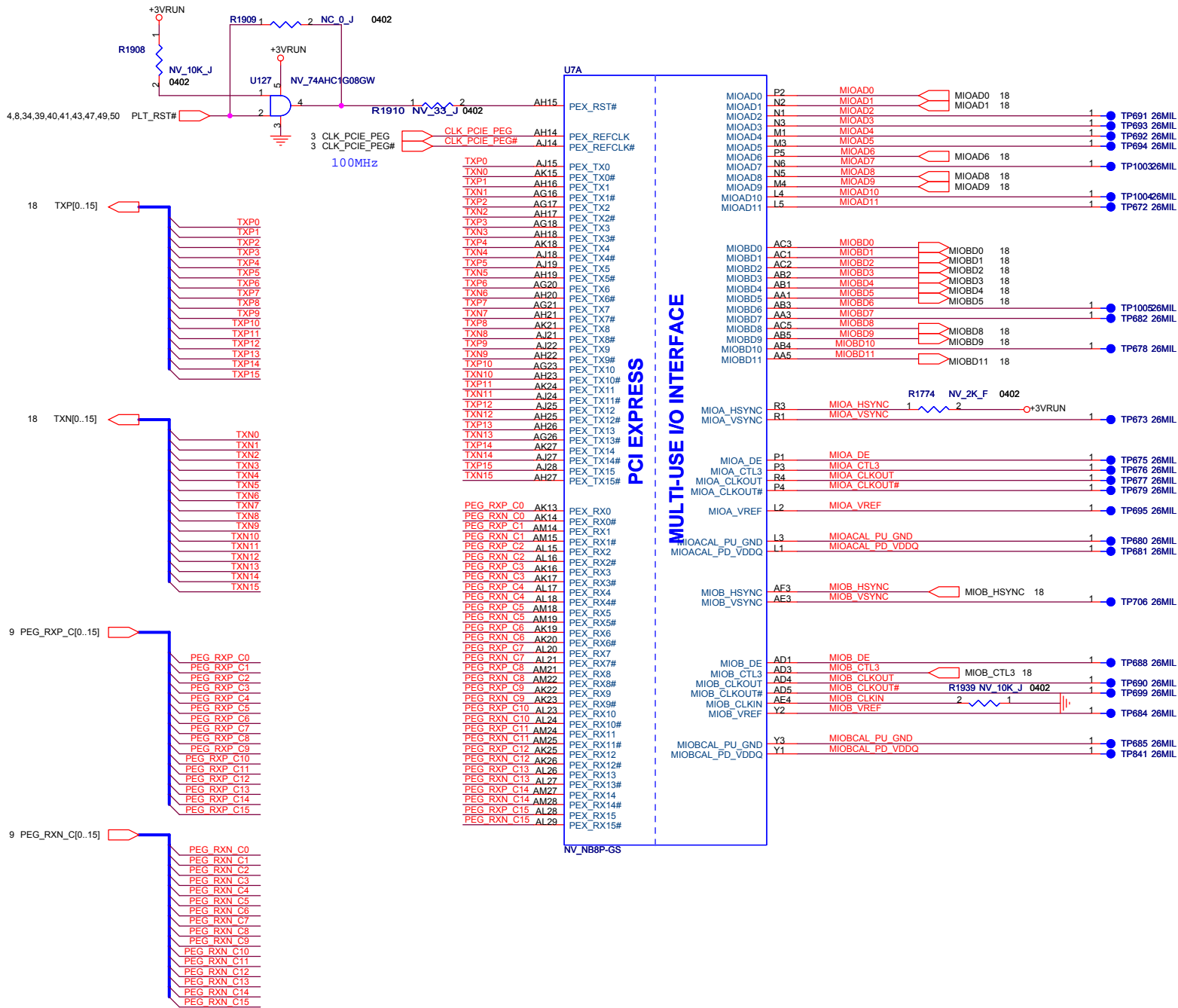




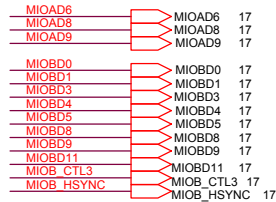
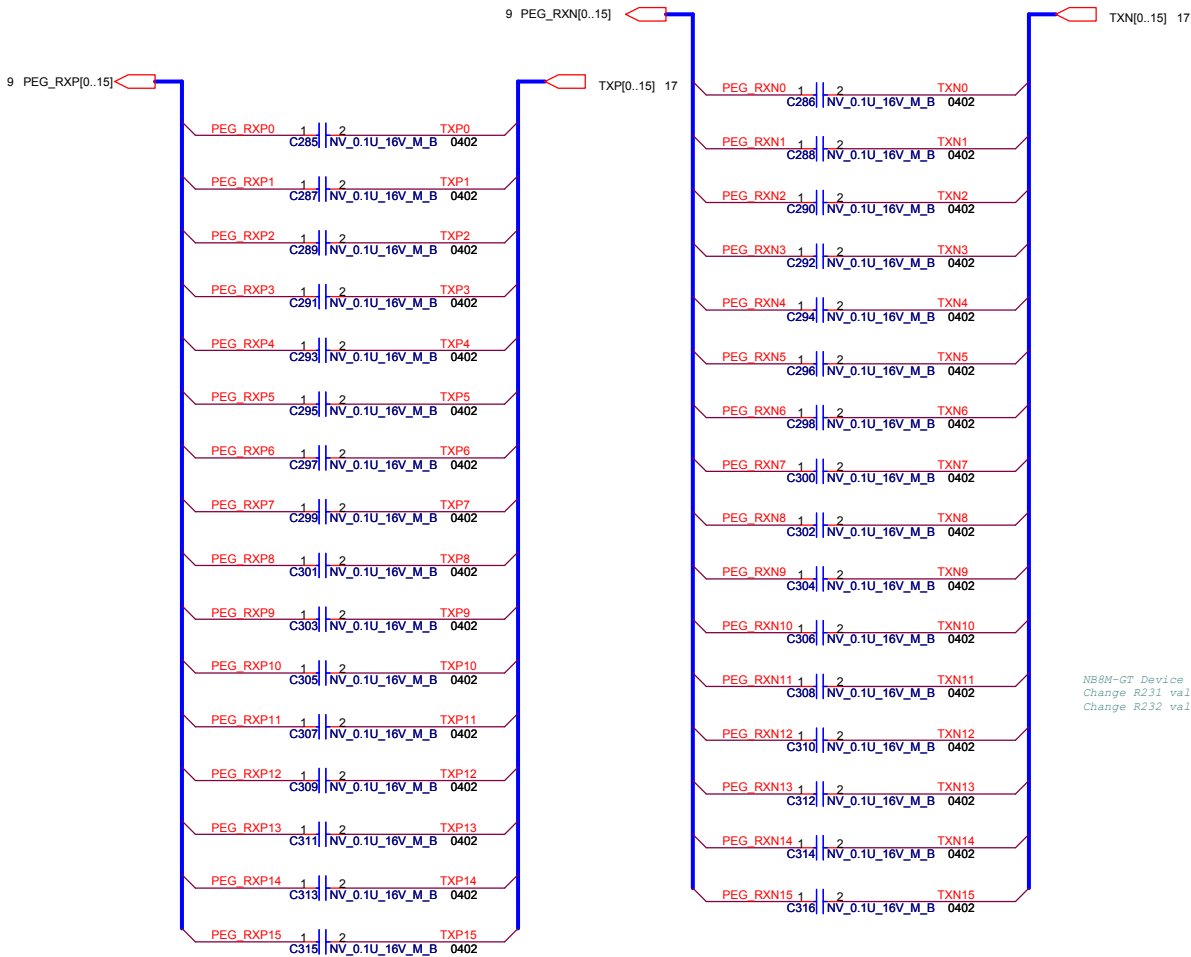








[MIOA\_HSYNC : SLOT\_CLOCK\_CFG]  
0 GPU and MCH share a common reference clock  
1 GPU and MCH do not share a common reference clock



NB8X Strap for GDDR3-136ball

0001 16Mx32Infineon  
0010 16Mx32Hynix  
0011 16Mx32Samsung  
0101 8Mx32Infineon  
0110 8Mx32Hynix  
0111 8Mx32Samsung

SUB\_VENDOR

0 (USE SYSTEM BIOS)  
1 (USE EXTERNAL ROM)

MIOAD0 is used to set the PCI Express PLL termination enable.  
DEFAULT "0"

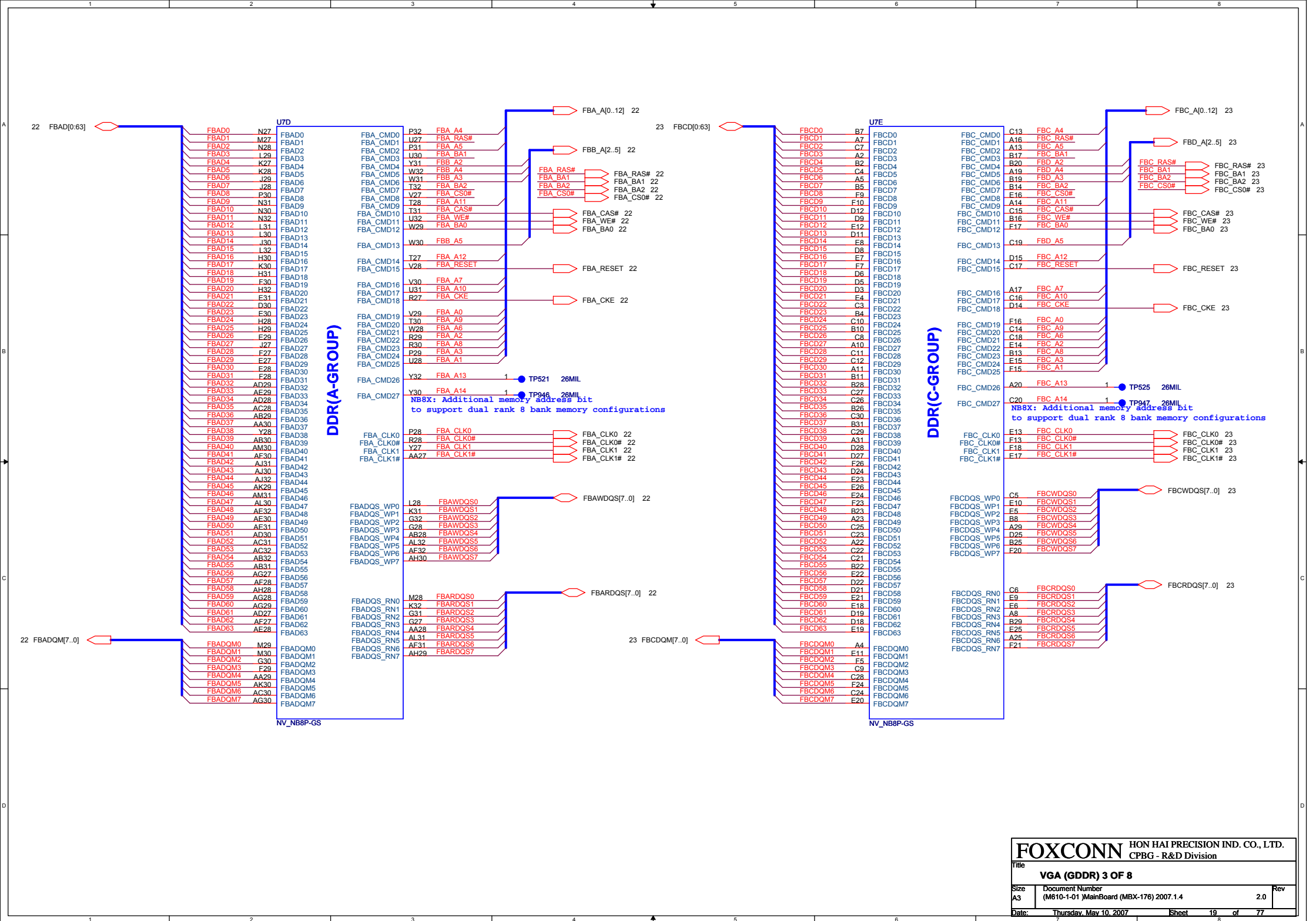
NB8X 3GIO\_PADCFG[3:0]  
0001

NB8M-GT Device ID setting mismatch between VBIOS and H/W Straps  
Change R231 value from NC\_ to NV8M\_  
Change R232 value from NV\_ to NV8P\_

NB8X PCI\_DEVID[4:0]  
NB8P-GS X0111 "X7"  
NB8M-GT X0110 "X6"

CRYSTAL(NB8X)  
0 (27M Hz)  
1 (Reserved)

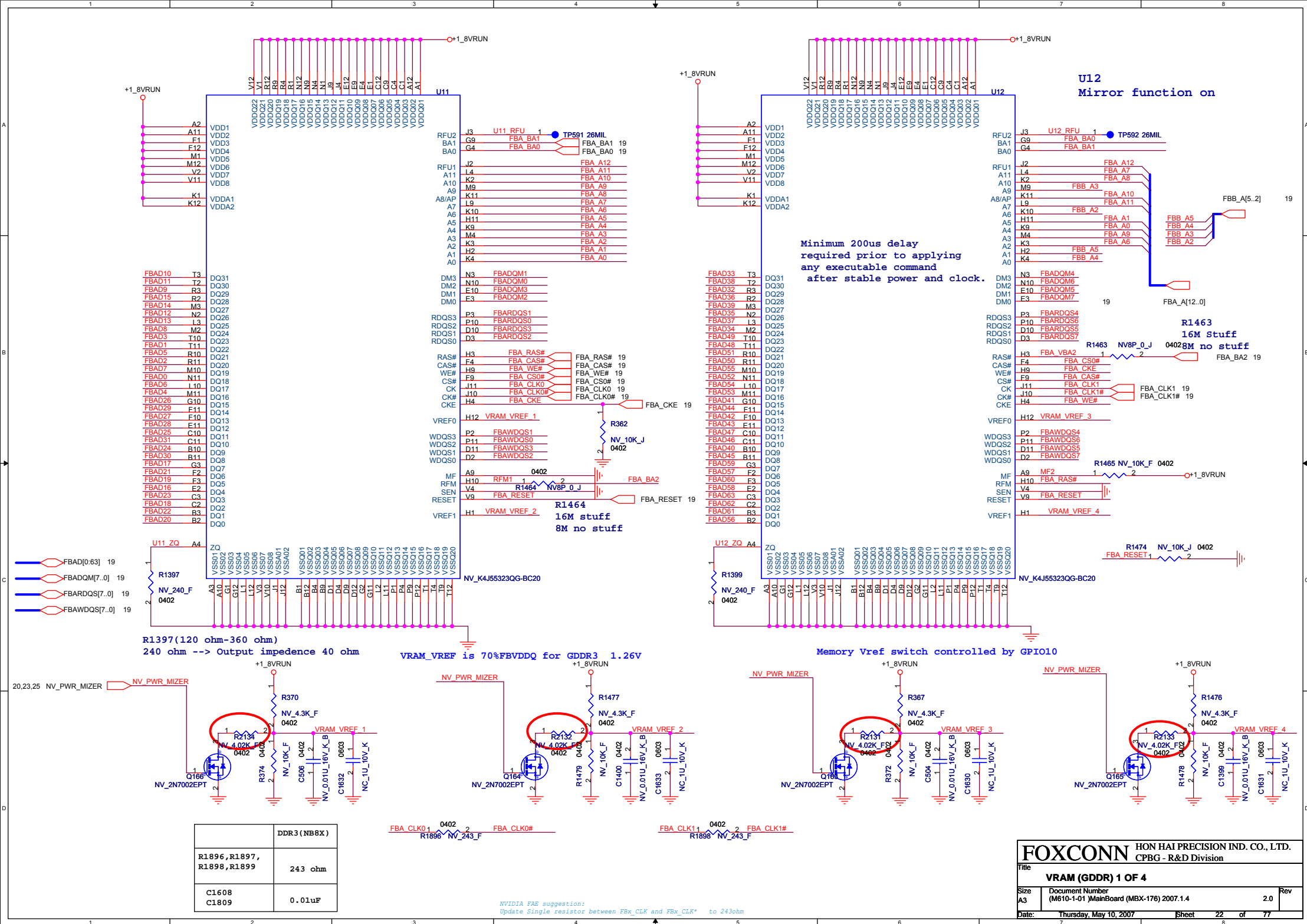


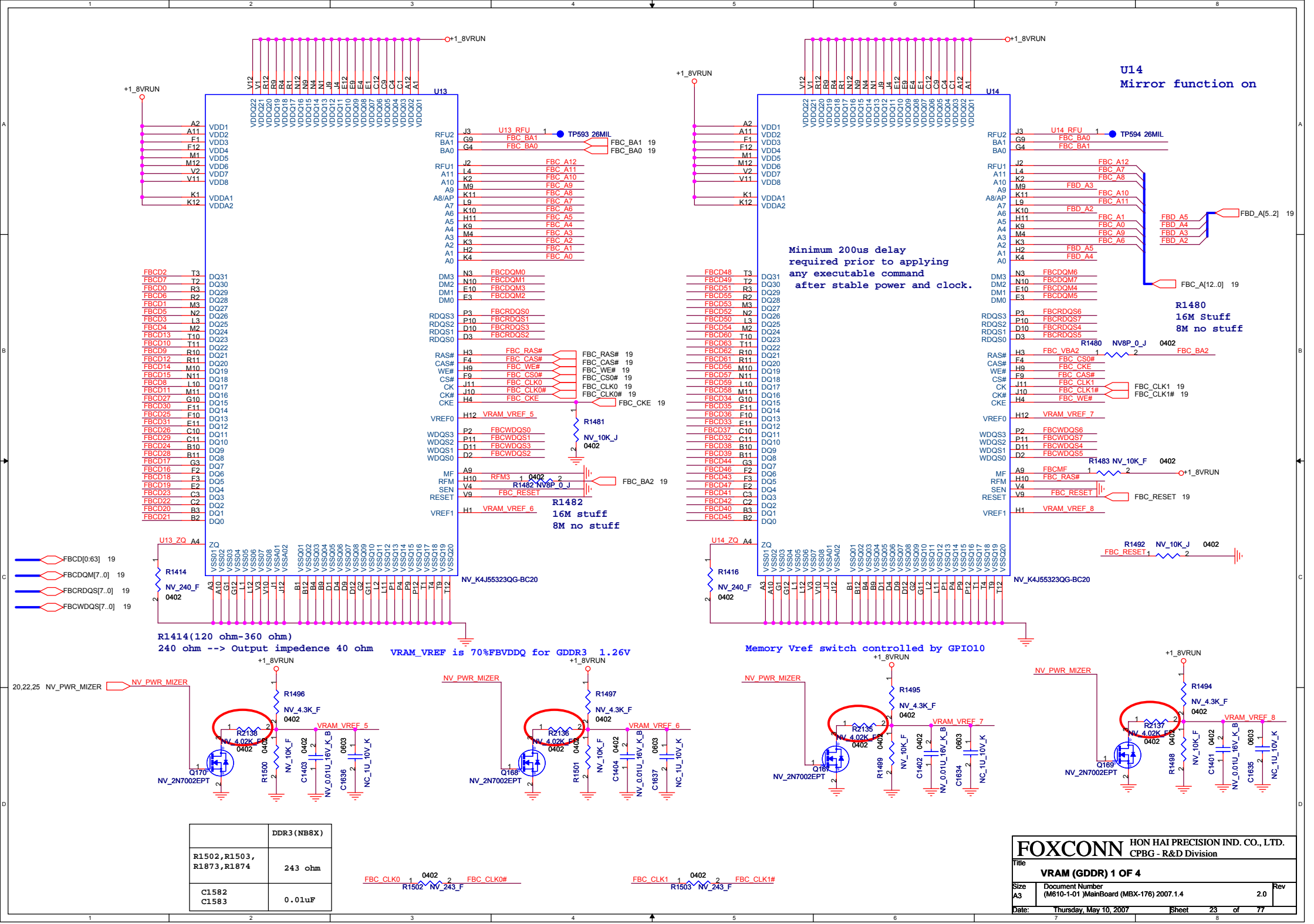










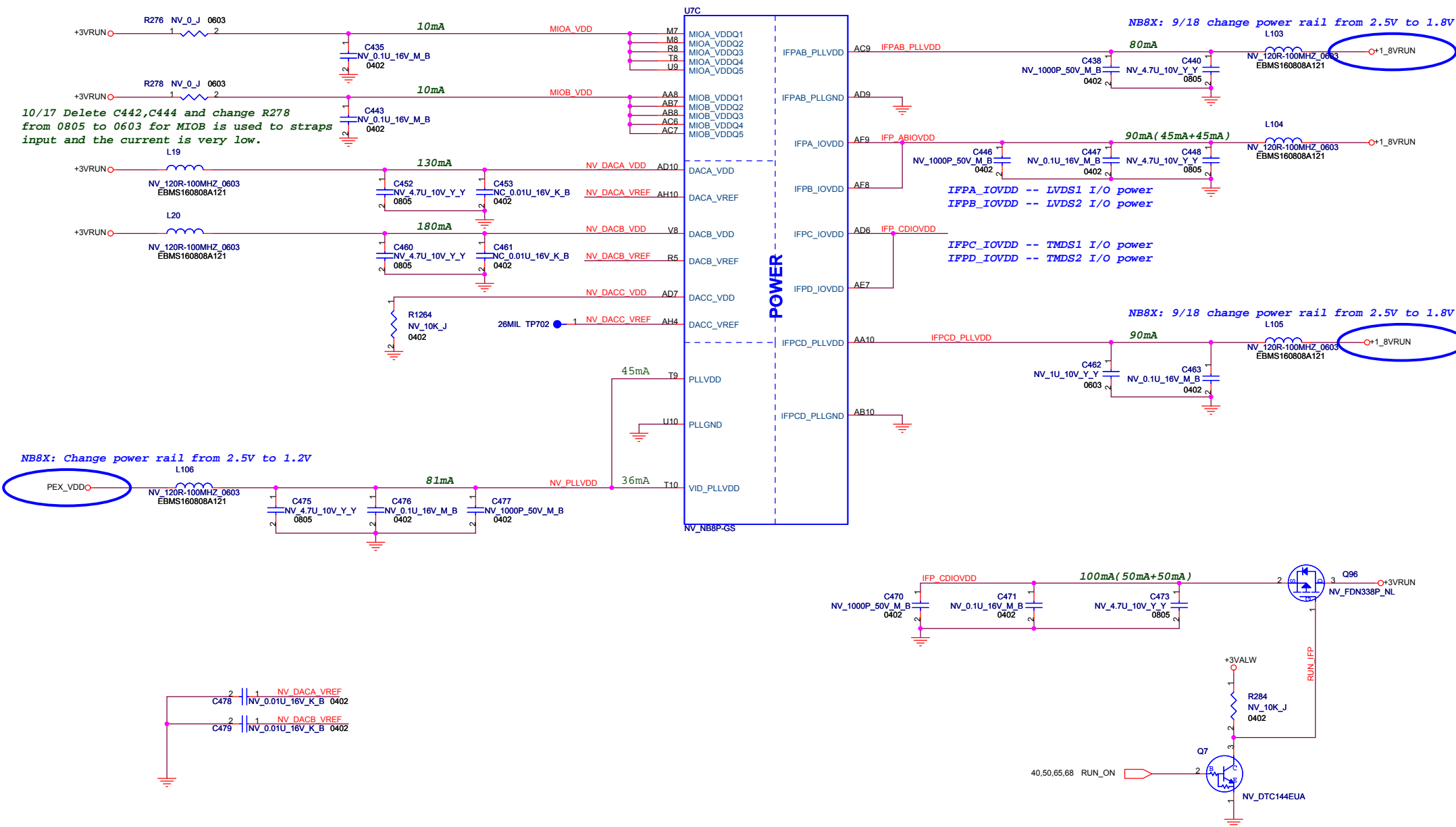


10/17 Delete C442,C444 and change R278 from 0805 to 0603 for MIOB is used to straps input and the current is very low.

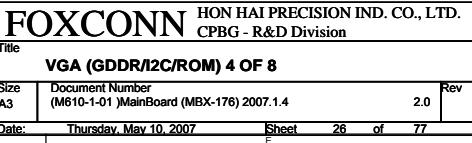
NB8X: Change power rail from 2.5V to 1.2V

NB8X: 9/18 change power rail from 2.5V to 1.8V

NB8X: 9/18 change power rail from 2.5V to 1.8V



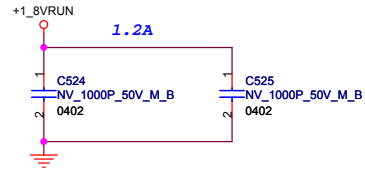
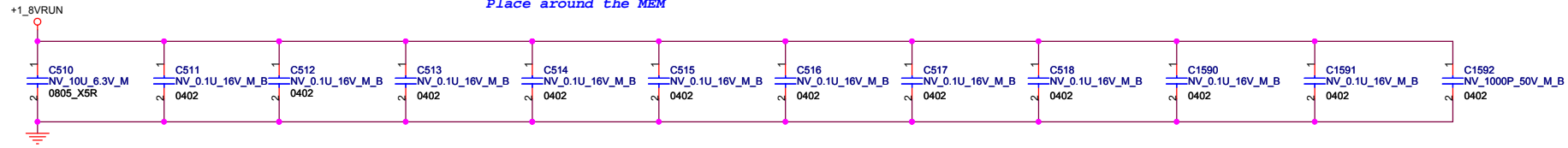






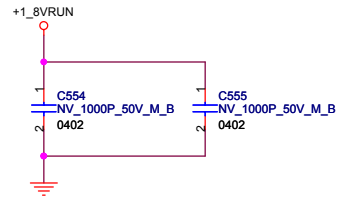
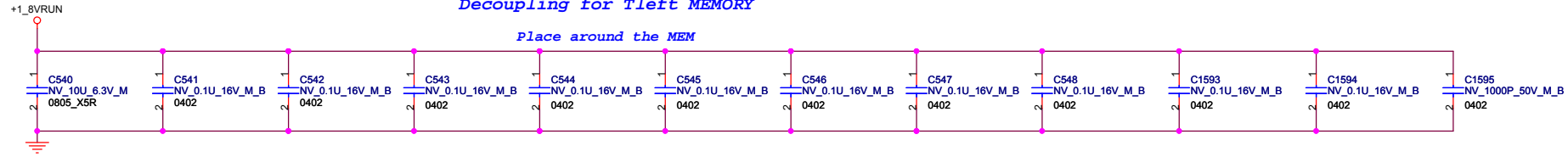
## Decoupling for Tright MEMORY

Place around the MEM



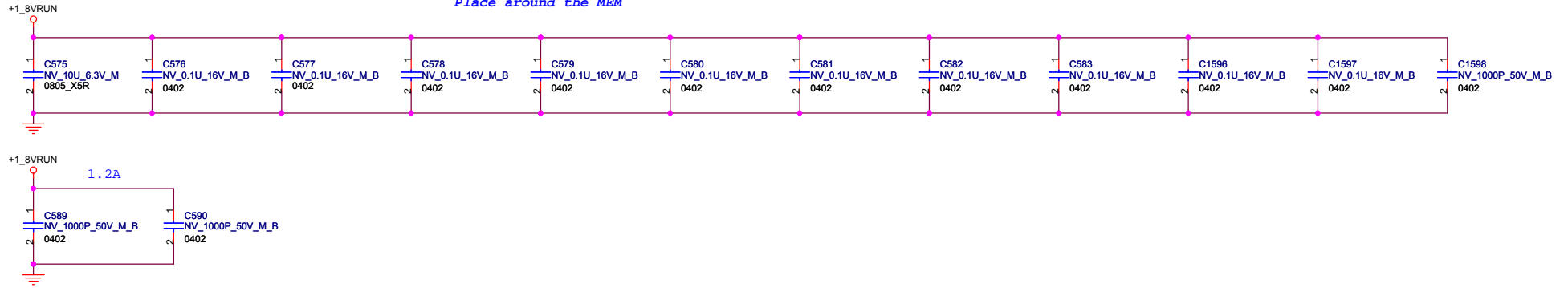
## Decoupling for Tleft MEMORY

Place around the MEM



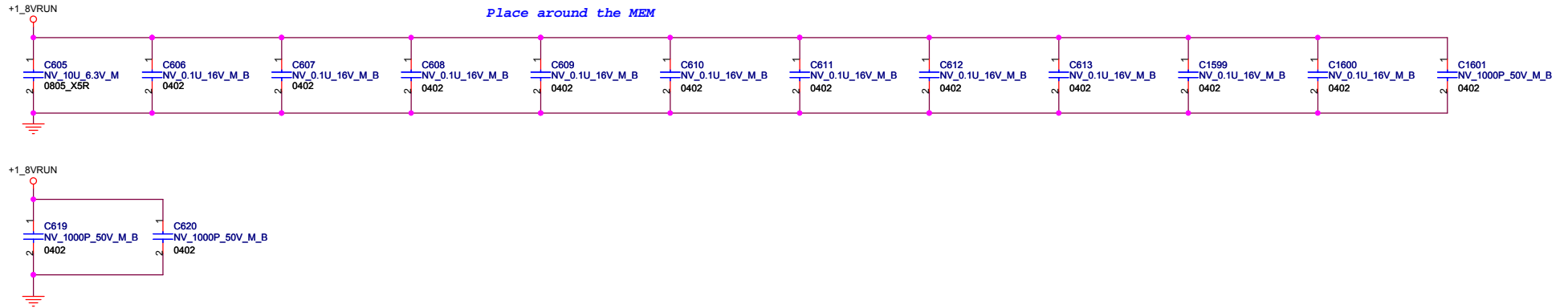
### Decoupling for Bright MEMORY

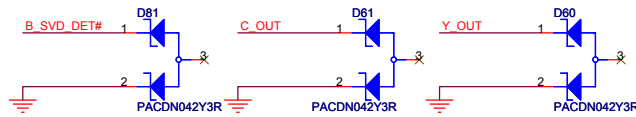
Place around the MEM



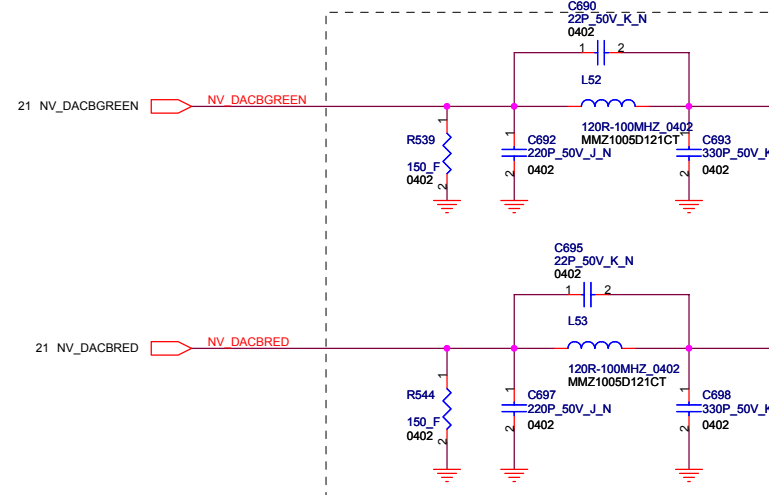
### Decoupling for Bleft MEMORY

Place around the MEM

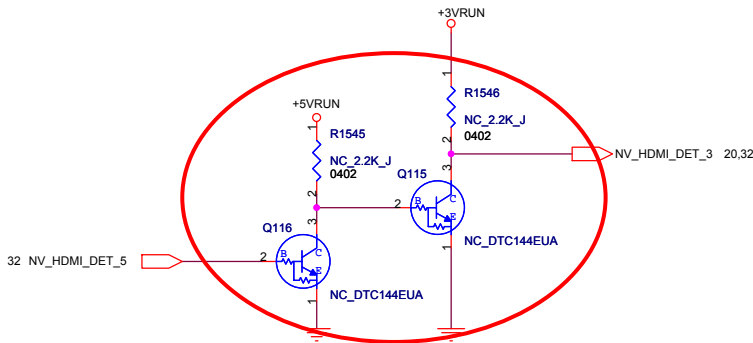
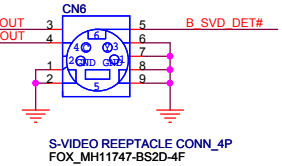




These component close to S-Video connector within 700 mil

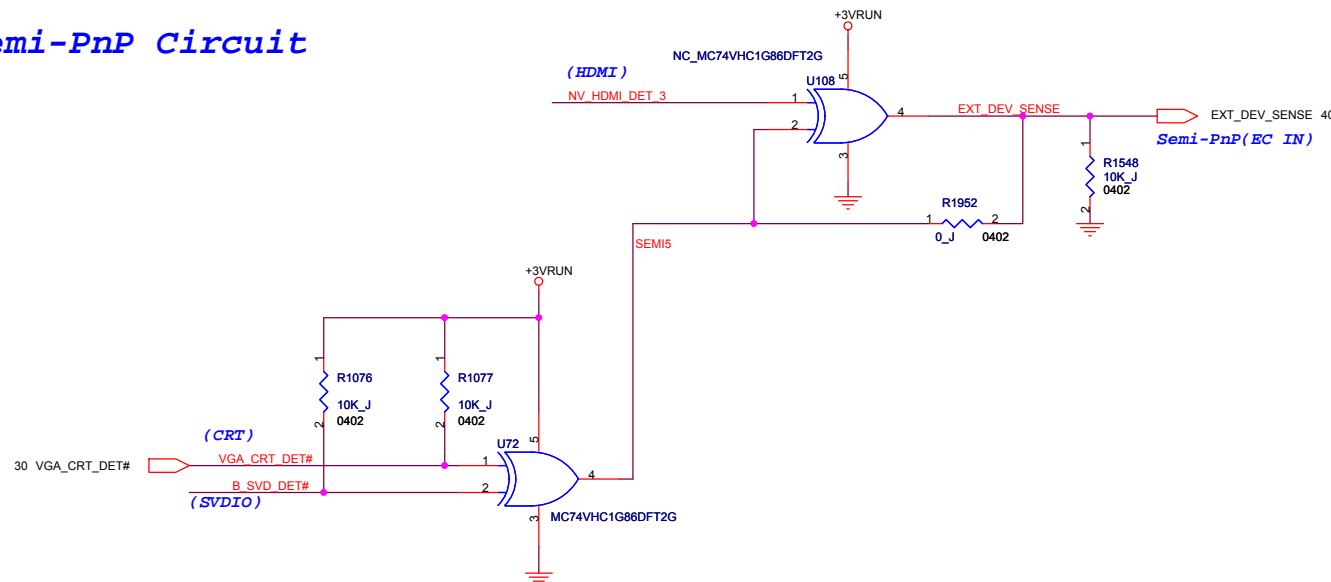


## S-VIDEO CONNECTOR

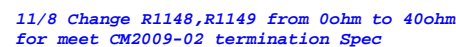


PS101 HPD has level shift function, so backup this circuit  
Change Q115, Q116, R1545, R1546 to NC

## Semi-PnP Circuit

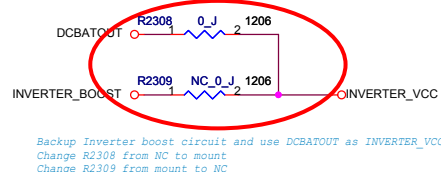
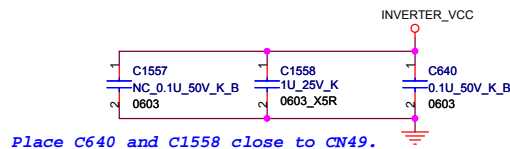


FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
Title			
S-VIDEO/Semi-PnP			
Size	Document Number	Rev	
A3	(M610-1-01 )MainBoard (MBX-176) 2007.1.4	2.0	
Date:	Thursday, May 10, 2007	Sheet	29 of 77

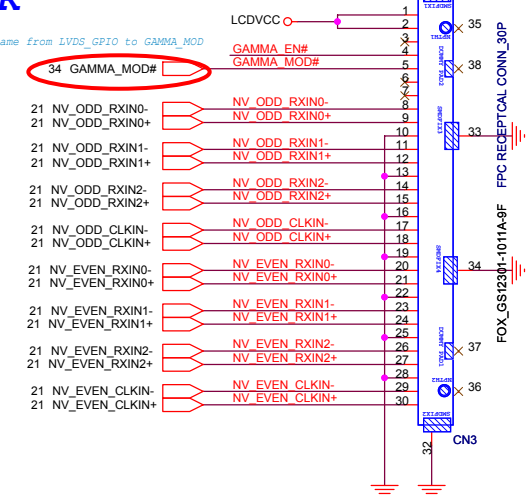
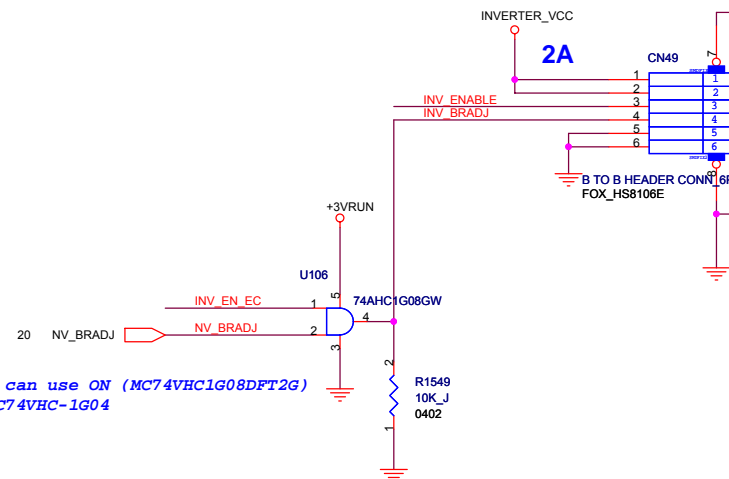


# LVDS CONNECTOR

## INVERTER CONNECTOR

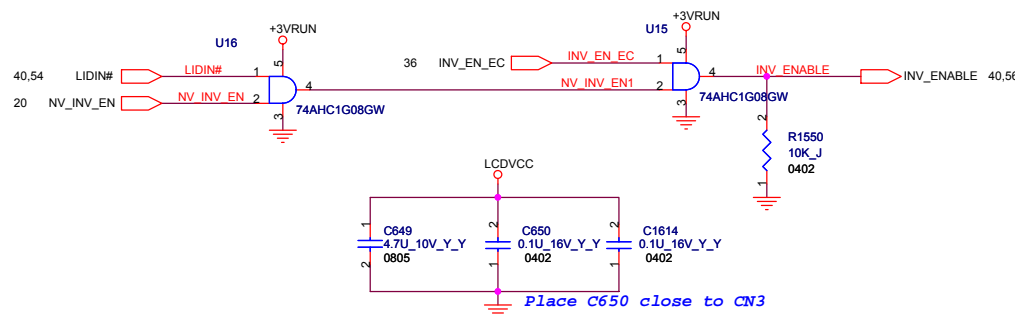


U106,U15,U16 can use ON (MC74VHC1G08DFT2G)  
H.H. PN:14-MC74VHC-1G04

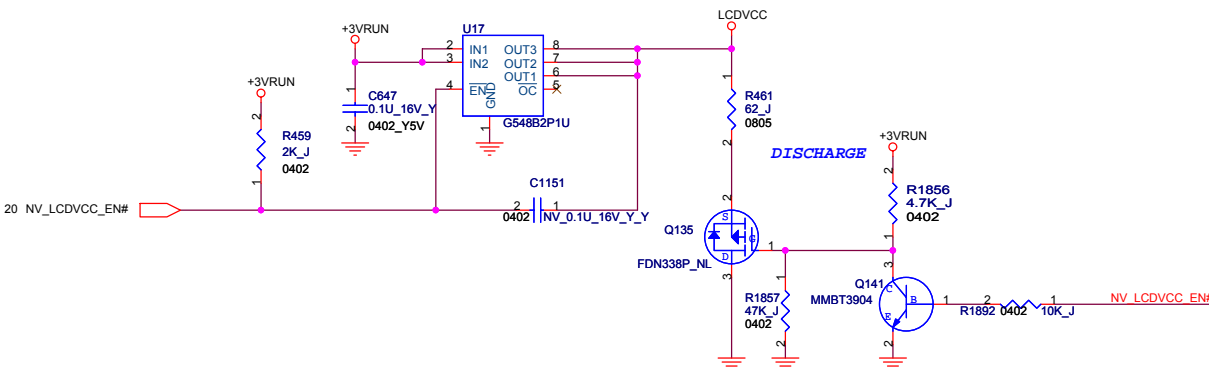


Use H/W selection to enable GAMMA function.  
Change R1937,R1938 from 4.7K to 0ohm

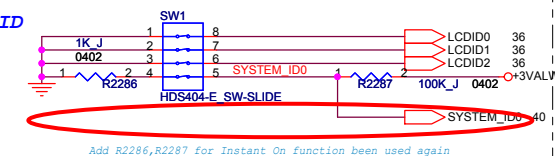
H: GAMMA Disable  
L: GAMMA Enable



Current limit is from 1.1A to 2.1A.



## PANEL ID



Type	WXGA+	WXGA+	WUXGA	WUXGA
Size	17" wide	17" wide	17" wide	17" wide
Vender	LG.PHILIPS	LG.PHILIPS	SHARP	SHARP
Device Name	LPI171WP74-TLA	LPI171WP74-TLA	LQ170M11LA4G	LQ170M11LA4G
Panel ID Check[2..0]	010	001	100	101

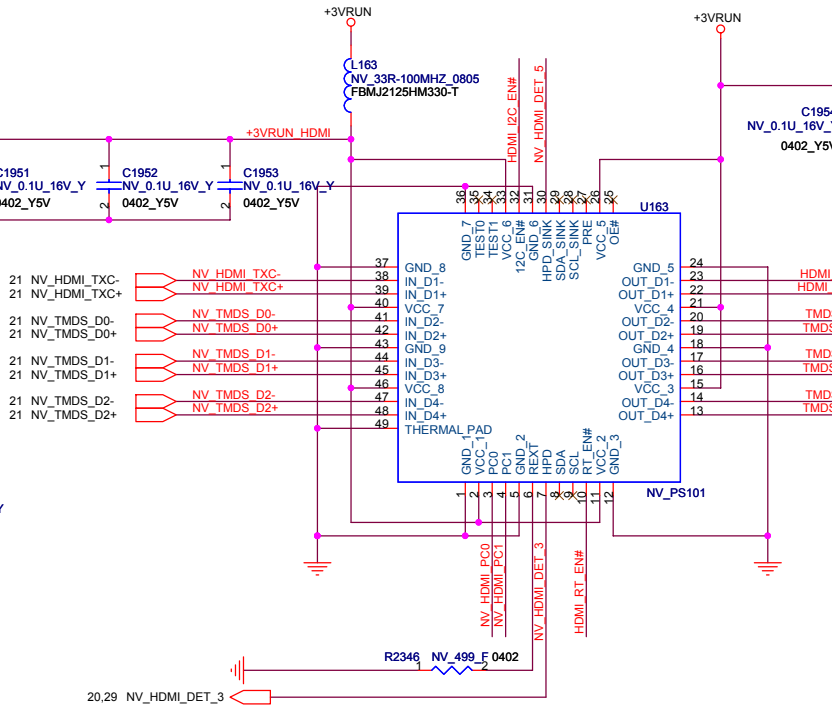
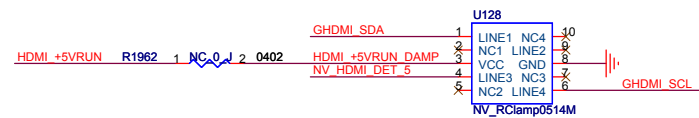
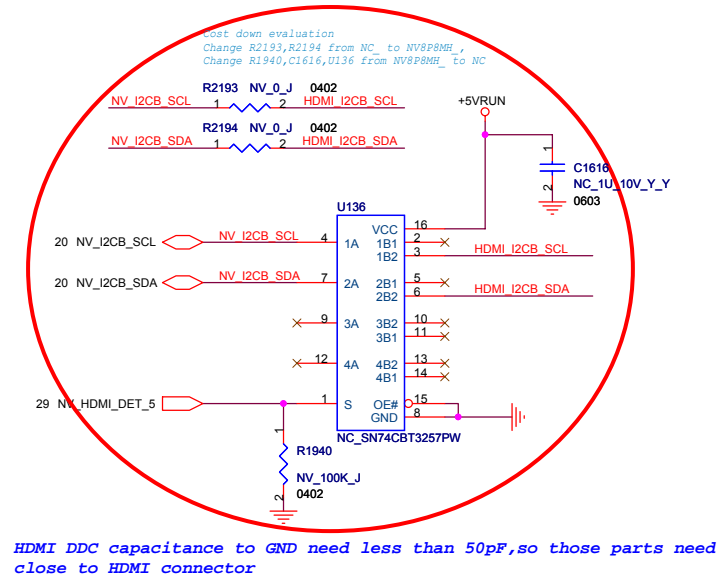
FOXCONN HON HAI PRECISION IND. CO., LTD.  
CPBG - R&D Division

Title  
LVDS

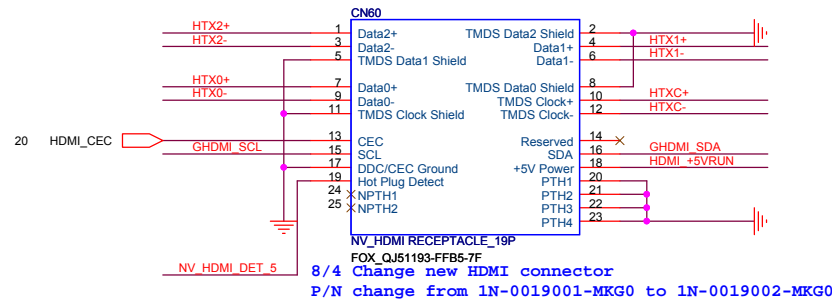
Size A3 Document Number (M610-1-01 )MainBoard (MBX-176) 2007.1.4 2.0 Rev

Date: Thursday, May 10, 2007 Sheet 31 of 77

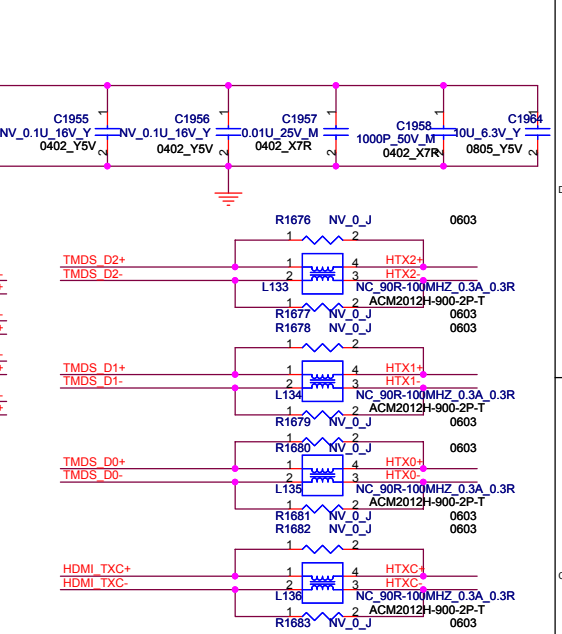
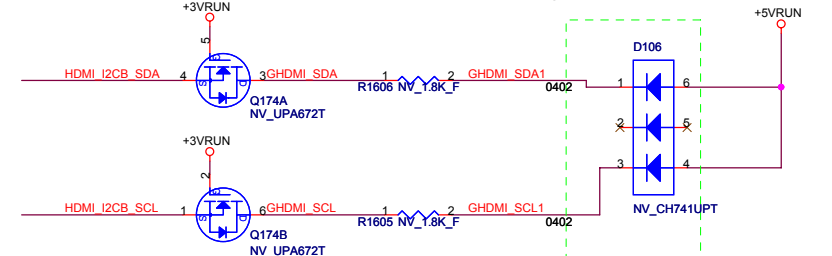
(TMDS inputs equalization control)  
PC1,PC0 Configuration  
00: 8 dB,  
01: 4 dB,  
10: 12 dB,  
11: 0 dB



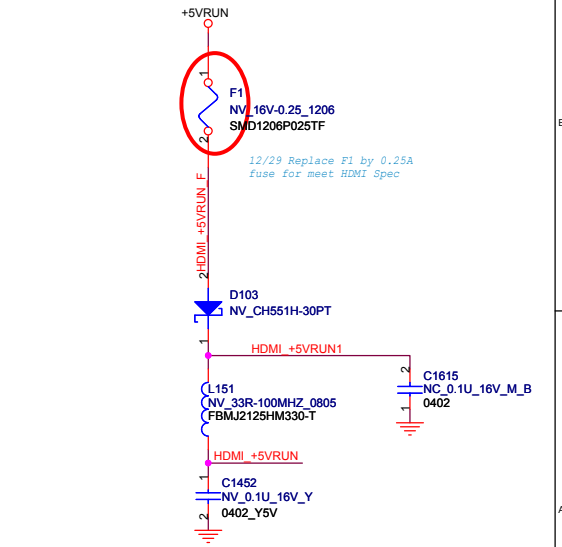
## HDMI CONNECTOR



## PVT Change to 16-CH741UP-T000



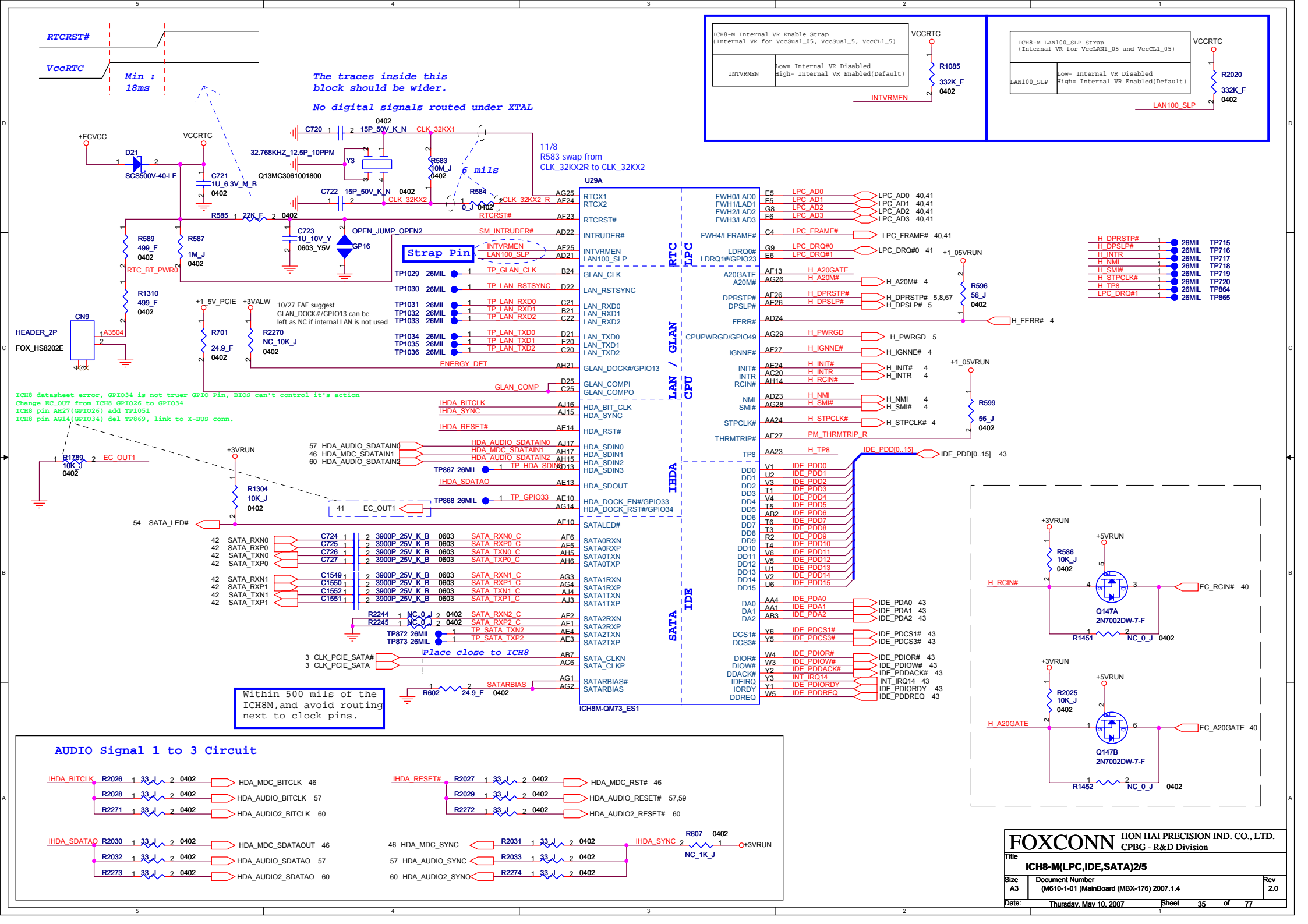
Data line capacitance to GND need less than 10pF, so those parts need close to HDMI connector

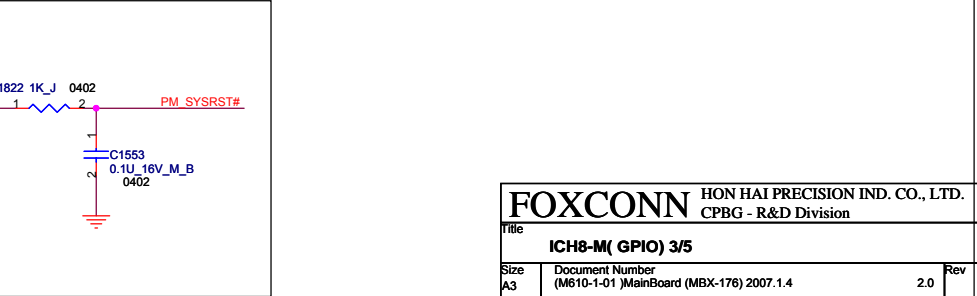
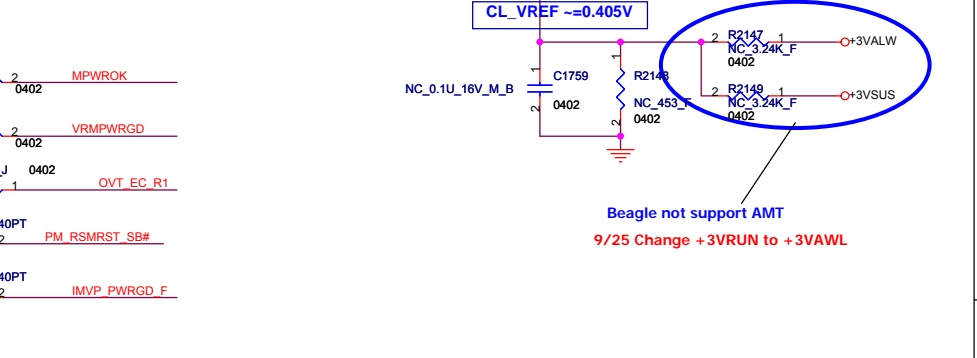
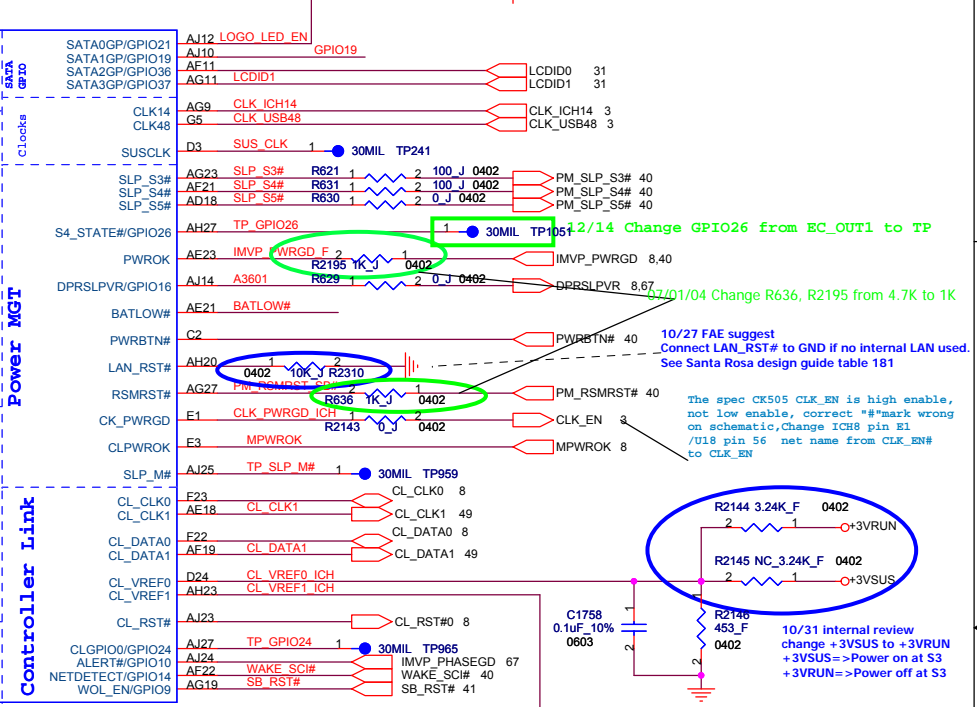
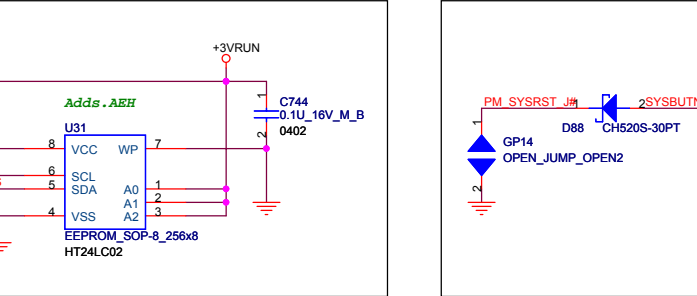
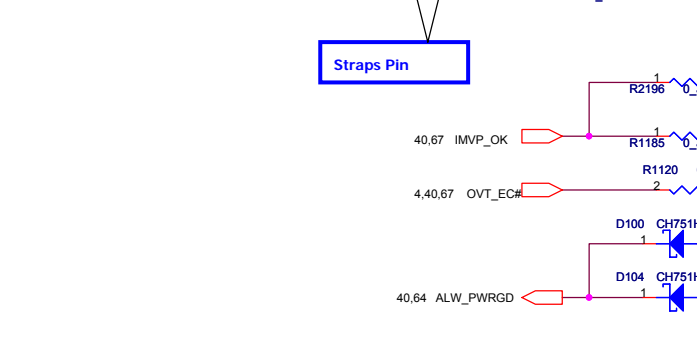
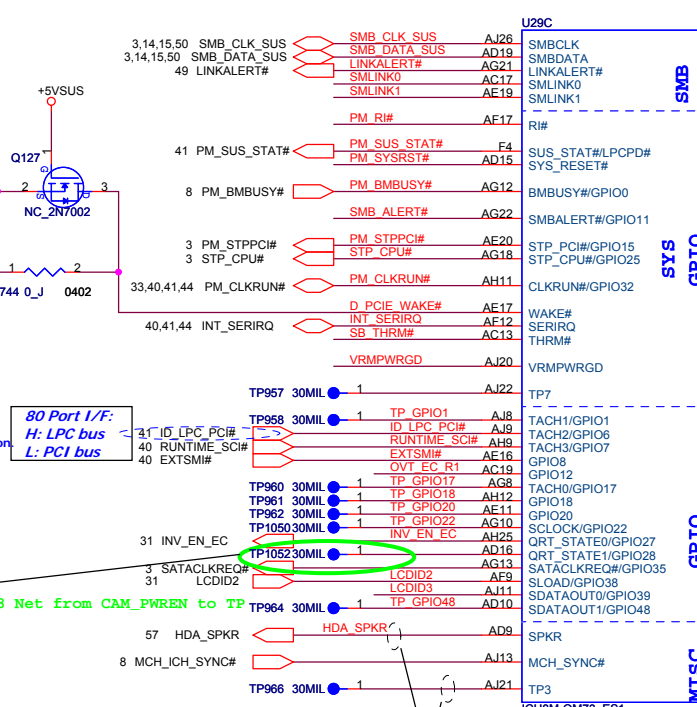
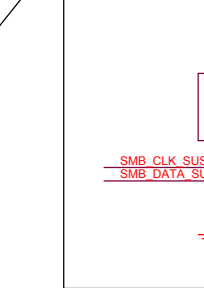
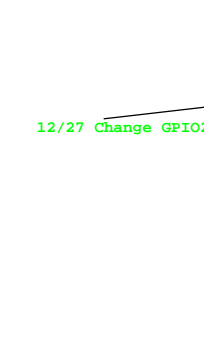
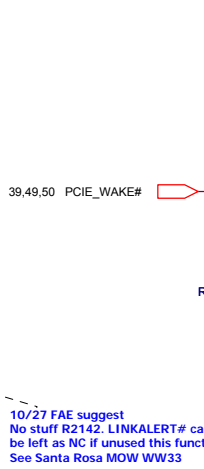
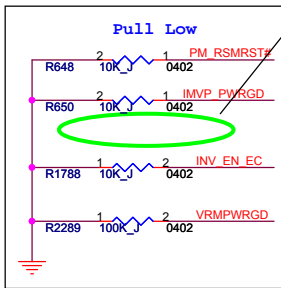
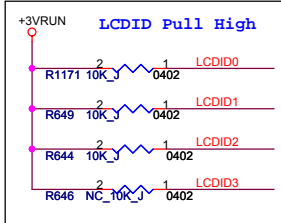
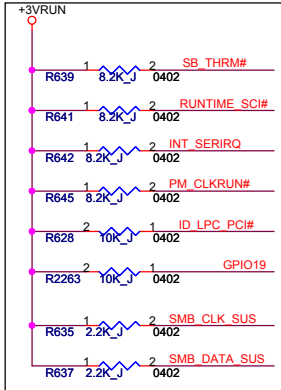
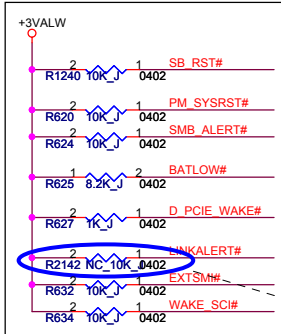
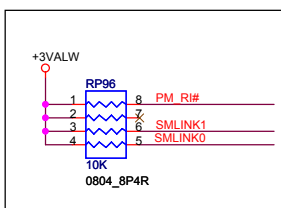


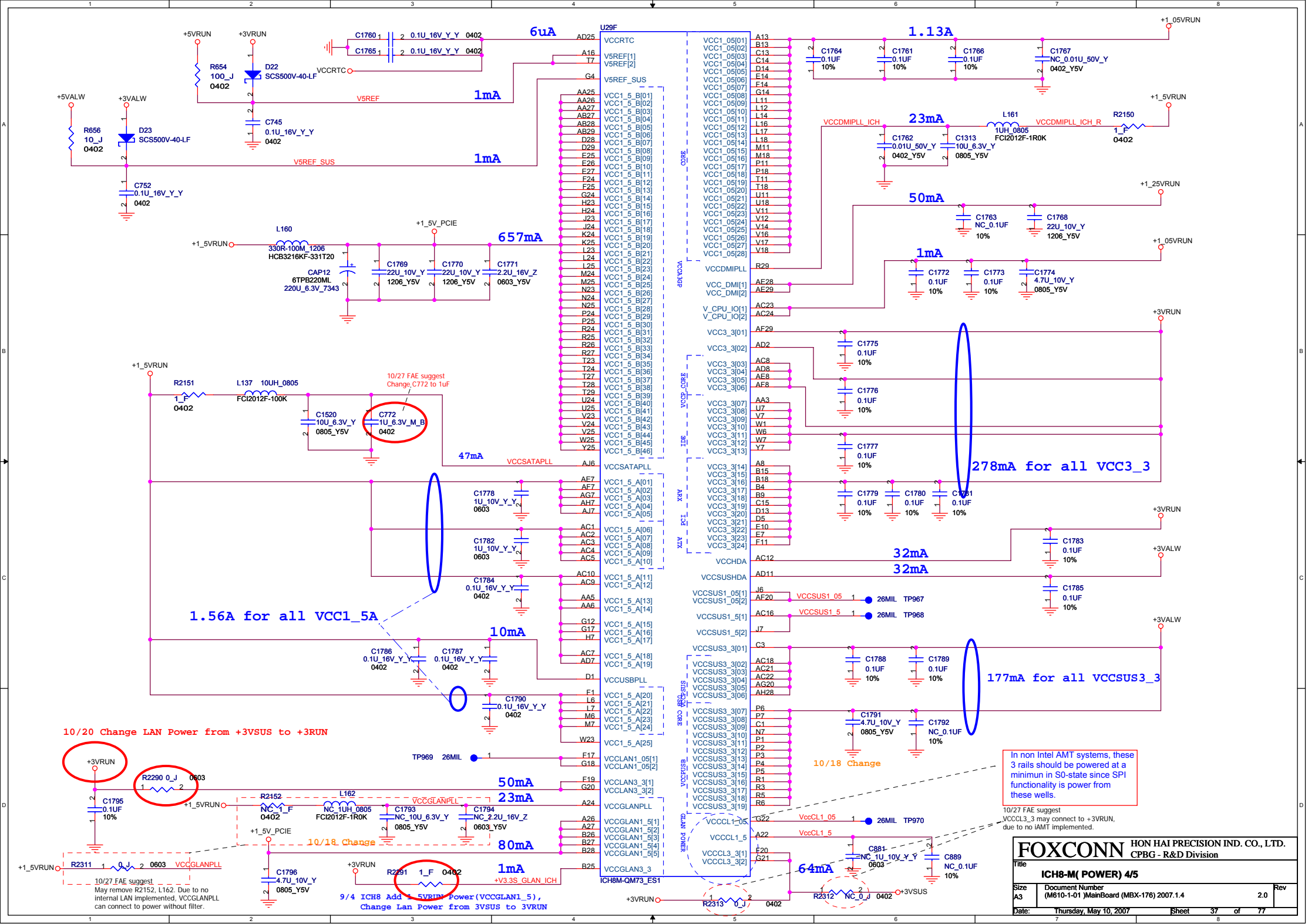




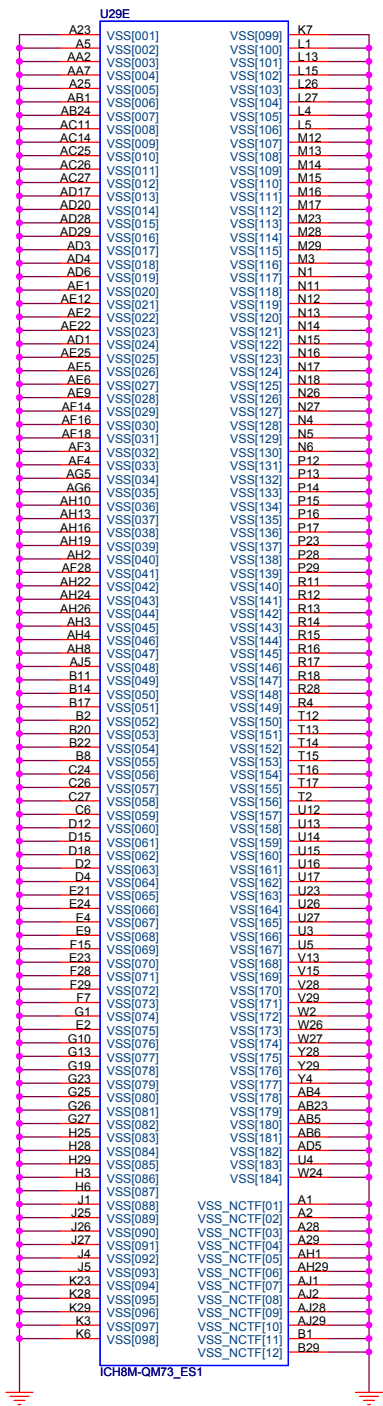






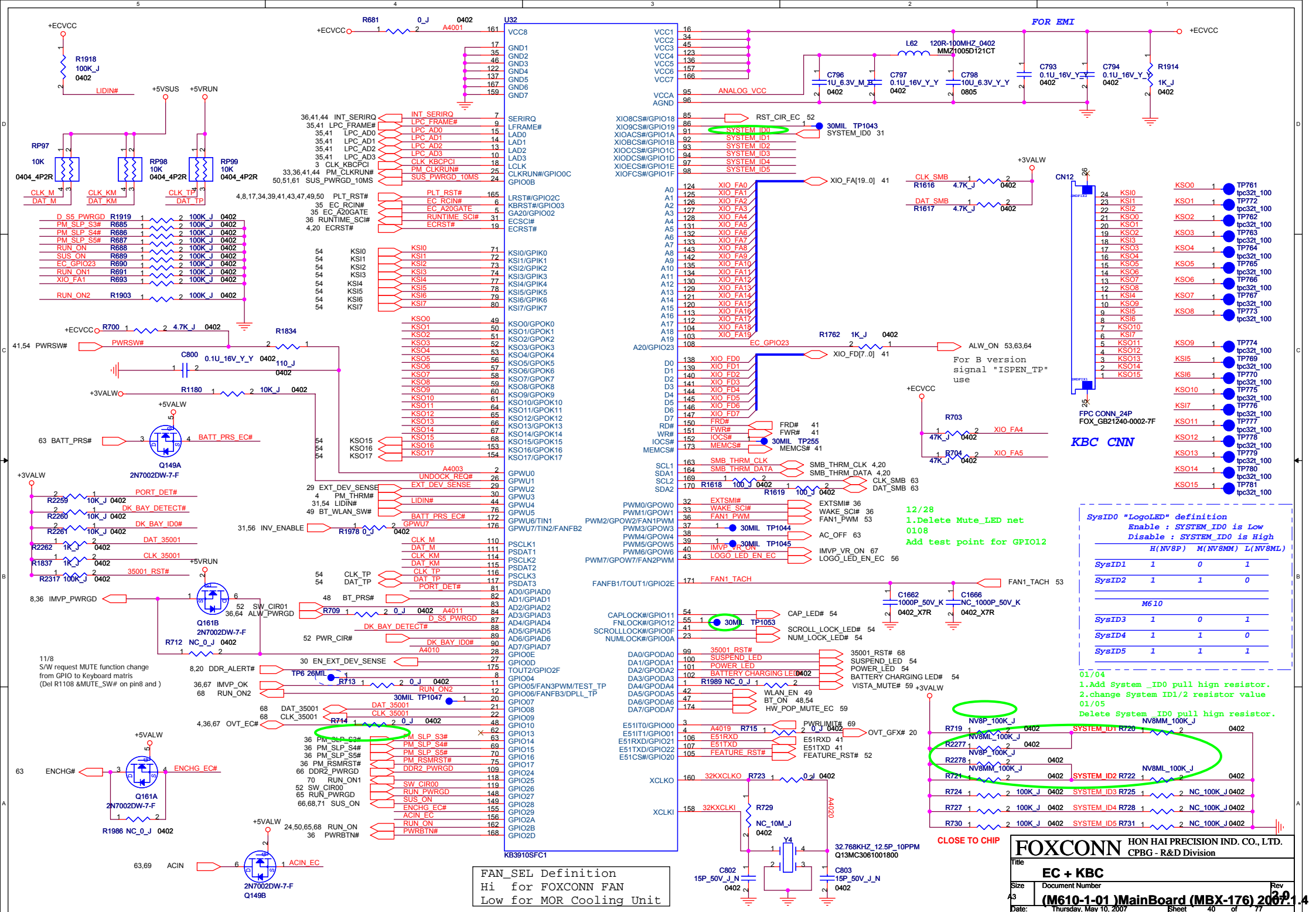












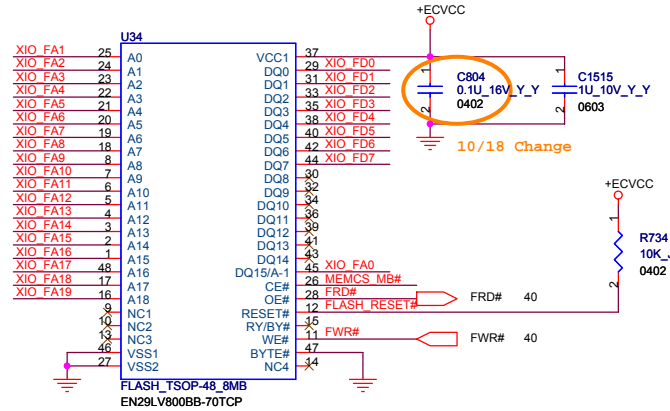
FAN\_SEL Definition  
Hi for FOXCONN FAN  
Low for MOR Cooling Unit

SysID0 "LogoLED" definition			
Enable : SYSTEM_ID0 is Low			
Disable : SYSTEM_ID0 is High			
	H(NV8P)	M(NV8MM)	L(NV8ML)
SysID1	1	0	1
SysID2	1	1	0
M610			
SysID3	1	0	1
SysID4	1	1	0
SysID5	1	1	1

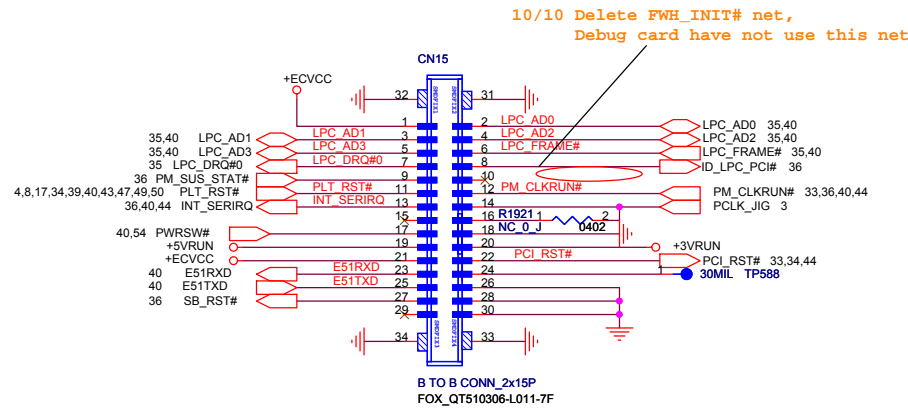
- 01/04  
1. Add System\_ID0 pull high resistor.  
2. change System\_ID1/2 resistor value  
01/05  
Delete System\_ID0 pull high resistor.

# FLASH BIOS

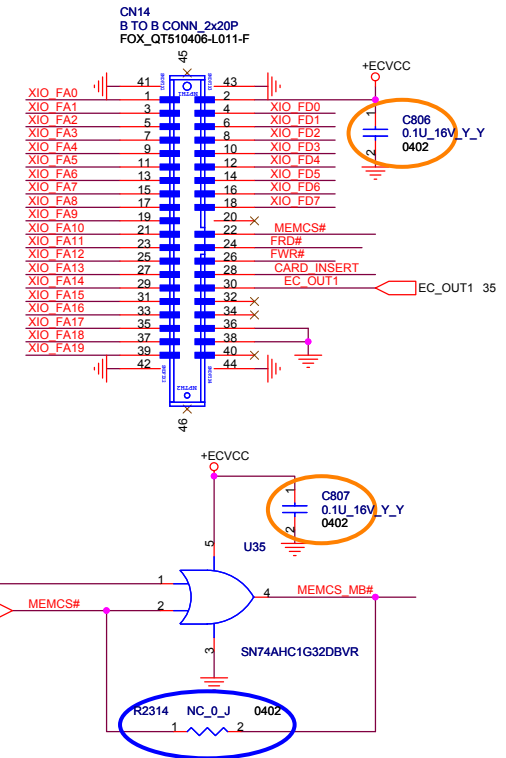
40 XIO\_FA[19..0]  
40 XIO\_FD[7..0]

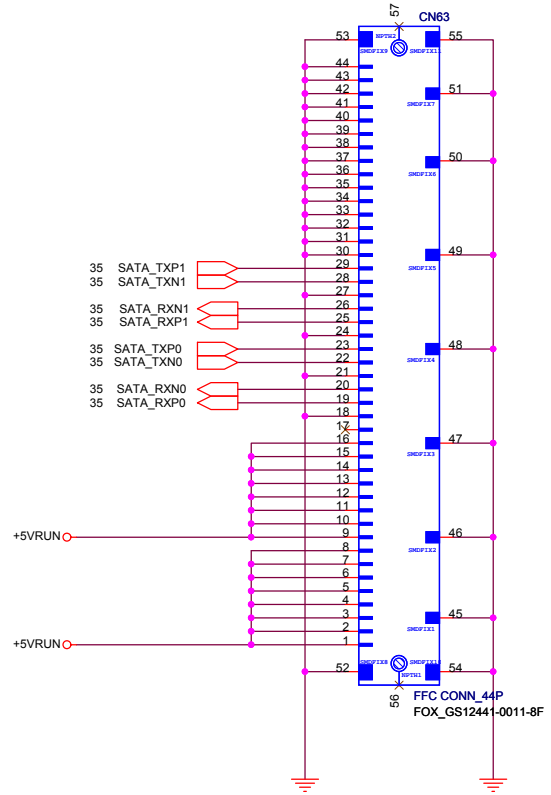
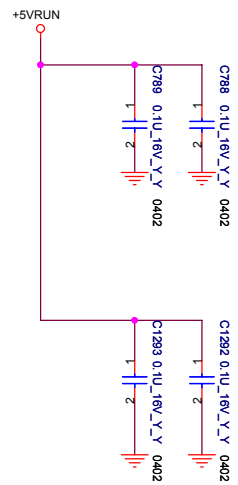


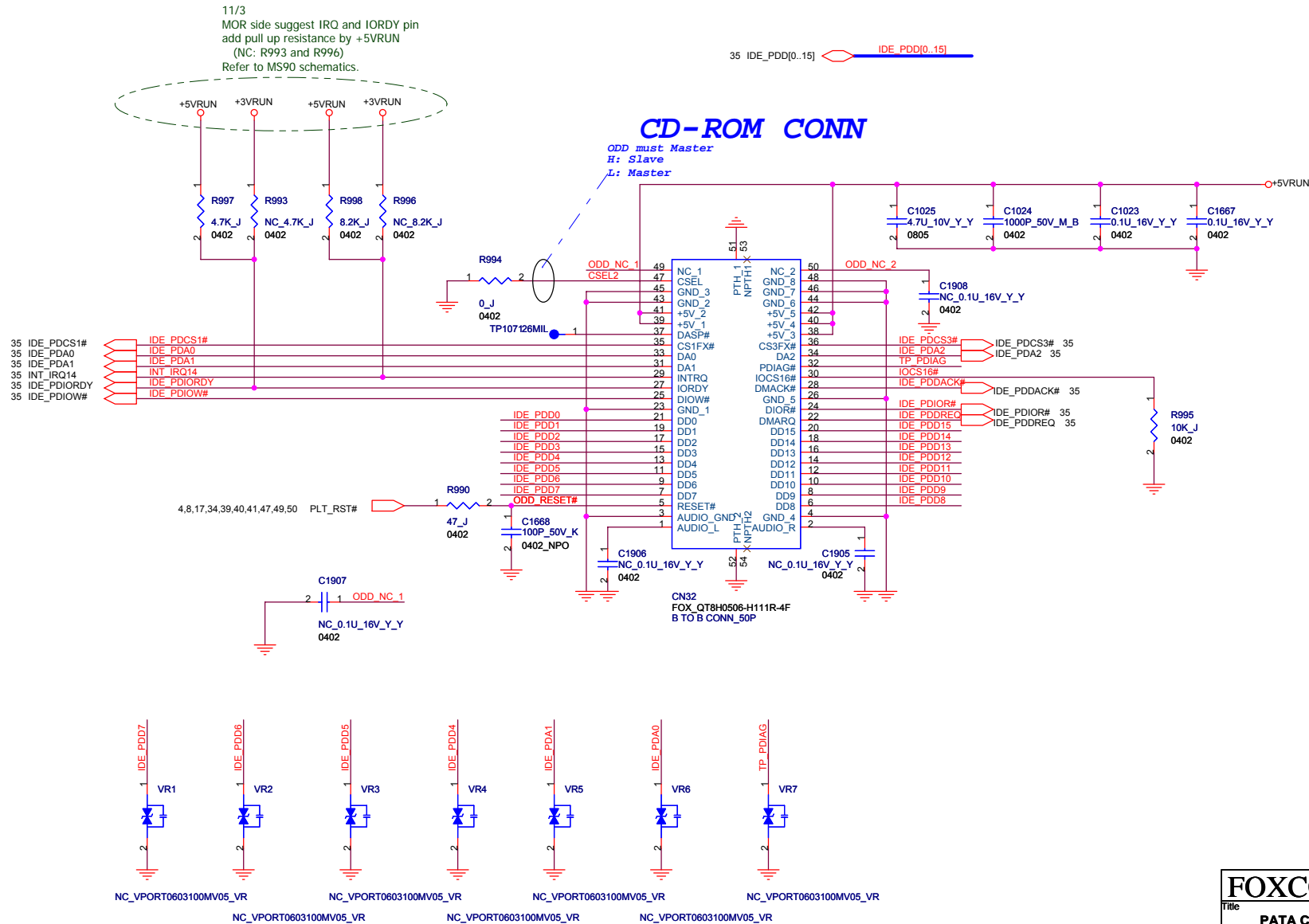
# JIG-120



# X-BUS







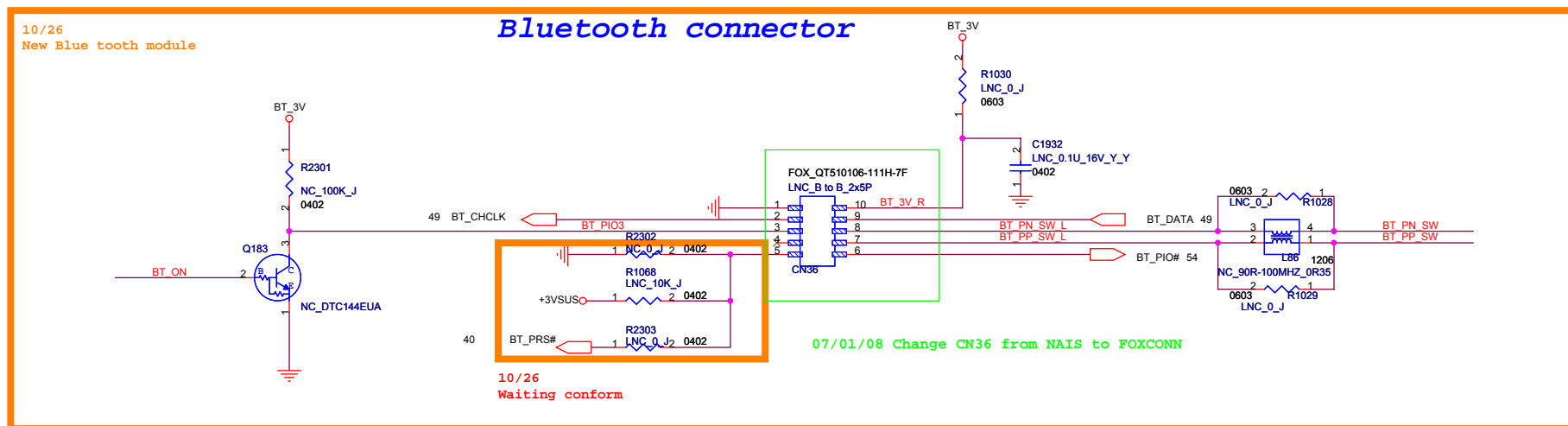
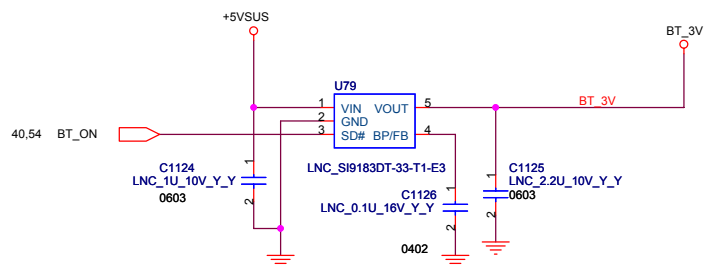








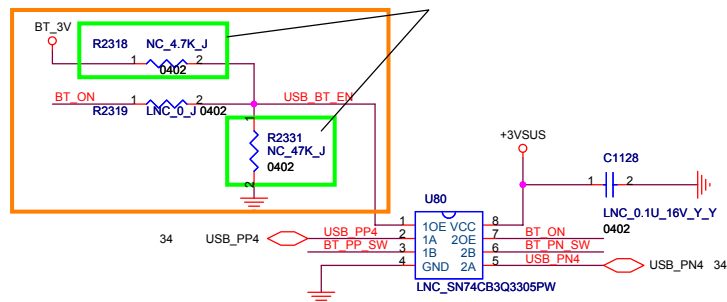




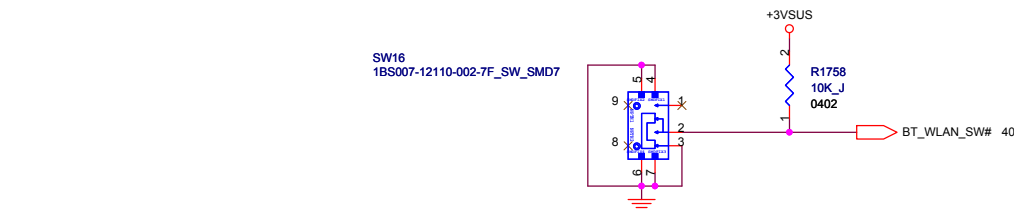
11/04 Change U80 Enable from BT\_ON to BT\_3V  
 U79 LDO Ton Max is 1000us  
 U80 BUS Switch Ton Max is 5ns

12/27 Change Bluetooth circuit Value to LNC\_\* for M610 DVT I SKU

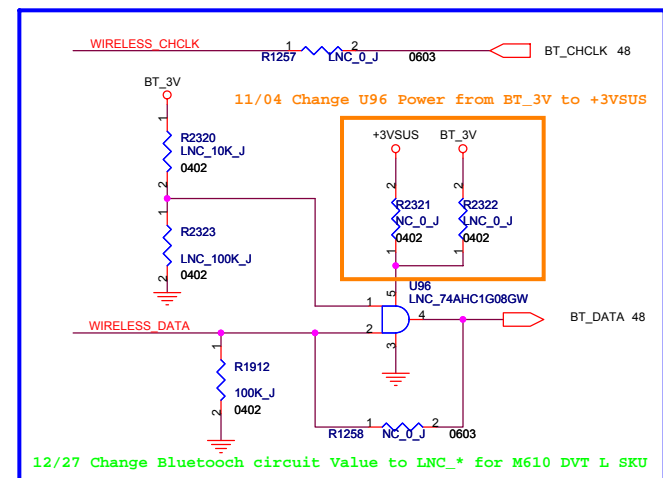
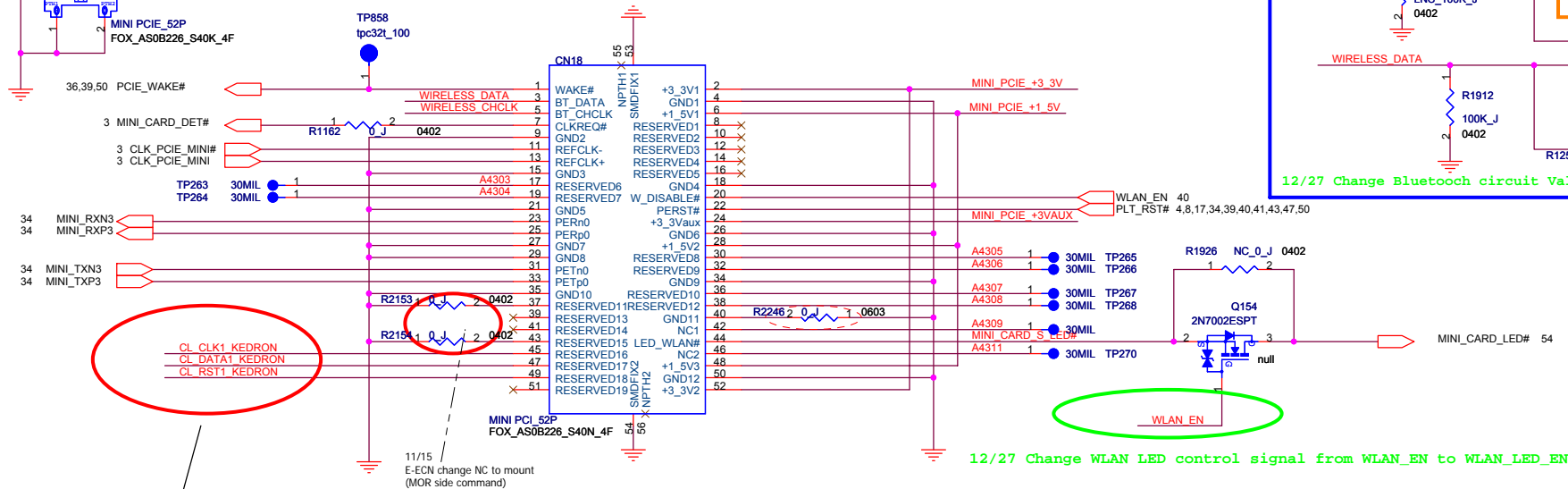
12/14 Change R2318 from 1K to 4.7K, Add one 47K pull up resistance



To solve U80 enable pin (net name USB\_BT\_EN) floating during U79 (BT\_3V from LDO )BT\_ON disable,  
 Add Pull low 47K(R2331) at net USB\_BT\_EN, Change R2318 from 10K to 1K.

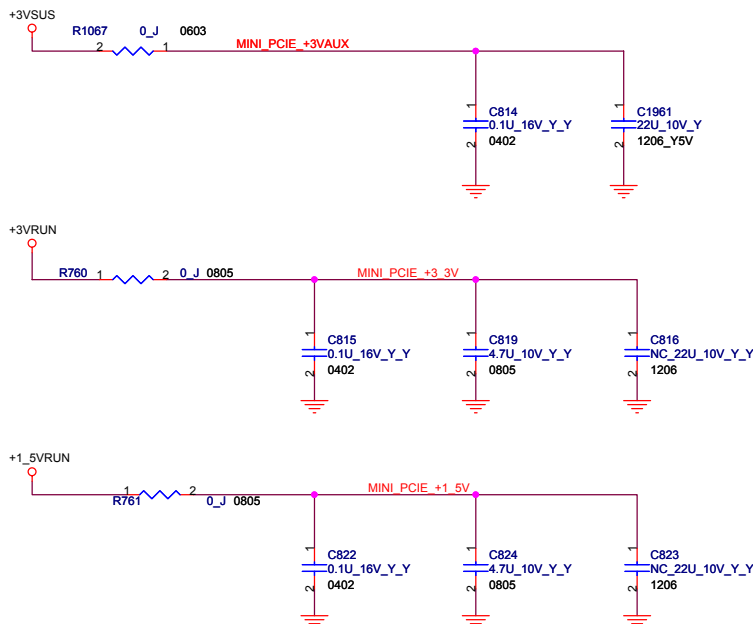
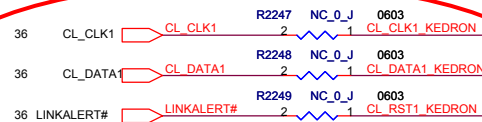


## Mini-PCIE Card connector

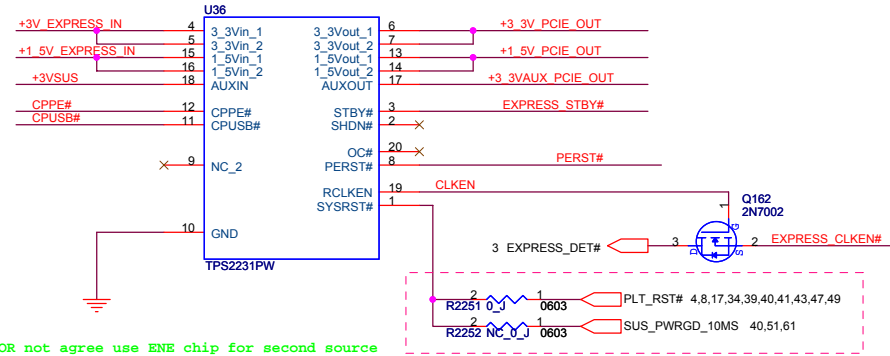


12/27 Change WLAN LED control signal from WLAN\_EN to WLAN\_LED\_EN

10/27 FAE suggest CL\_CLK1/CL\_DATA1/CL\_VREF1 can be left as NC if unused iAMT. Don't need to connect to WLAN card.



VOLTAGE INPUTS <sup>(1)</sup>			LOGIC INPUTS			VOLTAGE OUTPUTS <sup>(2)</sup>			MODE <sup>(3)</sup>
AUXIN	3.3VIN	1.5VIN	STBY	STBY	CP <sup>(4)</sup>	AUXOUT	3.3VOUT	1.5VOUT	
Off	x	x	x	x	x	Off	Off	Off	OFF
On	x	x	0	x	x	GND	GND	GND	Shutdown
On	x	x	1	x	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On	On	1	1	0	On	On	On	Card Inserted

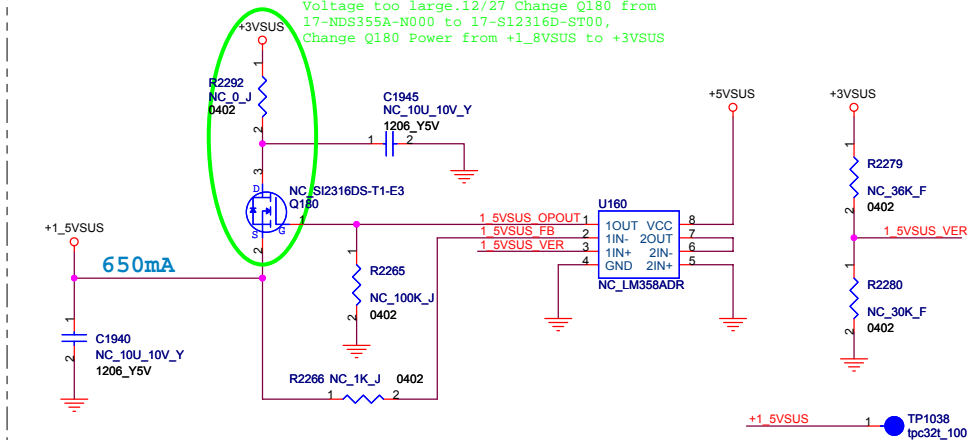


MOR not agree use ENE chip for second source  
Change Express Card Power Switch (U36) from ENE P2231TF to TI TPS2231PW

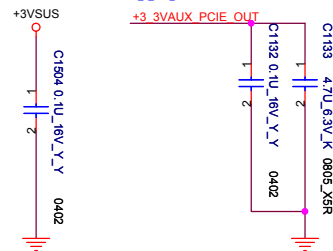


## Constant-voltage +1\_5VSUS

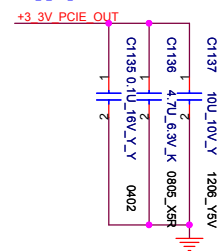
12/29 Load current test fial, 1.8V transfer 1.5V drop  
Voltage too large.12/27 Change Q180 from  
17-NDS355A-N000 to 17-S12316D-ST00,  
Change Q180 Power from +1\_8VSUS to +3VSUS



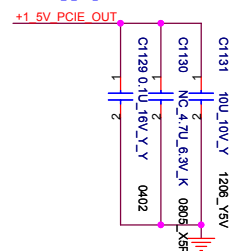
Supply Max 275mA



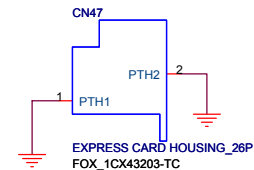
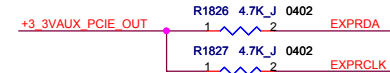
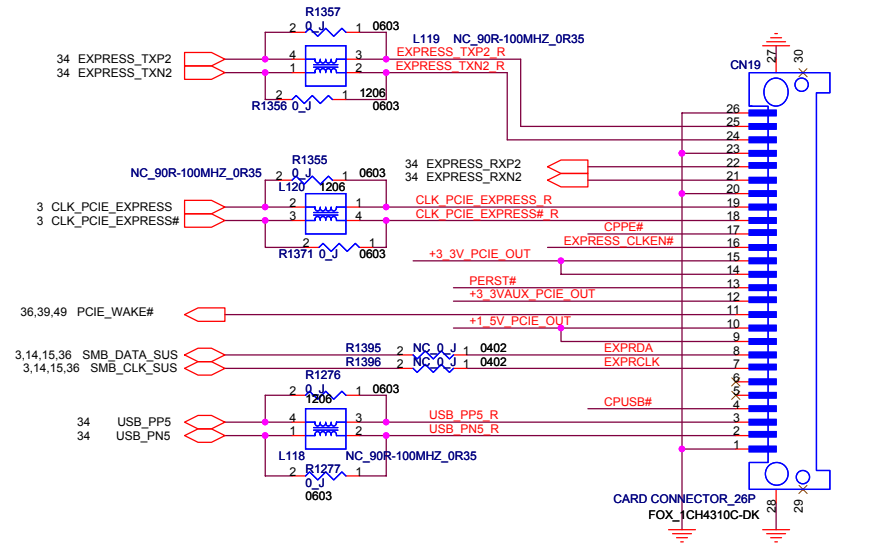
Supply Max 1300mA



Supply Max 650mA

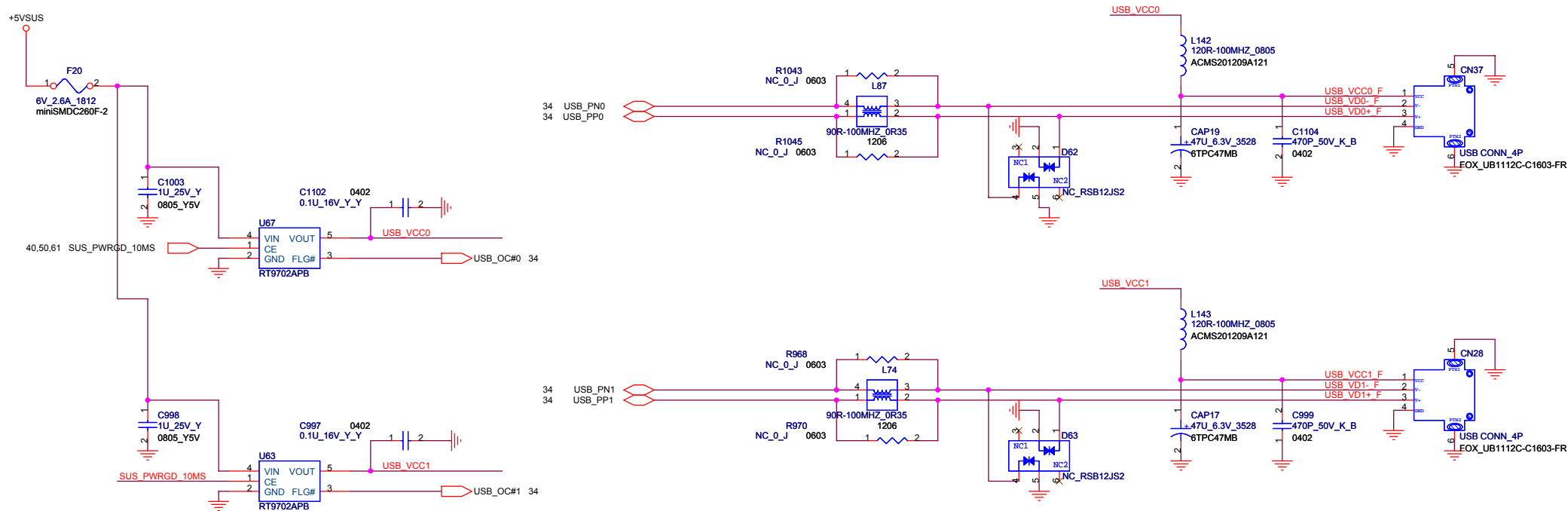


## EXPRESS Card



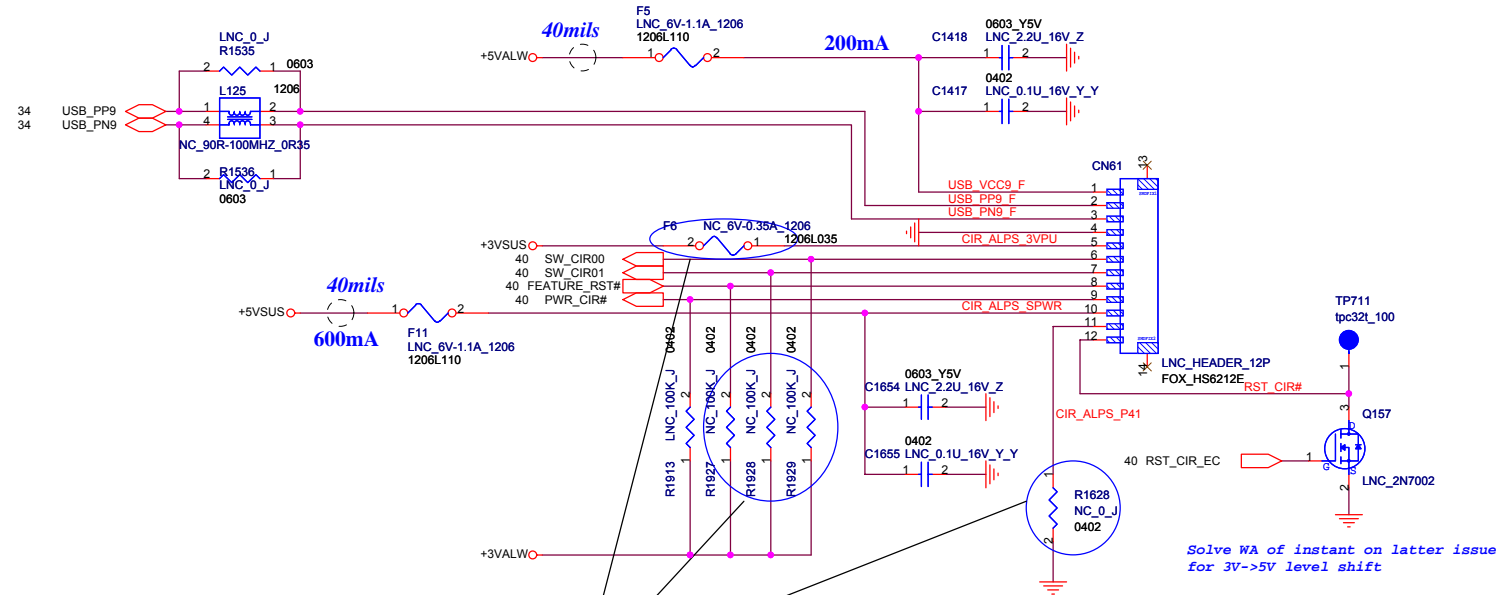
FOXCONN		HON HAI PRECISION IND. CO., LTD.	
EXPRESS CARD		CPBG - R&D Division	
Size	Document Number	Rev	
A3	(M610-1-01) MainBoard (MBX-176) 2007.1.4	2.0	
Date:	Thursday, May 10, 2007	Sheet	50 of 77

**USB connector \*2**





# IR Rreceiver connector



Button		SW1	SW0
VAIO button	Kick Instant On	L	L
Green button	Kick Windows	L	H
Shortcut button	Kick Windows	H	L
Standby button	Kick Windows	H	H

Num	Signal Name	I/O	Comment	Difference from ALPS.
1	+5VALW	VCC		<-
2	USB+	I/O		<-
3	USB-	I/O		<-
4	GND	GND		<-
5	+3VSUS	-	Not for use. Because SMK's IC use internal pull up resistor for D-.	ALPS's IC use this signal as a pull up plane of D- for low speed detection.
6	SW0	O	Use for detecting of the remote button. 3.3V CMOS output.	3.3V open drain output.
7	SW1	O	Use for detecting of the remote button. 3.3V CMOS output.	3.3V open drain output.
8	Feature_RST#	I	Software reset signal. (3.3V internal pull up resistor.)	Use for detecting of the remote button. 3.3V open drain output.
9	PWR#	O	Power on request signal. Open drain output.	<-
10	SPWR	I	Power OK signal. 5V input.	<-
11	EN	-	Not for use.	Low: Disable instant on feature Open or High: Enable instant on feature (3.3V internal pull up resistor.)
12	Hard_RST#	I	Hardware reset.	<-

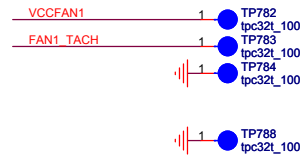
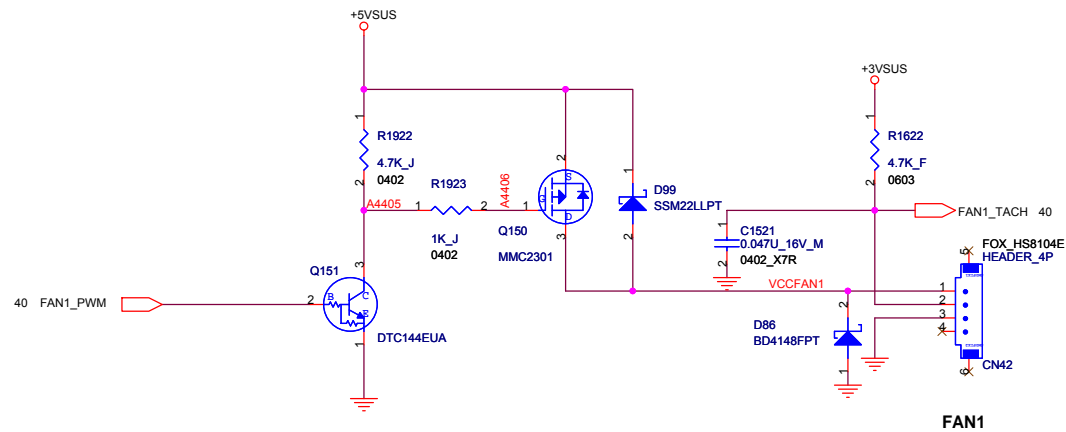
9/26 FOR NEW SMK IR module compatiy  
1.Change stuff to NC:F6,R1927,R1928,R1929,  
2.EC Page GPIO20(105),GPIAD2(83) pin swape

12/27 Change CIR circuit Value to LNC\_\* for M610 DVT L SKU

At Only USB Internal CIR, it's USB Power

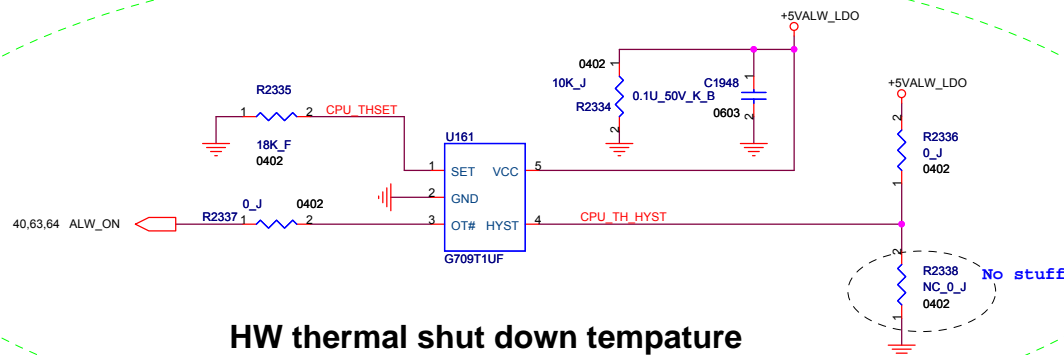
USB VCC9_F	1	TP847
USB PP9_F	1	TP848
USB PN9_F	1	TP849
	1	TP850
CIR_ALPS_3VPU	1	TP851
SW_CIR00	1	TP852
SW_CIR01	1	TP853
FEATURE_RST#	1	TP854
PWR_CIR#	1	TP855
CIR_ALPS_SPWR	1	TP856
	1	TP857

## FAN circuit



## HW THERMAL PROTECTION

07/01/09 Change HW THERMAL PROTECTION circuit to stuff

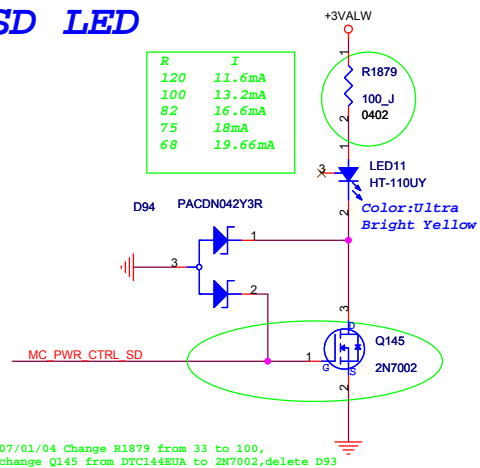


HW thermal shut down temperature setting 95 degree . Put Near CPU .

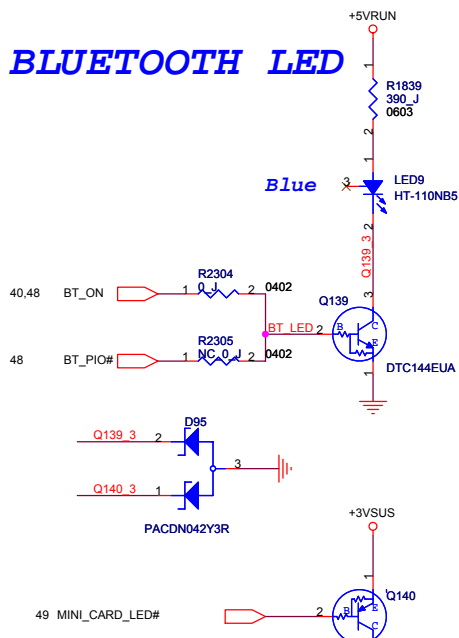
Base on MOR side request to add HW thermal protection circuit

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
Size		Document Number	
43		(M610-1-01) MainBoard (MBX-176) 2007	
Date:		Thursday, May 10, 2007	
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Rev		4.0	

## SD LED

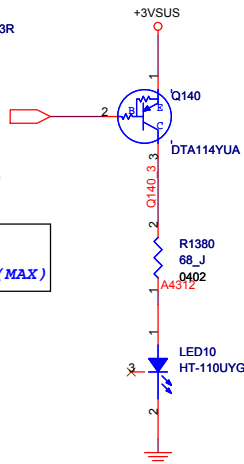


## BLUETOOTH LED

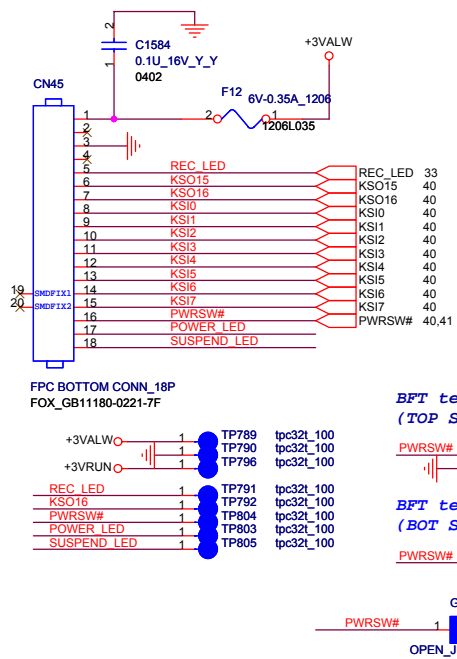


## WLAN LED

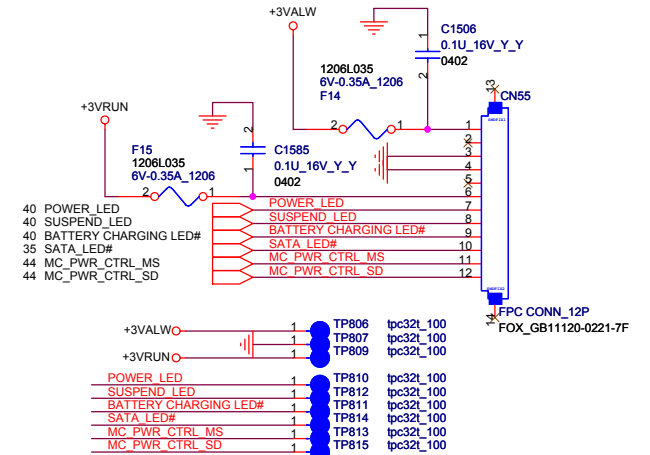
LED IF SPEC:  
20mA(TYP), 30mA(MAX)



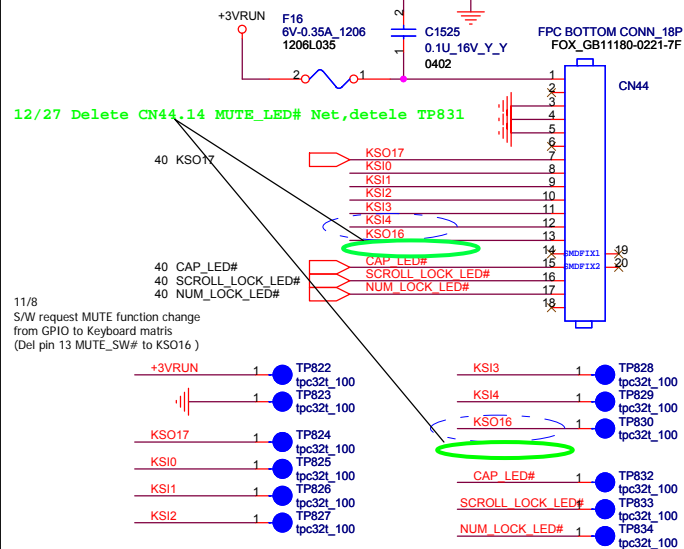
## To Power Button Board Connector



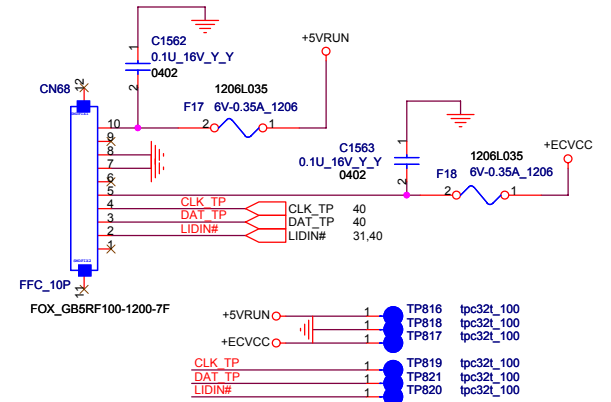
## To LED Board Connector



## To AV Function Board Connector



## To Touch Pad Board Connector



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CPBG - R&D Division

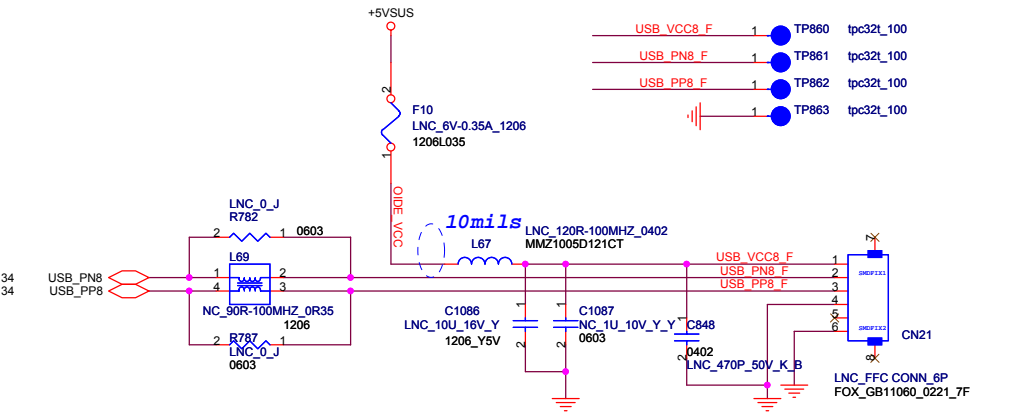
POWER BD + HOT KEY BD + TP&LED BD + LOGO LED

Size Document Number

43 (M610-1-01) MainBoard (MBX-176) 2007.1.4

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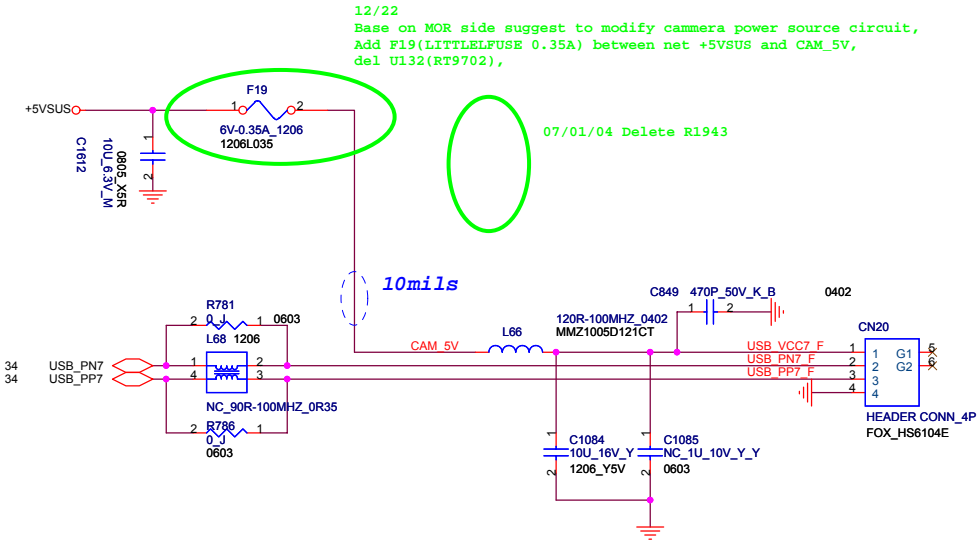
OIDE Connector



2006.1.4pin swape for ME request

12/27 Change Felica circuit Value to LNC\_\* for M610 DVT L SKU

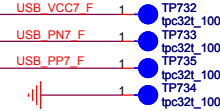
CAMERA Connector



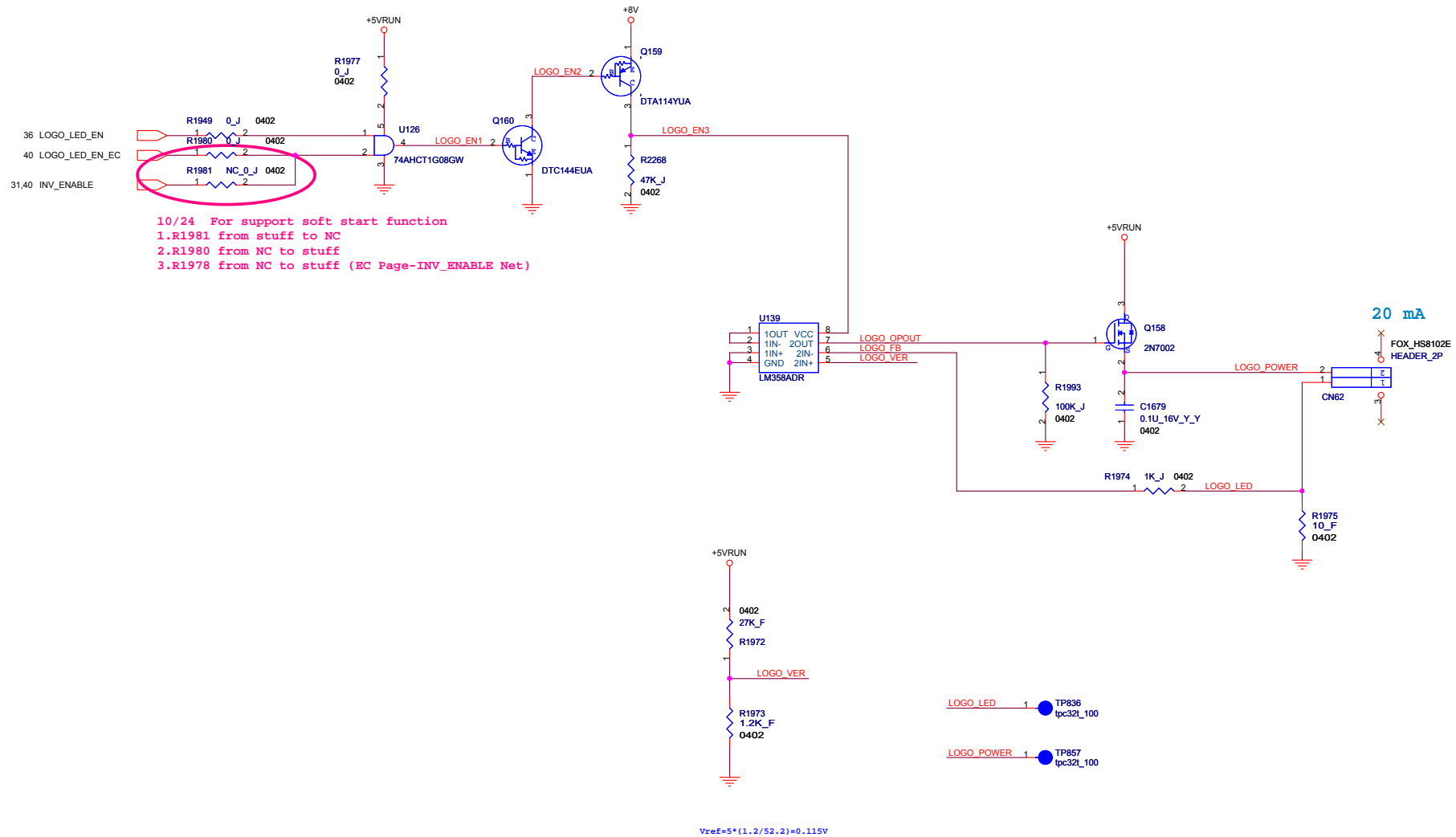
12/22  
Base on MOR side suggest to modify cammera power source circuit,  
Add F19(LITTLELFUSE 0.35A) between net +5VSUS and CAM\_5V,  
del U132(RT9702),

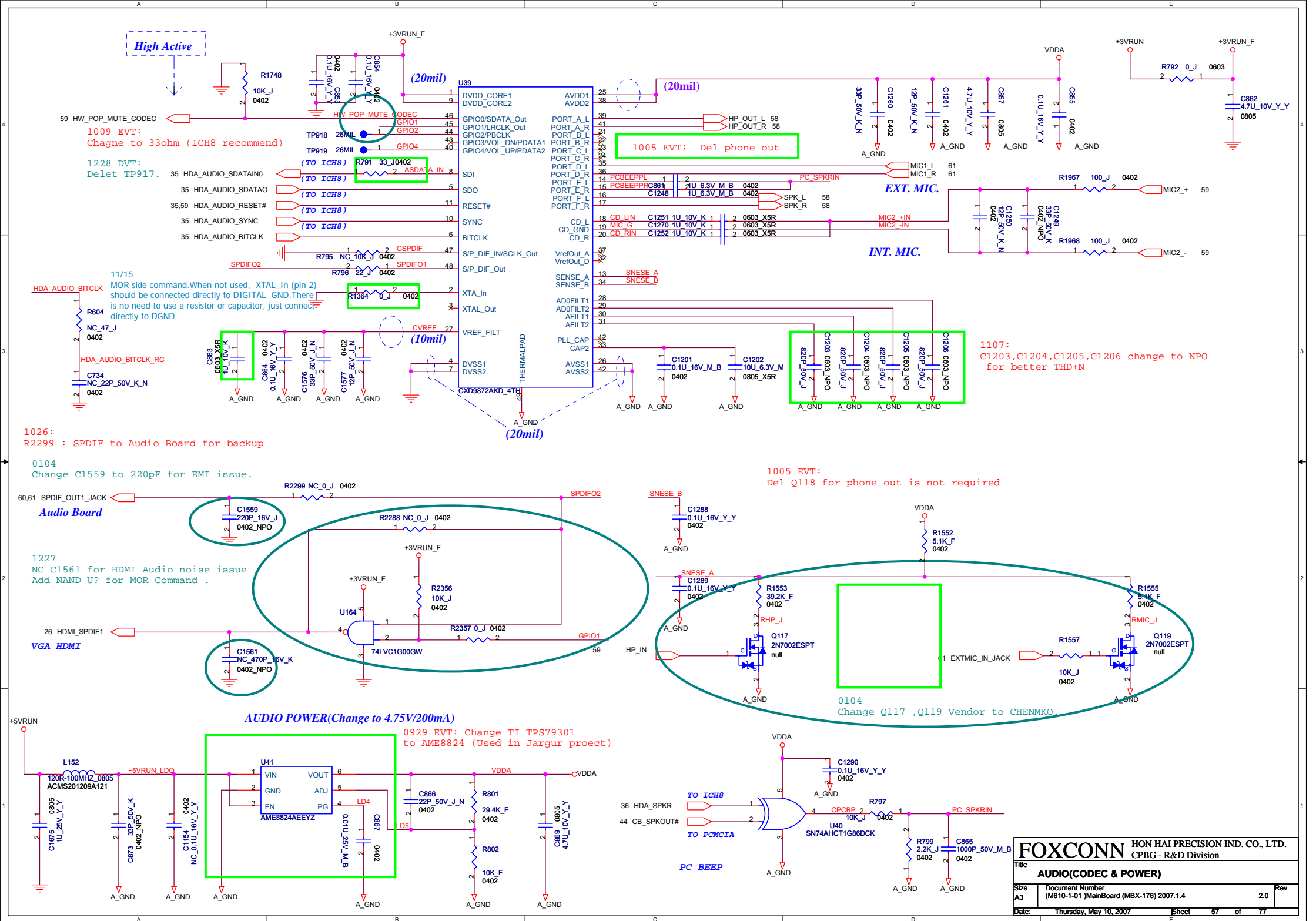
07/01/04 Delete R1943

12/21 BPT Test Pad



## Constant-Current SONY LOGO LED





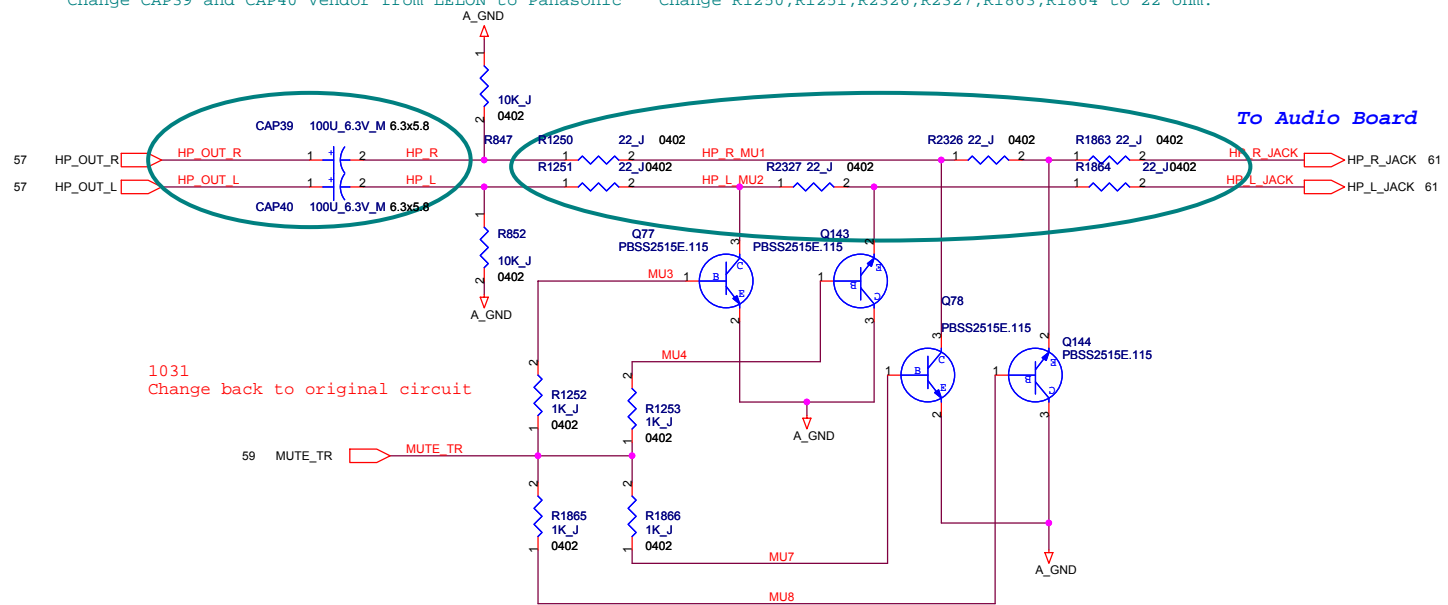
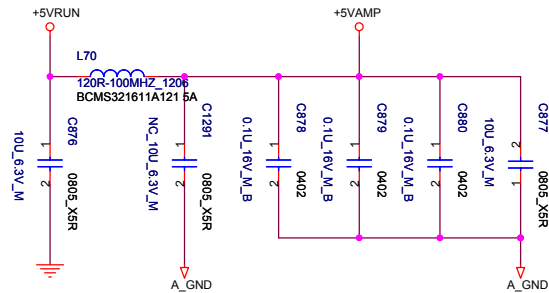
0920  
Add 2PCS CAP39,CAP40 100\_6.3V\_M  
Delet CAP24,CAP25

1103  
Change CAP39 and CAP40 Vendor from NIPPON CHEMI-CON to LELON

1228  
Change CAP39 and CAP40 Vendor from LELON to Panasonic

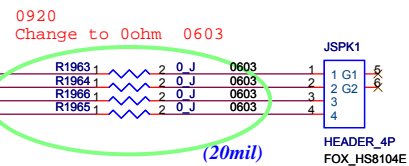
1229  
Change R1250,R1251,R2326,R2327,R1863,R1864 to 22 ohm.

Max 1.7A

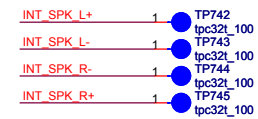


1031  
Change back to original circuit

## INTERNAL SPEAKER



## BFT Test Pad



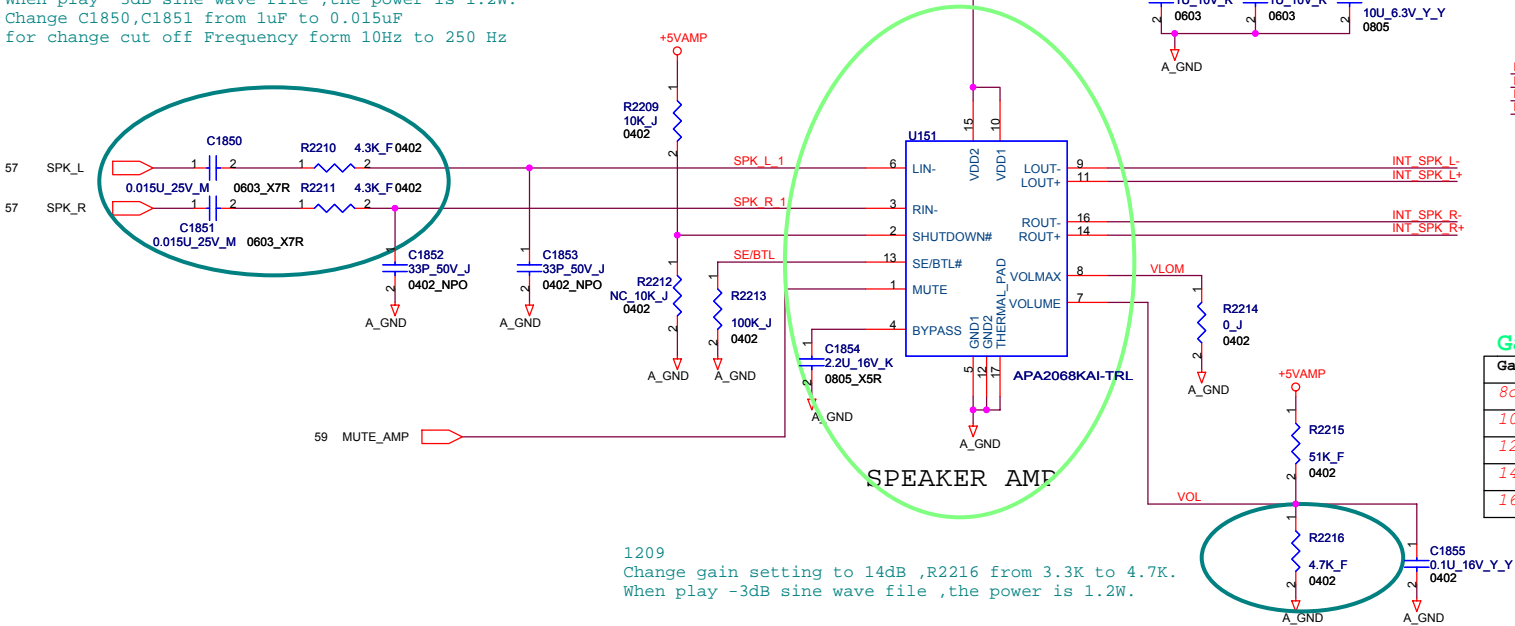
## Gain setting table

Gain	R2216	Voltage
8dB	9.1K	0.77V
10dB	7.68K	0.65V
12dB	6.2K	0.54V
14dB	4.7K	0.43V
16dB	3.3K	0.31V

## SPEAKER AMP

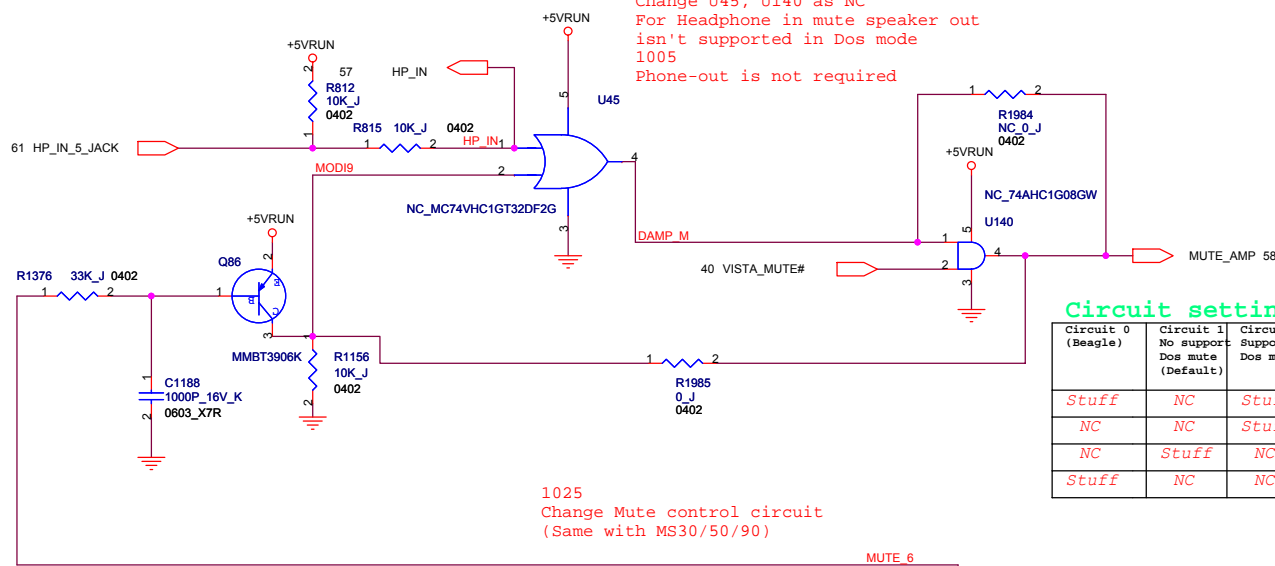
1211  
Change damping resistor to 4.3K  
When play -3dB sine wave file ,the power is 1.2W.  
Change C1850,C1851 from 1uF to 0.015uF  
for change cut off Frequency form 10Hz to 250 Hz

0920  
Change speaker AMP from TI to APA2068



1209  
Change gain setting to 14dB ,R2216 from 3.3K to 4.7K.  
When play -3dB sine wave file ,the power is 1.2W.

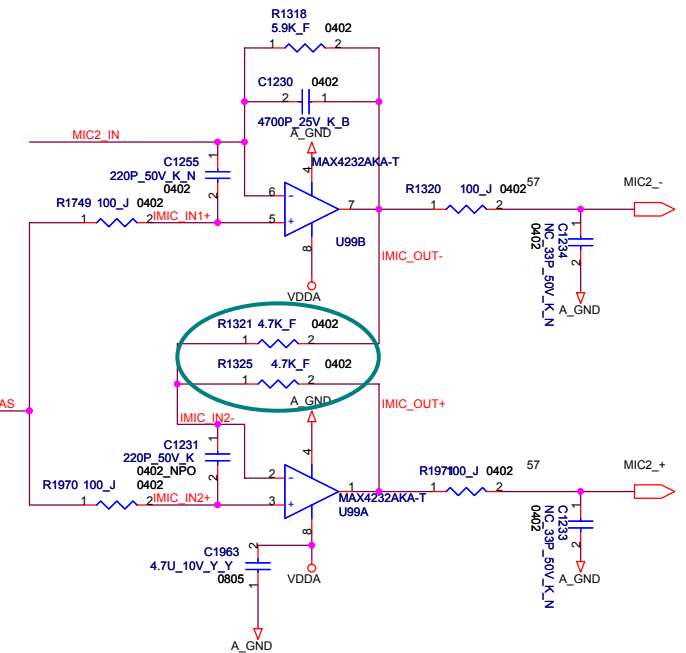




1025  
Change Mute control circuit  
(Same with MS30/50/90)

Circuit setting table

Circuit 0 (Beagle)	Circuit 1 No support Dos mute (Default)	Circuit 2 Support Dos mute	component
Stuff	NC	Stuff	U45
NC	NC	Stuff	U140
NC	Stuff	NC	R1985
Stuff	NC	NC	R1984



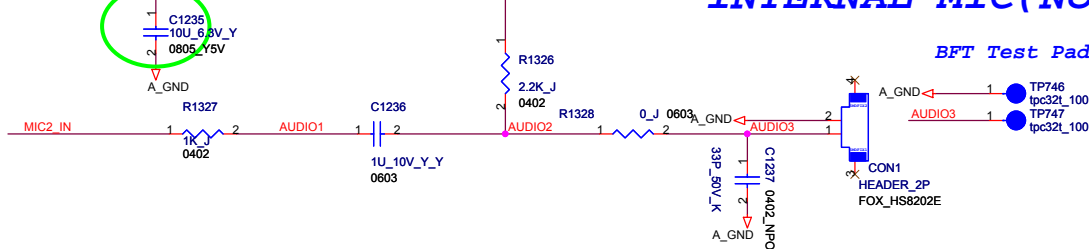
1227  
Change R1321 and R1325 from 4.7k\_J to 4.7K\_F  
for MOR Side Command.

1005  
Del phone-out mute circuit  
for phone-out is not required

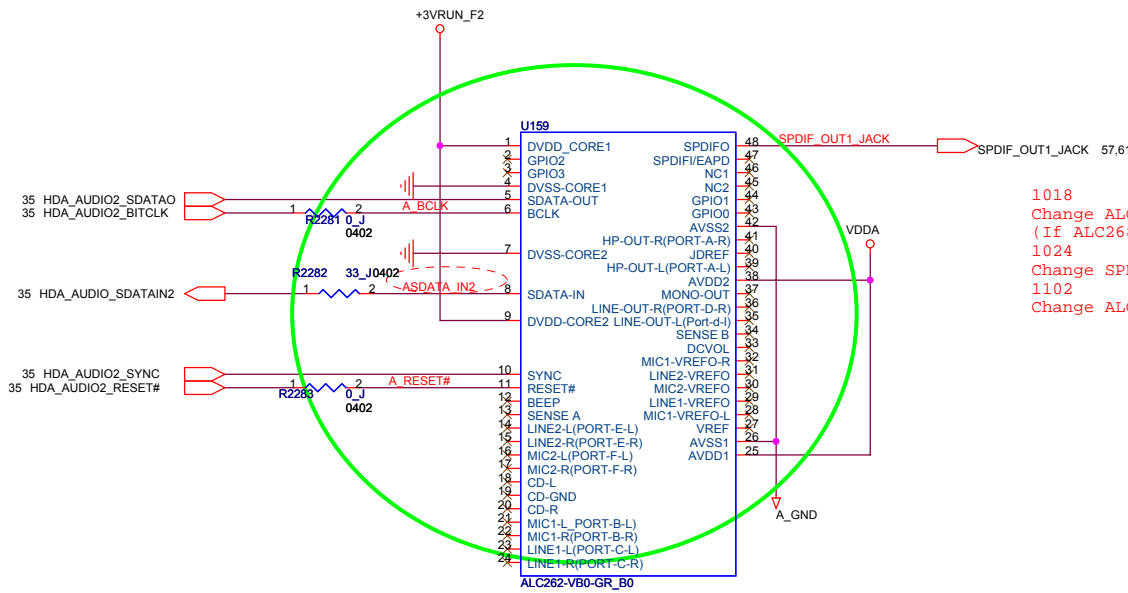
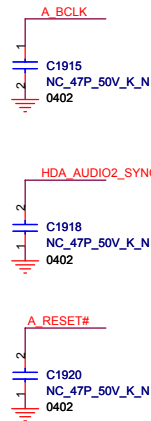
0111'07  
Change Q181 from 17-MMBT390-4000  
to 17-MMBT390-4001 for PUR can't buy issue

0104  
Change R1361 From 33k to 22k For improve Mute\_TR signal quality well.

## INTERNAL MIC(Non)

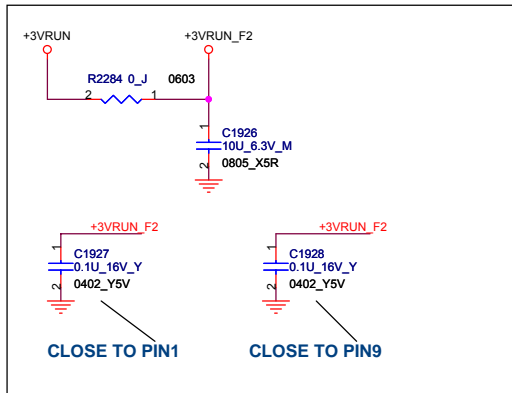


# Anti-Glitch

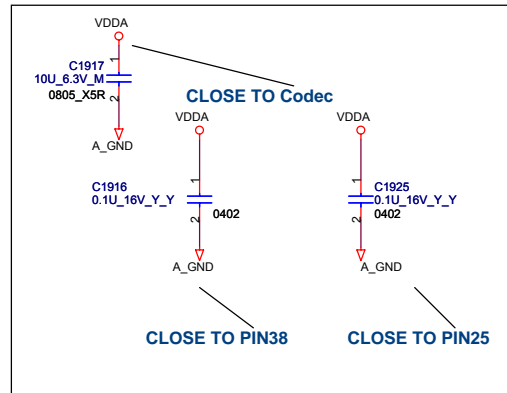


1018  
Change ALC262 to ALC268.  
(If ALC268 sample schedule delay, change to ALC262)  
1024  
Change SPDIF of Second codec to MB optical out  
1102  
Change ALC268 to ACL262

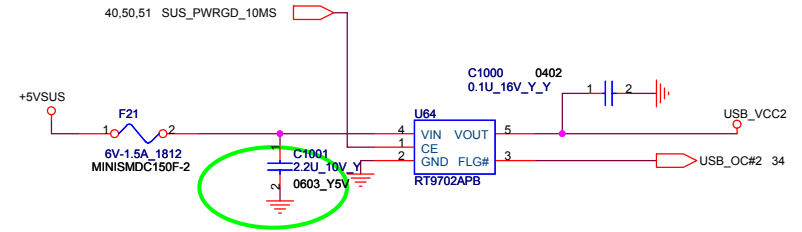
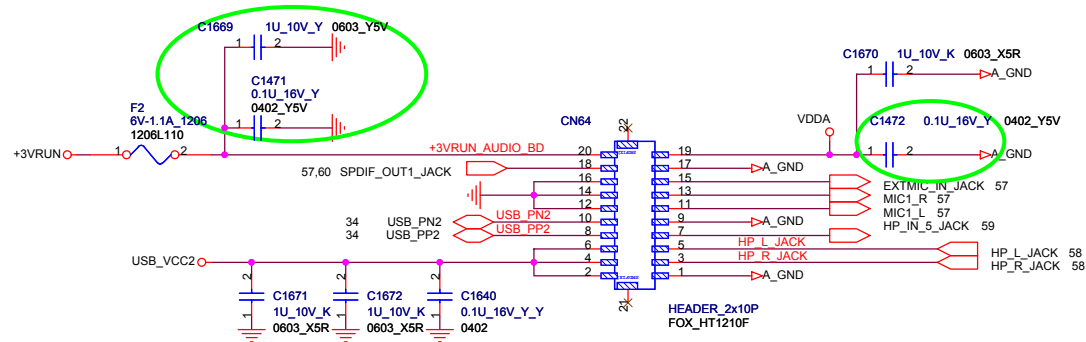
Decoupling Caps, place close to power pin.



Decoupling Caps, place close to power pin.

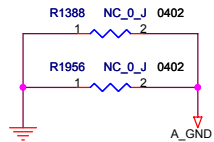


# Audio Board connector

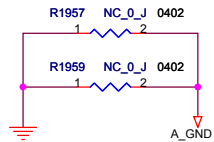


Backup two jumper resistors for bridge between GND and A\_GND

Close screw hole H3

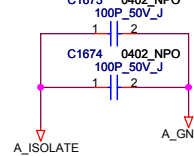


Close screw hole H5

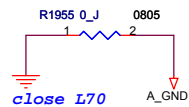


Isolate screw hole H4, and add EMI/ESD solution

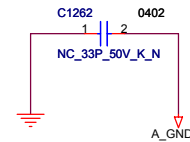
EMI



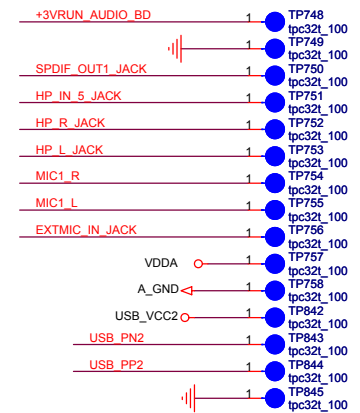
Add jumper resistor for Return patch



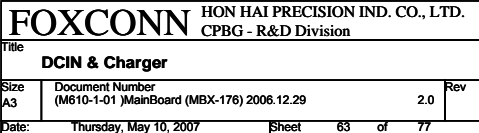
Original EMI back up solution to continue with MS20(bridge between GND and A\_GND)

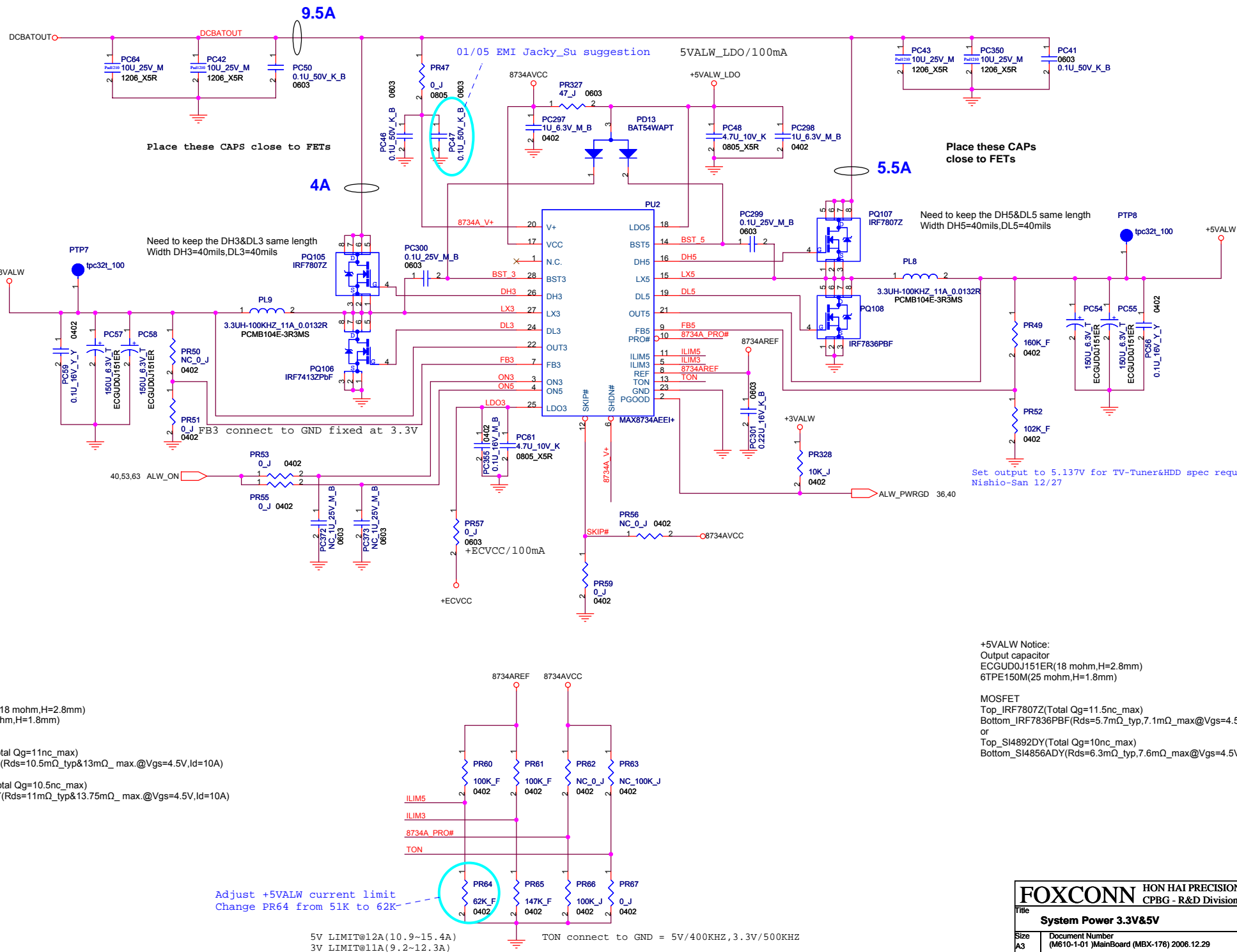


BFT Test Pad









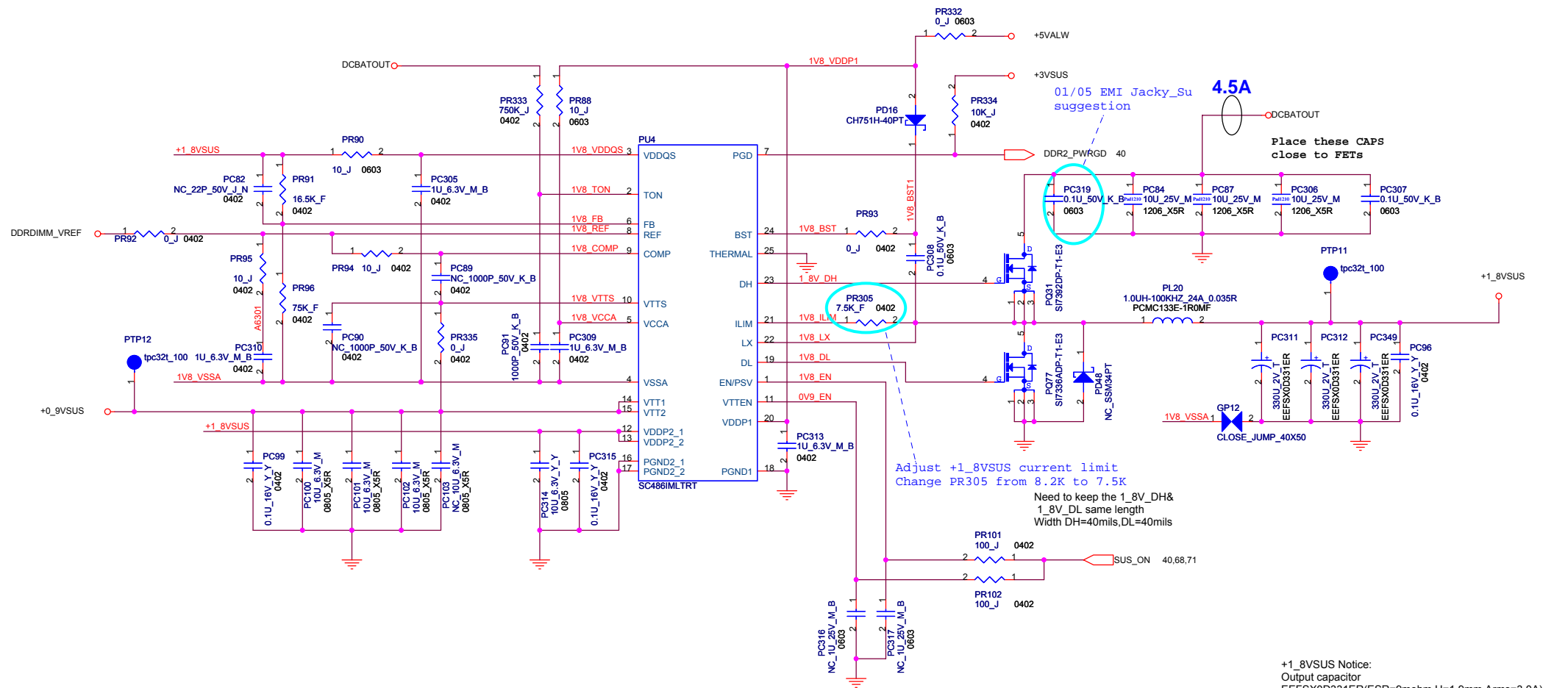
+5VALW Notice:  
Output capacitor  
ECGUD0J151ER(18 mohm,H=2.8mm)  
6TPE150M(25 mohm,H=1.8mm)

MOSFET  
Top\_IRF7807Z(Total Qg=11nc\_max)  
Bottom\_IRF7836PBF(Rds=5.7mΩ\_typ,7.1mΩ\_max@Vgs=4.5V,Id=13A)  
or  
Top\_SI4892DY(Total Qg=10.5nc\_max)  
Bottom\_SI4856ADY(Rds=6.3mΩ\_typ,7.6mΩ\_max@Vgs=4.5V,Id=14A)

FOXCONN HON HAI PRECISION IND. CO., LTD.			
CPBG - R&D Division			
Title System Power 3.3V&5V			
Size A3	Document Number (M610-1-01) MainBoard (MBX-176) 2006.12.29	2.0	Rev
Date: Thursday, May 10, 2007	Sheet 64	of 77	



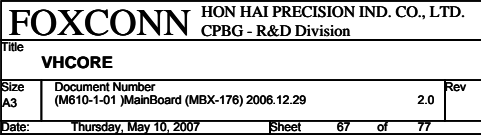


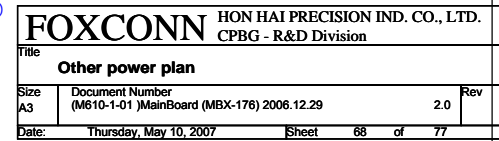


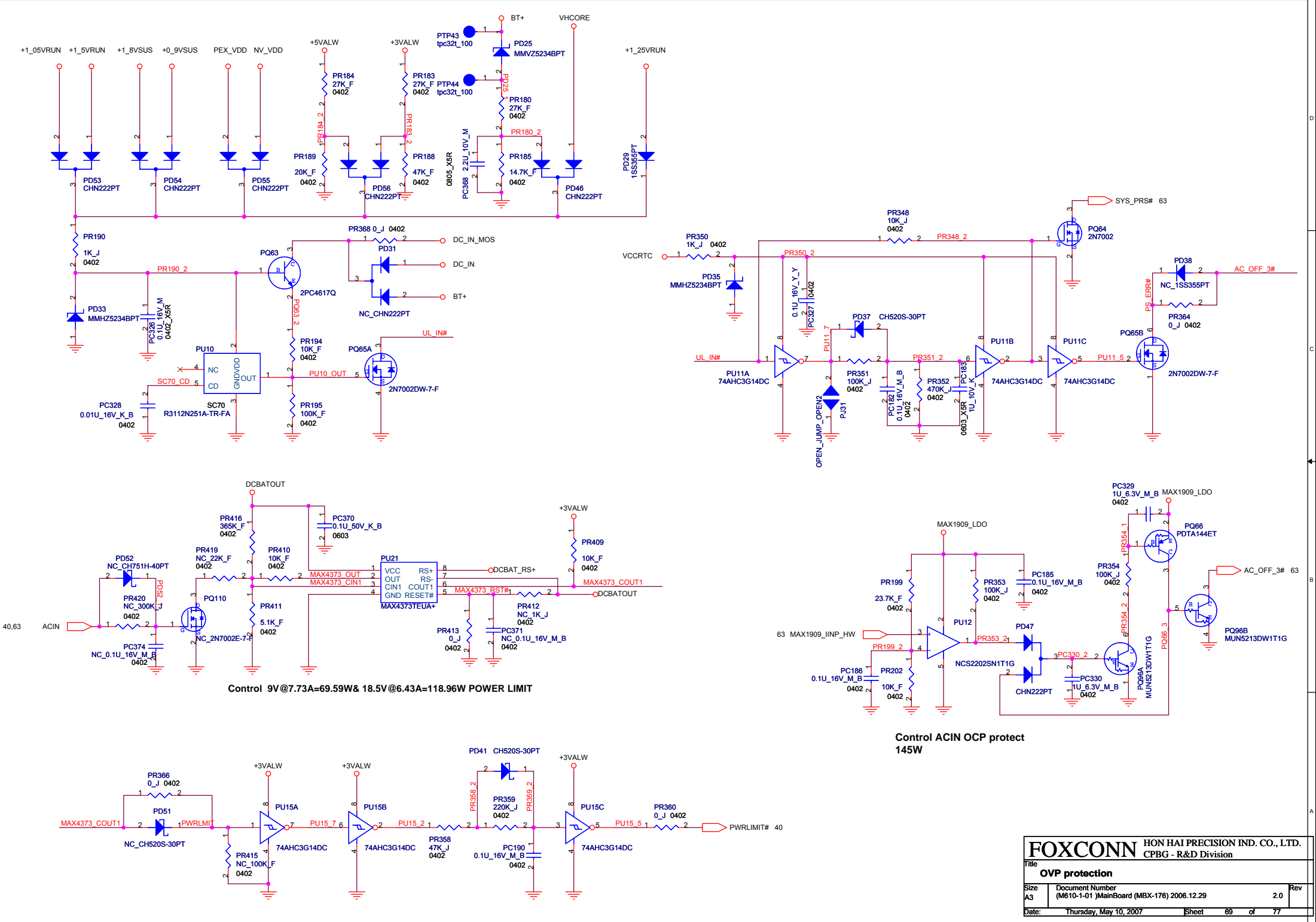
+1.8VSUS Notice:  
Output capacitor  
EEFSX0D331ER(ESR=9mohm,H=1.9mm,Arms=3.0A)  
2R5TPE330M9(ESR=9mohm,H=1.8mm,Arms=3.9A)

MOSFET  
Top\_Si7392DP(Total Qg=15nc\_max)  
Bottom\_Si7336ADP(Rds=3.1mQ\_typ,4.0mQ\_max@19A)  
or  
Top\_NTMFS4707N(Total Qg=15nc\_max)  
Bottom\_NTMFS4119N(Rds=3.1mQ\_typ,4.8mQ\_max@25A)

1.8V LIMIT@22A(20.2~25A)

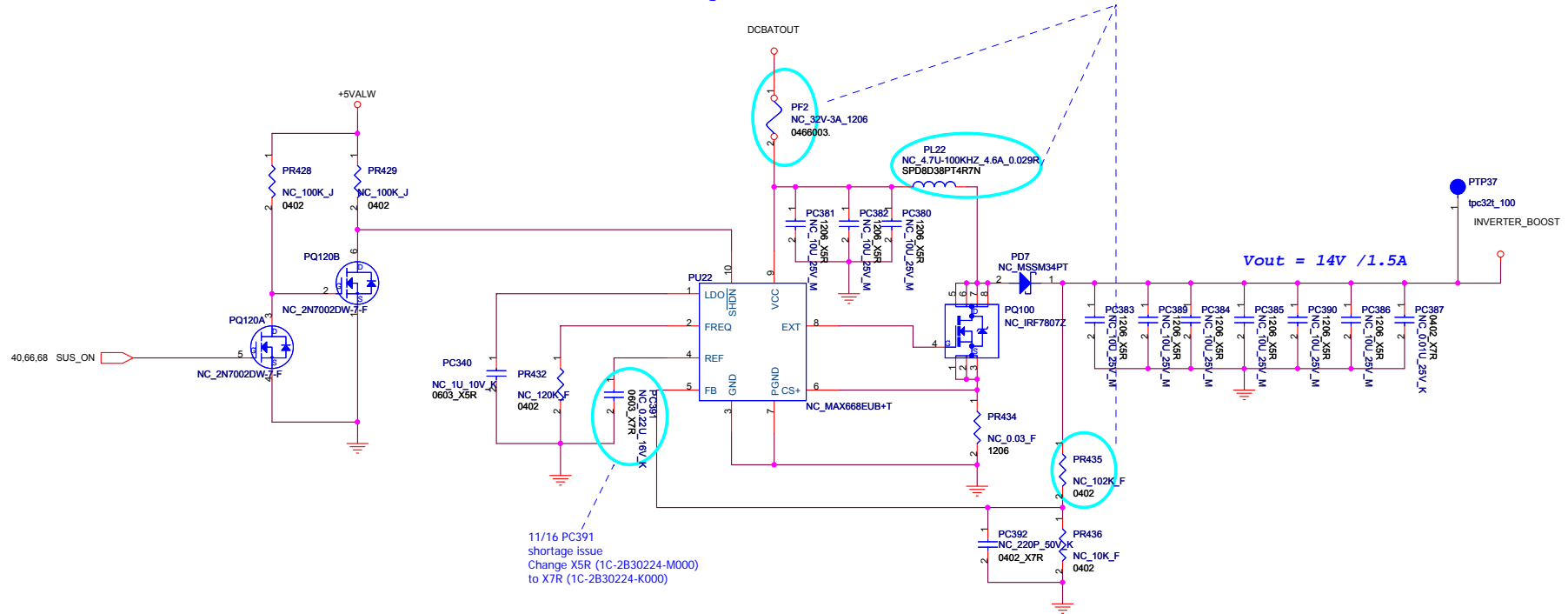






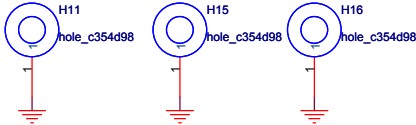


Boost circuit design change.  
 Add PF2 (32V-3A\_1206) fuse for boost circuit,  
 Change PL22 from 8UH-100KHZ\_2.5A\_0.07R to 4.7U-100KHZ\_4.6A\_0.029R.  
 Change PR435 from 95.3K to 102K



HOLE

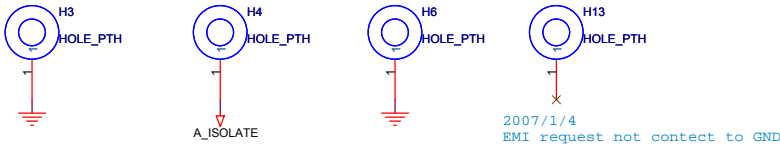
Type 1



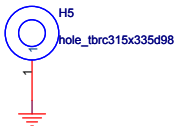
Type 2

Type 3

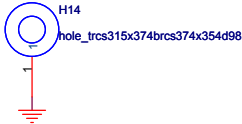
Type 4



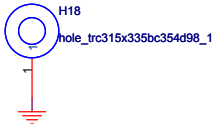
Type 5



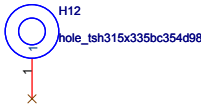
Type 6



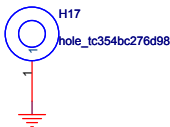
Type 7



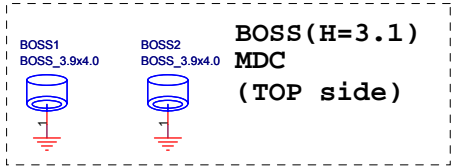
Type 8



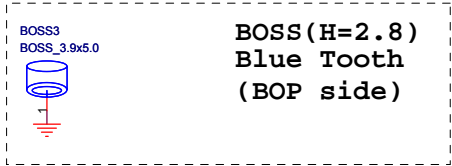
Type 9



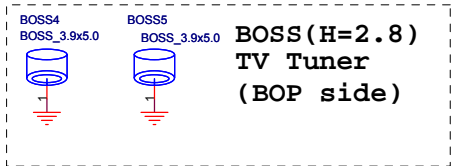
Type CPU



BOSS(H=3.1)  
MDC  
(TOP side)



BOSS(H=2.8)  
Blue Tooth  
(BOP side)



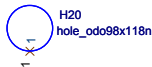
BOSS(H=2.8)  
TV Tuner  
(BOP side)

Type NPTH Guide (spherical)HOLD

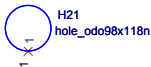


close H1

Type NPTH Guide (oval-shaped)HOLD



close H6



close H17



