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11	Crestline (POWER,VCC) 5/7	1.0	07'07'17	46	SYS Power(+1_5V/+1_05V)	1.0	07'07'17
12	Crestline (VCC CORE) 6/7	1.0	07'07'17	47	DDR2 Power(+1_8V/+0_9V)	1.0	07'07'17
13	Crestline (VSS) 7/7	1.0	07'07'17	48	CPU_Vcore---ISL6262A	1.0	07'07'17
14	DDRII(SO-DIMM_0) 1/3	1.0	07'07'17	49	Others power plane	1.0	07'07'17
15	DDRII(SO-DIMM_1) 2/3	1.0	07'07'17	50	OVP protection	1.0	07'07'17
16	DDRII(Termination) 3/3	1.0	07'07'17	51	GMCH power	1.0	07'07'17
17	CRT	1.0	07'07'17	52	HOLE	1.0	07'07'17
18	LVDS	1.0	07'07'17	53	History (1)	1.0	07'07'17
19	ICH8-M(PCI/USB) 1/5	1.0	07'07'17	54	History (2)	1.0	07'07'17
20	ICH8-M(LPC,IDE,SATA)2/5	1.0	07'07'17	55	History (3)	1.0	07'07'17
21	ICH8-M(GPIO) 3/5	1.0	07'07'17	56	History (4)	1.0	07'07'17
22	ICH8-M(POWER) 4/5	1.0	07'07'17	57	History (5)	1.0	07'07'17
23	ICH8-M(GND) 5/5	1.0	07'07'17	58			
24	SATA HDD/CD-ROM	1.0	07'07'17	59			
25	EC+KBC(3910)	1.0	07'07'17	60			
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31	AUDIO(AMP/HP/SPK) 2/4	1.0	07'07'17	66			
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M720 Main Board

M/B P/N: 1P-0076102-6010(FUBAI)
1P-0076200-6010(NANYA)
1P-0076502-6010(HANSTAR)
1P-0076G00-6010(TRIPOD)

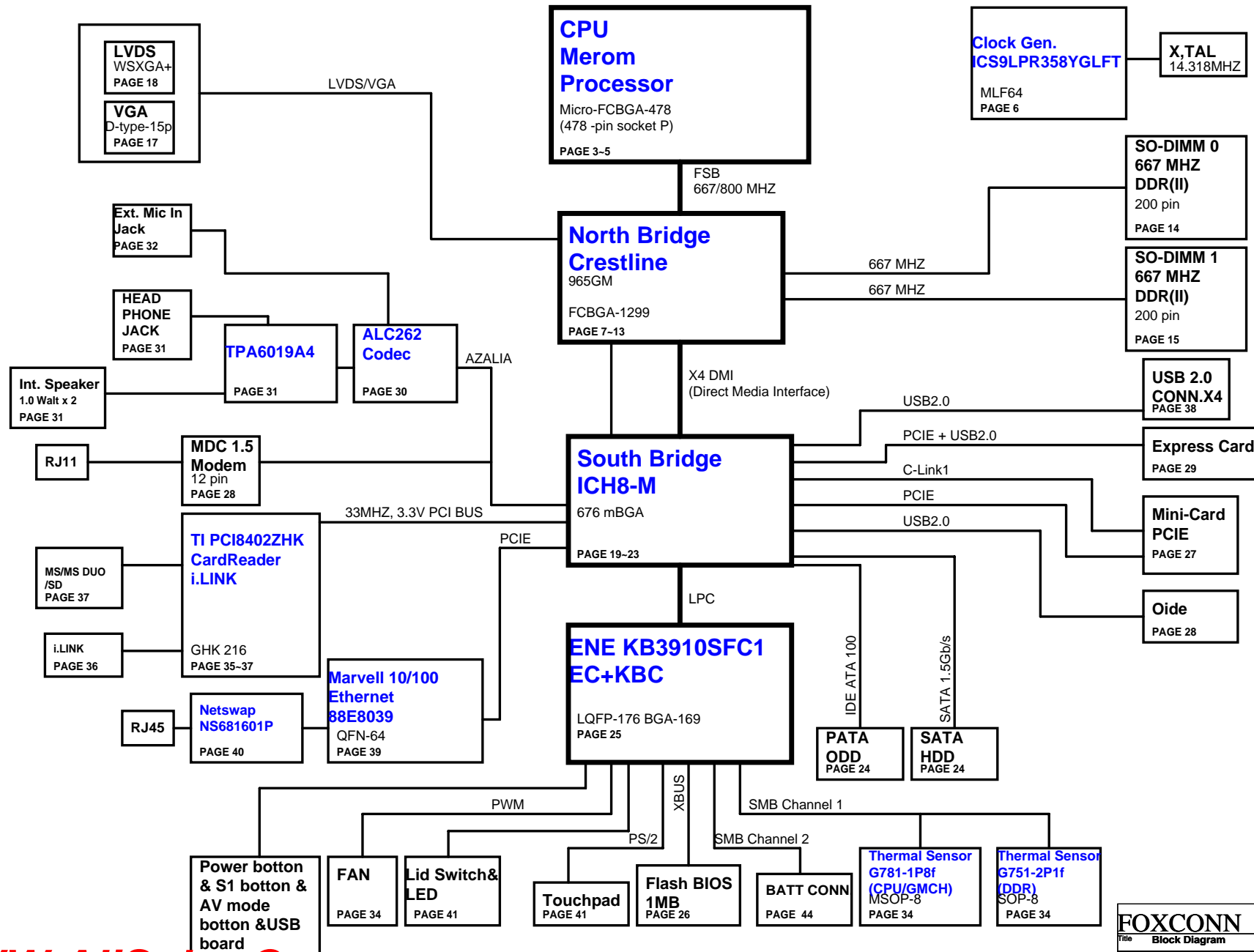
P/B P/N: 1P-1076105-6010(FUBAI)
1P-1076200-6010(NANYA)
1P-1076505-6010(HANSTAR)
1P-1076G00-6010(TRIPOD)

U/B P/N: 1P-1076106-6010(FUBAI)
1P-1076201-6010(NANYA)
1P-1076506-6010(HANSTAR)
1P-1076G01-6010(TRIPOD)

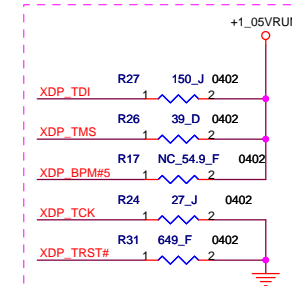
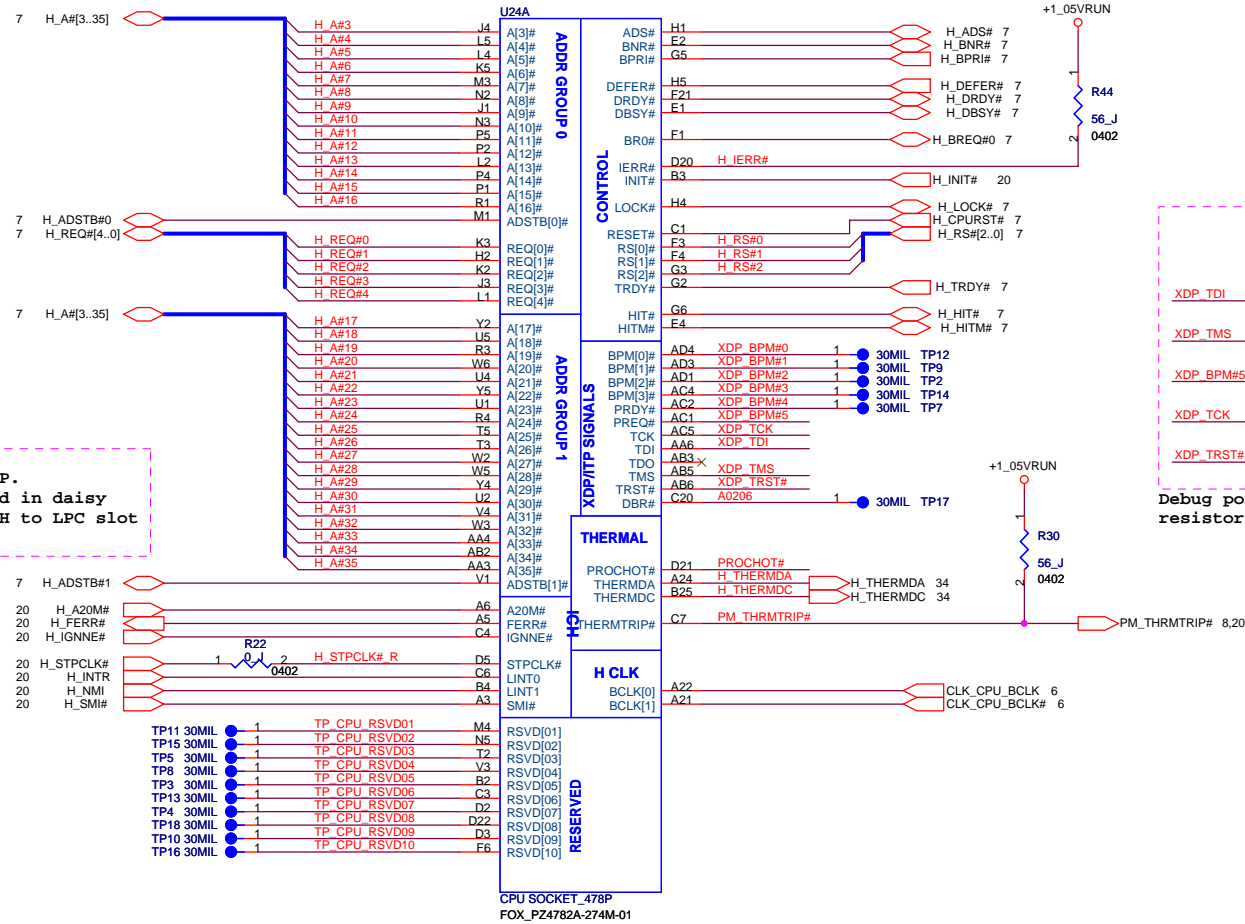
P. Leader	Check by	Design by

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title Index Page		
Size A3	Document Number M720-1-01	Rev 1.0
Date: Wednesday, July 18, 2007	Sheet 1 of 56	

M720(Crestline GM Block Diagram)



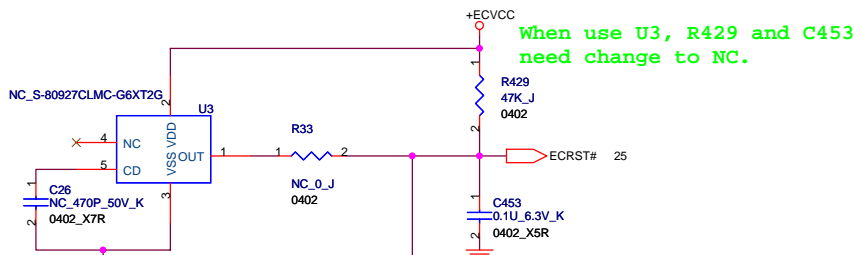
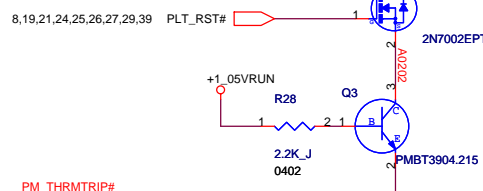
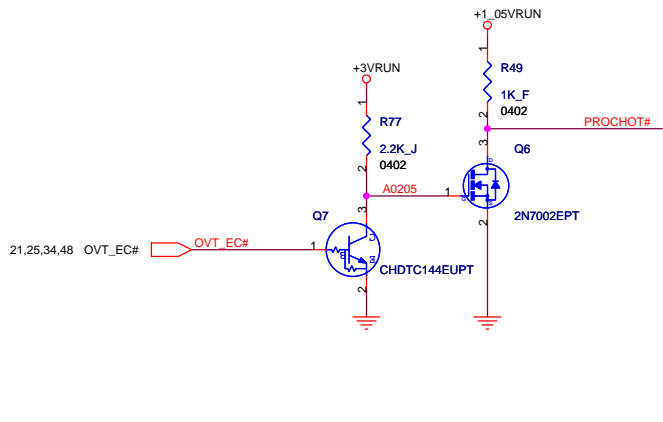
Layout note:
no stub on H_STPCLK TP.
H_STPCLK# to be routed in daisy chain fashion from ICH to LPC slot and then to CPU.

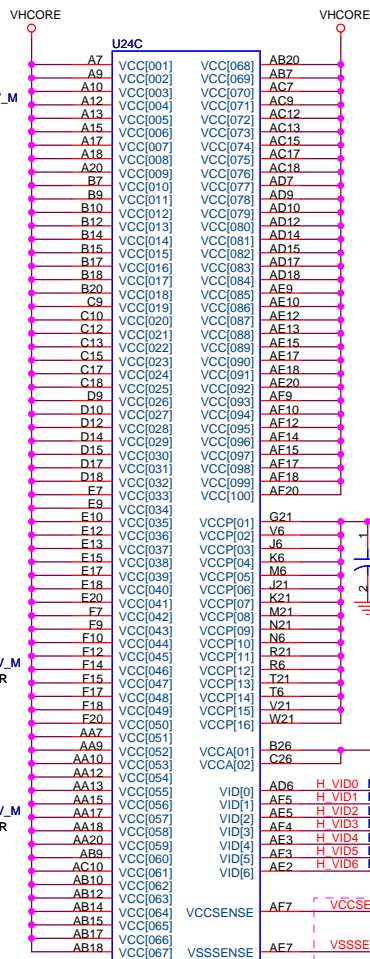
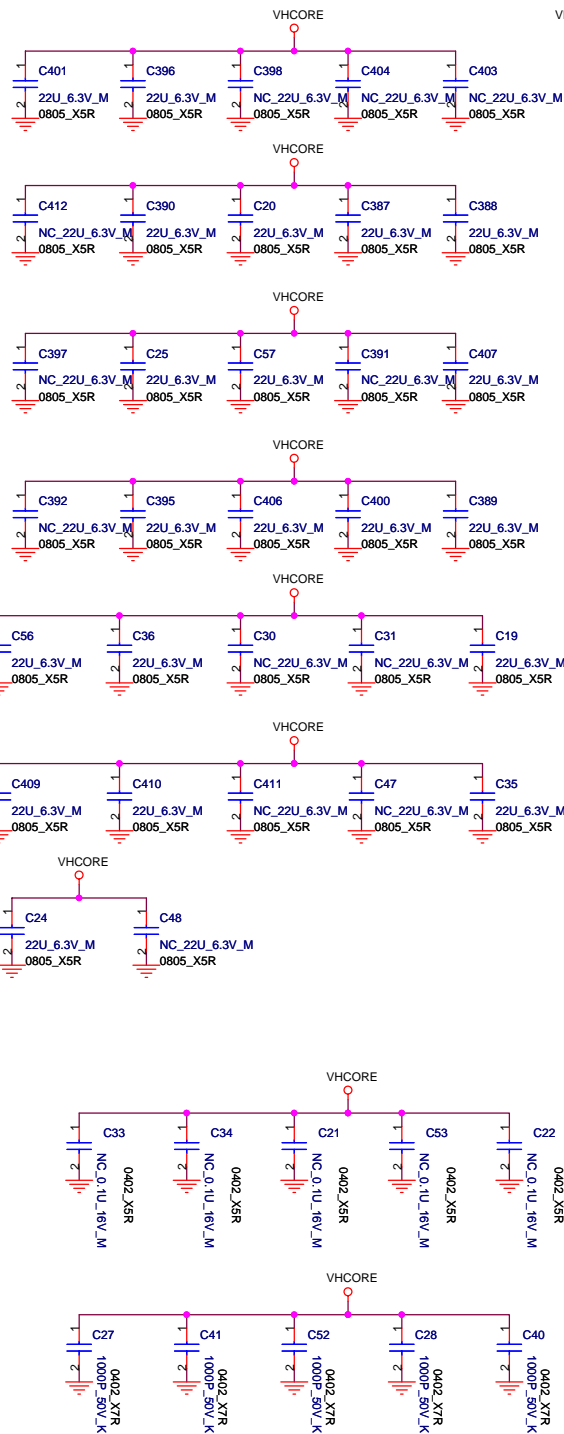


Debug port not used .
resistors close to CPU.

PM_THRMTRIP#
should connect to
ICH8-M and GMCH
without T-ing (No stub)

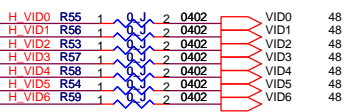
ICH8M's GPIO12: VIL---> -0.5V ~ 0.8V
VIH---> 2.0V ~ 3.3+0.5V
MEROM's PROCHOT#: VIL---> -0.1V ~ 0.3*VCCP
VIH---> 0.7*VCCP ~ VCCP+0.1



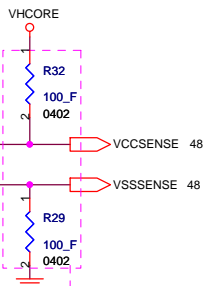


CPU_VCCA----->120mA
CPU_VCCP----->2.5A
CPU_VCC----->36A

Layout Note: Route
VCCSENSE & VSSSENSE
traces at 27.4 Ohms with
50 mil spacing. Place PU
and PD within 1 inch of
CPU.
width=18 mil
spacing=7 mil



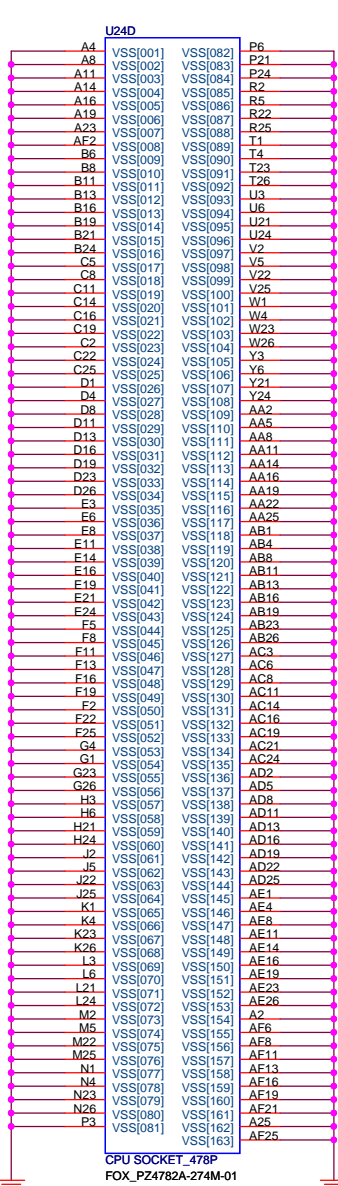
Same Length

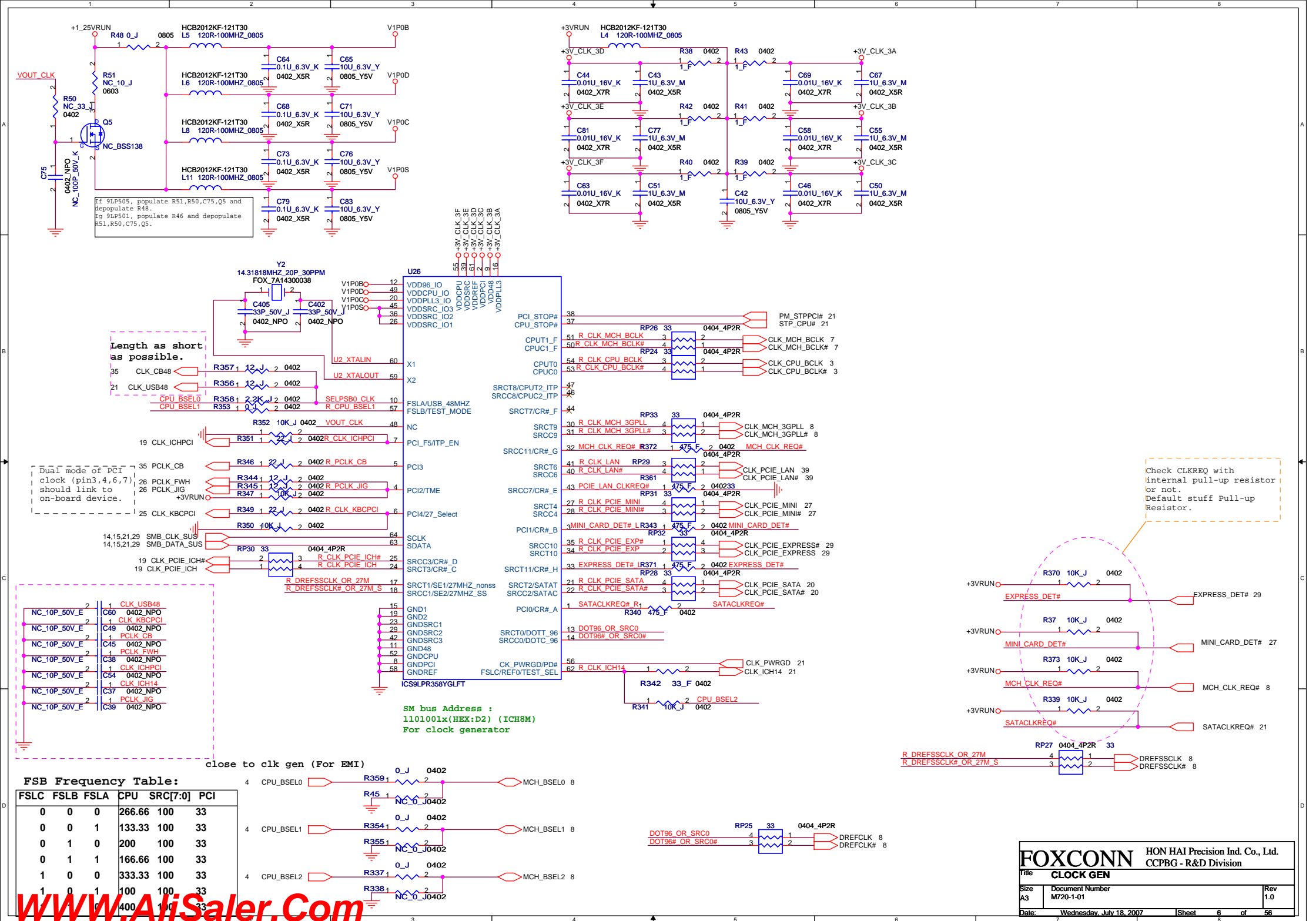


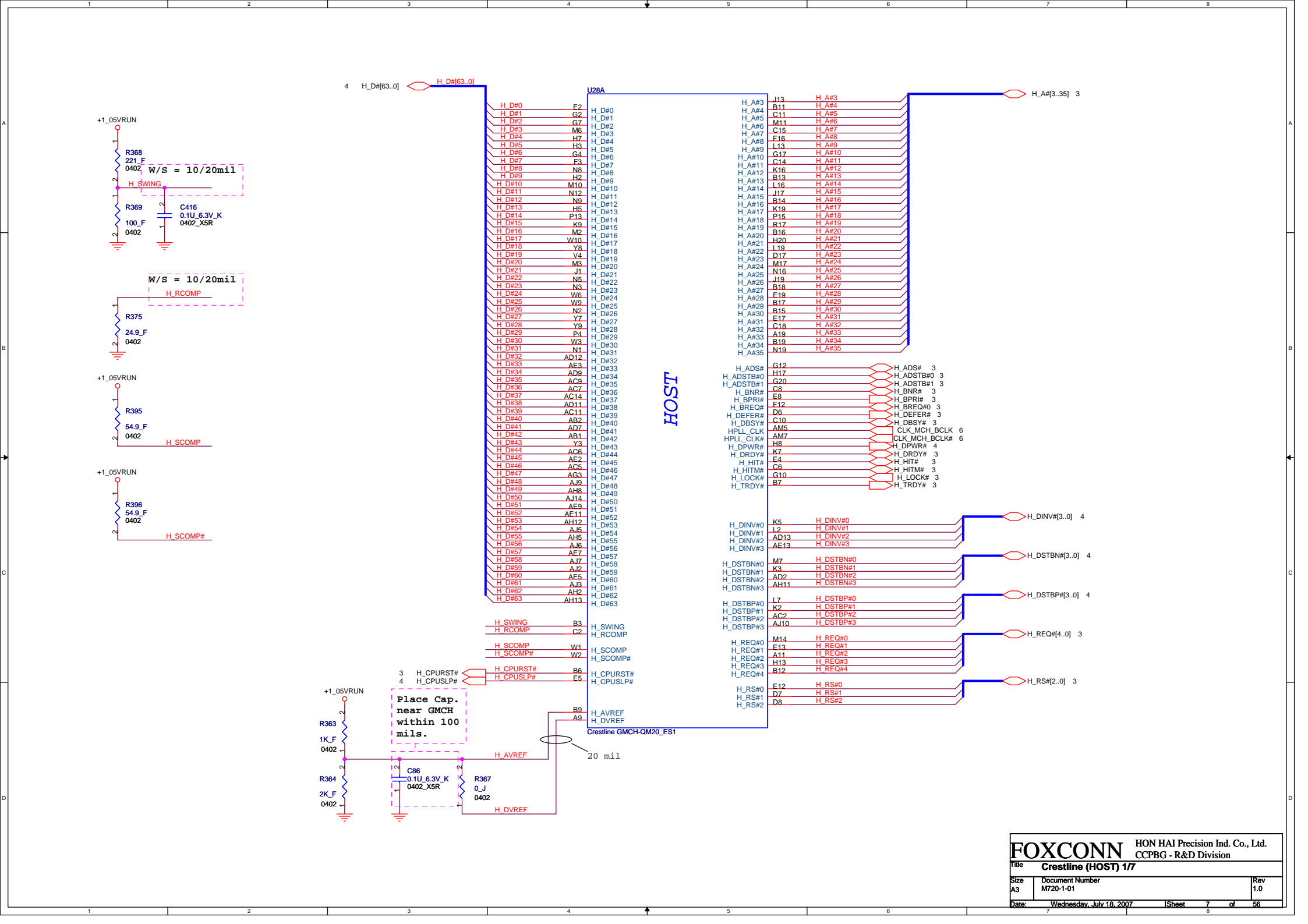
100 mil

20 mil

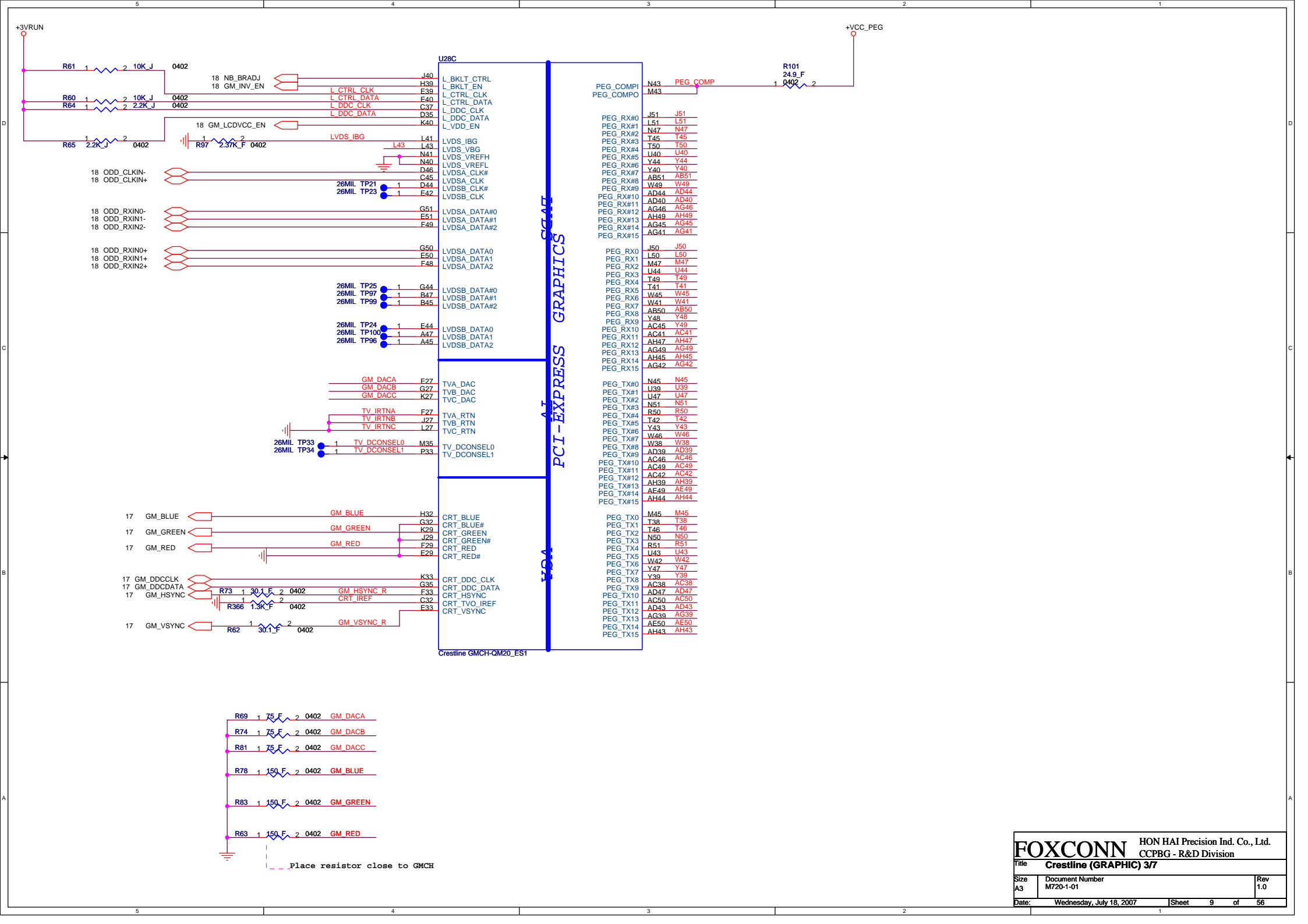
LAYOUT NOTE:
Place 0.01uF
near PIN B26

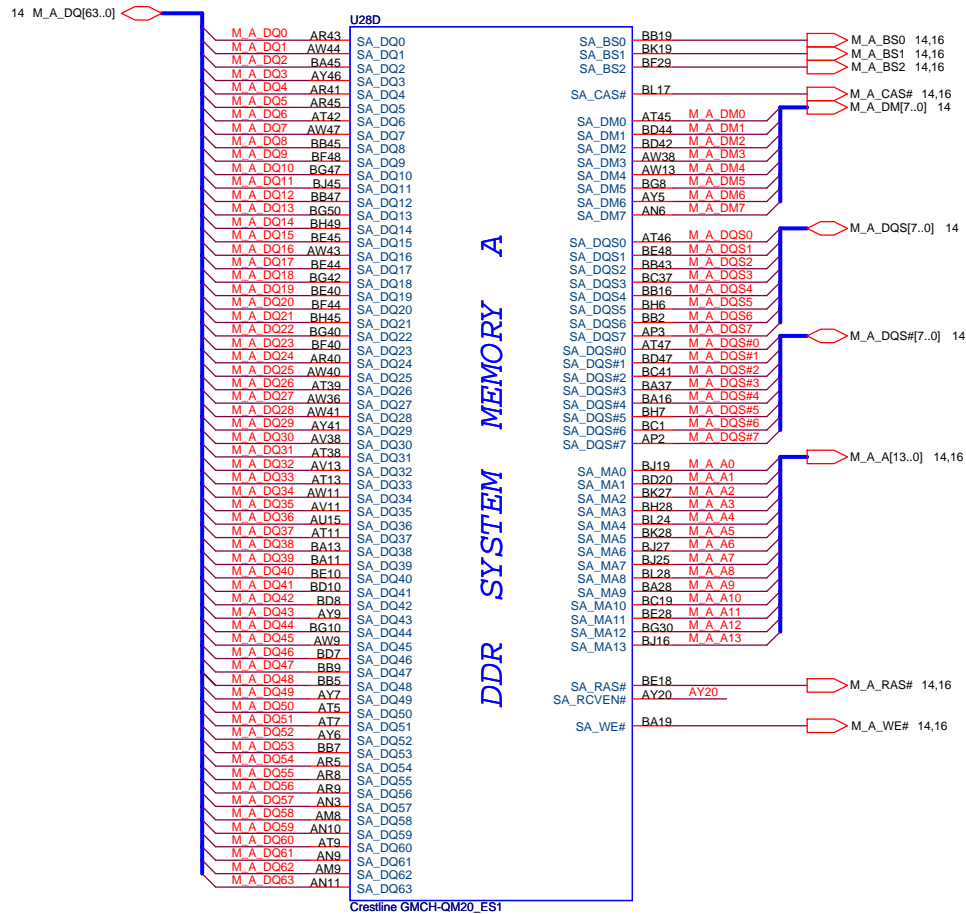




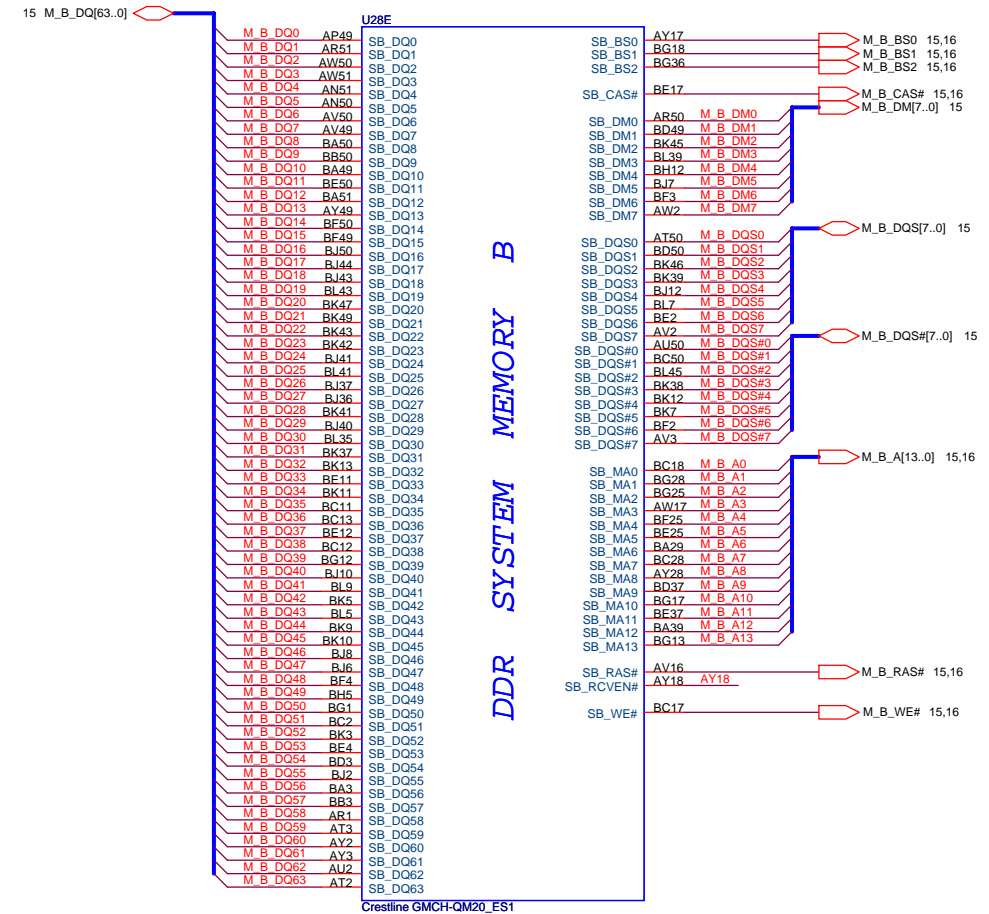




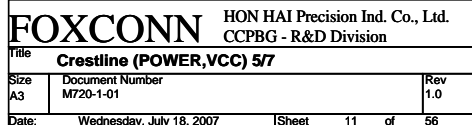


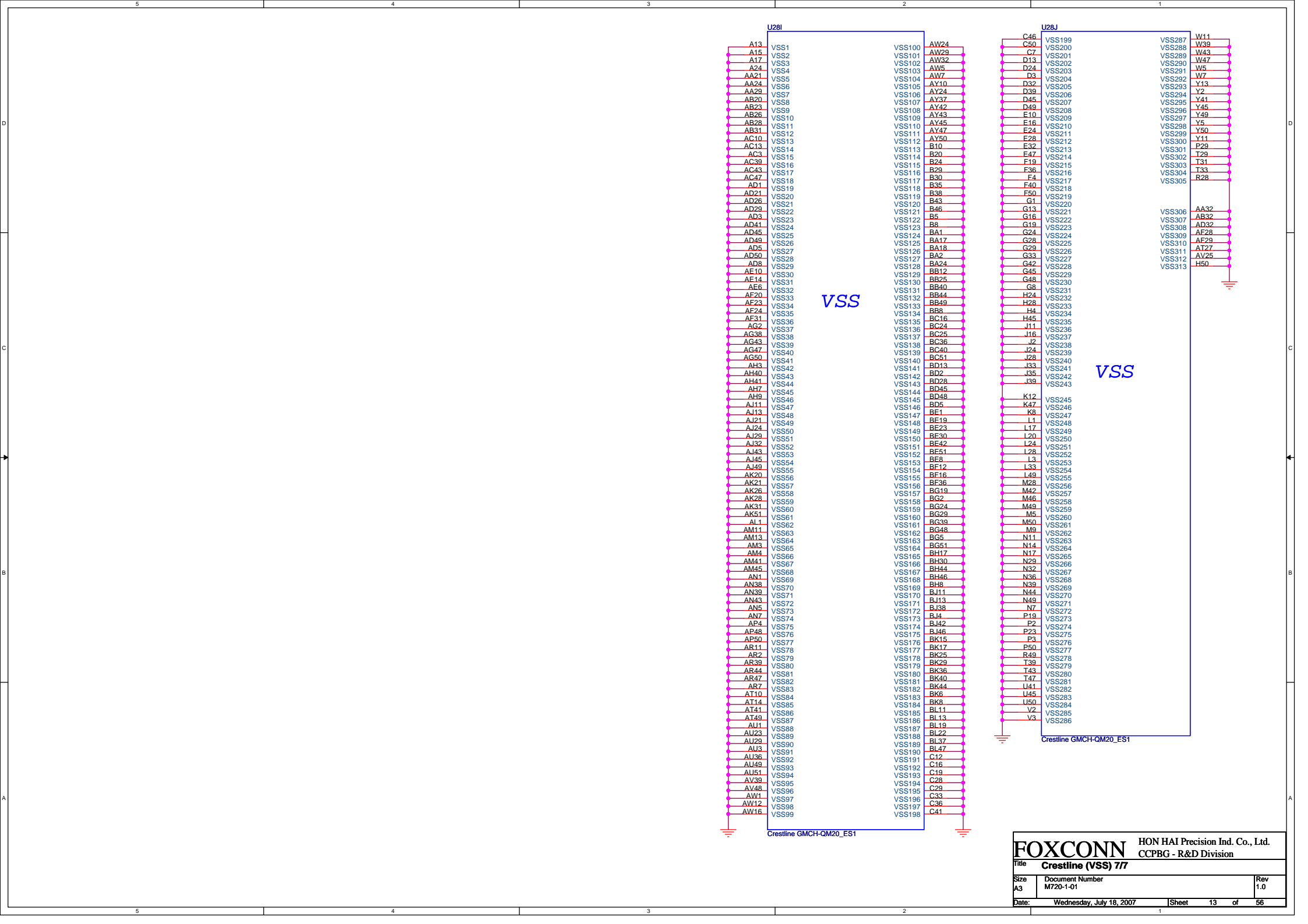


Crestline GMCH-QM20_ES1

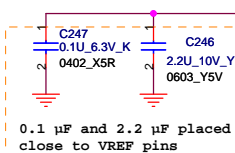


Crestline GMCH-QM20_ES1

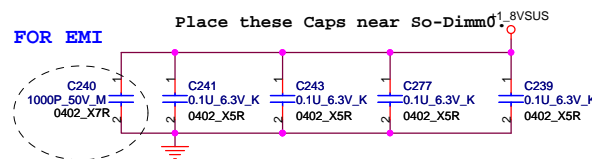
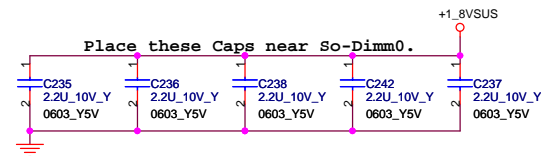
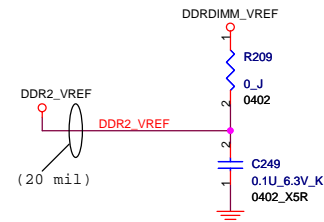
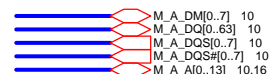
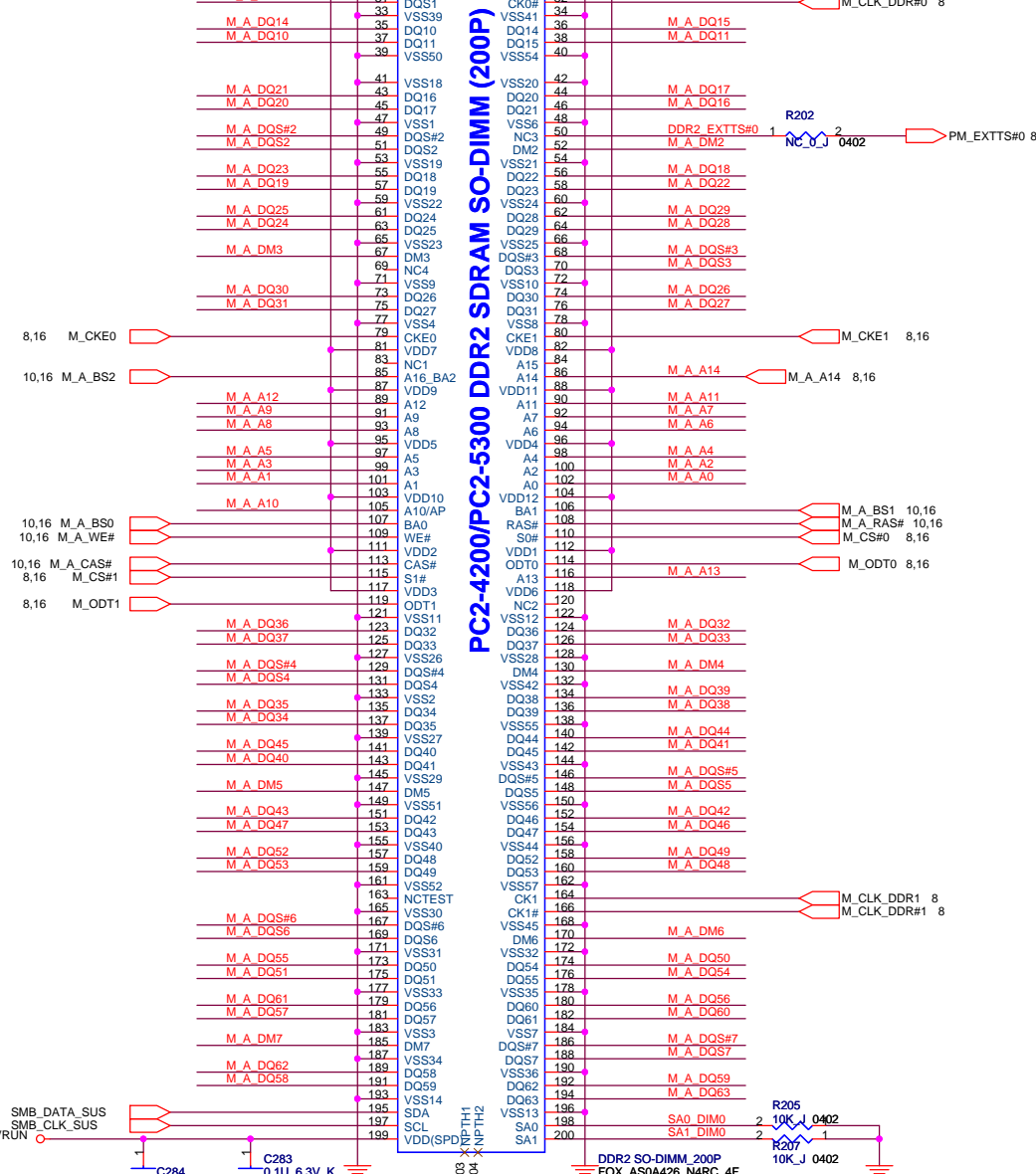


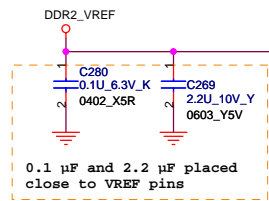


1.8V per DIMM=3.08A

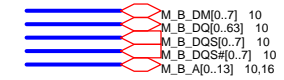


"Intel check list suggest a 330uF"





1.8V per DIMM=3.08A



8,16 M_CKE3

10,16 M_B_BS2

10,16 M_B_BS0

10,16 M_B_WE#

10,16 M_B_CAS#

8,16 M_CS#3

8,16 M_ODT3

6,14,21,29 SMB_DATA_SUS

6,14,21,29 SMB_CLK_SUS

+3VVRUN

C234 2.2U_10V_Y
0603_Y5V

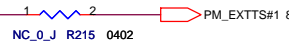
C245 0.1U_6.3V_K
0402_X5R

PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)

DIMM_1

SMBus Address: A4(W)/A5(R)

DIMM_1 is placed farther from the GMCH than DIMM_0



M_CKE4 8,16

M_B_A14 8,16

M_B_BS1 10,16

M_B_RAS# 10,16

M_CS#2 8,16

M_ODT2 8,16

M_CLK_DDR4 8

M_CLK_DDR#4 8

SA0_DIM1 2 0402

SA1_DIM1 2 0402

SA0 2 0402

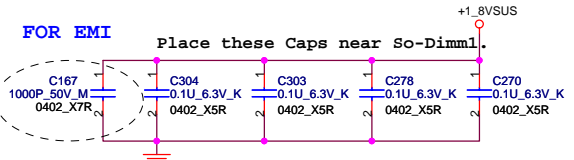
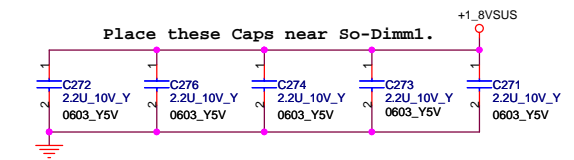
SA1 2 0402

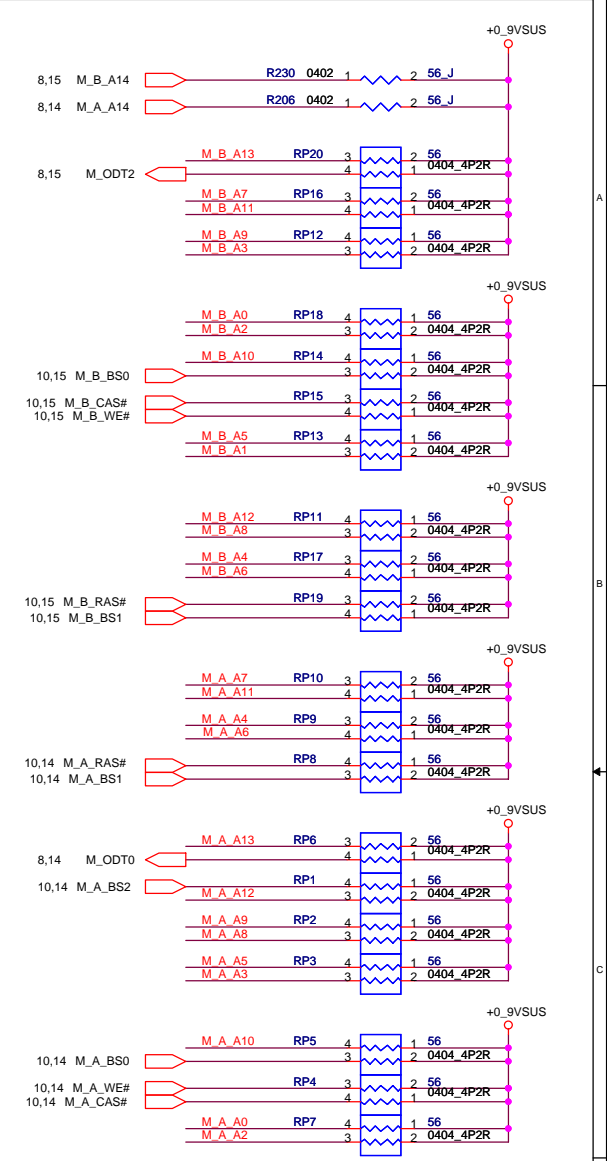
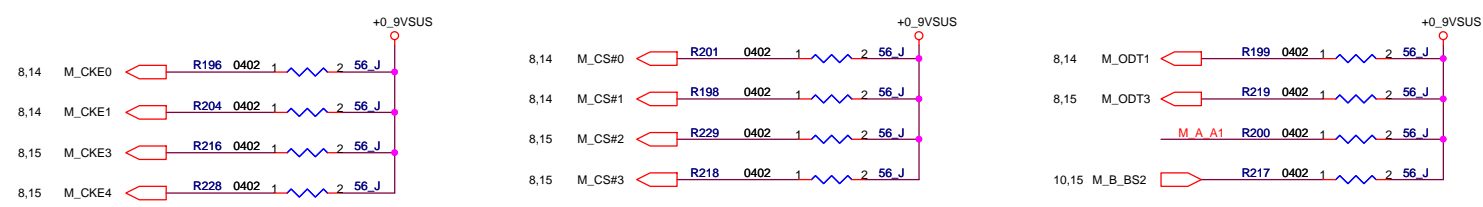
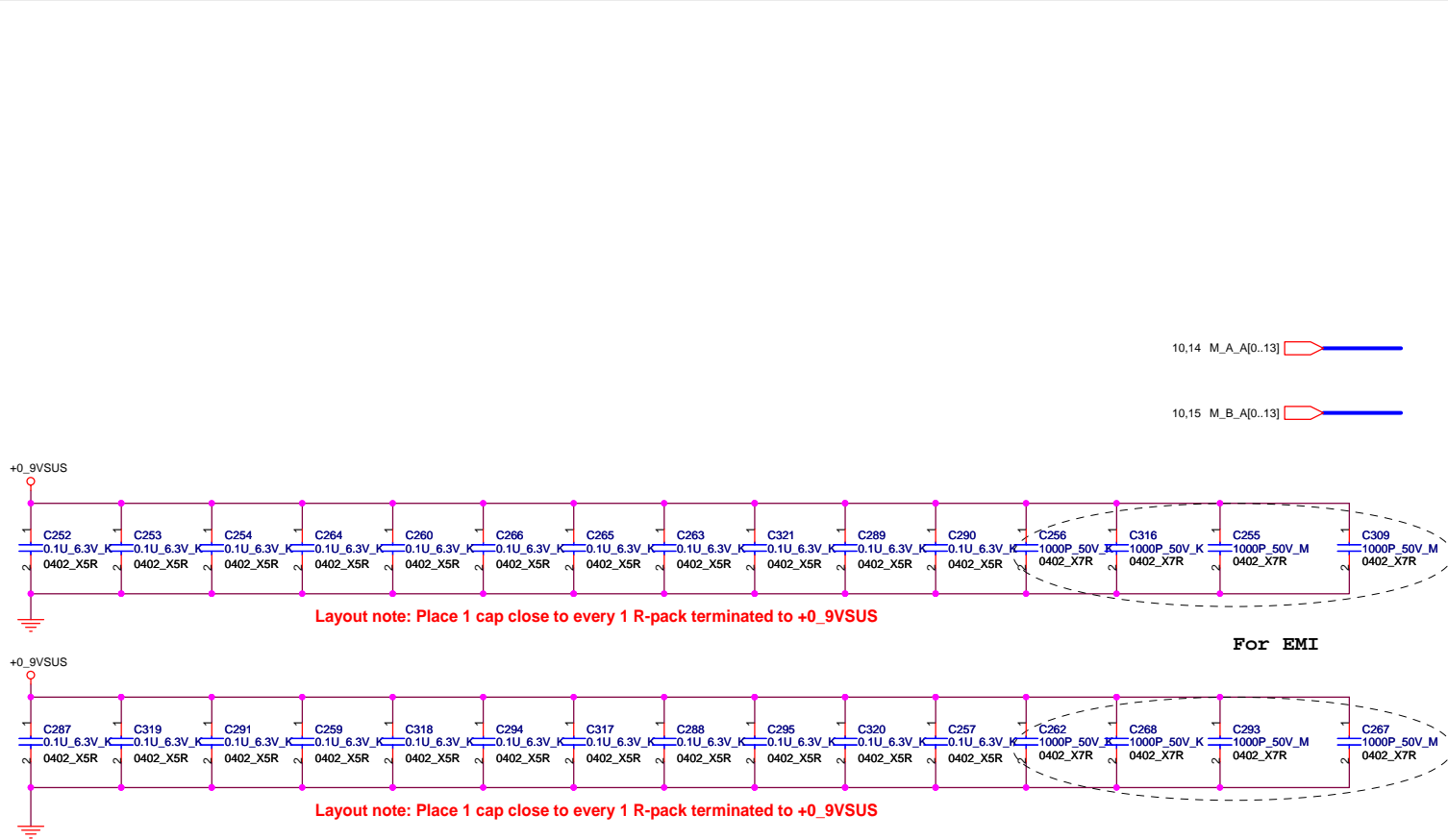
SA0 2 0402

SA1 2 0402

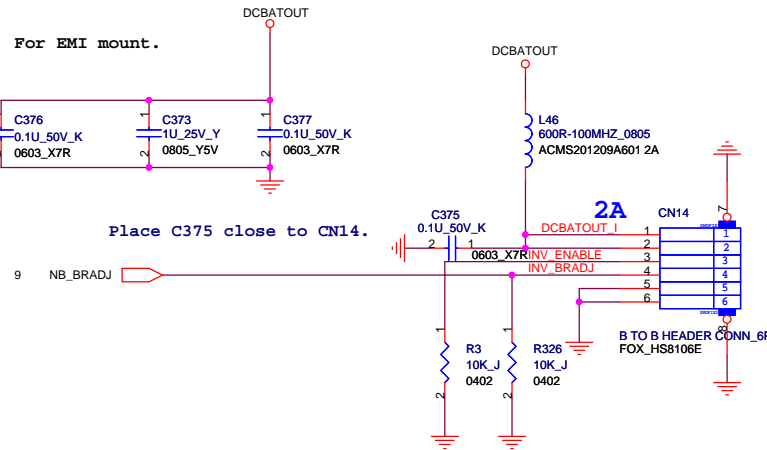
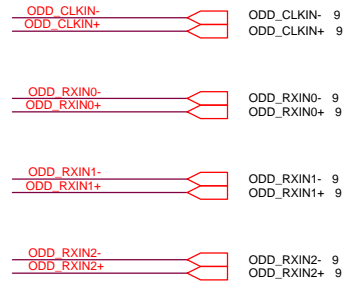
SA0 2 0402

SA1 2 0402

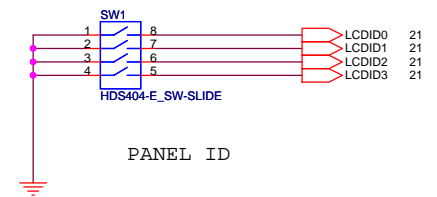
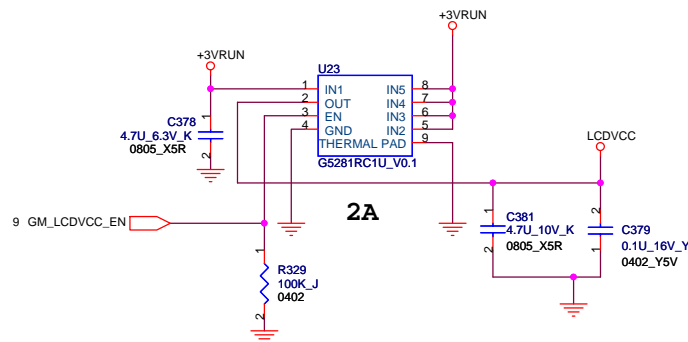
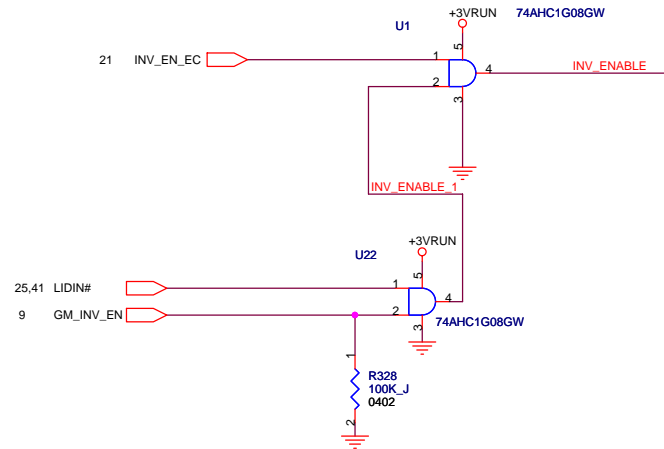
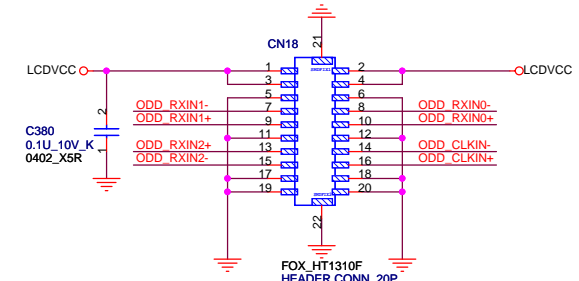




LVDS

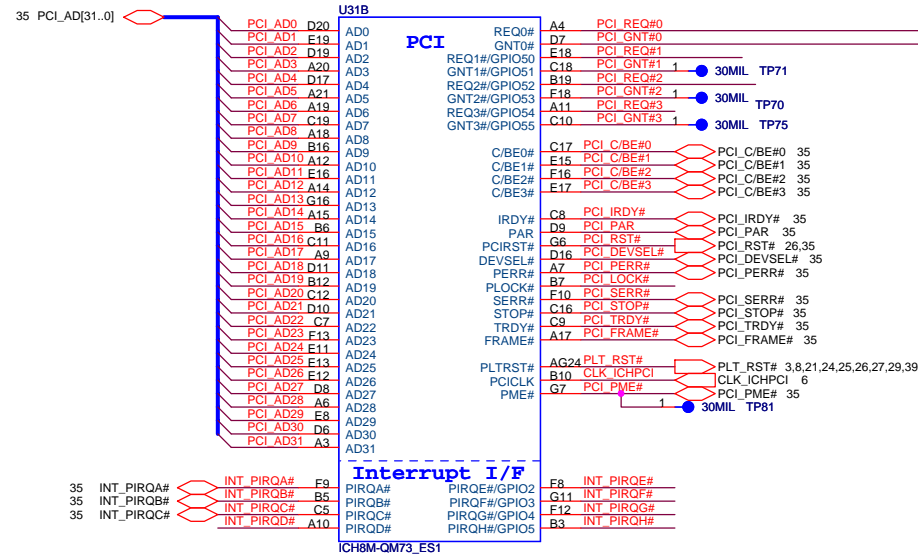


INVERTER CONN.

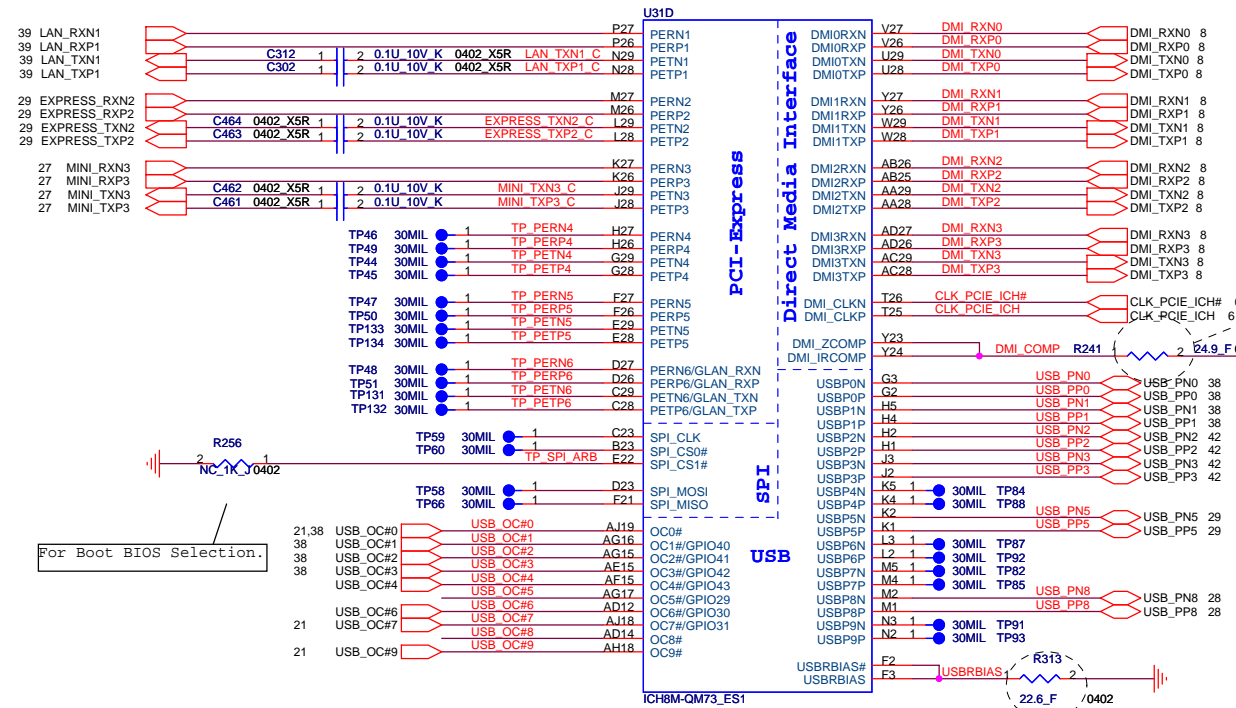


Type	WXGA	WXGA	WXGA
Size	15.4"W	15.4"W	15.4"W
Vendor	LPL	CPT	AUO
Device Name	LP154WX4	CLAA154WB05AN	B154EW02V7
Panel ID Check(3..0)	X001	X010	X001

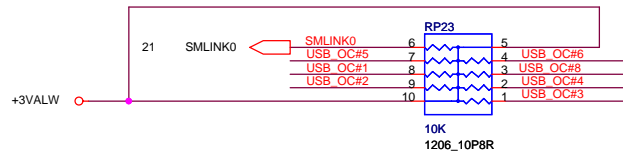
PCI Pullups



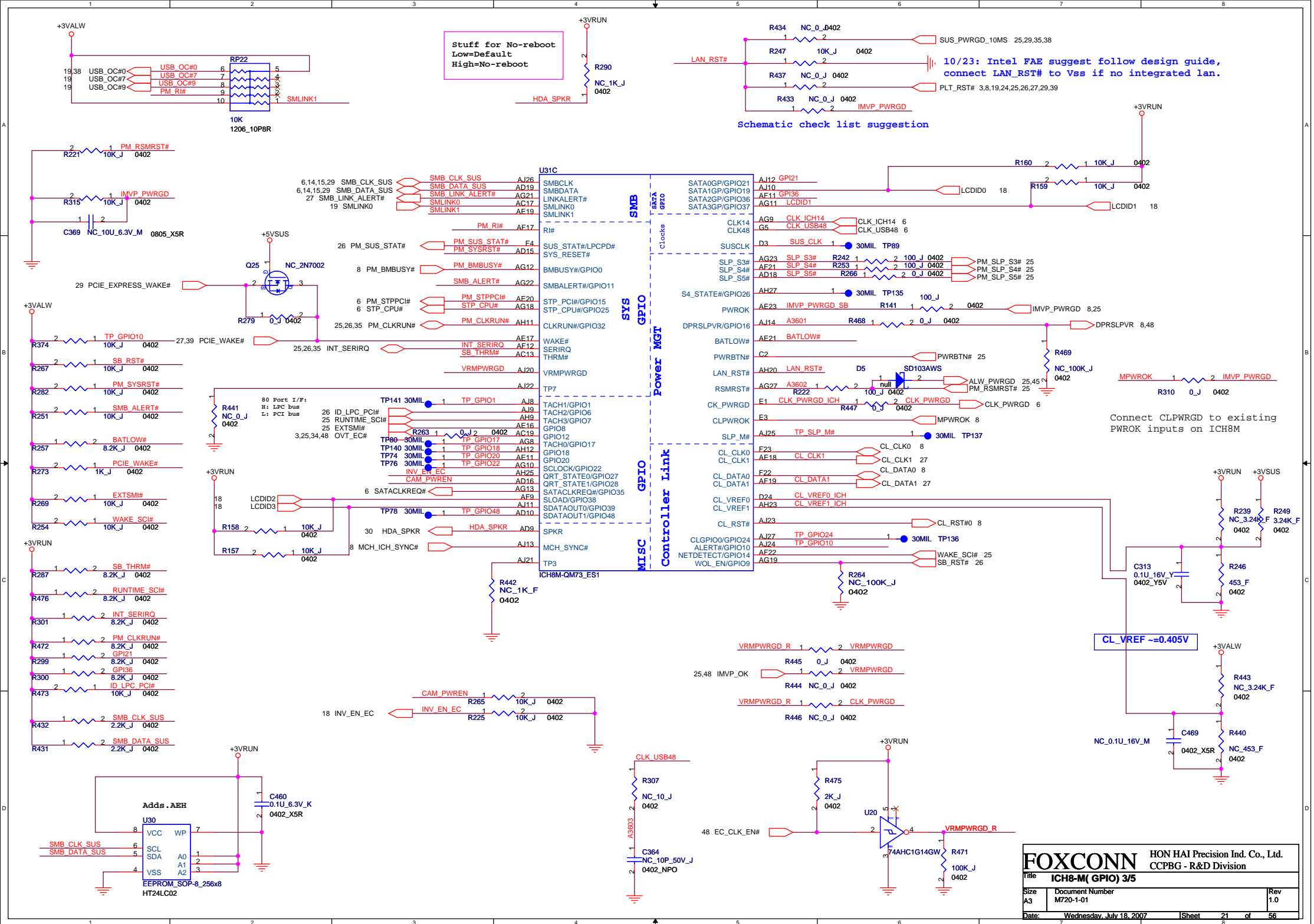
	GNT0#	SPI_CS1#
LPC(Default)	Hi	Hi
PCI	Hi	LOW
SPI	LOW	Hi

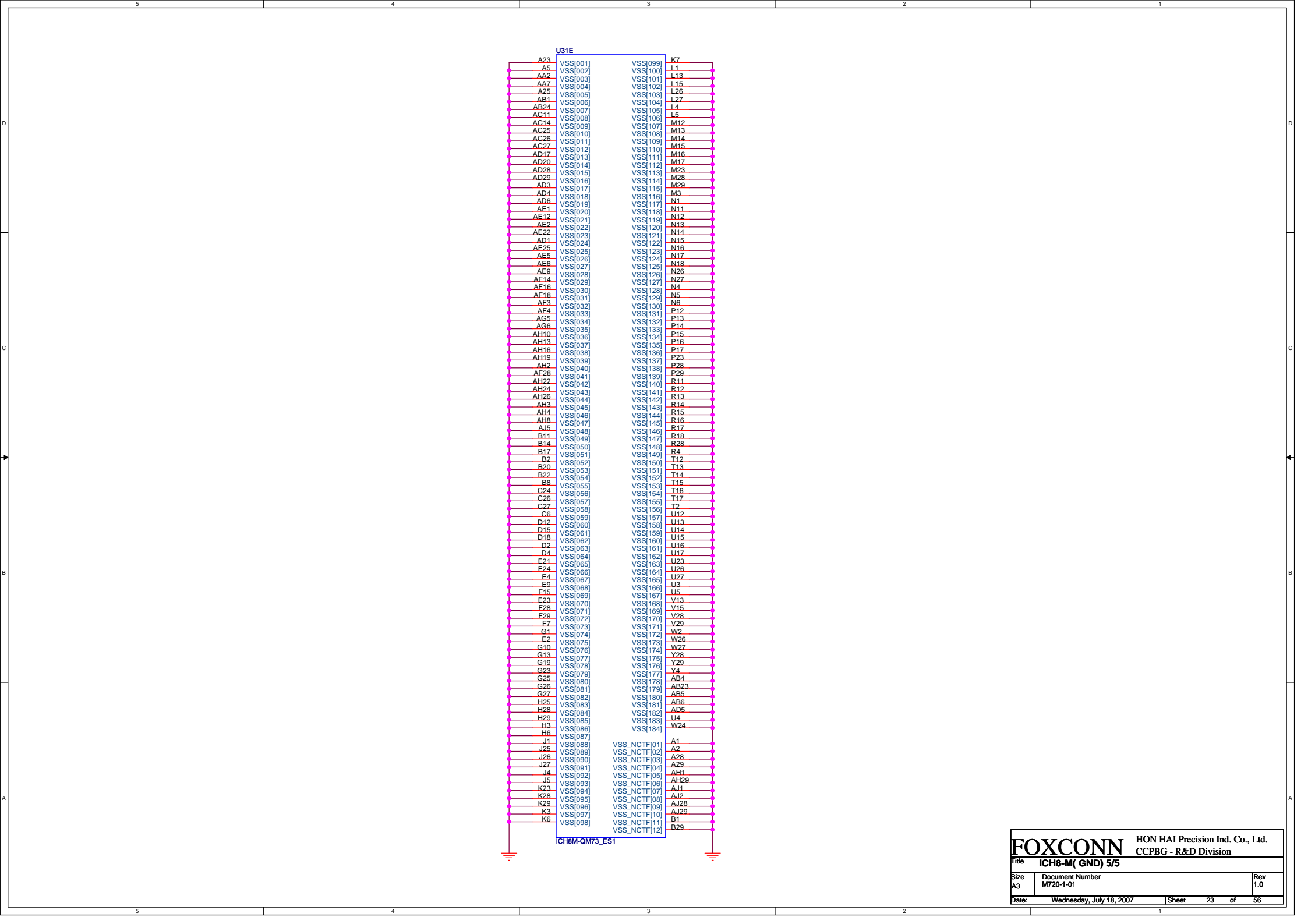


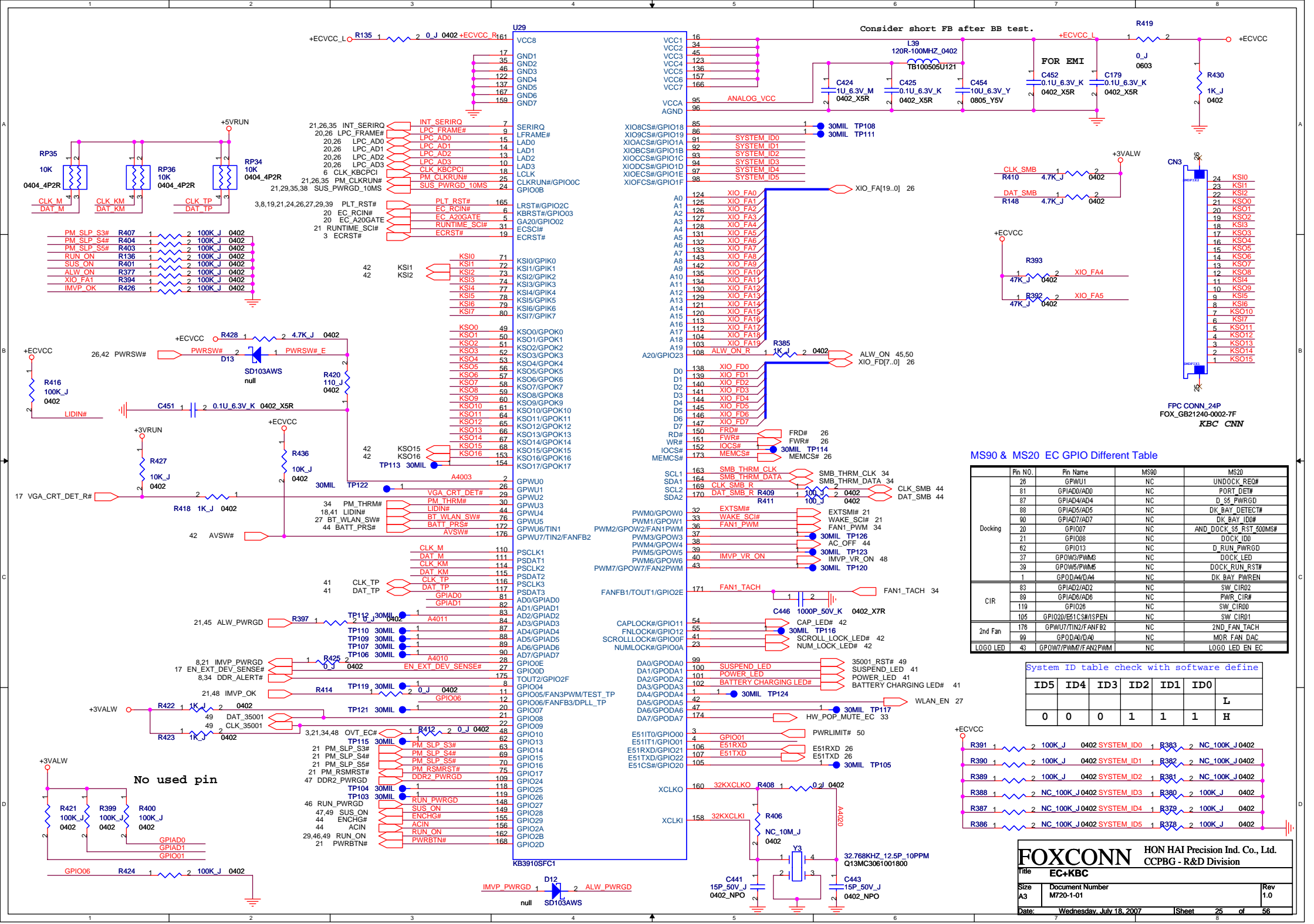
Place within
500 mils of
ICH



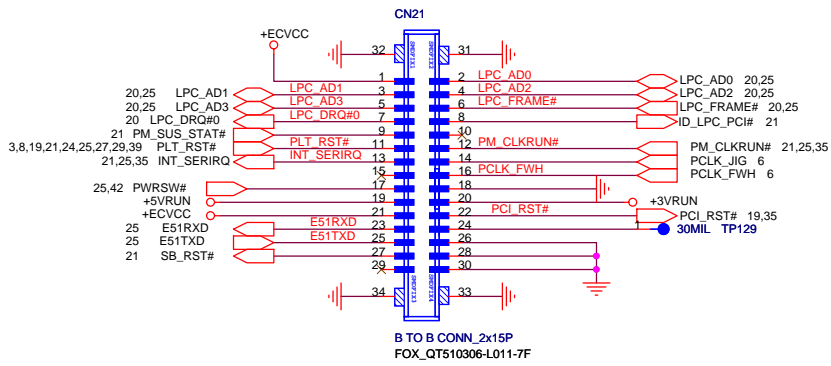
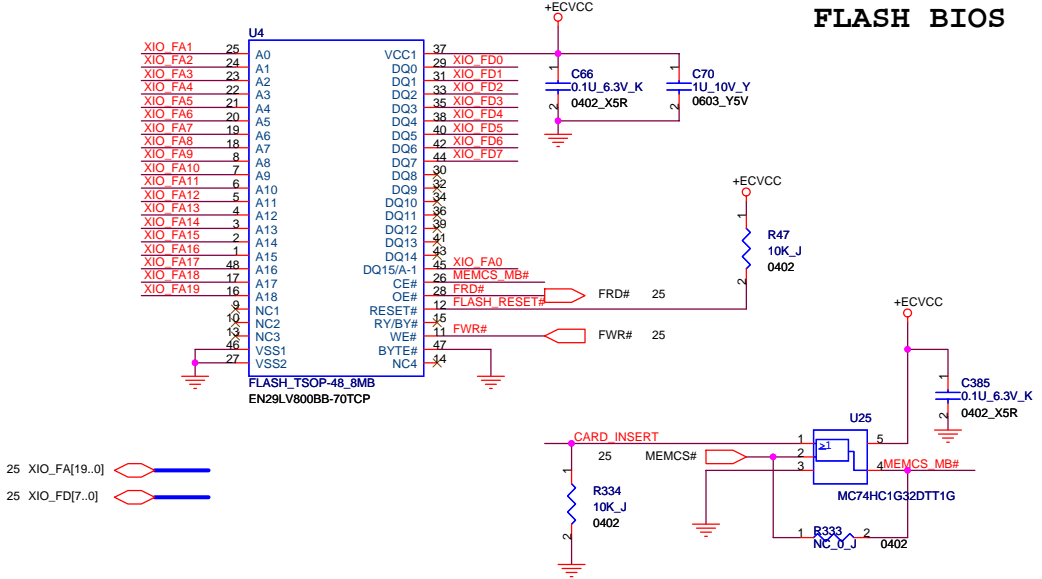
Place within 500 mils of
ICH and don't routing next
to high speed signals





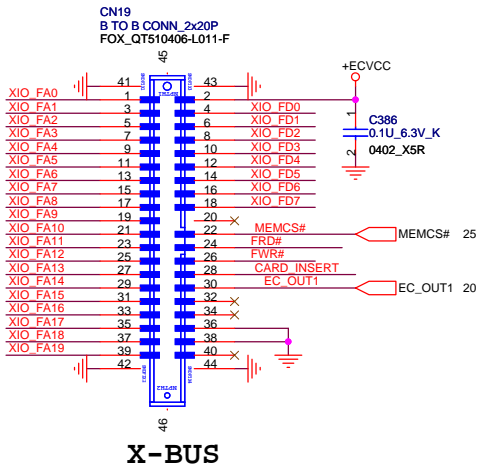


FLASH BIOS

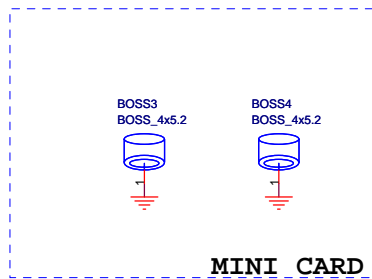


JIG-120

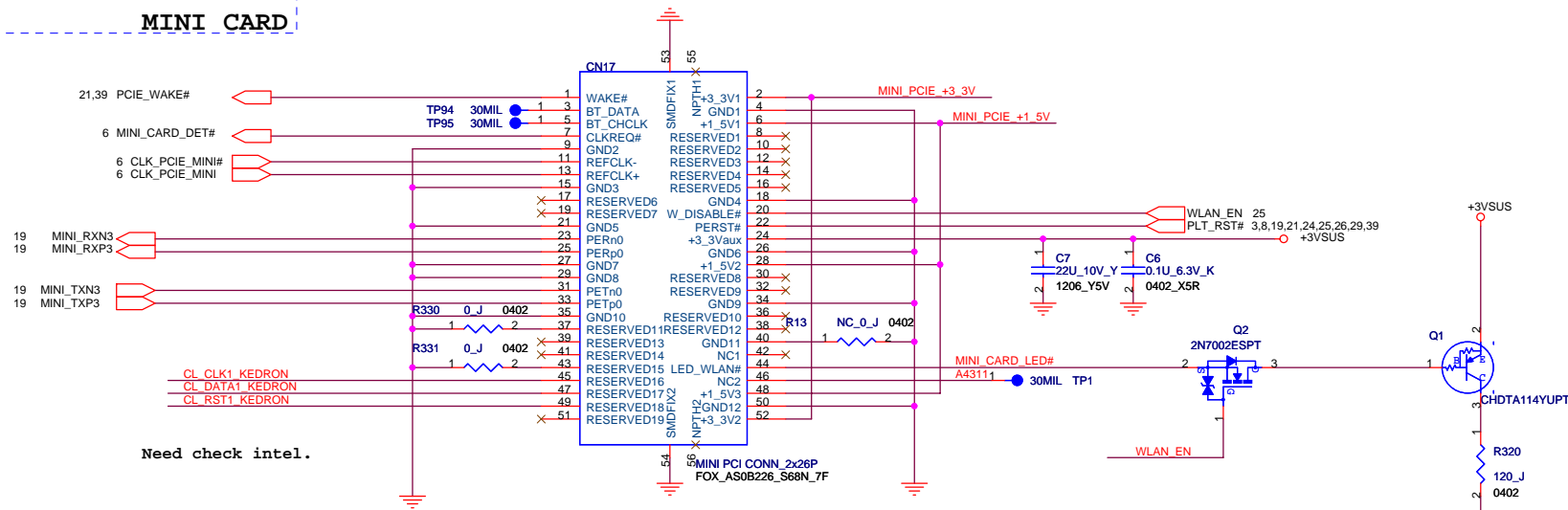
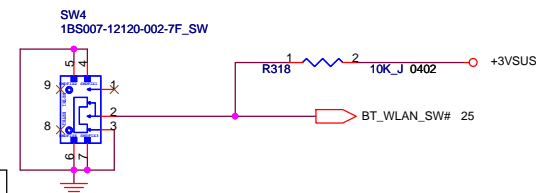
Pin 18 of JIG-120 is useless in debug board, so we let pin 18 NC.



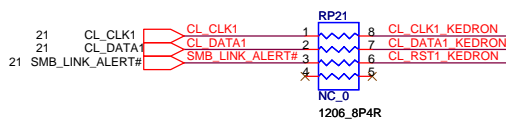
X-BUS



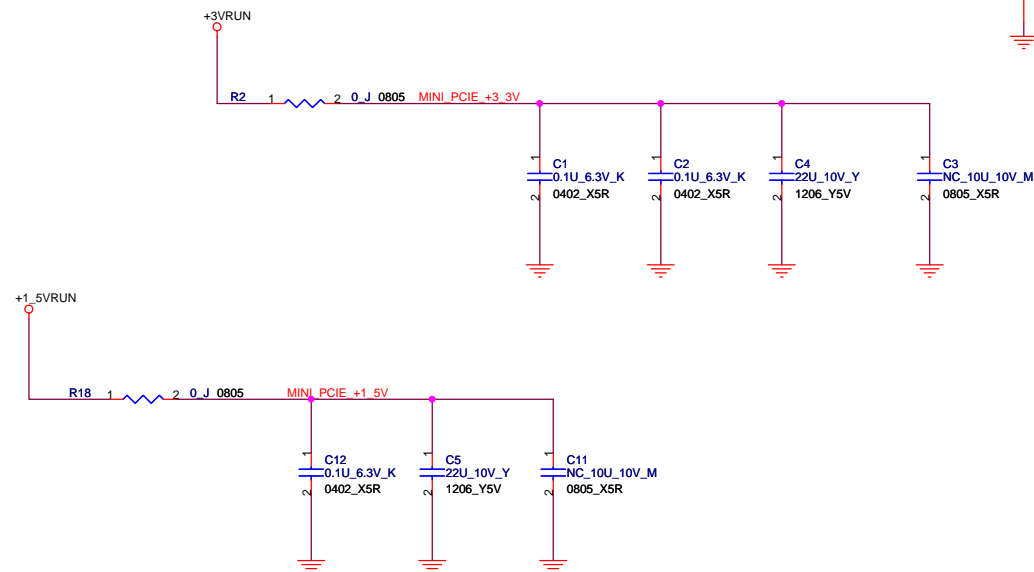
SW2 PIN8,9 : NPTH



Mini Card. WLAN



+1_5V=>0.5A
+3_3VAux=>0.33A
+3_3V=>1A

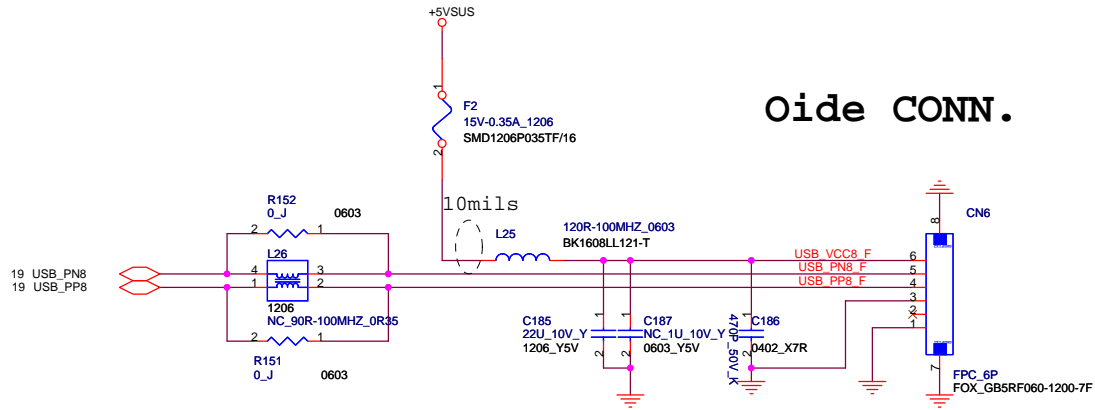


LED IF SPEC:
20mA (TYP) , 30mA (MAX)

Green

WLAN LED.

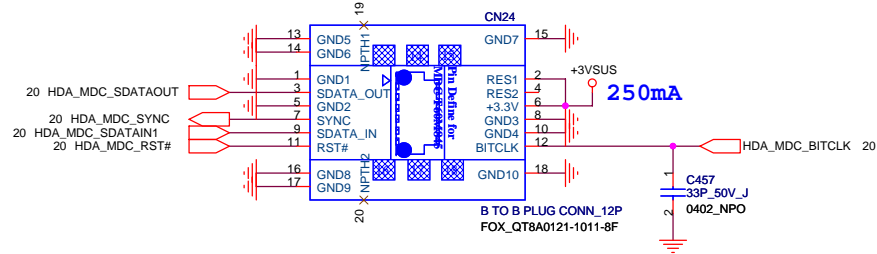
Oide CONN.

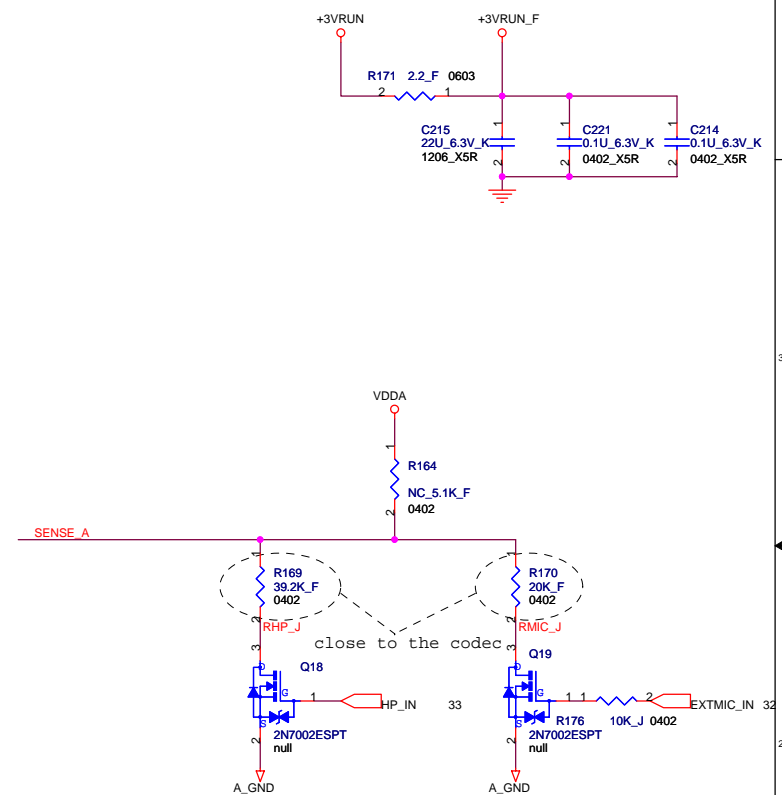


BOM Notice: OIDE_

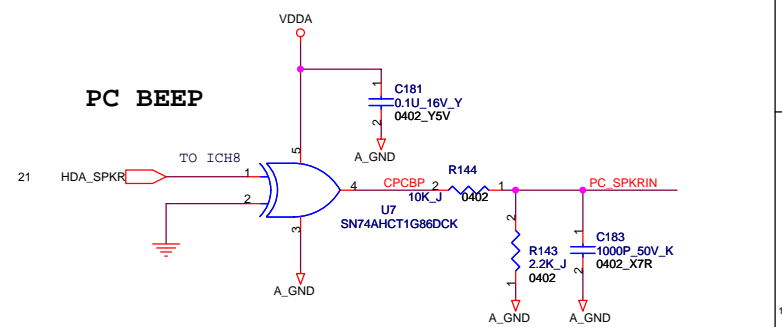
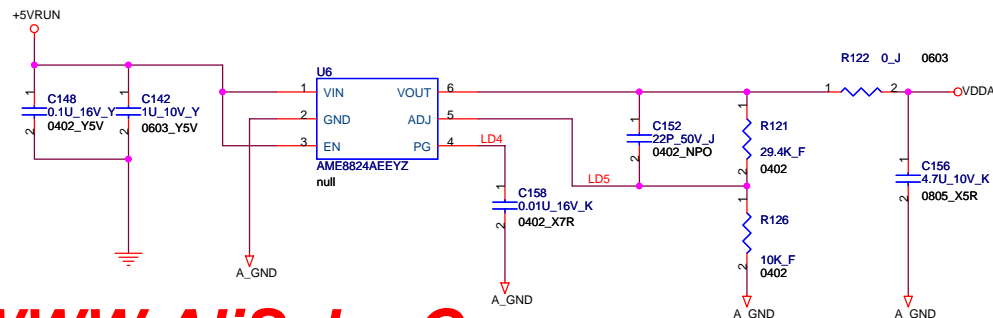
W/ Oide SKU	R151,R152,L25,C185,C186,F2,CN6	stuff
W/O Oide SKU	R151,R152,L25,C185,C186,F2,CN6	no stuff

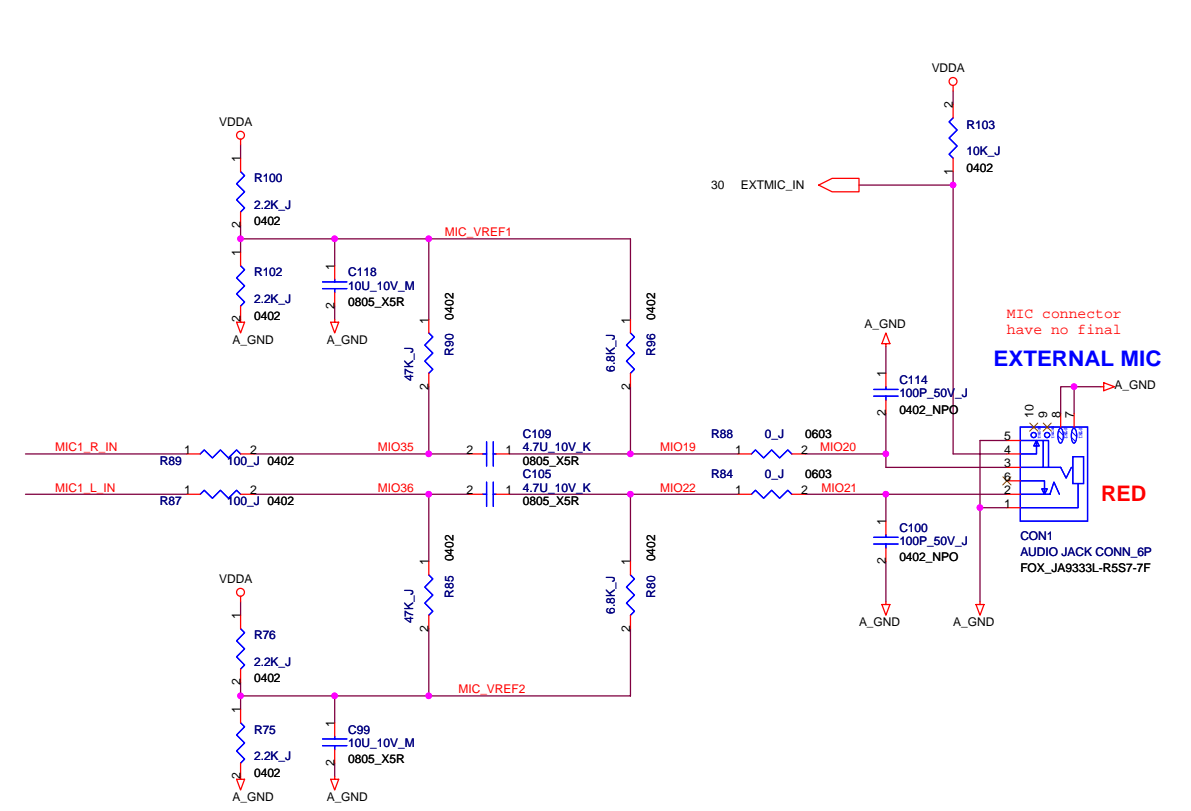
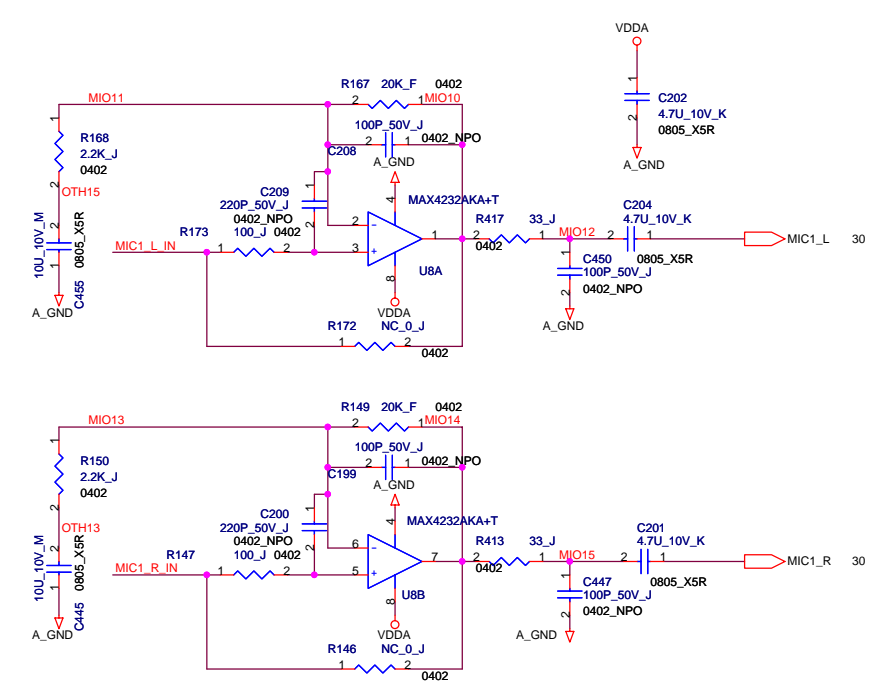
MDC CONN.

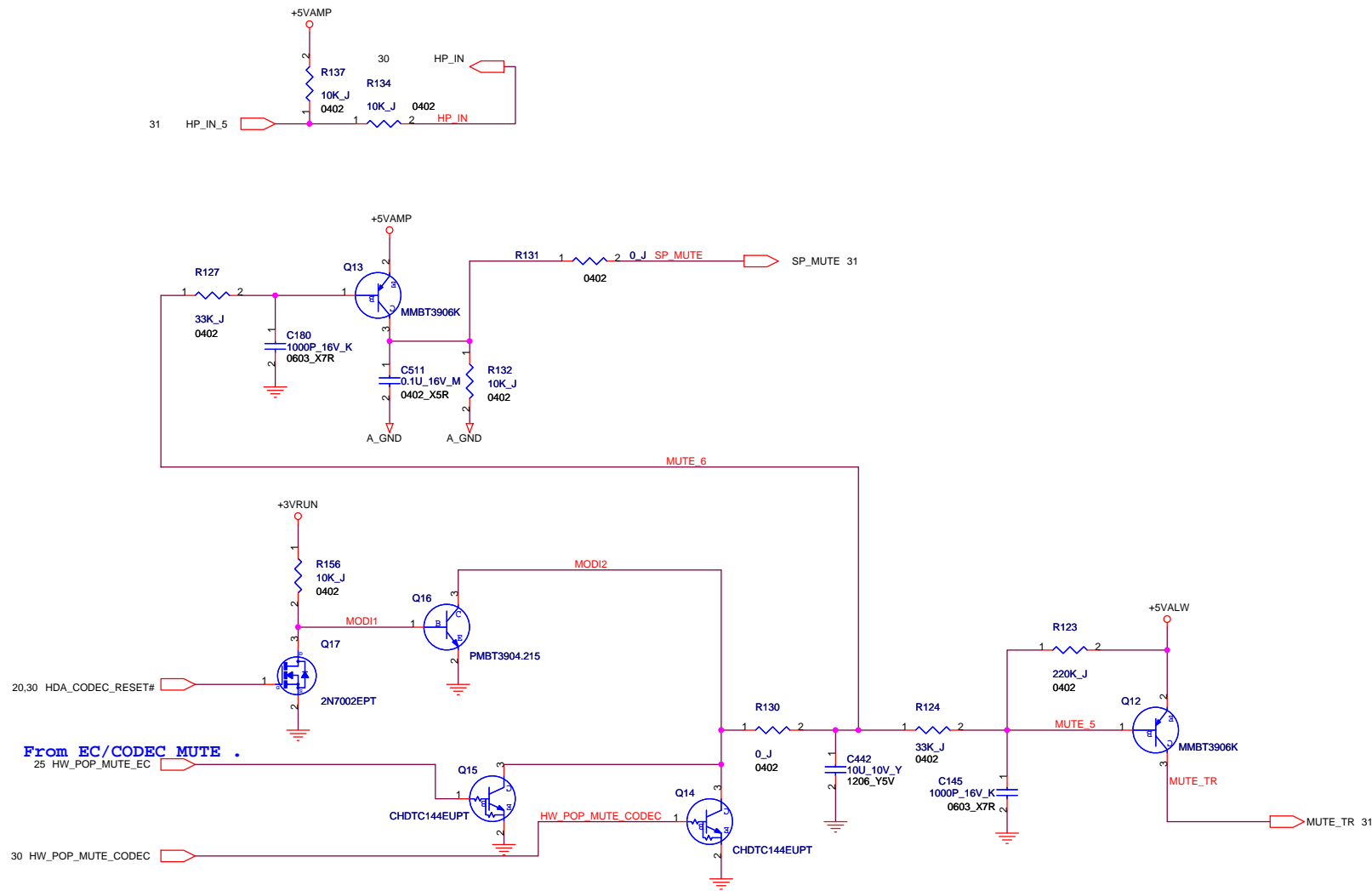




AUDIO POWER(Change to 4.75V/200mA)









The schematic diagram illustrates the SMBus interface circuit for the G781P81U. The circuit includes a +3V/RUN supply, a 4.7K pull-up resistor (R183), a 0.1uF capacitor (C224), and a 4.7K pull-down resistor (R190). The SMBus controller (U12) is connected to the G781P81U (U12) via a 30MIL bus. The G781P81U has pins for SMBCLK, SMBDATA, and THERM#.

TP43 30MIL 1
TP42 30MIL 1

R183 NC_4.7K_ 0402
C224 NC_0.1U_16V_M 0402_X5R
R190 NC_4.7K_ 0402

U12
VCC SMBCLK 8
TS11 SMBDATA 7
TS2 ALERT# 6
THERM# GND 5

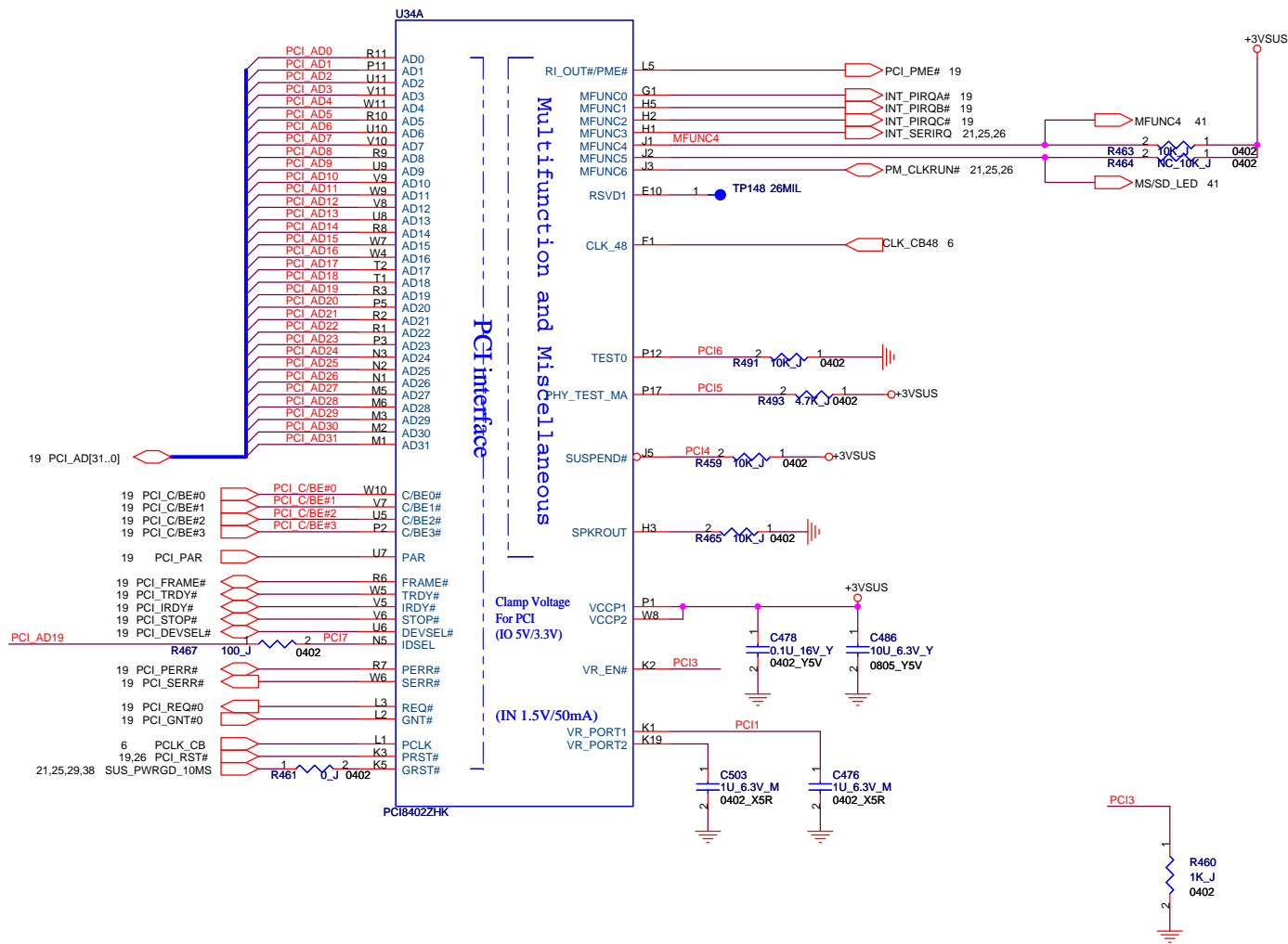
NC_G781P81U

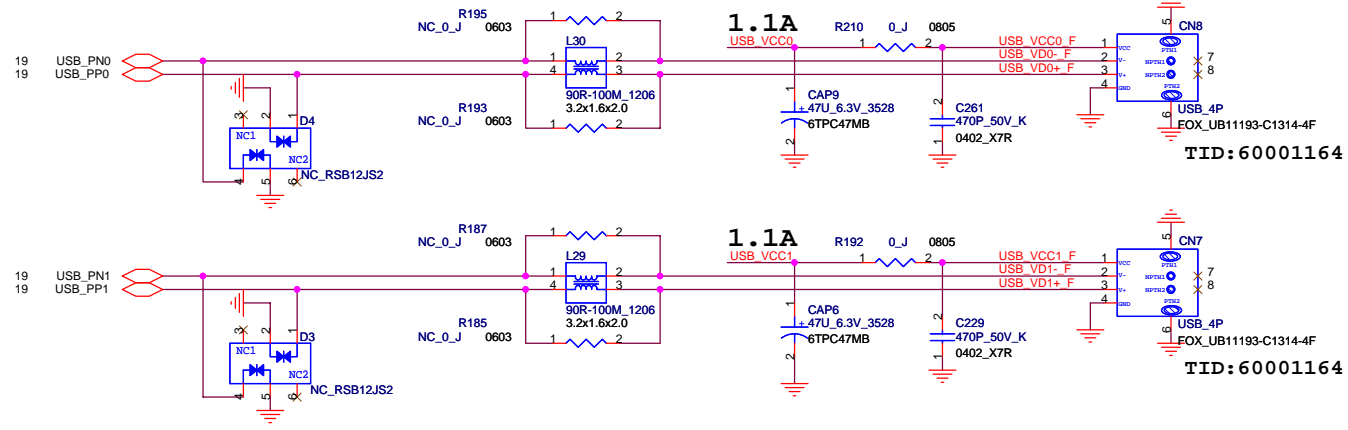
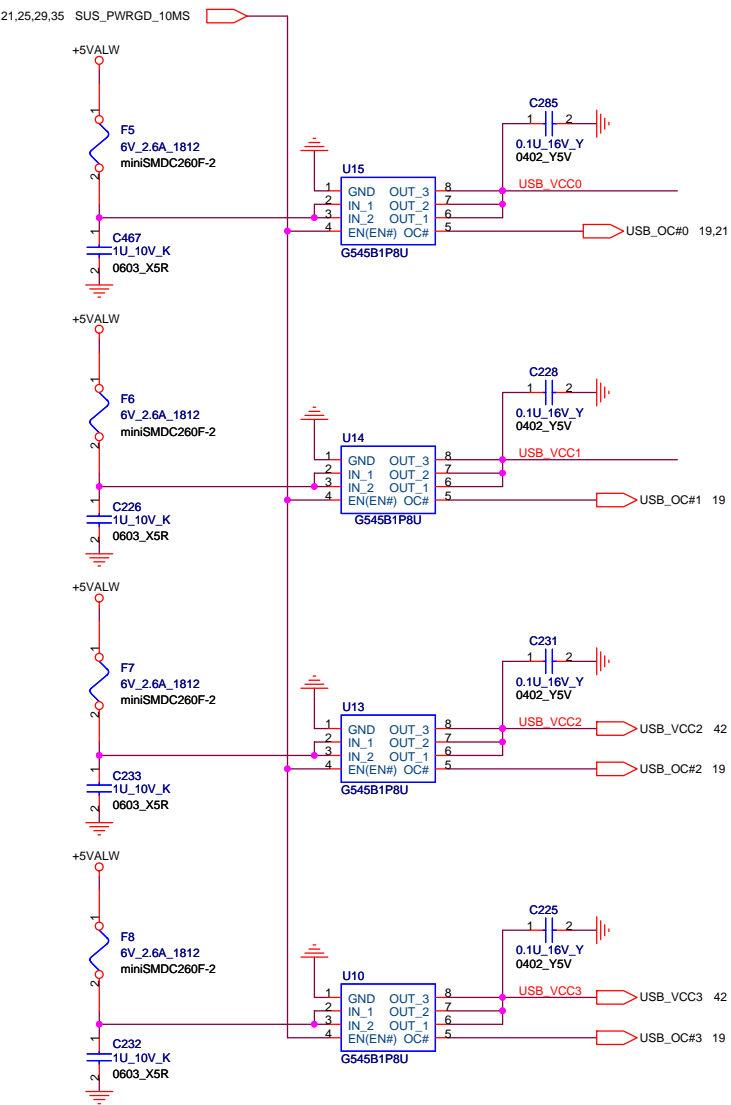
SMB_THRM_CLK 25
SMB_THRM_DATA 25
DDR_ALERT# 8.25

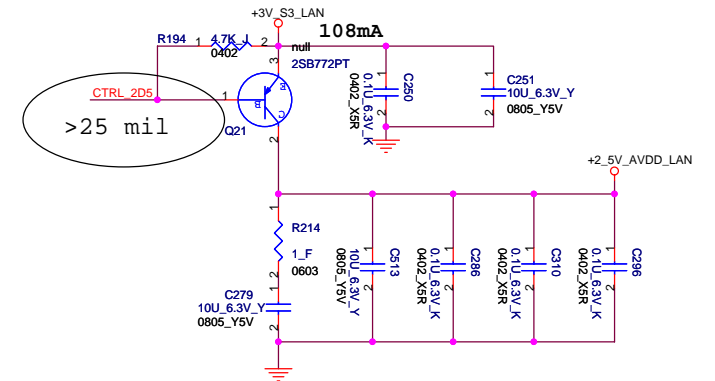
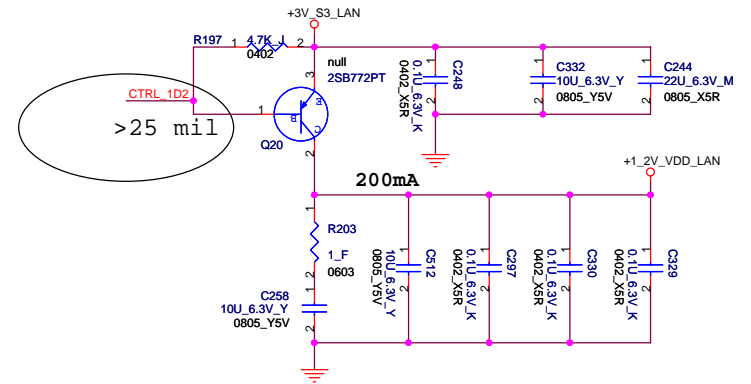
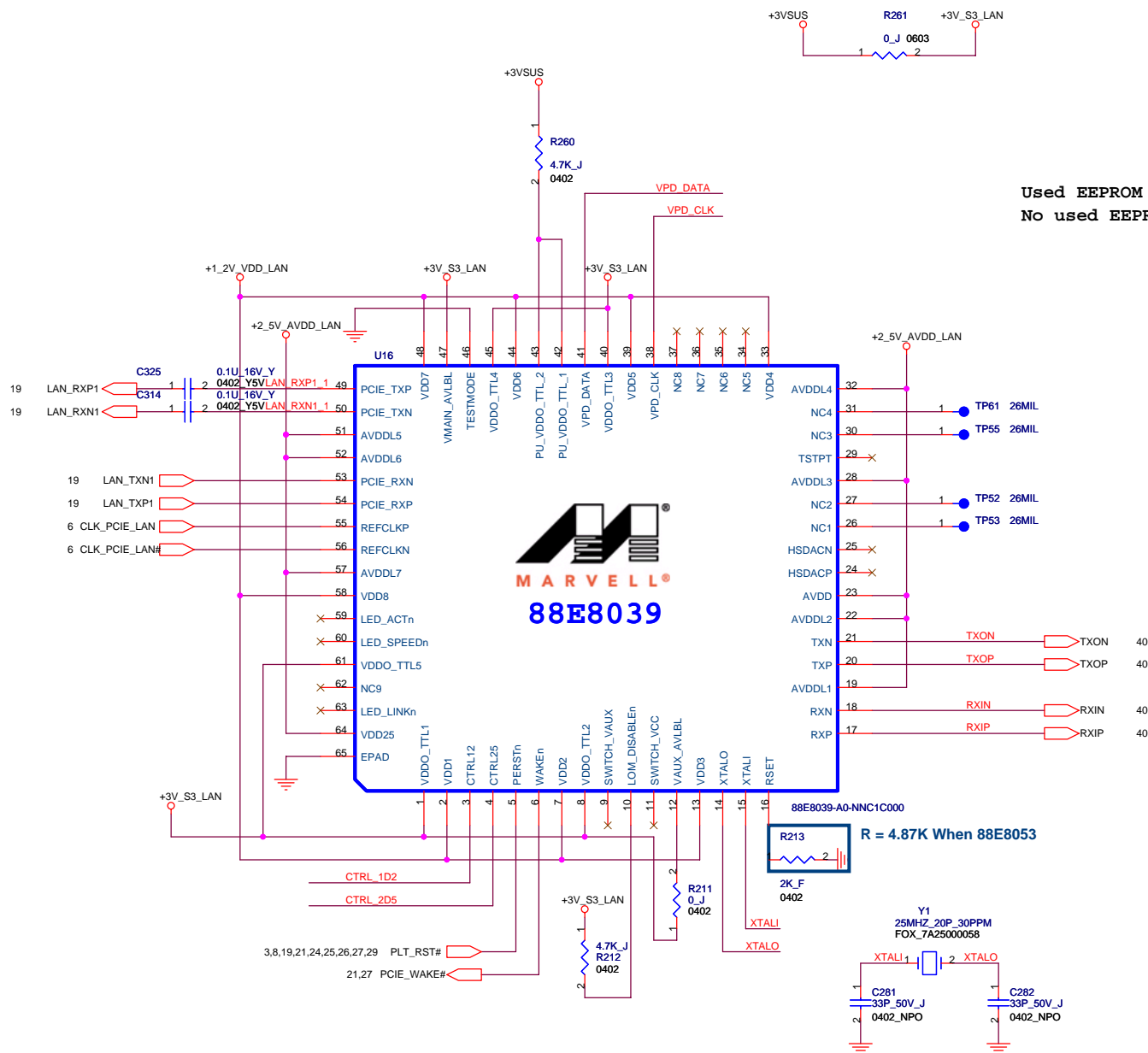
Close to CN25

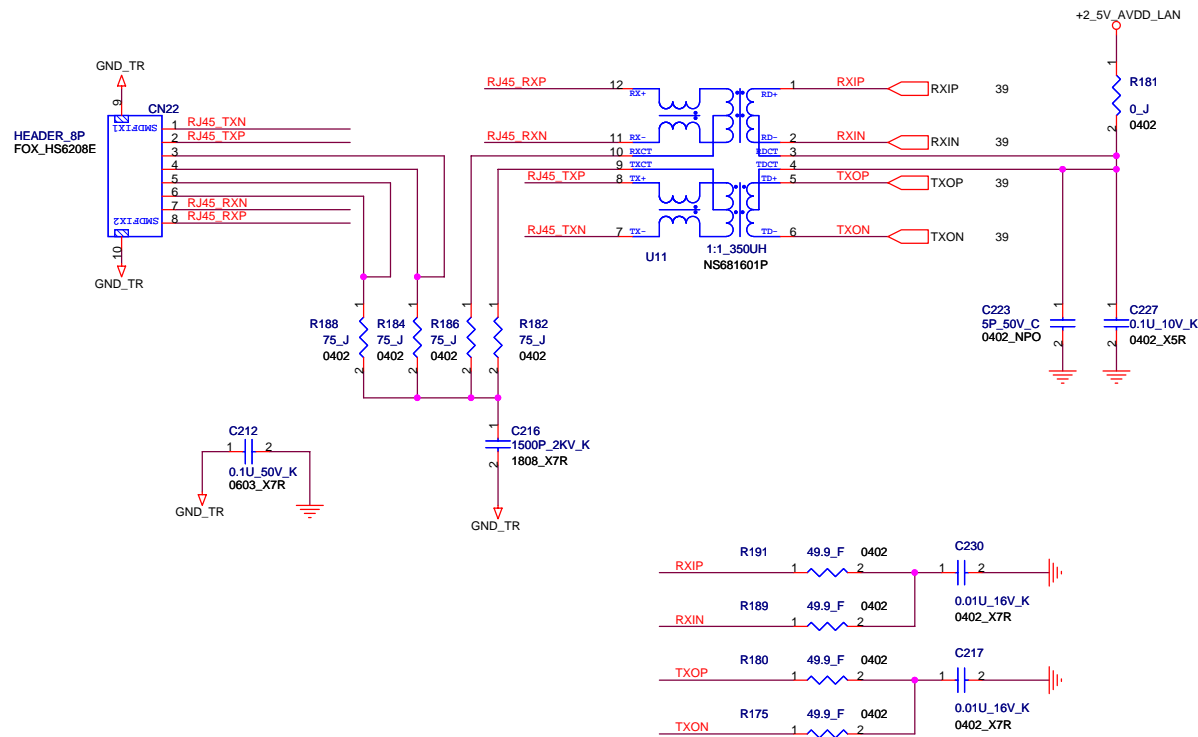
[illegible]

Close to U24



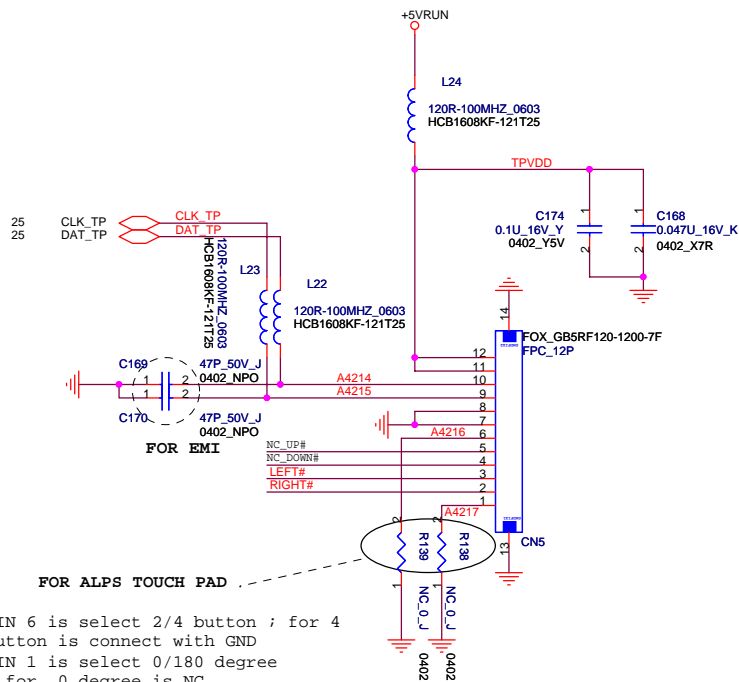




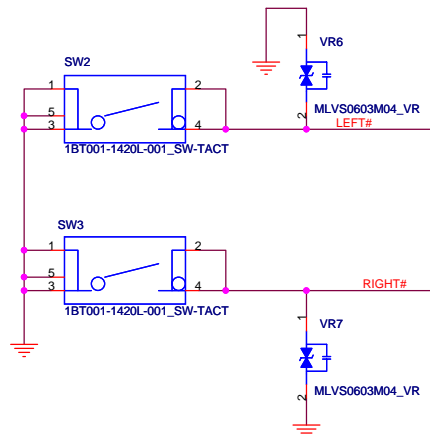


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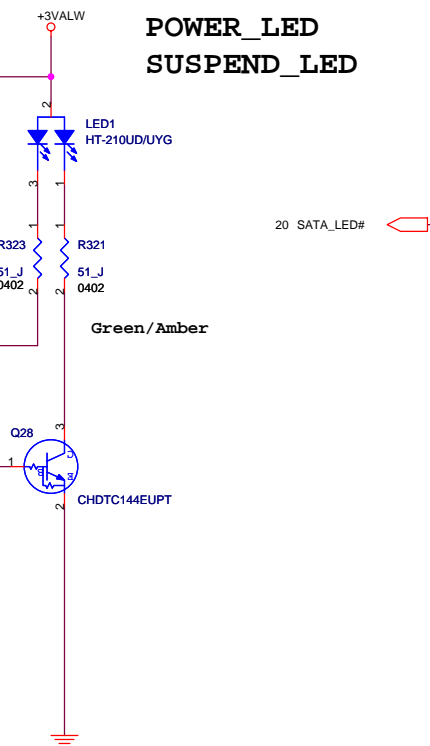
Touch Pad CONN.



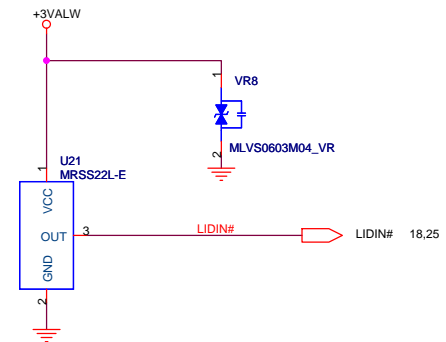
TP_LEFT Button



TP_Right Button



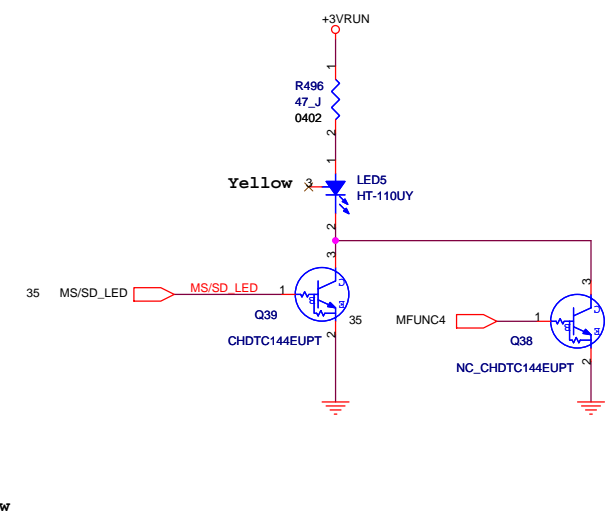
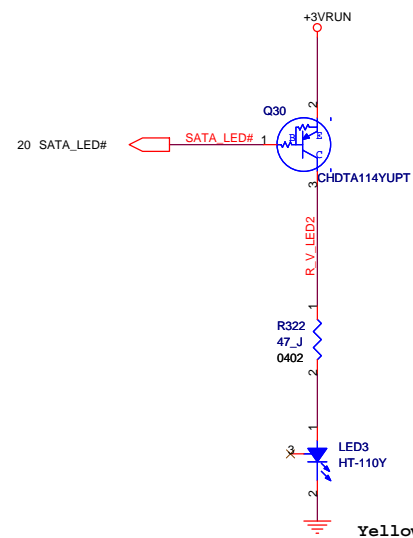
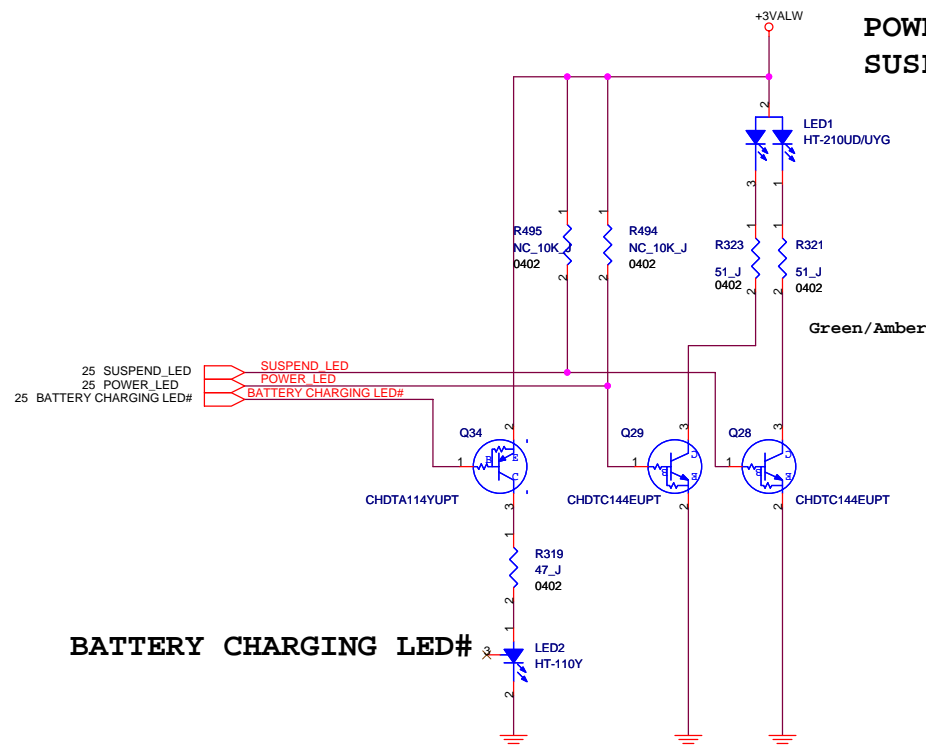
LID Switch



POWER_LED SUSPEND_LED

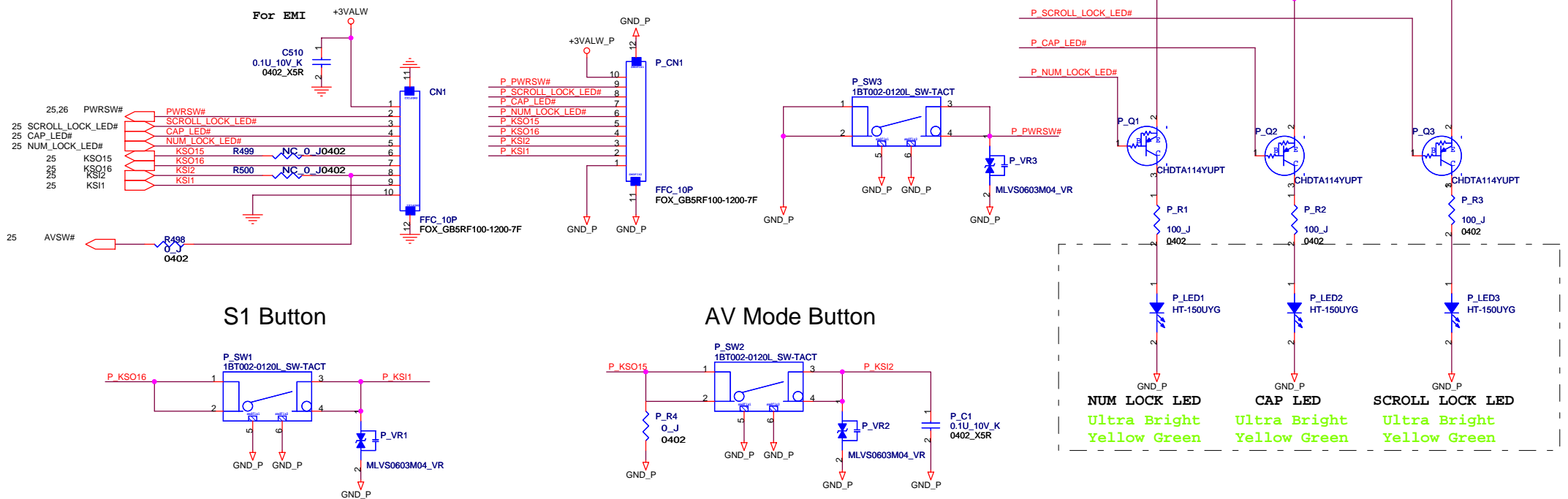
SATA_LED#

MS/SD LED

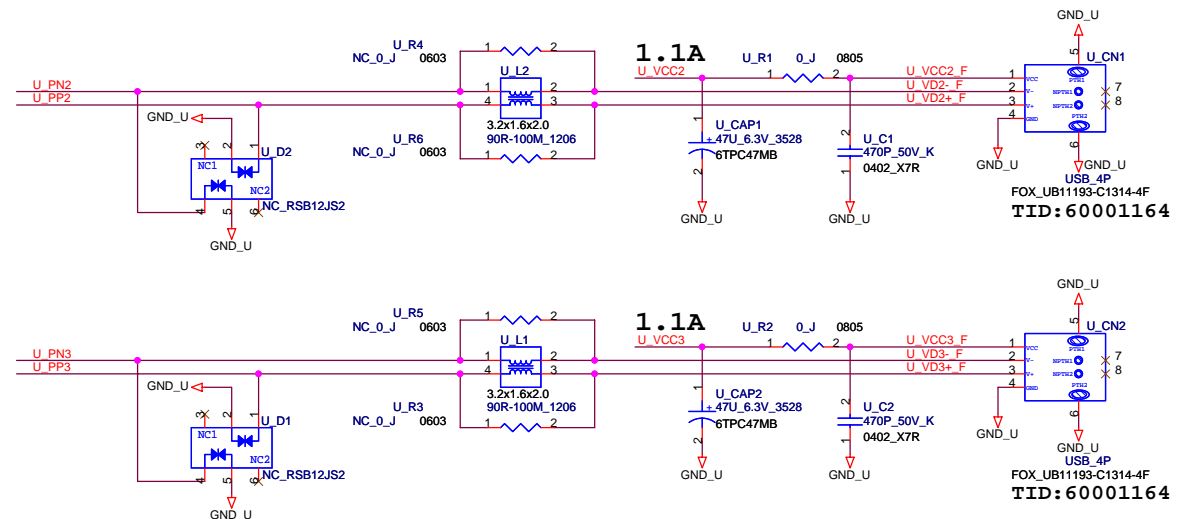
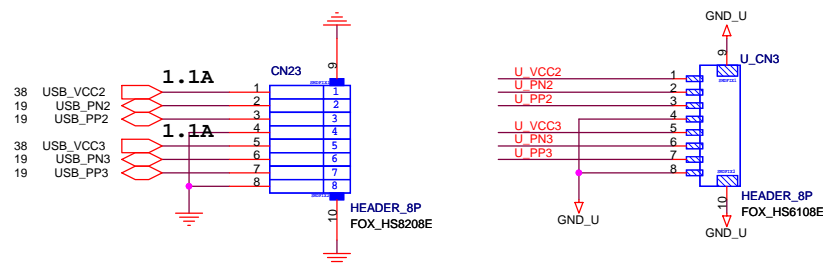


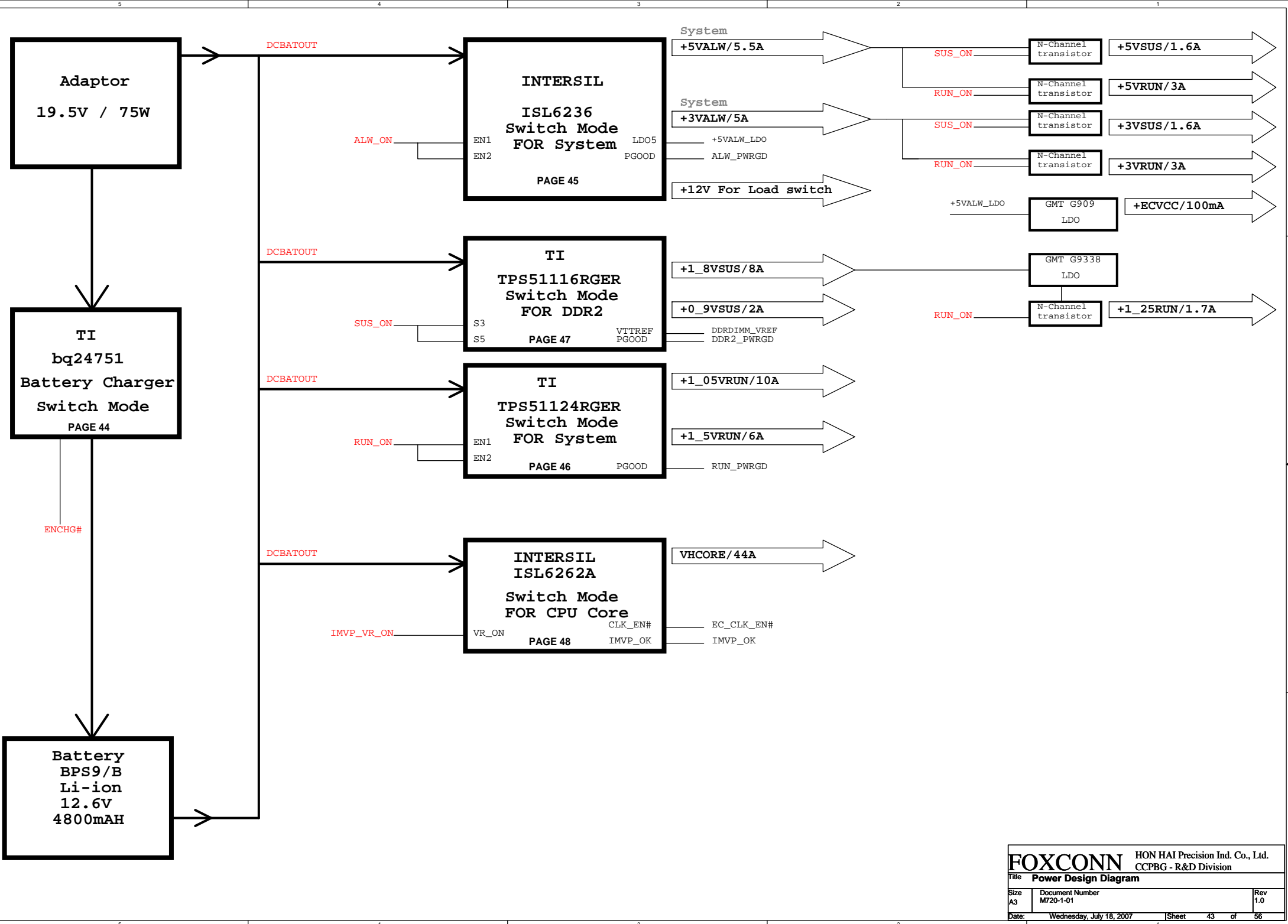
BATTERY CHARGING LED#

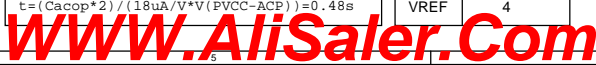
Power Button Board

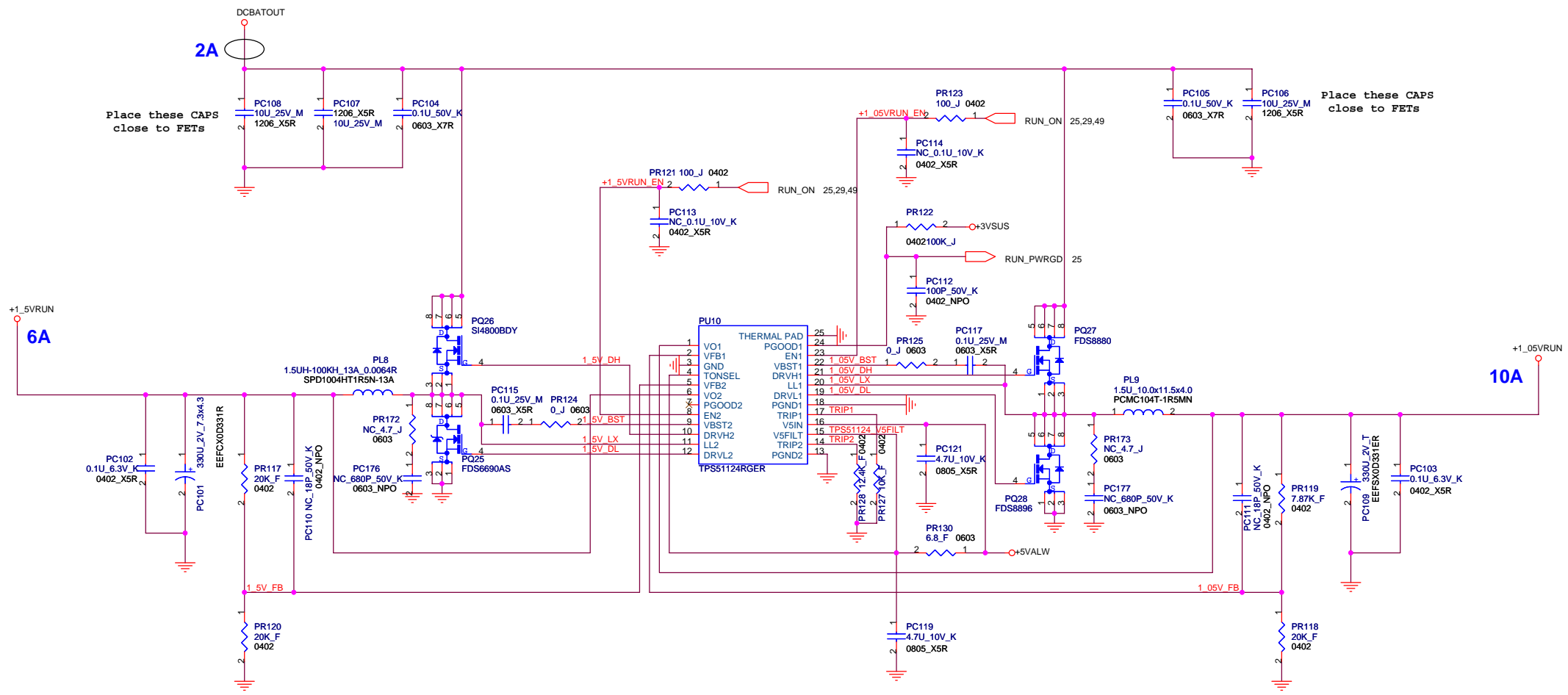


USB Board



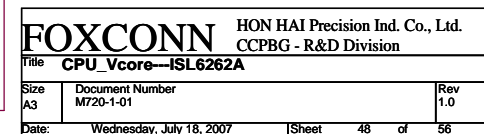


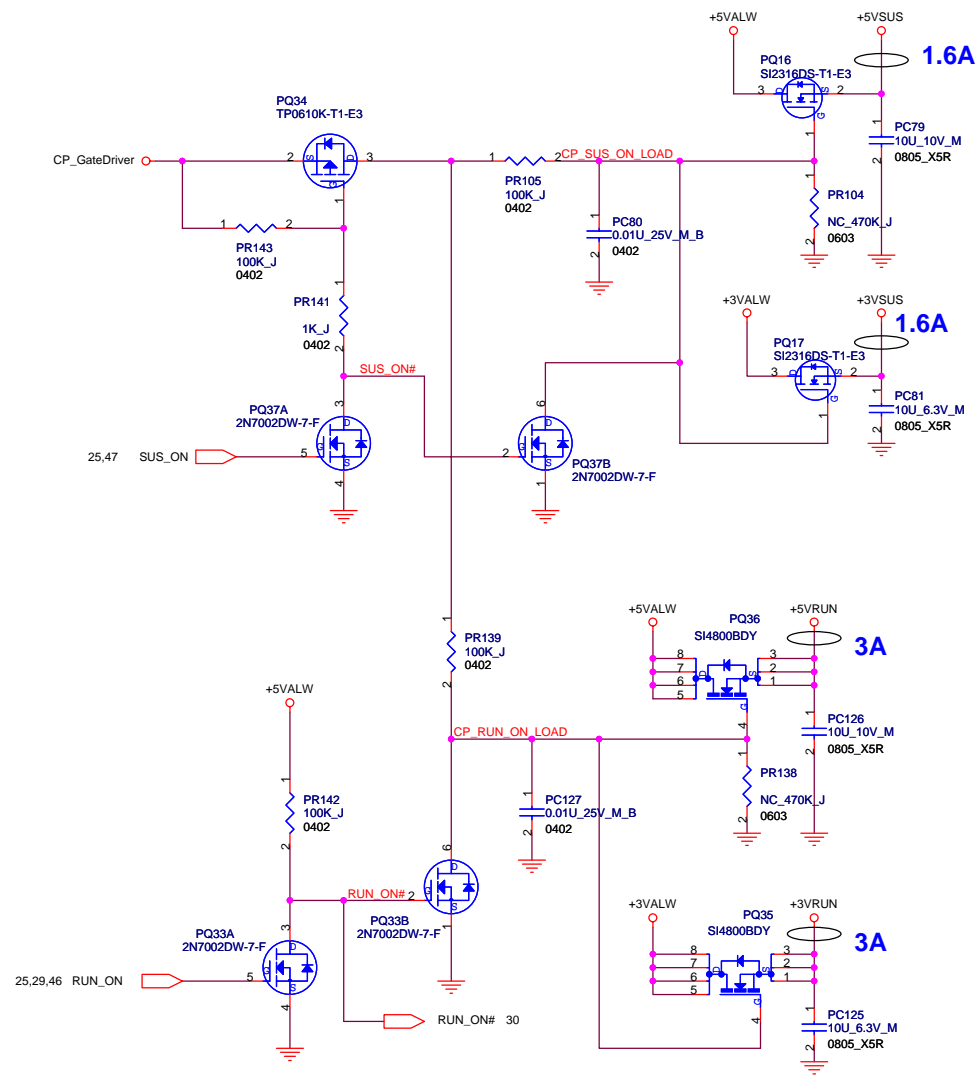




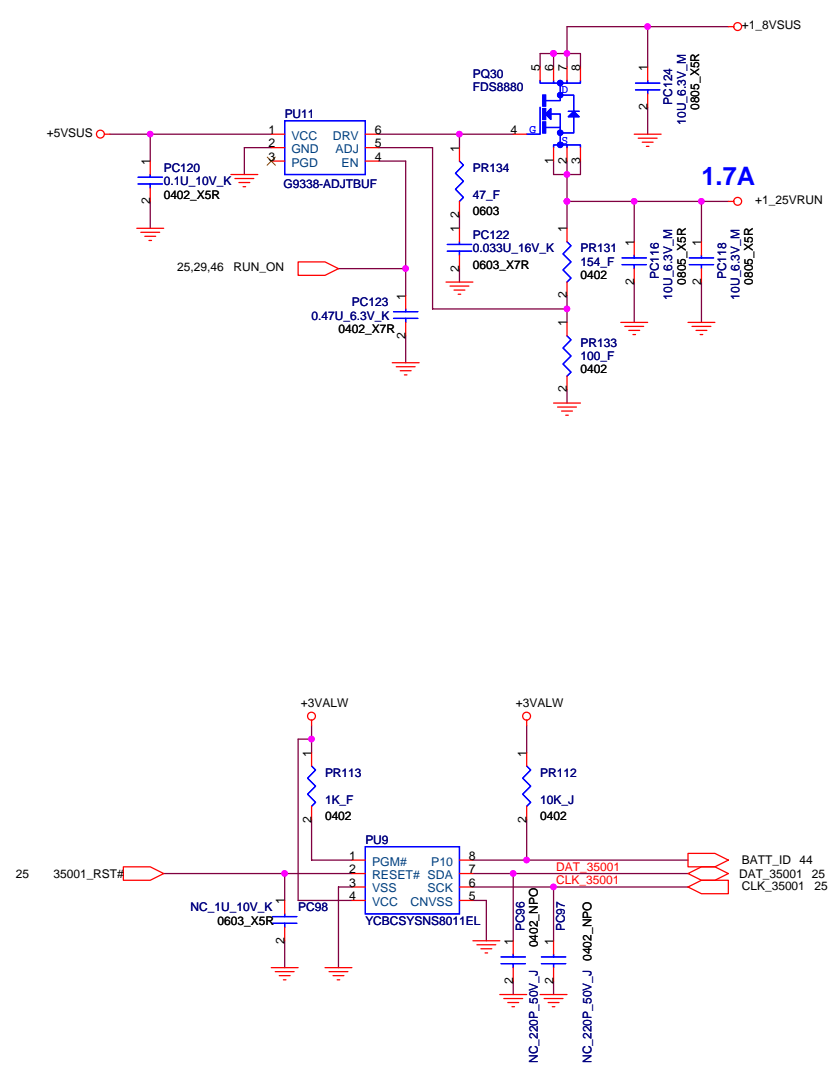
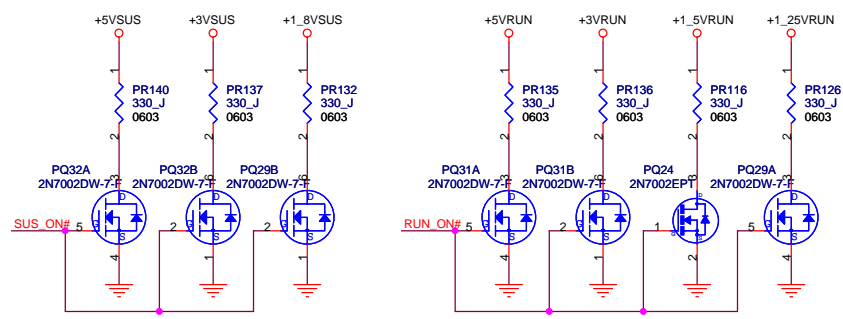
Setting +1_5VRUN OCP trigger point to 10.6A

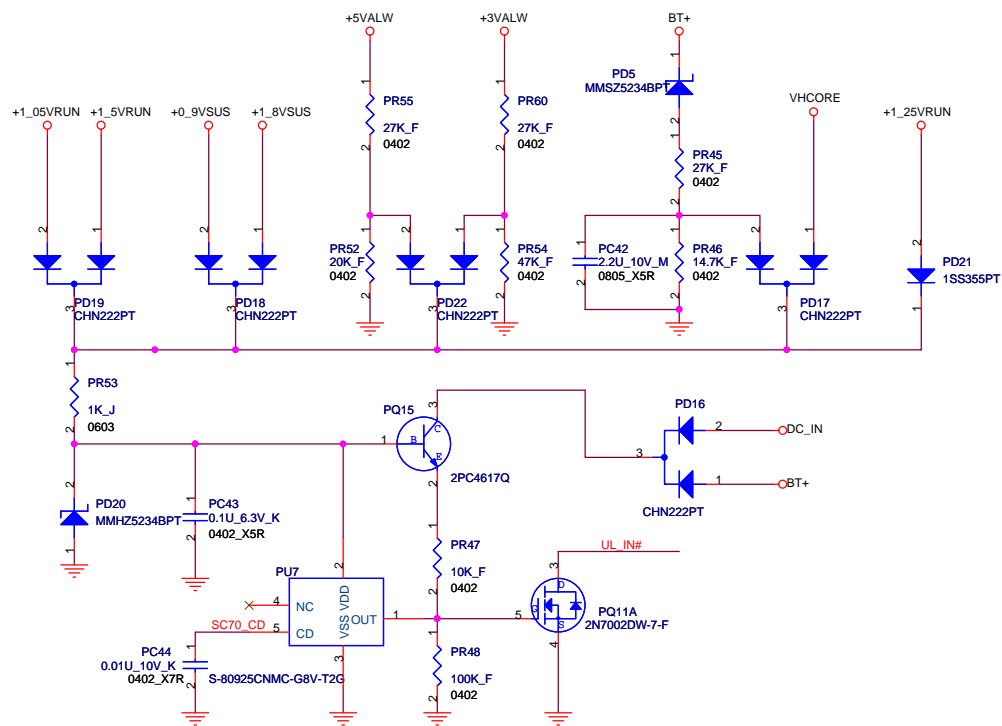
Setting +1_05VRUN OCP trigger point to 14.2A



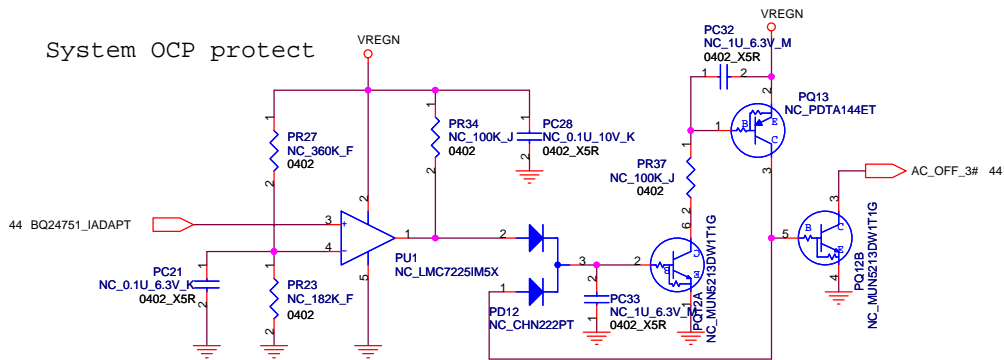


Discharge circuit for power-off

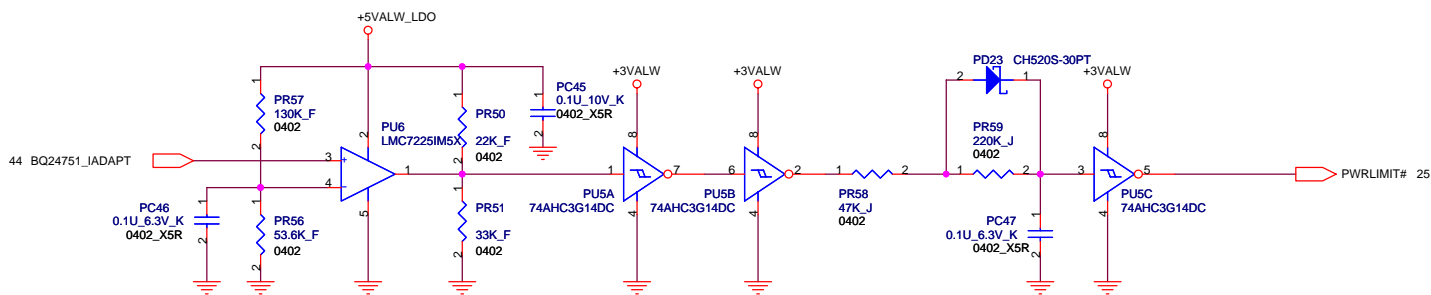


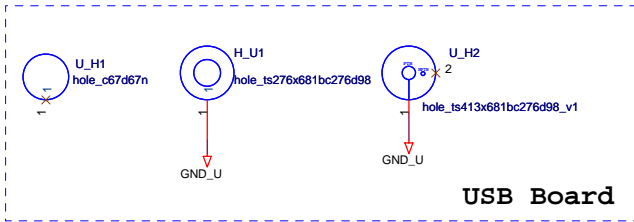
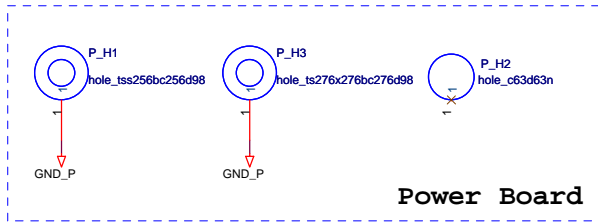
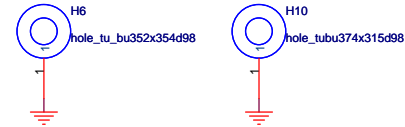
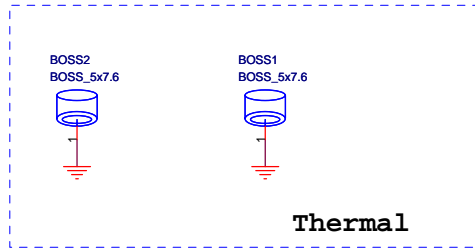
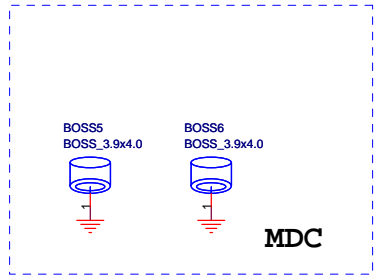
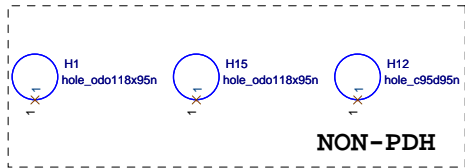
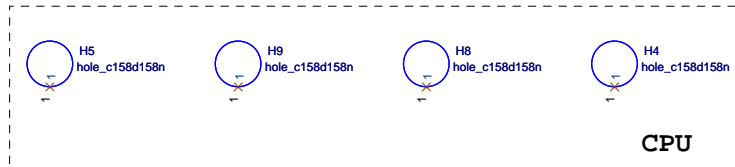


System OCP protect



Setting System OCP trigger point to 4.2A





M720 EVT

(2007/02/14)

P.27 Change Q104 for DTC144 to 2N7002,delete R2217
P.38 Change U64,U65,U66,U69 from G5250 to G545

(2007/02/26)

P.41 Add Q158 for MS/SD LED.

(2007/02/27)

P.49 Add PC147 and PC149 0.01uF_25V 0402 for soft start circuit.
P.50 Add DC_IN OVP, DC_IN UVP, System_OCP and System_SCP protection circuit.
P.50 Change PR270 from 33K_F 0402 to 53.6K_F 0402 for Setting PWRLIMIT# trigger point to 3.64A

(2007/02/28)

Delete GMCH power
P.12 Delete PJ13 for +VGFX_CORE power change to +1_05VRUN.
P.20 Delete TP263,add R1790 pull down for LAN_RST function on intel ICH8M request.
P.49 Delete PR243~PR245,PQ8 for GMCH power IC delete.
P.50 PD21 from CHN222PT change to 1SS355PT for GMCH power IC delete.

(2007/03/05)

P.50 Change DC_IN OVP, DC_IN UVP, System_OCP and System_SCP protection circuit to no mount.

(2007/03/06)

For layout request swap L69,L75,L80,LVDS signal.
P.44 Change PF1.
P.48 Change PU8 pin25 from VHCORE_AGND to GND for layout convenient

(2007/03/07)

For layout request swap U_L1,U_L2 signal.

(2007/03/08)

Update LED tepe for ID.
P.25 Update system ID table.
P.42 Add S1/S2 function,Change CN22,P_CN1 to 10pin.
P.44 Add PR7 10K_F 0402 and PC38 0.1uF_50V 0603 X7R for DC_IN soft start circuit.
P.46 Change PL11 from MPO104-1R5 to PCMC104T-1R5MN
P.49 Add PR220 1K_J 0603 for soft start circuit.
P.50 Mount System SCP circuit.

(2007/03/12)

Battery/LVDS/RJ45/USB board connector,change new type,Touch pad/Wlan switch change new type.
P.44 Change PC20 from 0.01U_25V 0402 to 0.01U_50V 0603.
P.44 Change PR10 from 40.2K_F 0402 to 226K_F 0402 for setting charger current to 1.5A.
P.44 Change PR13 from 24.9K_F 0402 to 44.2K_F 0402 for setting constant power to 3.47A.
P.46 Change +1_05VRUN power rating to 10A.
P.48 Add PR361, PR362, PR363 and PR364 0_J 0603 for testing.
P.51 Update Screw pad size.

(2007/03/13)

P.11 Add L98,C1089,L22,R678,C155,L89,L21,C168,Change +V1.5S_CRT to +V1.5S_TVDAC,Change +VCC_DMI to +VCC_RXR_DMI.

P.17 Delete R1145,R1146,Change F6 to 1206L035,R1148,R1149 to 24ohm,D7 to SSM24APT.

P.18 Delete R457,R1272,ODD_RXIN3-,ODD_RXIN3+ signal.

(2007/03/14)

P.9 Add R124,R125,R126
P.11 Delete R149
P.18 Delete R461

(2007/03/15)

P.11 Delete L92,L94,L96,L97
P.18 Delete R1268,R2225.
P.27 Delete CN39
P.52 Update Power /USB board screw pad.Change H28,H29 to Boss5,Boss6,Delete H3,H4,H6,H7,H10,H19~H22,Add Boss3.Boss4 for Mini-PCI-E

(2007/03/16)

P.17 Change D7 to SSM24APT
P.18 Update LVDS connector pin define.
P.44 Delete close jump GP1 and change PU3 bq24751_AGND to GND for layout convenient

(2007/03/19)

SWAP RP9,RP10,RP12,RP13,RP17,RP20,RP22,RP23,RP25,RP30 for layout.
CON1/CON2 pin7,pin8 connector to D_GND
P.51 Update Power /USB board screw pad GND.

(2007/03/20)

P.27 Change Q104 to 2N7002ESPT,Add R2225.
P.44 Change PR2 from NC_4.7_J 0805 to 1_J 0805.
Change PC24 from NC_4.7U_25V 0805 to 10U_25V 1206
Add PC39 10U_25V 1206
Change PC6 from 0.1U_50V to no mount
Change PC8 from 10U_25V_K to no mount
Delete PC2 and PC3 10U_25V
Above change are for damping input inrush voltage from TI application note.
P.44 Change PC29 from 10U_25V_K to no mount for TI application note.
P.45 Add PR139 0_J 0402 for testing
P.46 Delete GP3 Close_Jump for TI application note.
P.47 Delete GP4 Close_Jump for TI application note.
P.49 Change PQ70 from 2N7002EPT to 2N7002DW-7-F
Change PR220 from 1K_J 0603 to 100K_J 0402
These change are for load switch slow ON and fast OFF.
P.51 Update H18,P_H1,P_H2,U_H2,U_H3,Add P_H3

(2007/03/21)

P.19 SWAP RP92~RP94 for Layout.
P.24 Update ODD/HDD connector.

(2007/03/22)

P.16 SWAP RP21 for Layout.
P.31 SWAP JSPK1 for Layout.

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(2007/03/23)

- P.8 Delete R1929,R1930.
- P.9 Change R124~R127 to 75ohm.
- P.25 Delete R2029,Add TP322.
- P.27 Delete R2225.
- P.30 Delete C1840.Change SNESE_A to SENSE_A.
- P.31 Change R2153,R2154,R2156,R2157 to 2.2Kohm.HP_IN_DET to SP_MUTE.
- P.32 Change C1811,C1819 to 100P,C1814,C1824,C1810 tp 4.7uF/10V.
- P.33 Delete R2185,U146,U147,Change HP_IN_DET to SP_MUTE.
- P.48 Delete PJ7 for layout convenient.
- P.42 Change netname of U_D1.2 and U_D2.2 from GND to GND_U.
- P.51 Delete U_H1.1 net for U_H1 is N-PTH.

(2007/03/26)

- Add C1858~C1860 for EMI request.
- P.46 Change PC67 to mount for +1_05VRUN 10A loading.

(2007/03/27)

- Add C1861~C1864_NC for EMI request.
- P.41 Change LED12 to HT-110Y for MOR request.

(2007/03/28)

- Rename location.
- P.8 U8 nc pin add net for repair. Add C509 for CL_CLK0 and CL_DATA0 through +1_05VRUN,+1_5VRUN.
- P.9 U8 nc pin add net for repair.
- P.42 Add C510 for EMI request.

(2007/03/29)

- P.29 Change Q37,R479 to mount,R480 to NC.

DVT

(2007/04/11)

- P.25 Add KSI015/KSI2 for AV mode function.
- P.42 Update CN1,P_CN1 pin define for AV mode functin,Mirror P_CN1 for M/E easy a'ssy.

(2007/04/12)

- P.34 Mirror U12 SMBUS_CLK and SMBUS_DATA signal.
- P.44 ACGOOD# pull high voltage chenge from BQ24751_VREF to +5VALW_LDO for charger LED abnormal issue.
- P.44 PR32 0 ohm change to PD27 CH520S-30PT Schottky Diode for PU2 OVP issue.

(2007/04/20)

- P.20 Add PM_THRMTRIP# signal and R497 connect to N.B and CPU.
- P.41 Change LED5 to HT-110UY for MS/SD LED brightness issue.

(2007/04/24)

- P.19/39 Change Express LAN interface to port5 for S/W issue.
- P.44 Delete PL4 BCMS451616A600 8A
- P.44 Change PL2 from BCMS451616A600 8A to SMH 100805-4T for EMI request

(2007/04/30)

- P.22 Delete R436,L43,NC C470 for Intel D.G.(2.0).

(2007/05/08)

- P.41 Change SW2/SW3 botton switch for MOR request.

(2007/05/10)

- P.27 Change SW4 WLAN switch.

(2007/05/11)

- P.20 Change C300/C301 to 12pF.
- P.39 Change C281/C282 to 33pF.

(2007/05/15)

- P.16 Mount C255,C267,C293,C309 for EMI.
- P.18 Mount C376 for EMI.
- P.44 Add PC167~PC175 for EMI.
- P.45 Change PR157,PR164 to 3.3ohm,Add PC178,PC179(680pF), PR170,PR171(4.7ohm) to mount for EMI.
- P.46 Add PC176,PC177(680pF),PR172,PR173 no mount for EMI.
- P.48 Change PC88,PC95 to mount for EMI.

(2007/05/17)

- P.44 PC84 change from NC to mount for reducing charger ripple/noise.
- P.44 PC23 change from 0.47U_16V_M 20% to 0.47U_16V_K 10% for Purchase difficult.
- P.45 Add PR174 NC_10K_F 0402 and PR175 0_J 0402 for reserving +3VALW output adjustable.
- P.49 Change PQ30 from VISHAY SI4800BDY to FAIRCHILD FDS8880 for more safety power rating.

(2007/05/18)

- P.30 Change C444 from 10uF to 2.2uF,add C511 for Audio POP issue.
- P.20 Change R223 to no mount.

(2007/05/21)

- P.44 Delete PC6, PC7 and PC12 for layout space.
- P.44 Delete PR10, PC19, PC20
- Change PC3 from 10uF_25V_1206 to 22uF_35V EC CAP
- Change PC38 from 1uF_25V_0603 to 4.7uF_25V_0805
- Add PR176 10_J_0805
- These change are for DC_IN damping circuit.
- P.44 Change PU2 pin28 net-name from DC_IN_MOS to PVCC
- P.44 Change PR2 from 0.02_F_1206 to 0.02_F_2512 for more safety power rating.

(2007/05/22)

- P.19 Back PCI-E from port5 to port1.

(2007/05/24)

- P.38 Add F5~F8 for MOR request.
- P.44 Change PL2 from SMH 100805-4T to 860R-100MHZ_0.045R for purchase difficult.
- P.50 Change PU1 and PQ13 supply voltage from +5VALW_LDO to VREGN for application modification.
- P.51 Change BOSS1 and BOSS2 for Thermal request.

(2007/05/25)

- P.34 Change U12,R183,R190,C224 to no mount for DDR thrermal disable..

(2007/05/26)

- P.25 Add R436 for AV mode botton function.
- P.41 Add R498~R500 P_R4,P_C1 for AV mode botton function.

(2007/05/28)

- P.25 Change GPWU1 to GPWU7 for AV botton.

(2007/05/29)

- P.30 Change R171 to 22ohm,C215 to 22uf.
- P.33 Change C201,C202,C204 to X5R.

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PVT

(2007/06/25)

- P.24 Change CAP7 to mount, and C275 to no mount for HDD noise issue.
- P.28 Update OIDE pin define foe A'SSY issue.
- P.39 Add C512,C513 for LAN noise issue
- P.51 Update H17 screw hole pad.

(2007/06/27)

- P.44 Change PR2 vendor from YAGEO to CYNTEC for purchase difficult.
- P.44 Change PC24 from 120pF 10% to 120pF 5% for purchase difficult.
- P.44 Delete PR25, PR41 and PR42 0ohm for application note.
- P.45 Delete PR162 and PR163 0ohm for application note.
- P.45 Delete PJ4 and PJ5 for application note.
- P.46 Delete PR129 0ohm for application note.
- P.46 Delete PJ1 and PJ2 for application note.
- P.47 Delete PR151 0ohm for application note.
- P.47 Delete PJ3 for application note.
- P.48 Change PC67 from 270pF 10% to 270pF 5% for purchase difficult.
- P.48 Delete PR70, PR71, PR84, PR86, PR90, PR93, PR94, PR96, PR97, PR99 and PR102 0ohm for application note.
- P.48 Add TP150, TP151, TP152 and TP153 test pin for application note.
- P.49 Delete PR110, PR111 and PR114 0ohm for application note.
- P.50 Delete PR20 and PR49 0ohm for application note.
- P.51 Update H14 screw hole pad.

(2007/06/29)

- P.45 Change PU13 pin9,10 net name to +5VALW.

(2007/07/02)

- P.27 Change LED4 to HT-110YG for LED issue.
- P.41 Change R321,R323 to 51ohm,LED2,LED3 to HT-110Y for LED issue.

(2007/07/03)

- P.38 Change F5~F8 to 2.6A poly-switch for USB loading and noise issue.
- P.42 Change CN23 to HS-8208E.

(2007/07/04)

- P.44 Change PC3 from mount to dummy for application note.
- P.44 Change PC38 from 4.7uF_25V 0805 to 1uF_25V 0603 for application note.
- P.44 Remove PR176 10_J for application note.
- P.44 Add PR177, PR178 1_J 1206 and PC180, PC181 4.7uF_25V 0805 for DC_IN RC snubber circuit.

(2007/07/09)

- P.11 Change L9,L28 to 250mA for component spec. issue.
- P.44 Change PR177, PR178 from 1_J 1206 to 1_J 1210 for power rating safety.

(2007/07/12)

- P.18 Add L46 for EMI issue.
- P.31 Add C514~C517 for EMI issue.

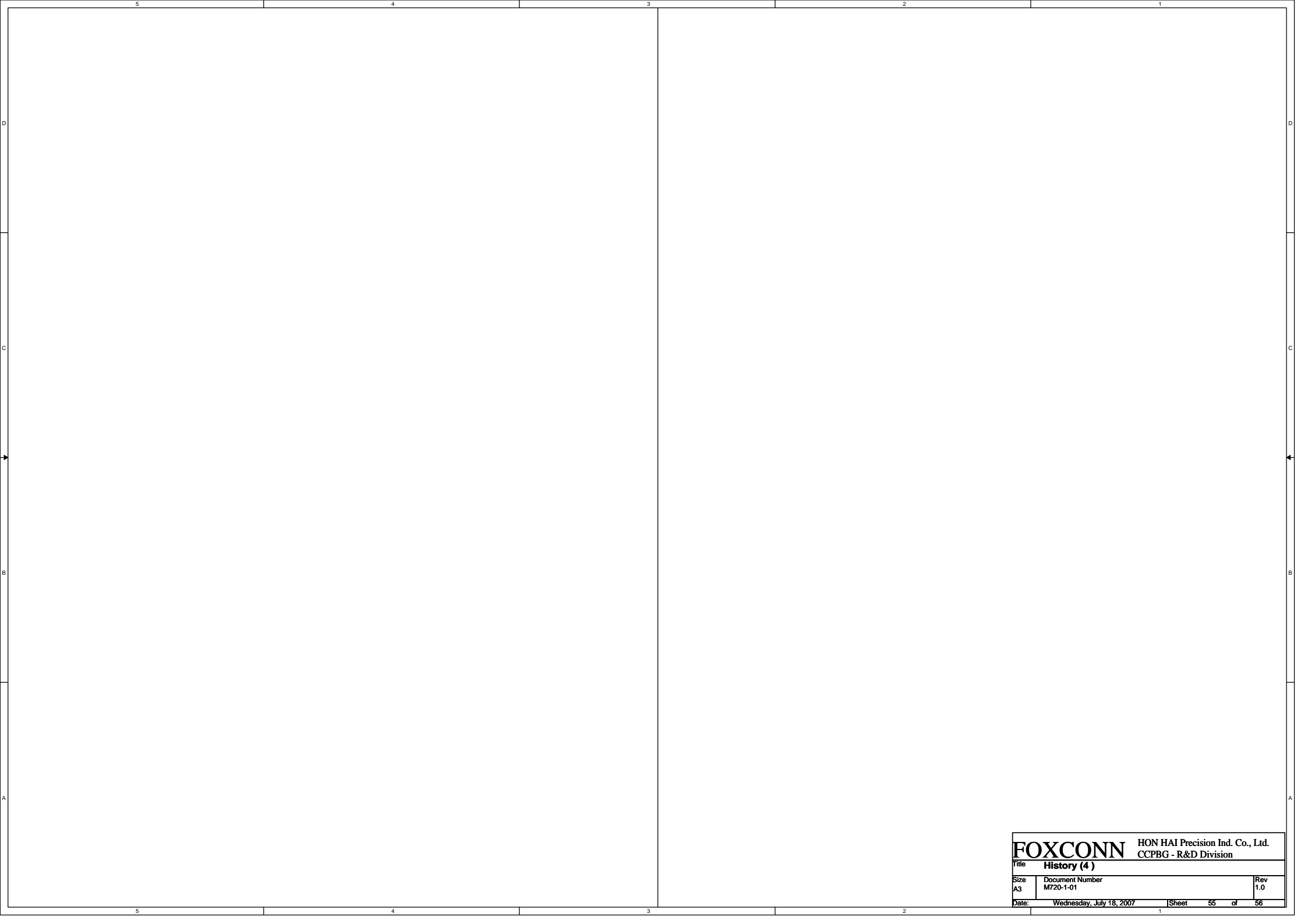
(2007/07/16)

- P.32 Change C455,C445 to 10uF,R167,R149 to 20 Kohm for MIC. THD+N issue.

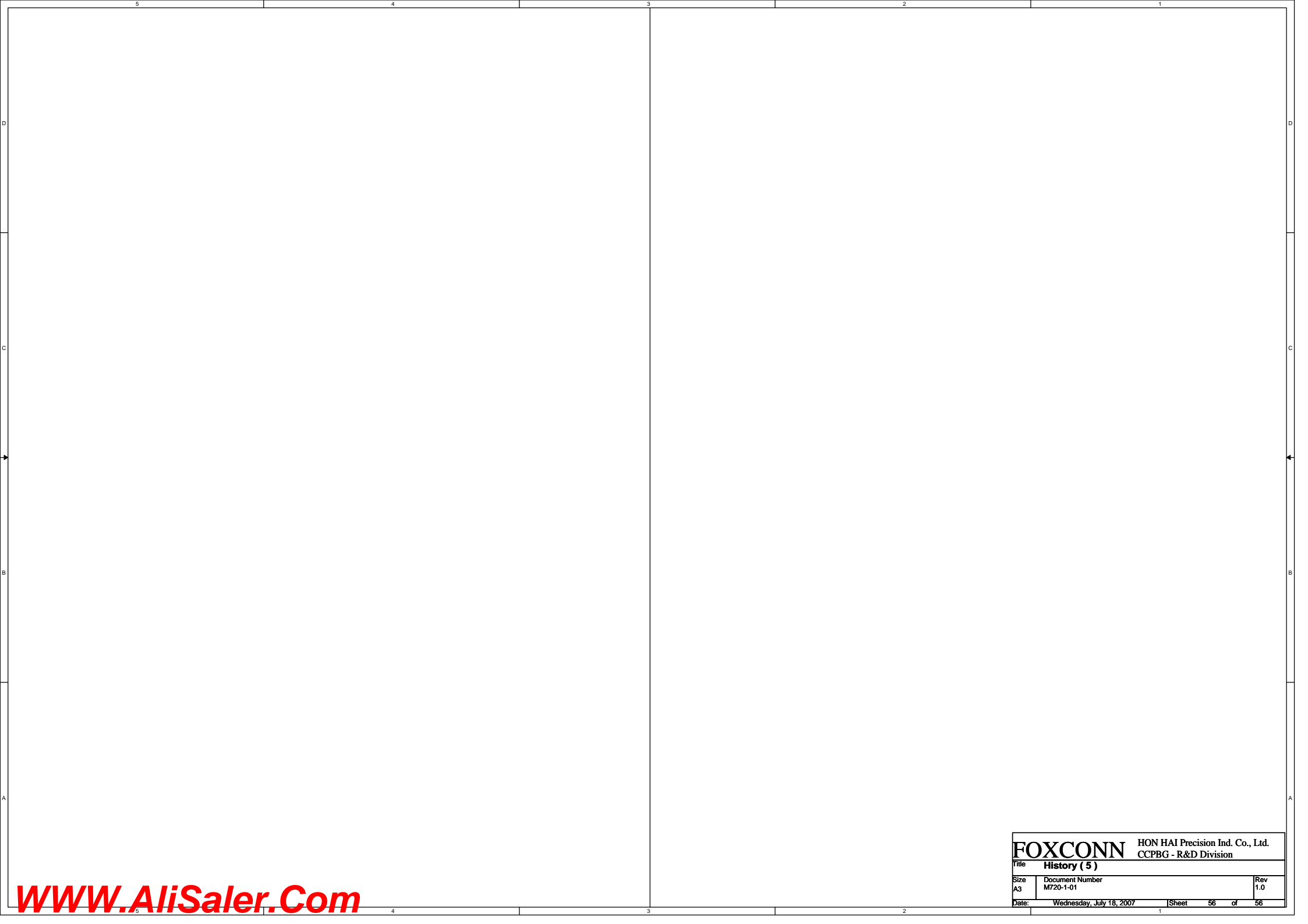
(2007/07/17)

- P.27 Change LED4 to HT-110UYG for MOR request.
- P.45 Change PR177,PR178 to 1/3W for EMI issue.

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