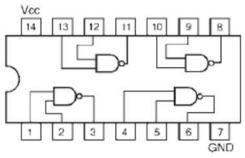
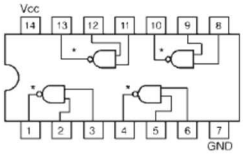
ANNEXE I : Datasheet

Circuits intégrés logiques

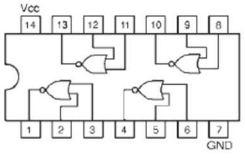
74 00 *4 portes ET-NON à 2 entrées*



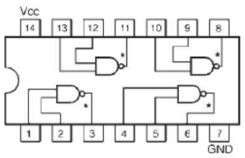
74 01 *4 portes ET-NON à 2 entrées C.O.*



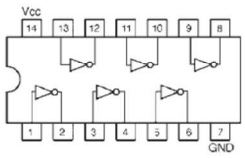
74 02 *4 portes OU-NON à 2 entrées*



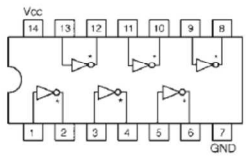
74 03 *4 portes ET-NON à 2 entrées C.O.*



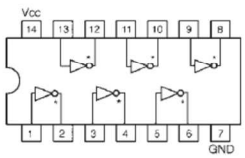
74 04 *6 inverseurs*



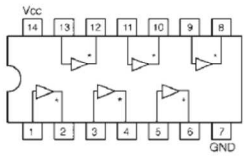
74 05 *6 inverseurs C.O.*



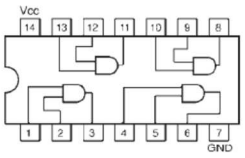
74 06 *6 inverseurs C.O. 30 V*



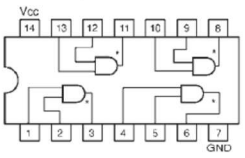
74 07 *6 amplificateurs C.O. 30 V*



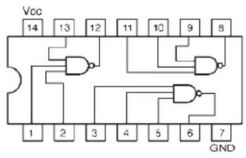
74 08 *4 portes ET à 2 entrées*



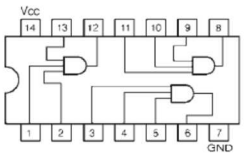
74 09 *4 portes et à 2 entrées C.O.*



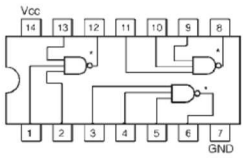
74 10 *3 portes ET-NON à 3 entrées*



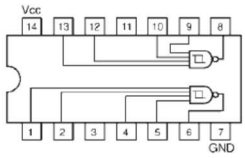
74 11 *3 portes ET à 3 entrées*



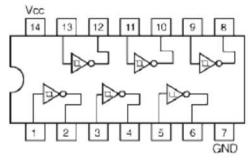
74 12 *3 portes ET-NON à 3 entrées C.O.*



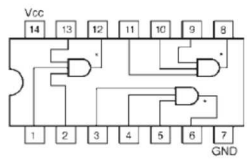
74 13 *2 portes ET-NON à 4 entrées avec bascule de schmitt*



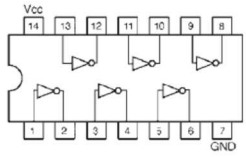
74 14 *6 inverseurs avec bascule de schmitt*



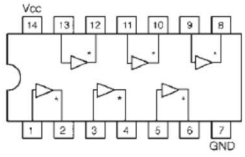
74 15 *3 portes ET à 3 entrées C.O.*



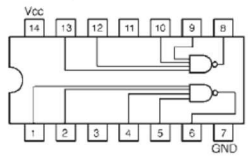
74 16 *6 inverseurs C.O.*



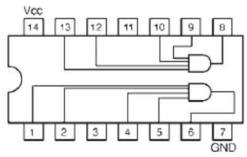
74 17 *6 amplificateurs C.O. 15 V*



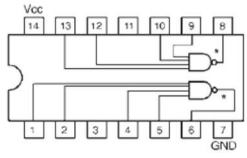
74 20 *2 portes ET-NON à 4 entrées*



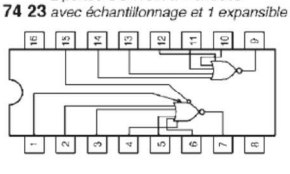
74 21 *2 portes ET à 4 entrées*



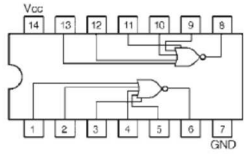
74 22 *2 portes ET-NON à 4 entrées C.O.*



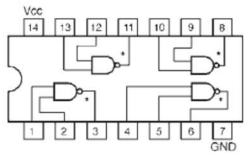
74 23 *2 portes OU-NON à 4 entrées avec échantillonnage et 1 expansible*



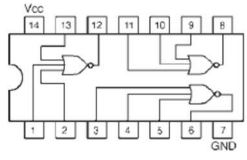
74 25 *2 portes OU-NON à 4 entrées et échantillonnage*



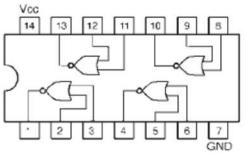
74 26 *4 portes ET-NON à 2 entrées C.O.*



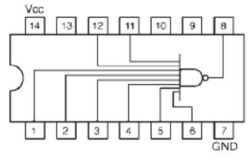
74 27 *3 portes OU-NON à 3 entrées*



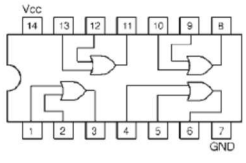
74 28 *4 portes OU-NON à 2 entrées*



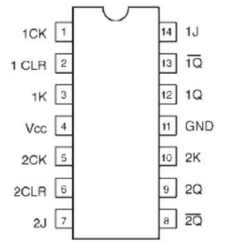
74 30 *1 porte ET-NON à 8 entrées*



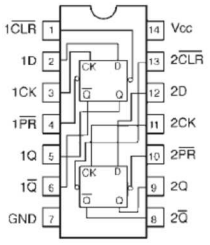
74 32 *4 portes OU à 2 entrées*



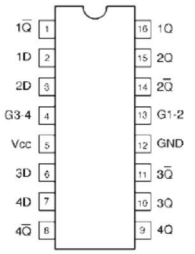
74 73 *2 bascules JK avec RAZ*



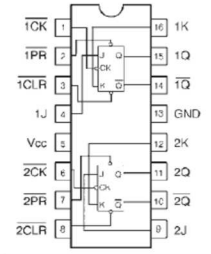
74 74 *2 bascules D avec R et S*



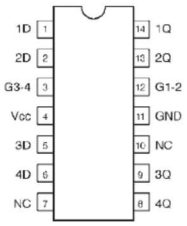
74 75 *2 doubles bascules à verrouillage*



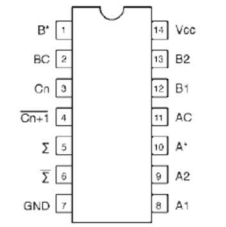
74 76 *2 bascules JK avec R et S*



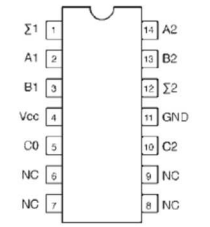
74 77 *verrou 4 bits*



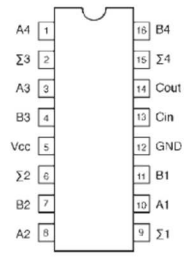
74 80 *additionneur complet 1 bit*



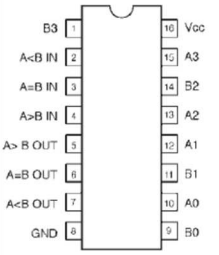
74 82 *additionneur complet 2 bits*



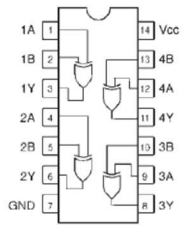
74 83 *additionneur complet 4 bits*



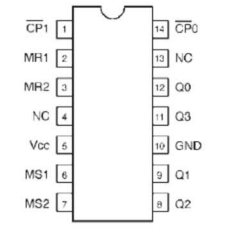
74 85 *comparateur 4 bits*



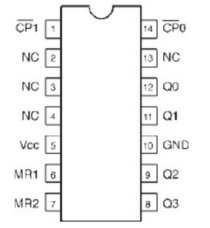
74 86 *4 portes OU-EXCLUSIF à 2 entrées*



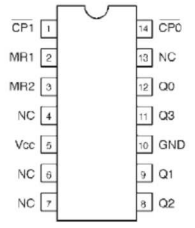
74 90 *compteur décimal*



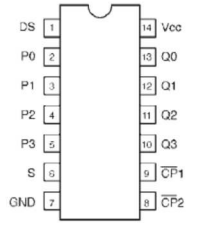
74 92 *compteur hexadécimal*



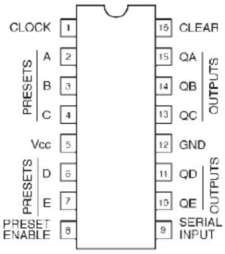
74 93 *compteur binaire asynchrone 4 bits*



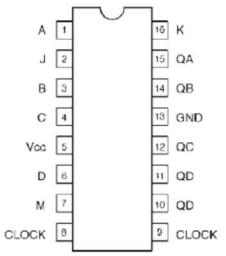
74 95 *registre à décalage 4 bits*



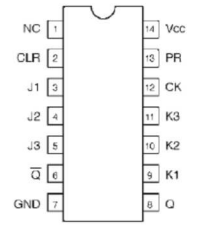
74 96 *registre à décalage 5 bits*



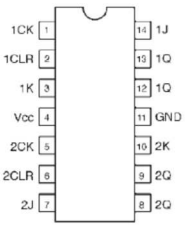
74 99 *4 bit R shift L shift register*



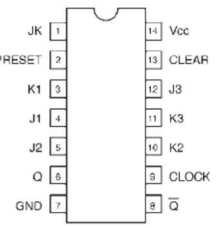
74 102 *1 bascule JK maître-esclave à 3 entrées avec R et S*



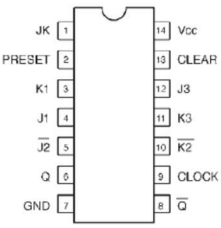
74 103 *JK flip flop*



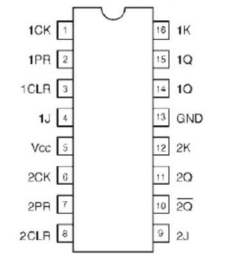
74 104 *1 bascule JK maître-esclave à 3 entrées av ec R et S*



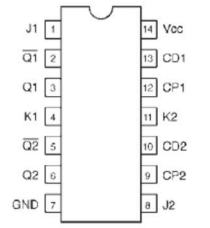
74 105 *1 bascule JK maître-esclave à 3 entrées av ec R et S*



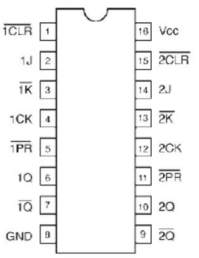
74 106 *dual JK flip flop*



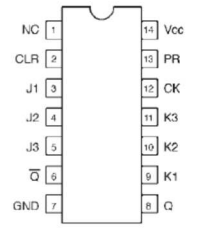
74 107 *2 bascules JK avec RAZ*



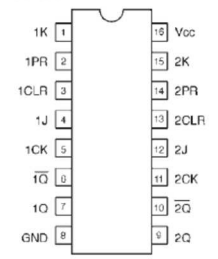
74 109 *2 bascules JK à déclenchement sur front montant*



74 110 *dual JK flip flop with data lockout*



74 111 *2 bascules JK avec R et S*



SN74LS283

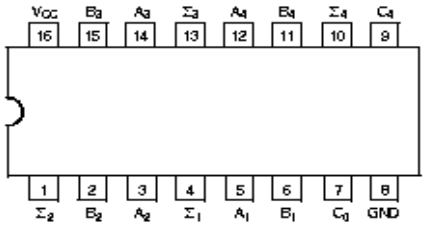
4-Bit Binary Full Adder with Fast Carry

The SN74LS283 is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1–A_4, B_1–B_4) and a Carry Input (C_0). It generates the binary Sum outputs (Σ_1–Σ_4) and the Carry Output (C_4) from the most significant bit. The LS283 operates with either active HIGH or active LOW operands (positive or negative logic).

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA

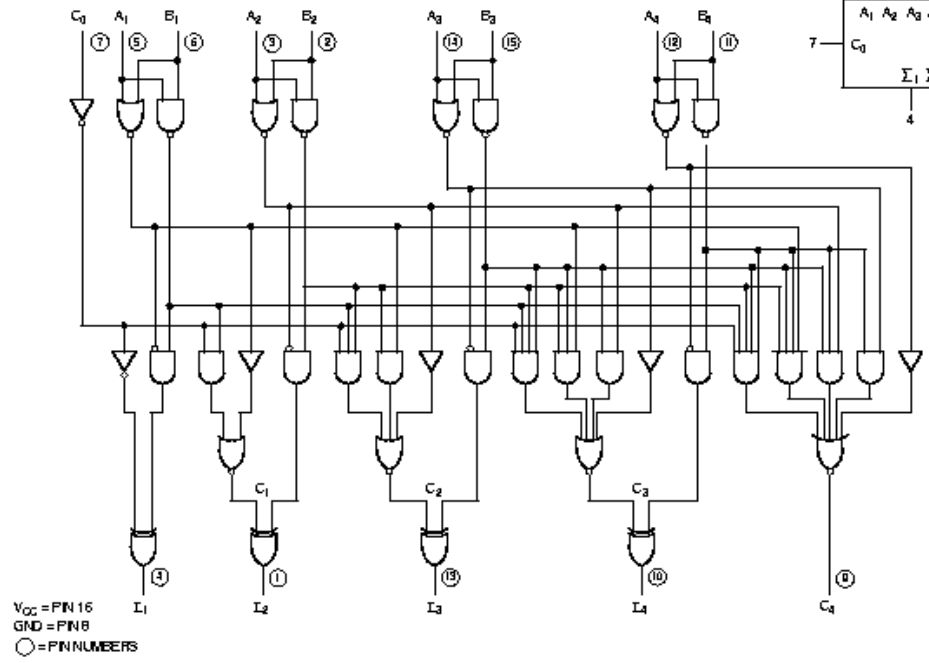
CONNECTION DIAGRAM DIP (TOP VIEW)



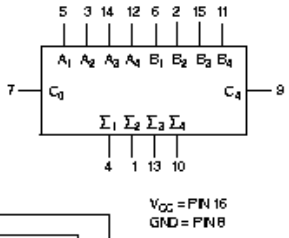
PIN NAMES		LOADING (Note a) HIGH	LOW
A_1 – A_4	Operand A Inputs	1.0 U.L.	0.5 U.L.
B_1 – B_4	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_0	Carry Input	0.5 U.L.	0.25 U.L.
Σ_1 – Σ_4	Sum Outputs	10 U.L.	5 U.L.
C_4	Carry Output	10 U.L.	5 U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.

LOGIC DIAGRAM



LOGIC SYMBOL



FUNCTIONAL DESCRIPTION

The LS283 adds two 4-bit binary words (A plus B) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1–Σ_4) and outgoing carry (C4) outputs.

$C_0 + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_4$

Where: (+) = plus

Due to the symmetry of the binary add function the LS283 can be used with either all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that with active HIGH inputs, Carry Input can not be left open, but must be held LOW when no carry in is intended.

Example:

	C_0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_4	
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10+9=19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry+5+6=12)

Interchanging inputs of equal weight does not affect the operation, thus C_0, A_1, B_1, can be arbitrarily assigned to pins 7, 5 or 3.

74H/HC193
Presettable synchronous 4-bit binary
Presettable synchronous 4-bit binary, up/down counter

FEATURES

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard
- ICC category: MSI

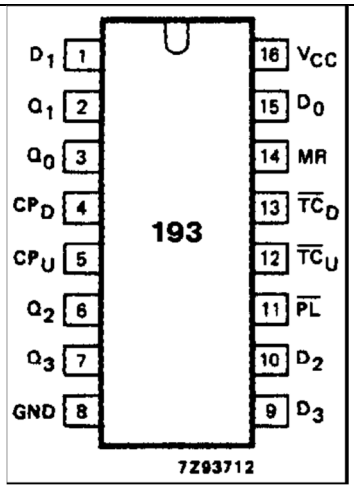
GENERAL DESCRIPTION

The 74HC/HCT193 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDECstandard no. 7A.The 74HC/HCT193 are 4-bit synchronous binary up/down counters. Separate up/down clocks, CPU and CPD respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CPU clock is pulsed while CPD is held HIGH, the device will count up. If the CPD clock is pulsed while CPU is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input (PL). The “193” contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions. Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CPD input will decrease the count by one, while a similar transition on the CPU input will advance the count by one.One clock should be held HIGH while counting with the other, otherwise the circuit will either count by two’s or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts. The terminal count up (TCU) and terminal count down (TCD) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CPU will cause TCU to go LOW. TCU will stay LOW until CPU goes HIGH again, duplicating the count up clock. Likewise, the TCD output will go LOW when the circuit is in the zero state and the CPD goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added. The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs (Q0 to Q3) regardless of the conditions of the clock inputs when the parallel load (PL) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q0 to Q3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

PIN DESCRIPTION

PIN NO.	SYMBOL NAME AND FUNCTION
3, 2, 6, 7	Q0 to Q3 flip-flop outputs
4	CPD count down clock input(1)
5	CPU count up clock input(1)
8	GND ground (0 V)
11	PL asynchronous parallel load input (active LOW)
12	TCU terminal count up (carry) output (active LOW)
13	TCD terminal count down (borrow) output (active LOW)
14	MR asynchronous master reset input (active HIGH)
15, 1, 10, 9	D0 to D3 data inputs
16	VCC positive supply voltage

(1) LOW-to-HIGH, edge triggered



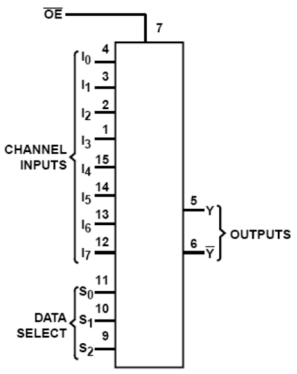
Function Table :

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC_U}$	$\overline{TC_D}$
reset (clear)	H H	X X	X X	L H	X X	X X	X X	X X	L L	L L	L L	L L	H H	L H
parallel load	L L L L	L L L L	X X L H	L H X X	L L H H	L L H H	L L H H	L L H H	L L H H	L L H H	L L H H	L L H H	H H L H	L H H H
count up	L	H	↑	H	X	X	X	X	count up				$H^{(2)}$	H
count down	L	H	H	↑	X	X	X	X	count down				H	$H^{(3)}$

Notes

1. H = HIGH voltage level L = LOW voltage level X = don't care
   ↑ = LOW-to-HIGH clock transition
2. TCU = CPU at terminal count up (HHHH) 3. TCD = CPD at terminal count down (LLLL)

74HC251



TRUTH TABLE

INPUTS				OUTPUT	
SELECT			OUTPUT CONTROL $\overline{OE}$		
S2	S1	S0		Y	$\overline{Y}$
X	X	X	H	Z	Z
L	L	L	L	I_0	$\overline{I}_0$
L	L	H	L	I_1	$\overline{I}_1$
L	H	L	L	I_2	$\overline{I}_2$
L	H	H	L	I_3	$\overline{I}_3$
H	L	L	L	I_4	$\overline{I}_4$
H	L	H	L	I_5	$\overline{I}_5$
H	H	L	L	I_6	$\overline{I}_6$
H	H	H	L	I_7	$\overline{I}_7$

H = High Voltage Level, L = Low Voltage Level, X = Don't Care, Z = High Impedance (Off), I_0, I_1...I_7 = the level of the respective input.

DESCRIPTION

The HEF40194B is a 4-bit bidirectional shift register with two mode control inputs (S_0 and S_1), a clock input (CP), a serial data shift left input (D_{SL}), a serial data shift right input (D_{SR}), four parallel data inputs (P_0 to P_3), an overriding asynchronous master reset input ($\overline{MR}$), and four buffered parallel outputs (O_0 to O_3). When LOW, $\overline{MR}$ resets all stages and forces O_0 to O_3 LOW, overriding all other input conditions. When $\overline{MR}$ is HIGH, the operation mode is controlled by S_0 and S_1 as shown in the function table.

Serial and parallel operation are edge-triggered on the LOW to HIGH transition of CP. The inputs at which the data are to be entered and S_0, S_1 must be stable for a set-up time before the LOW to HIGH transition of CP.

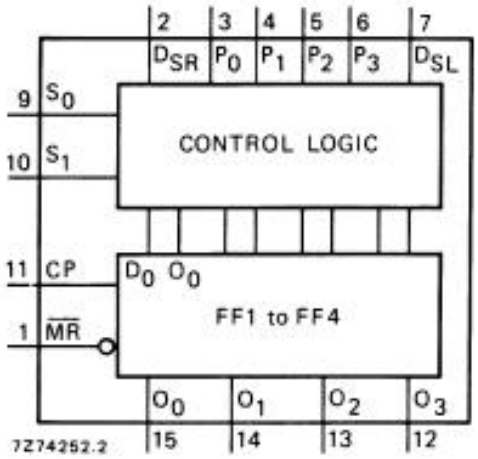


Fig.1 Functional diagram.

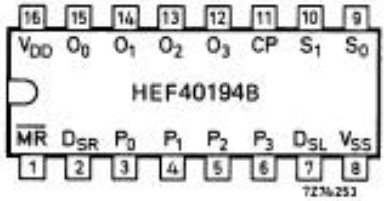


Fig.2 Pinning diagram.

HEF40194BP(N): 16-lead DIL; plastic (SOT38-1)

HEF40194BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)

HEF40194BT(D): 16-lead SO; plastic (SOT109-1)

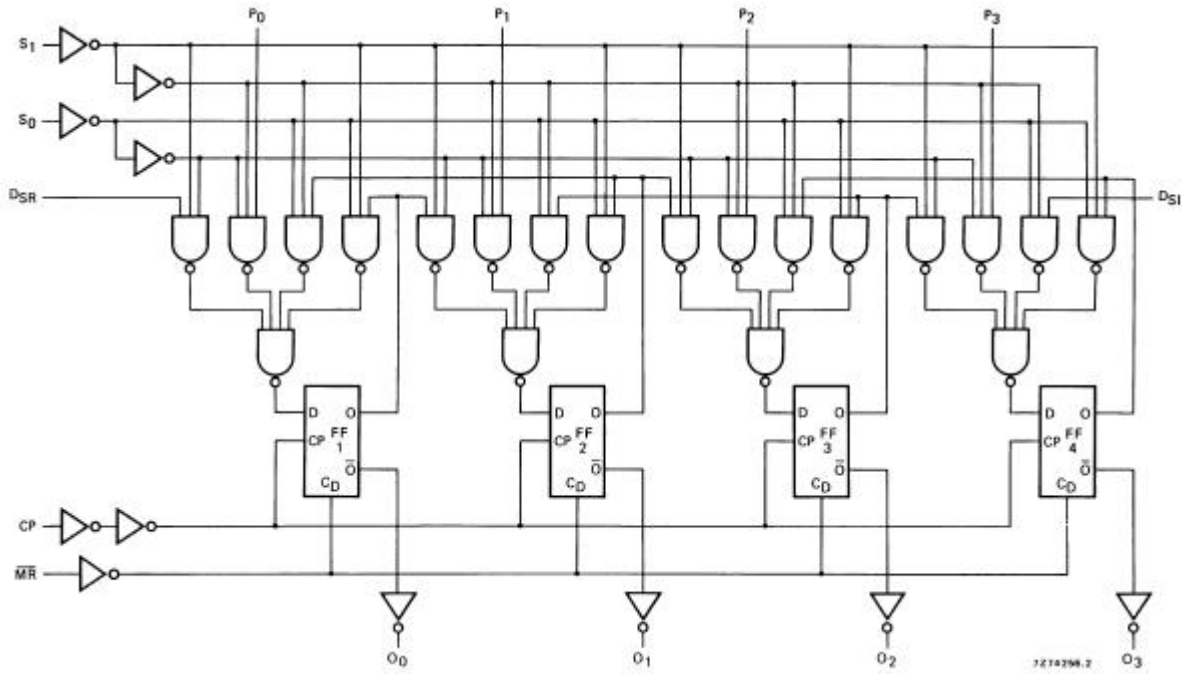
( ): Package Designator North America

PINNING

S_0, S_1	mode control inputs
P_0 to P_3	parallel data inputs
D_{SR}	serial data shift right input
D_{SL}	serial data shift left input
CP	clock input (LOW to HIGH edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	buffered parallel outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications



FUNCTION TABLE

OPERATING MODE	INPUTS ($\overline{MR}$ = HIGH)					OUTPUTS AT T_{n+1}			
	S_1	S_0	D_{SR}	D_{SL}	P_0 TO P_3	O_0	O_1	O_2	O_3
hold	L	L	X	X	X	O_0	O_1	O_2	O_3
shift left	H	L	X	L	X	O_1	O_2	O_3	L
	H	L	X	H	X	O_1	O_2	O_3	H
shift right	L	H	L	X	X	L	O_0	O_1	O_2
	L	H	H	X	X	H	O_0	O_1	O_2
parallel load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4. t_{n+1} = state after next LOW to HIGH transition of CP

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	1 500 $f_i + \Sigma (f_o C_L) \times V_{DD}^2$	where
	10	6 900 $f_i + \Sigma (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	15	18 900 $f_i + \Sigma (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load cap. (pF)
			$\Sigma (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)