Datorsystem VT 2022

F13

Inför Tentamen,

Summering av F1-F11

Stockholm University

- **F1**
  - Computer Level Hierarchy
  - Von Neumann Model
- **F2-F3**
  - Converting Between Bases
  - Signed Integer Representation
  - Floating-Point Representation
  - **IEEE-754 single precision floating point standard**

- **F4**
  - CPU Basic
  - The Bus
  - CPU: executes program instructions
  - Interrupts
  - Maskable & NonMaskable Interrupts
- **F5**
  - **Instruction Formats**
  - **Instruction Types**
  - **Addressing**
  - **Instruction Pipelining**

- **F6**
  - Types of Memory
  - Cache memory
    - direct mapped
    - Associative
    - **Replacement policy** (FIFO, RANDOM)
    - **cache coherence problems**
      - **lösning : write-through eller write-back protocol**
  - Virtual Memory
    - Addressing, paging and TLB

- **F7**
  - Data storage I/O
    - Architectures
    - Control and Programmed
    - Buses
  - Interrupts Vectors & Interrupt-Driven I/O
  - Memory-Mapped I/O (DMA)
  - Channel-attached I/O
  - Connecting Buses to I/O devices
  - Redundant Array of Independent Disks (RAID (0-6))

- **F8 & F9 (operating systems)**
  - Introduction
  - Kernel & System programs
  - Processer (Kontroll, Tillstånd , trådar och schemaläggning)
  - Process management

F10-F11

- Characteristics and basic functions of Computer communication
- Network Organization & Architecture
- Internet & Transport protocols overview (TCP/IP)
- Hyper Text Transfer Protocol (HTTP)
- IP Addressing Structure