GVISION200_SCH_TOP

FPGA_POWER_SUPPLY
FPGA_POWER_SUPPLY.SchDoc

FPGA_PSU
FPGA_PSU.SchDoc

FPGA_CONFIG&CLOCK
FPGA_CONFIG&CLOCK.SchDoc

FPGA_GCLK
FPGA_CCLK
FPGA_Din
FPGA_Init

CAMERA_LINK
CAMERA_LINK.SchDoc

CLK_MAIN_OUT/TDIG1
FPGA_GCLK
CLKIN_N
CLKIN_P
CLK_MAIN_OUT/TDIG1_BUF

FPGA_CTRL&LVDS
FPGA_CTRL&LVDS.SchDoc

CLK_MAIN_OUT/TDIG1_BUF
FPGA_CCLK
FPGA_Din
FPGA_Init
OUT0_BOT_N
OUT0_BOT_P
OUT1_BOT_N
OUT1_BOT_P
OUT2_BOT_N
OUT2_BOT_P
OUT3_BOT_N
OUT3_BOT_P
OUT4_BOT_N
OUT4_BOT_P
OUT5_BOT_N
OUT5_BOT_P
OUT6_BOT_N
OUT6_BOT_P
OUT7_BOT_N
OUT7_BOT_P
OUT8_BOT_N
OUT8_BOT_P
OUT9_BOT_N
OUT9_BOT_P
OUT10_BOT_N
OUT10_BOT_P
OUT11_BOT_N
OUT11_BOT_P
OUT12_BOT_N
OUT12_BOT_P
OUT13_BOT_N
OUT13_BOT_P
OUT14_BOT_N
OUT14_BOT_P
OUT15_BOT_N
OUT15_BOT_P
OUT0_TOP_N
OUT0_TOP_P
OUT1_TOP_N
OUT1_TOP_P
OUT2_TOP_N
OUT2_TOP_P
OUT3_TOP_N
OUT3_TOP_P
OUT4_TOP_N
OUT4_TOP_P
OUT5_TOP_N
OUT5_TOP_P
OUT6_TOP_N
OUT6_TOP_P
OUT7_TOP_N
OUT7_TOP_P
OUT8_TOP_N
OUT8_TOP_P
OUT9_TOP_N
OUT9_TOP_P
OUT10_TOP_N
OUT10_TOP_P
OUT11_TOP_N
OUT11_TOP_P
OUT12_TOP_N
OUT12_TOP_P
OUT13_TOP_N
OUT13_TOP_P
OUT14_TOP_N
OUT14_TOP_P
OUT15_TOP_N
OUT15_TOP_P
CLKOUT_N
CLKOUT_P
LVDS_CTR_N
LVDS_CTR_P
CLK_MAIN
SYS_RST_N
RST
SEL
TX2
TX1
HDR
SYNC_X
BLSUN_HG_LG
TREF_TSIG
VTZERO
READ
ADC_PC
SAMPLE_BOT
SAMPLE_TOP
COL_INIT_BOT
COL_INIT_TOP
COL_PC_FRAME_REQ
SPI_READ
SPI_OUT
SPI_WRITE
SPI_DATA
SPI_CLK
ROW<0>
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ROW<2>
ROW<3>
ROW<4>
ROW<5>
ROW<6>
ROW<7>
ROW<8>
ROW<9>
ROW<10>
ROW<11>

USB3.0
USB3.0.SchDoc

DQ0
DQ1
DQ2
DQ4
DQ5
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
USB_A0
USB_A1
PCLK
SLCS
SLWR
SLOE
SLRD
PKTEND
CLKIN_FPGA
INT
USB_SCK_FPGA
USB_SSN_FPGA
USB_MISO_FPGA
USB_MOSI_FPGA
FLAGA
FLAGB
DQ3
DQ6
DQ7
USB_GPIO0
USB_GPIO1

SENSOR
SENSOR.SchDoc

CLK_MAIN_OUT/TDIG1
CLKIN_N
CLKIN_P
OUT0_BOT_N
OUT0_BOT_P
OUT1_BOT_N
OUT1_BOT_P
OUT2_BOT_N
OUT2_BOT_P
OUT3_BOT_N
OUT3_BOT_P
OUT4_BOT_N
OUT4_BOT_P
OUT5_BOT_N
OUT5_BOT_P
OUT6_BOT_N
OUT6_BOT_P
OUT7_BOT_N
OUT7_BOT_P
OUT8_BOT_N
OUT8_BOT_P
OUT9_BOT_N
OUT9_BOT_P
OUT10_BOT_N
OUT10_BOT_P
OUT11_BOT_N
OUT11_BOT_P
OUT12_BOT_N
OUT12_BOT_P
OUT13_BOT_N
OUT13_BOT_P
OUT14_BOT_N
OUT14_BOT_P
OUT15_BOT_N
OUT15_BOT_P
OUT0_TOP_N
OUT0_TOP_P
OUT1_TOP_N
OUT1_TOP_P
OUT2_TOP_N
OUT2_TOP_P
OUT3_TOP_N
OUT3_TOP_P
OUT4_TOP_N
OUT4_TOP_P
OUT5_TOP_N
OUT5_TOP_P
OUT6_TOP_N
OUT6_TOP_P
OUT7_TOP_N
OUT7_TOP_P
OUT8_TOP_N
OUT8_TOP_P
OUT9_TOP_N
OUT9_TOP_P
OUT10_TOP_N
OUT10_TOP_P
OUT11_TOP_N
OUT11_TOP_P
OUT12_TOP_N
OUT12_TOP_P
OUT13_TOP_N
OUT13_TOP_P
OUT14_TOP_N
OUT14_TOP_P
OUT15_TOP_N
OUT15_TOP_P
CLKOUT_N
CLKOUT_P
LVDS_CTR_N
LVDS_CTR_P
CLK_MAIN
SYS_RST_N
RST
SEL
TX2
TX1
HDR
SYNC_X
BLSUN_HG_LG
TREF_TSIG
VTZERO
READ
ADC_PC
SAMPLE_BOT
SAMPLE_TOP
COL_INIT_BOT
COL_INIT_TOP
COL_PC_FRAME_REQ
SPI_READ
SPI_OUT
SPI_WRITE
SPI_DATA
SPI_CLK
ROW<0>
ROW<1>
ROW<2>
ROW<3>
ROW<4>
ROW<5>
ROW<6>
ROW<7>
ROW<8>
ROW<9>
ROW<10>
ROW<11>
RAMP_VSIG
RAMP_VREF
VTREF_DRIV
VREF

FPGA_DDR3
FPGA_DDR3.SchDoc

DDR3_1_A[0..14]
DDR3_1_DQ[0..15]
DDR3_1_BA0
DDR3_1_BA1
DDR3_1_BA2
DDR3_1_WE#
DDR3_1_RAS#
DDR3_1_CAS#
DDR3_1_CK_P
DDR3_1_CK_N
DDR3_1_CKE
DDR3_1_RESET#
DDR3_1_ODT
DDR3_1_LDQS_P
DDR3_1_LDQS_N
DDR3_1_UDQS_P
DDR3_1_UDQS_N
DDR3_1_LDM
DDR3_1_UDM

DDR3_1
DDR3_1.SchDoc

DDR3_1_A[0..14]
DDR3_1_DQ[0..15]
DDR3_1_BA0
DDR3_1_BA1
DDR3_1_BA2
DDR3_1_WE#
DDR3_1_RAS#
DDR3_1_CAS#
DDR3_1_CK_P
DDR3_1_CK_N
DDR3_1_CKE
DDR3_1_RESET#
DDR3_1_ODT
DDR3_1_LDQS_P
DDR3_1_LDQS_N
DDR3_1_UDQS_P
DDR3_1_UDQS_N
DDR3_1_LDM
DDR3_1_UDM

DDR3_2_A[0..14]
DDR3_2_DQ[0..15]
DDR3_2_BA0
DDR3_2_BA1
DDR3_2_BA2
DDR3_2_WE#
DDR3_2_RAS#
DDR3_2_CAS#
DDR3_2_CK_P
DDR3_2_CK_N
DDR3_2_CKE
DDR3_2_RESET#
DDR3_2_ODT
DDR3_2_LDQS_P
DDR3_2_LDQS_N
DDR3_2_UDQS_P
DDR3_2_UDQS_N
DDR3_2_LDM
DDR3_2_UDM

DDR3_2
DDR3_2.SchDoc

DDR3_2_A[0..14]
DDR3_2_DQ[0..15]
DDR3_2_BA0
DDR3_2_BA1
DDR3_2_BA2
DDR3_2_WE#
DDR3_2_RAS#
DDR3_2_CAS#
DDR3_2_CK_P
DDR3_2_CK_N
DDR3_2_CKE
DDR3_2_RESET#
DDR3_2_ODT
DDR3_2_LDQS_P
DDR3_2_LDQS_N
DDR3_2_UDQS_P
DDR3_2_UDQS_N
DDR3_2_LDM
DDR3_2_UDM

SENSOR_POWER_SUPPLY
SENSOR_POWER_SUPPLY.SchDoc

RAMP_VSIG
RAMP_VREF
VTREF_DRIV
VREF

U_REVISION_HISTORY
REVISION_HISTORY.SchDoc

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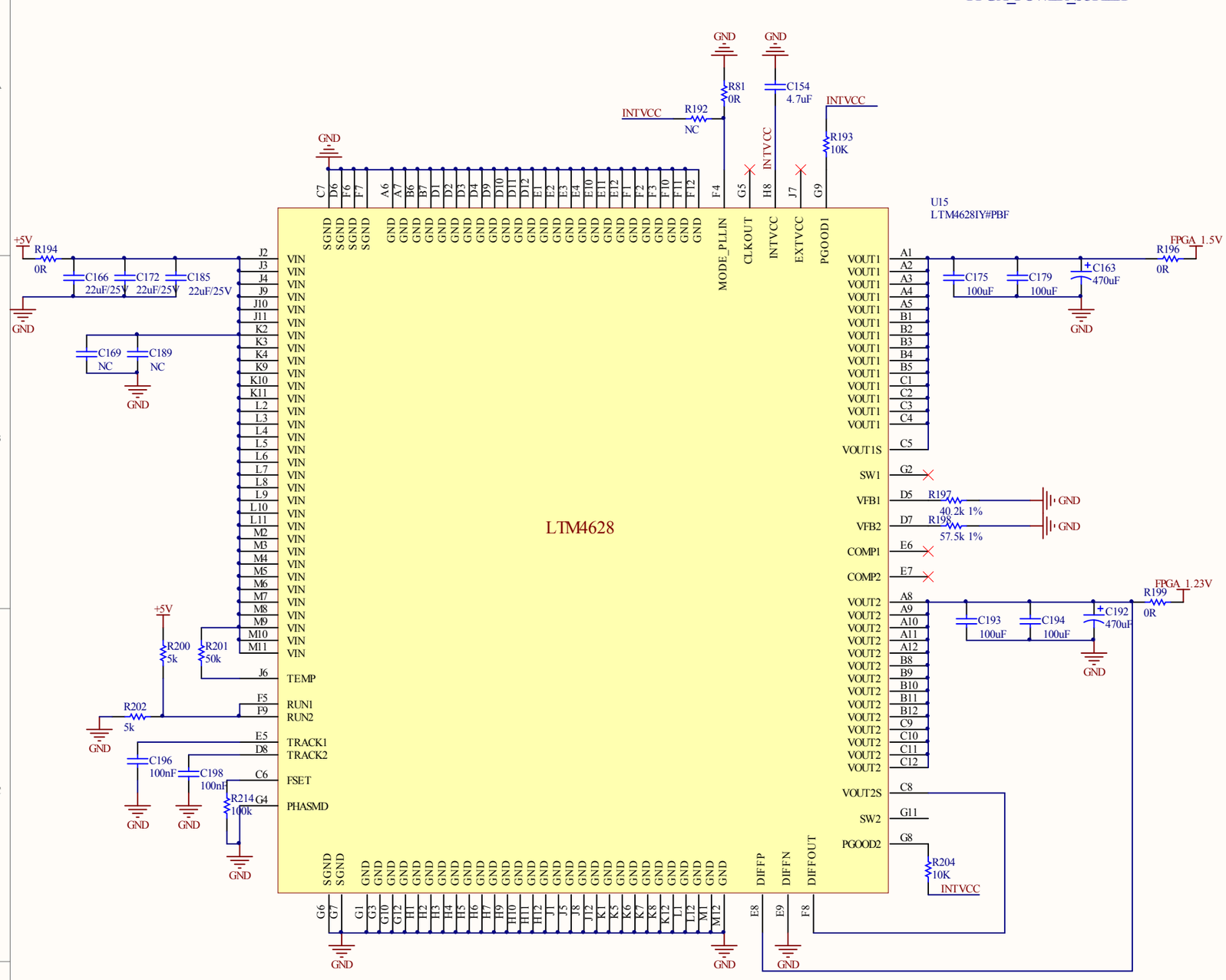
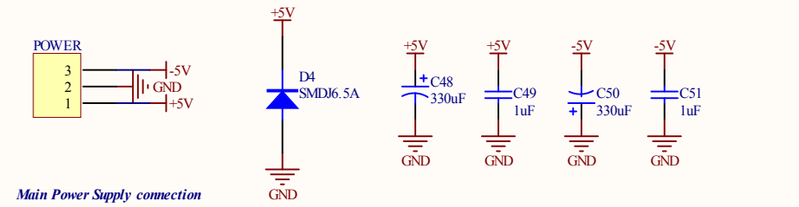
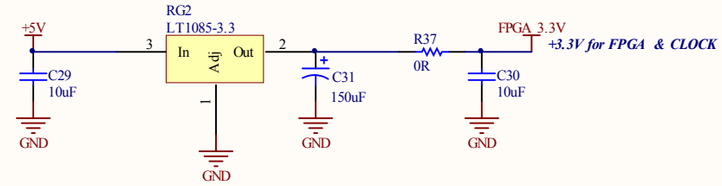
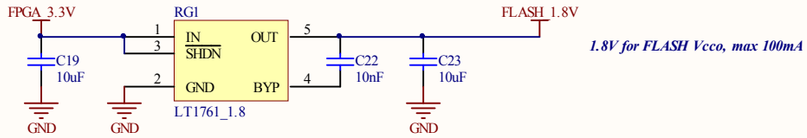
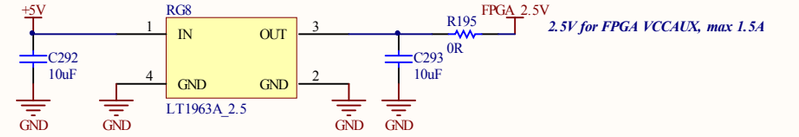
FPGA_POWER_SUPLLY

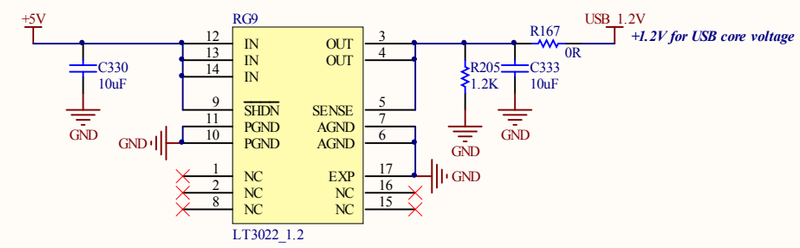












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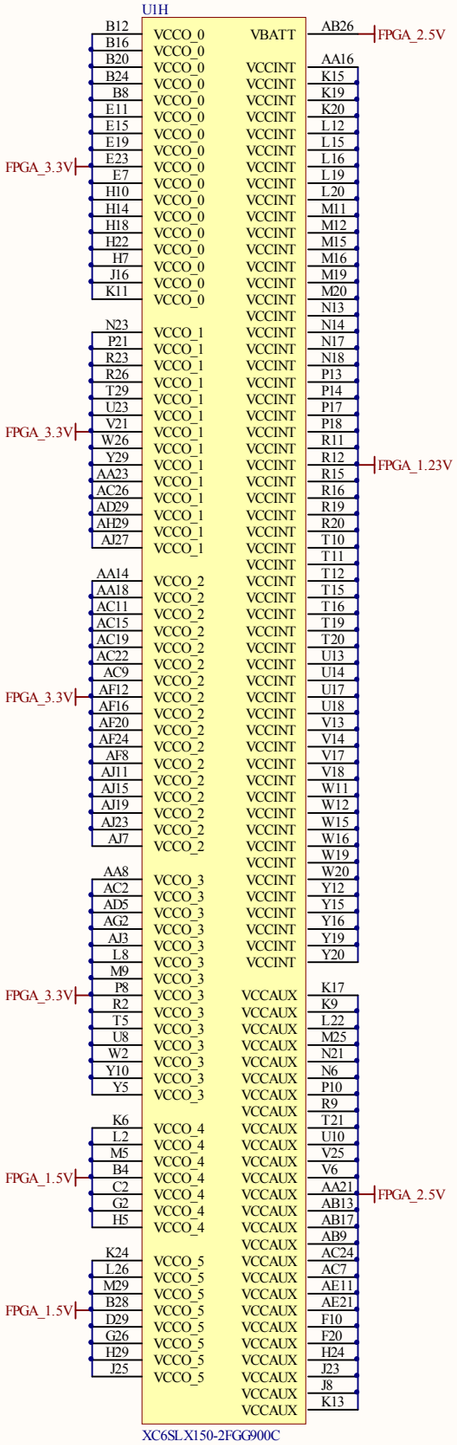
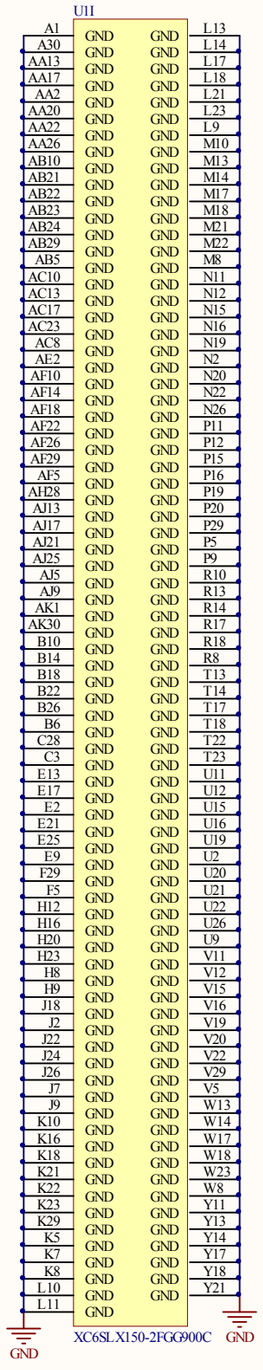
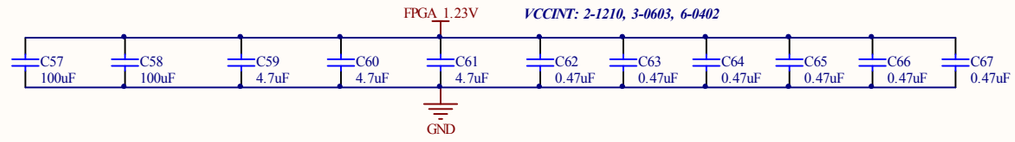
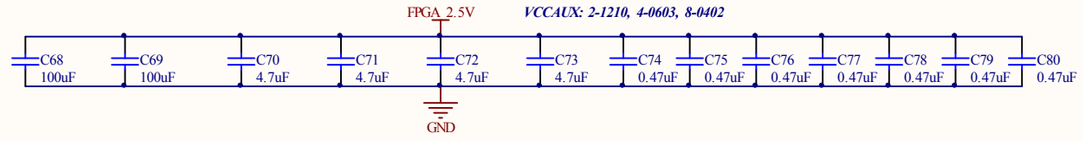
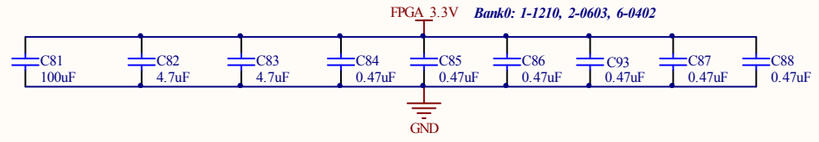
FPGA_PSU

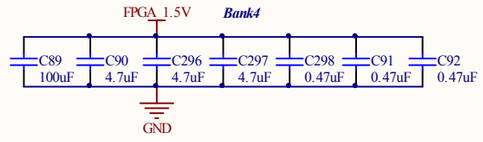


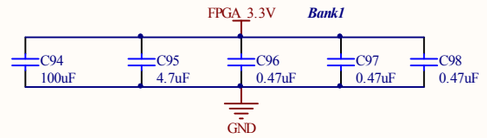


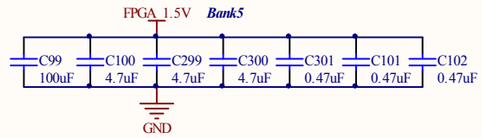


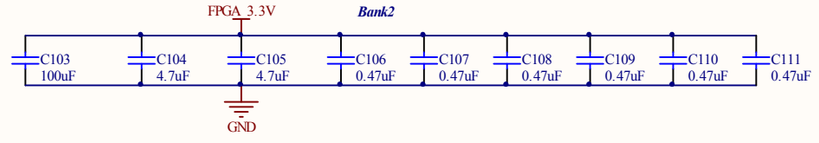


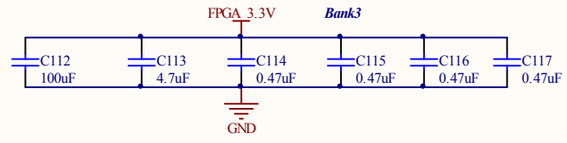












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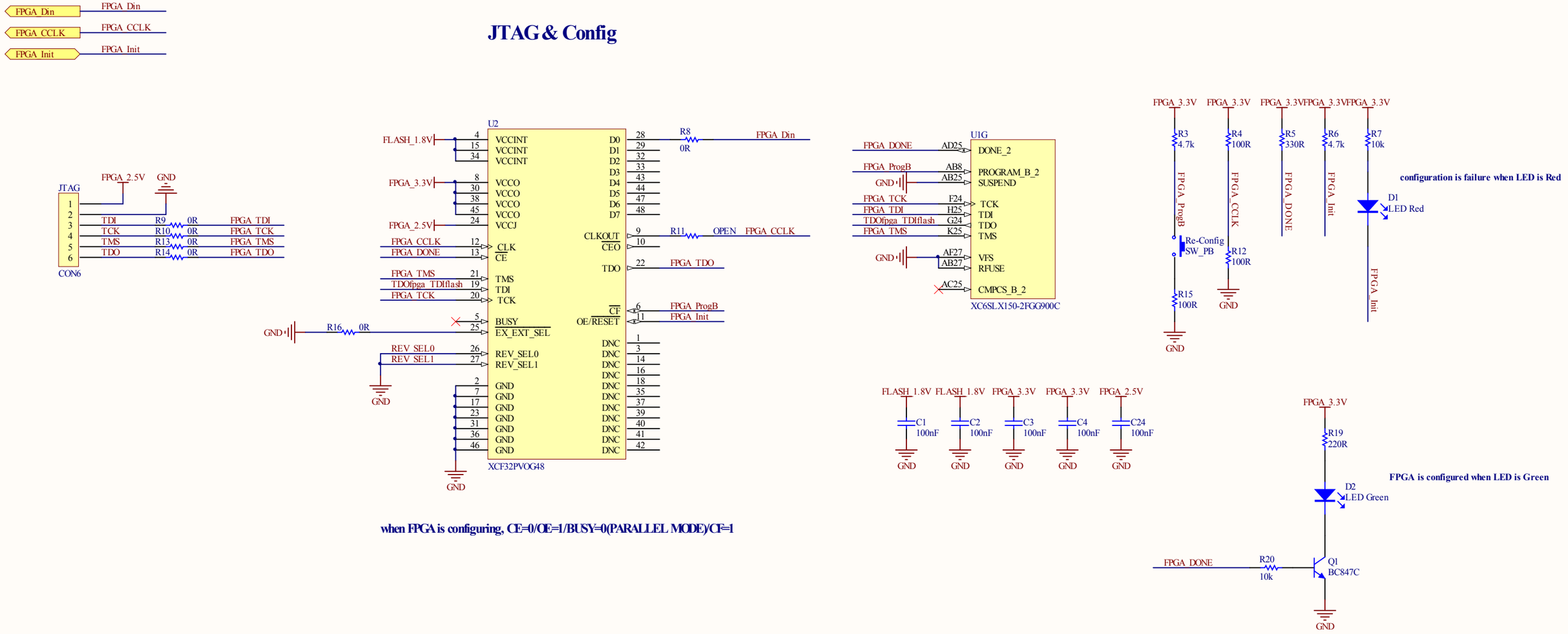
JTAG & Config



Global Clock

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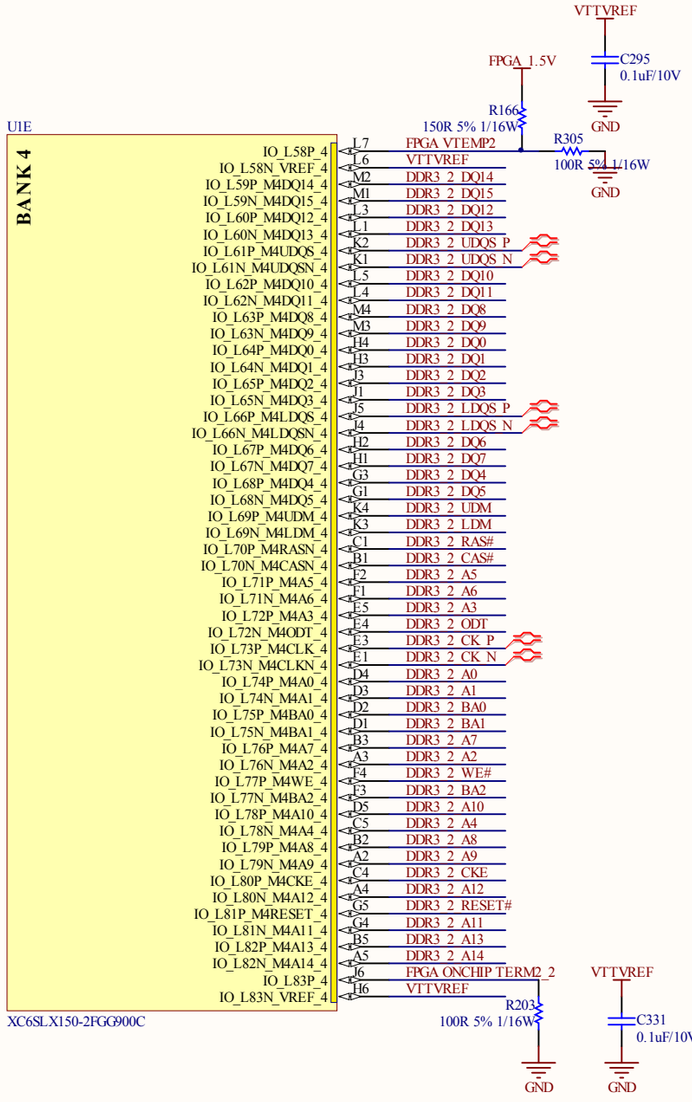
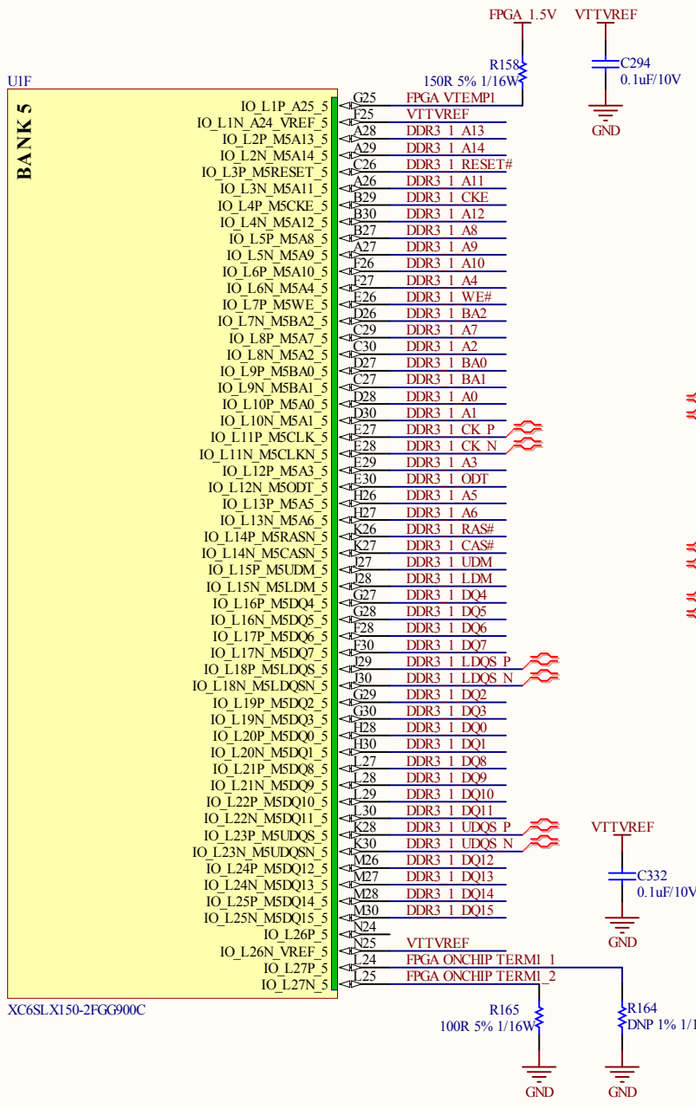
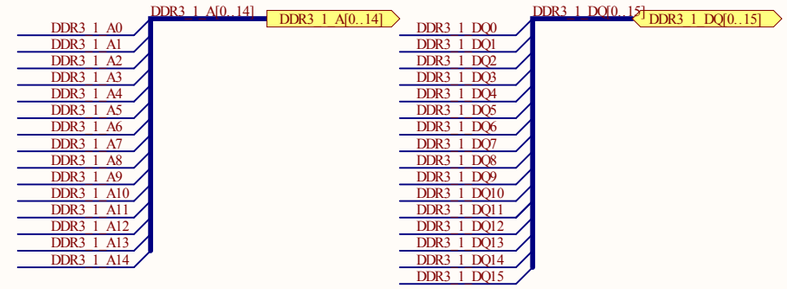
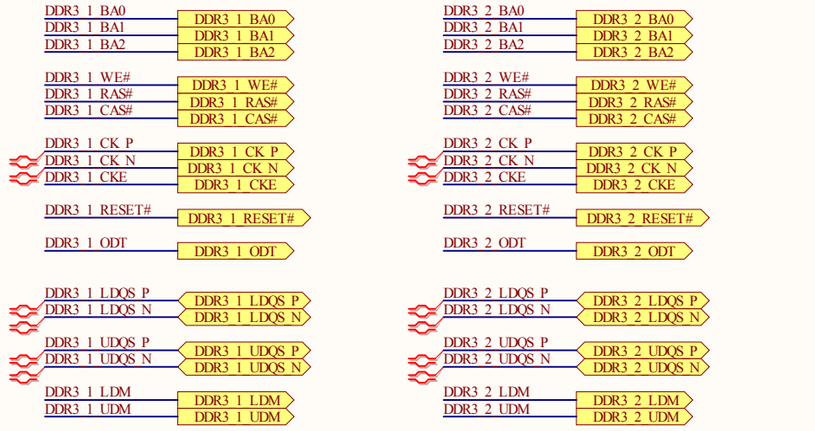
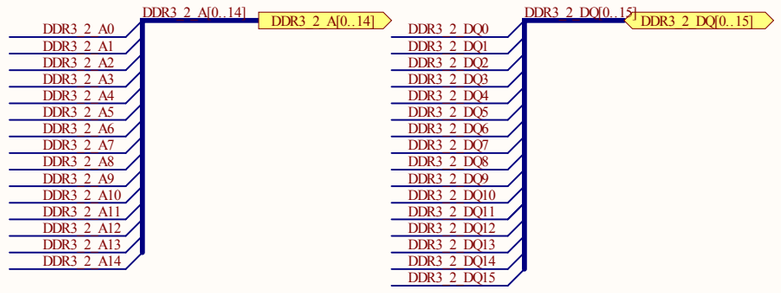
FPGA_DDR3











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FPGA_CTRL&LVDS

U1D

BANK 3

IO_L1P_3	AA10	
IO_L1N_VREF_3	AA9	
IO_L2P_3	AD7	
IO_L2N_3	AE7	
IO_L3P_3	Y9	
IO_L3N_3	Y8	
IO_L4P_3	AE6	USB_GPIO1
IO_L4N_3	AF6	USB_GPIO0
IO_L5P_3	AA12	
IO_L5N_3	AA11	
IO_L6P_3	AE5	DQ21
IO_L6N_3	AG5	SYS_RST_N
IO_L7P_3	T7	
IO_L7N_3	T6	
IO_L8P_3	AA7	
IO_L8N_3	AA6	
IO_L9P_3	AC6	
IO_L9N_3	AD6	
IO_L10P_3	AH5	
IO_L10N_3	AK5	USB_SCK_FPGA
IO_L11P_3	W10	
IO_L11N_3	W9	
IO_L12P_3	AB7	
IO_L12N_3	AB6	
IO_L13P_3	W7	
IO_L13N_3	W6	
IO_L14P_3	AH4	DQ23
IO_L14N_3	AK4	USB_MOSI_FPGA
IO_L15P_3	T9	
IO_L15N_3	T8	
IO_L16P_3	AH3	
IO_L16N_3	AK3	USB_SSN_FPGA
IO_L17P_3	Y7	
IO_L17N_VREF_3	Y6	
IO_L18P_3	AD5	HDR
IO_L18N_3	AK2	SEL
IO_L19P_3	AE4	DQ17
IO_L19N_3	AF4	DQ29
IO_L20P_3	AF3	DQ16
IO_L20N_3	AG3	DQ18
IO_L21P_3	V8	
IO_L21N_3	V7	
IO_L22P_3	AH1	TX1
IO_L22N_3	AJ1	TX2
IO_L23P_3	V10	
IO_L23N_3	V9	
IO_L24P_3	AG4	DQ22
IO_L24N_3	AH4	
IO_L25P_3	N10	
IO_L25N_3	N9	
IO_L26P_3	AF2	DQ20
IO_L26N_3	AH2	DQ19
IO_L27P_3	R7	
IO_L27N_3	R6	
IO_L28P_3	AF1	SPI_READ
IO_L28N_3	AG1	RST
IO_L29P_3	U7	
IO_L29N_3	U6	
IO_L30P_3	AE3	SPI_WRITE
IO_L30N_3	AE1	SPI_CLK
IO_L31P_3	N8	
IO_L31N_VREF_3	N7	
IO_L32P_M3DQ14_3	AC5	
IO_L32N_M3DQ15_3	AC4	DQ25
IO_L33P_M3DQ12_3	AD4	DQ24
IO_L33N_M3DQ13_3	AD3	FLAGB
IO_L34P_M3UDQS_3	AB4	DQ26
IO_L34N_M3UDQSN_3	AB3	DQ14
IO_L35P_M3DQ10_3	AD2	SPI_OUT
IO_L35N_M3DQ11_3	AD1	SPI_DATA
IO_L36P_M3DQ8_3	AC3	DQ15
IO_L36N_M3DQ9_3	AC1	
IO_L37P_M3DQ0_3	Y4	
IO_L37N_M3DQ1_3	Y3	
IO_L38P_M3DQ2_3	Y2	DQ11
IO_L38N_M3DQ3_3	Y1	DQ13
IO_L39P_M3LDQS_3	AA5	DQ27
IO_L39N_M3LDQSN_3	AA4	DQ31
IO_L40P_M3DQ6_3	W3	DQ10
IO_L40N_M3DQ7_3	W1	DQ12
IO_L41P_GCLK27_M3DQ4_3	AA3	DQ9
IO_L41N_GCLK26_M3DQS_3	AA1	PCLK
IO_L42P_GCLK25_TRDY2_M3LDM_3	AB2	USB_A0
IO_L42N_GCLK24_M3LDM_3	AB1	USB_A1
IO_L43P_GCLK23_M3RASN_3	W5	CLK_MAIN_OUT/TDIG1_BUF
IO_L43N_GCLK22_IRDY2_M3CASN_3	W4	
IO_L44P_GCLK21_M3A5_3	V4	DQ28
IO_L44N_GCLK20_M3A6_3	V3	DQ30
IO_L45P_M3A3_3	V2	DQ8
IO_L45N_M3ODT_3	V1	SLOE
IO_L46P_M3CLK_3	U5	DQ2
IO_L46N_M3CLKN_3	U4	DQ5
IO_L47P_M3A0_3	U3	DQ6
IO_L47N_M3A1_3	U1	SLWR
IO_L48P_M3BA0_3	T4	DQ3
IO_L48N_M3BA1_3	T3	DQ7
IO_L49P_M3A7_3	T2	INT
IO_L49N_M3A2_3	T1	SLRD
IO_L50P_M3WE_3	R5	
IO_L50N_M3BA2_3	R4	DQ1
IO_L51P_M3A10_3	R3	DQ4
IO_L51N_M3A4_3	R1	SLCS
IO_L52P_M3A8_3	P4	
IO_L52N_M3A9_3	P3	DQ0
IO_L53P_M3CKE_3	N5	
IO_L53N_M3A12_3	N4	
IO_L54P_M3RESET_3	P2	PKTEND
IO_L54N_M3A11_3	P1	FLAGA
IO_L55P_M3A13_3	N3	
IO_L55N_M3A14_3	N1	CLKIN_FPGA
IO_L56P_3	P7	
IO_L56N_3	P6	
IO_L57P_3	M7	
IO_L57N_VREF_3	M6	

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U1C

BANK 2

IO_L1P_CCLK_2	AJ26	FPGA_CCLK
IO_L1N_M0_CMPMISO_2	AK26	FPGA_3.3V
IO_L2P_CMPCLK_2	AD24	
IO_L2N_CMPMOSI_2	AE24	
IO_L3P_D0_DIN_MISO_MISO1_2	AH25	FPGA_Din
IO_L3N_MOSI_CSI_B_MISO0_2	AK25	CLK_MAIN
IO_L4P_2	AF25	OUT15_TOP_P
IO_L4N_VREF_2	AG25	OUT15_TOP_N
IO_L5P_2	AG24	OUT13_TOP_P
IO_L5N_2	AH24	OUT13_TOP_N
IO_L6P_2	AD23	
IO_L6N_2	AE23	
IO_L7P_2	AD22	OUT10_TOP_P
IO_L7N_2	AE22	OUT10_TOP_N
IO_L8P_2	AC21	
IO_L8N_2	AD21	
IO_L9P_2	AF23	OUT12_TOP_P
IO_L9N_2	AG23	OUT12_TOP_N
IO_L10P_2	AD20	
IO_L10N_2	AE20	
IO_L11P_2	AJ24	OUT14_TOP_P
IO_L11N_2	AK24	OUT14_TOP_N
IO_L12P_D1_MISO2_2	AH23	OUT11_TOP_P
IO_L12N_D2_MISO3_2	AK23	OUT11_TOP_N
IO_L13P_M1_2	AJ22	GND
IO_L13N_D10_2	AK22	
IO_L14P_D11_2	AH21	OUT7_TOP_P
IO_L14N_D12_2	AK21	OUT7_TOP_N
IO_L15P_2	AG22	OUT9_TOP_P
IO_L15N_2	AH22	OUT9_TOP_N
IO_L16P_2	AJ20	OUT5_TOP_P
IO_L16N_VREF_2	AK20	OUT5_TOP_N
IO_L17P_2	AF21	OUT8_TOP_P
IO_L17N_2	AG21	OUT8_TOP_N
IO_L18P_2	AB20	
IO_L18N_2	AC20	
IO_L19P_2	AD19	
IO_L19N_2	AE19	
IO_L20P_2	AG20	OUT6_TOP_P
IO_L20N_2	AH20	OUT6_TOP_N
IO_L21P_2	AD18	
IO_L21N_2	AE18	
IO_L22P_2	AA19	
IO_L22N_2	AB19	
IO_L23P_2	AF19	OUT4_TOP_P
IO_L23N_2	AG19	OUT4_TOP_N
IO_L24P_2	AG18	OUT2_TOP_P
IO_L24N_VREF_2	AH18	OUT2_TOP_N
IO_L25P_2	AB18	
IO_L25N_2	AC18	
IO_L26P_2	AF17	
IO_L26N_2	AG17	
IO_L27P_2	AD17	
IO_L27N_2	AE17	
IO_L28P_2	AD16	
IO_L28N_2	AE16	
IO_L29P_GCLK3_2	AH19	OUT3_TOP_P
IO_L29N_GCLK2_2	AK19	OUT3_TOP_N
IO_L30P_GCLK1_D13_2	AJ18	OUT1_TOP_P
IO_L30N_GCLK0_USERCCLK_2	AK18	OUT1_TOP_N
IO_L31P_GCLK31_D14_2	AJ16	CLKOUT_P
IO_L31N_GCLK30_D15_2	AK16	CLKOUT_N
IO_L32P_GCLK29_2	AH17	OUT0_TOP_P
IO_L32N_GCLK28_2	AK17	OUT0_TOP_N
IO_L33P_2	AB16	
IO_L33N_2	AC16	
IO_L34P_2	AF15	
IO_L34N_2	AG15	
IO_L35P_2	AG16	
IO_L35N_2	AH16	
IO_L36P_2	AD15	COL_INIT_TOP
IO_L36N_2	AE15	COL_INIT_BOT
IO_L37P_2	AA15	
IO_L37N_2	AB15	
IO_L38P_2	AH15	LVDS_CTR_P
IO_L38N_2	AK15	LVDS_CTR_N
IO_L39P_2	AJ14	OUT1_BOT_P
IO_L39N_2	AK14	OUT1_BOT_N
IO_L40P_2	AB14	
IO_L40N_2	AC14	
IO_L41P_2	AH13	OUT3_BOT_P
IO_L41N_VREF_2	AK13	OUT3_BOT_N
IO_L42P_2	AD14	
IO_L42N_2	AE14	READ
IO_L43P_2	AF13	OUT2_BOT_P
IO_L43N_2	AG13	OUT2_BOT_N
IO_L44P_2	AG14	OUT0_BOT_P
IO_L44N_2	AH14	OUT0_BOT_N
IO_L45P_2	AG12	OUT4_BOT_P
IO_L45N_2	AH12	OUT4_BOT_N
IO_L46P_2	AD13	
IO_L46N_2	AE13	SAMPLE_TOP
IO_L47P_2	AD12	
IO_L47N_2	AE12	
IO_L48P_D7_2	AH11	OUT7_BOT_P
IO_L48N_RDWR_B_VREF_2	AK11	OUT7_BOT_N
IO_L49P_D3_2	AJ12	OUT5_BOT_P
IO_L49N_D4_2	AK12	OUT5_BOT_N
IO_L50P_2	AB12	SYNC_X
IO_L50N_2	AC12	
IO_L51P_2	AF11	OUT6_BOT_P
IO_L51N_2	AG11	OUT6_BOT_N
IO_L52P_2	AB11	
IO_L52N_2	AD11	SAMPLE_BOT
IO_L53P_2	AJ10	OUT9_BOT_P
IO_L53N_2	AK10	OUT9_BOT_N
IO_L54P_2	AH9	OUT11_BOT_P
IO_L54N_2	AK9	OUT11_BOT_N
IO_L55P_2	AG10	OUT8_BOT_P
IO_L55N_2	AH10	OUT8_BOT_N
IO_L56P_2	AD10	
IO_L56N_2	AE10	COL_PC_FRAME_REQ
IO_L57P_2	AF9	OUT10_BOT_P
IO_L57N_2	AG9	OUT10_BOT_N
IO_L58P_2	AG8	OUT12_BOT_P
IO_L58N_2	AH8	OUT12_BOT_N
IO_L59P_2	AF7	OUT14_BOT_P
IO_L59N_2	AG7	OUT14_BOT_N
IO_L60P_2	AD9	
IO_L60N_2	AE9	VTZERO
IO_L61P_2	AD8	
IO_L61N_VREF_2	AE8	ADC_PC
IO_L62P_D5_2	AJ8	OUT13_BOT_P
IO_L62N_D6_2	AK8	OUT13_BOT_N
IO_L63P_2	AG6	BLSUN_HG_LG
IO_L63N_2	AH6	TREF_TSIG
IO_L64P_D8_2	AH7	OUT15_BOT_P
IO_L64N_D9_2	AK7	OUT15_BOT_N
IO_L65P_INIT_B_2	AJ6	FPGA_Init
IO_L65N_CSO_B_2	AK6	USB_MISO_FPGA

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U1B

BANK 1

IO_L1P_1	M23	
IO_L1N_VREF_1	M24	
IO_L2P_A23_M1A13_1	N29	
IO_L2N_A22_M1A14_1	N30	FPGA_IO7
IO_L3P_A21_M1RESET_1	N27	
IO_L3N_A20_M1A11_1	N28	
IO_L4P_A19_M1CKE_1	P28	
IO_L4N_VREF_1	P30	FPGA_IO6
IO_L5P_A18_M1A12_1	P26	
IO_L5N_A17_M1A8_1	P27	
IO_L6P_A16_M1A9_1	R29	
IO_L6N_A15_M1A10_1	R30	FPGA_IO5
IO_L7P_A14_M1A4_1	R27	
IO_L7N_A13_M1WE_1	R28	
IO_L8P_A12_M1BA2_1	L26	
IO_L8N_A11_M1A7_1	L27	
IO_L9P_A10_M1A2_1	L28	
IO_L9N_A9_M1BA0_1	L30	FPGA_IO4
IO_L10P_A8_M1BA1_1	L29	
IO_L10N_A7_M1A0_1	L30	FPGA_IO3
IO_L11P_A6_M1A1_1	J27	
IO_L11N_A5_M1CLK_1	J28	
IO_L12P_A4_M1CLKN_1	J28	
IO_L13P_M1A3_1	V30	FPGA_IO2
IO_L13N_M1ODT_1	V26	
IO_L14P_GCLK31_M1A5_1	V27	
IO_L14N_GCLK30_M1A6_1	W27	
IO_L15P_GCLK9_IRDY1_M1RASN_1	W28	
IO_L15N_GCLK8_M1CASN_1	AB28	ROW<4>
IO_L16P_GCLK7_M1UDM_1	AB30	ROW<1>
IO_L16N_GCLK6_TRDY1_M1LDM_1	W29	
IO_L17P_GCLK5_M1DQ4_1	W30	FPGA_IO1
IO_L17N_GCLK4_M1DQ5_1	Y28	
IO_L18P_A3_M1DQ6_1	Y30	FPGA_IO0
IO_L18N_A2_M1DQ7_1	AA29	ROW<5>
IO_L19P_A1_M1LDQS_1	AA30	ROW<0>
IO_L19N_A0_M1LDQSN_1	AA27	
IO_L20P_FCS_B_M1DQ0_1	AA28	
IO_L20N_FOE_B_M1DQ3_1	Y26	
IO_L21P_FWE_B_M1DQ0_1	Y27	
IO_L21N_LDC_M1DQ1_1	AD28	
IO_L22P_HDC_M1DQ6_1	AD30	ROW<3>
IO_L22N_M1DQ9_1	AC27	
IO_L23P_M1DQ10_1	AC28	
IO_L23N_M1DQ11_1	AC29	
IO_L24P_M1UDQS_1	AC30	ROW<2>
IO_L24N_M1UDQSN_1	AE29	
IO_L25P_M1DQ12_1	AE30	ROW<6>
IO_L25N_M1DQ13_1	AE27	
IO_L26P_M1DQ14_1	AE28	
IO_L26N_M1DQ15_1	W24	
IO_L27P_1	W25	
IO_L27N_VREF_1	R21	
IO_L28P_1	R22	
IO_L28N_1	AF30	ROW<7>
IO_L29P_1	AF22	
IO_L29N_1	AG29	
IO_L30P_1	AG30	ROW<8>
IO_L30N_1	P24	
IO_L31P_1	P25	
IO_L31N_1	AH30	ROW<9>
IO_L32P_1	AJ30	ROW<10>
IO_L32N_1	R24	
IO_L33P_1	R25	
IO_L33N_1	AJ29	
IO_L34P_1	AK29	ROW<11>
IO_L34N_1	T24	
IO_L35P_1	T25	
IO_L35N_1	AJ28	
IO_L36P_1	AK28	
IO_L36N_1	U24	
IO_L37P_1	U25	
IO_L37N_1	AG27	
IO_L38P_1	AG28	
IO_L38N_1	V23	
IO_L39P_1	V24	
IO_L39N_1	AD26	
IO_L40P_1	AD27	
IO_L40N_1	W21	
IO_L41P_1	W22	
IO_L41N_1	AD27	
IO_L42P_1	AK27	
IO_L42N_1	Y22	
IO_L43P_1	Y23	
IO_L43N_1	AE25	
IO_L44P_1	AE26	
IO_L44N_1	Y24	
IO_L45P_1	Y25	
IO_L45N_1	AG26	
IO_L46P_1	AH26	
IO_L46N_1	AA24	
IO_L47P_AWAKE_1	AA25	
IO_L47N_DOUT_BUSY_1		

XC6SLX150-2FGG900C

CLK_MAIN — CLK_MAIN

SYS_RST_N — SYS_RST_N

RST	RST
SEL	SEL
TX2	TX2
TX1	TX1
HDR	HDR
SYNC_X	SYNC_X
BLSUN_HG_LG	BLSUN_HG_LG
TREF_TSIG	TREF_TSIG
VTZERO	VTZERO
READ	READ
ADC_PC	ADC_PC
SAMPLE_BOT	SAMPLE_BOT
SAMPLE_TOP	SAMPLE_TOP
COL_INIT_BOT	COL_INIT_BOT
COL_INIT_TOP	COL_INIT_TOP
COL_PC_FRAME_REQ	COL_PC_FRAME_REQ

SPI_READ	SPI_READ
SPI_OUT	SPI_OUT
SPI_WRITE	SPI_WRITE
SPI_DATA	SPI_DATA
SPI_CLK	SPI_CLK

ROW<0>	ROW<0>
ROW<1>	ROW<1>
ROW<2>	ROW<2>
ROW<3>	ROW<3>
ROW<4>	ROW<4>
ROW<5>	ROW<5>
ROW<6>	ROW<6>
ROW<7>	ROW<7>
ROW<8>	ROW<8>
ROW<9>	ROW<9>
ROW<10>	ROW<10>
ROW<11>	ROW<11>

DQ3	DQ3
DQ6	DQ6
DQ7	DQ7

OUT0_BOT_N	OUT0_BOT_N
OUT0_BOT_P	OUT0_BOT_P
OUT1_BOT_N	OUT1_BOT_N
OUT1_BOT_P	OUT1_BOT_P
OUT2_BOT_N	OUT2_BOT_N
OUT2_BOT_P	OUT2_BOT_P
OUT3_BOT_N	OUT3_BOT_N
OUT3_BOT_P	OUT3_BOT_P
OUT4_BOT_N	OUT4_BOT_N
OUT4_BOT_P	OUT4_BOT_P
OUT5_BOT_N	OUT5_BOT_N
OUT5_BOT_P	OUT5_BOT_P
OUT6_BOT_N	OUT6_BOT_N
OUT6_BOT_P	OUT6_BOT_P
OUT7_BOT_N	OUT7_BOT_N
OUT7_BOT_P	OUT7_BOT_P
OUT8_BOT_N	OUT8_BOT_N
OUT8_BOT_P	OUT8_BOT_P
OUT9_BOT_N	OUT9_BOT_N
OUT9_BOT_P	OUT9_BOT_P
OUT10_BOT_N	OUT10_BOT_N
OUT10_BOT_P	OUT10_BOT_P
OUT11_BOT_N	OUT11_BOT_N
OUT11_BOT_P	OUT11_BOT_P
OUT12_BOT_N	OUT12_BOT_N
OUT12_BOT_P	OUT12_BOT_P
OUT13_BOT_N	OUT13_BOT_N
OUT13_BOT_P	OUT13_BOT_P
OUT14_BOT_N	OUT14_BOT_N
OUT14_BOT_P	OUT14_BOT_P
OUT15_BOT_N	OUT15_BOT_N
OUT15_BOT_P	OUT15_BOT_P

FPGA_Din — FPGA_Din

FPGA_CCLK — FPGA_CCLK

FPGA_Init — FPGA_Init

DQ0	DQ0
DQ1	DQ1
DQ2	DQ2
DQ4	DQ4
DQ5	DQ5
DQ8	DQ8
DQ9	DQ9
DQ10	DQ10
DQ11	DQ11
DQ12	DQ12
DQ13	DQ13
DQ14	DQ14
DQ15	DQ15
DQ16	DQ16
DQ17	DQ17
DQ18	DQ18
DQ19	DQ19
DQ20	DQ20
DQ21	DQ21
DQ22	DQ22
DQ23	DQ23
DQ24	DQ24
DQ25	DQ25
DQ26	DQ26
DQ27	DQ27
DQ28	DQ28
DQ29	DQ29
DQ30	DQ30
DQ31	DQ31
USB_GPIO1	USB_GPIO1
USB_GPIO0	USB_GPIO0

USB_A1	USB_A1
USB_A0	USB_A0

PCLK	PCLK
SLCS	SLCS
SLWR	SLWR
SLOE	SLOE
SLRD	SLRD
PKTEND	PKTEND
CLKIN_FPGA	CLKIN_FPGA
INT	INT

USB_SCK_FPGA	USB_SCK_FPGA
USB_SSN_FPGA	USB_SSN_FPGA
USB_MISO_FPGA	USB_MISO_FPGA
USB_MOSI_FPGA	USB_MOSI_FPGA

FLAGA	FLAGA
FLAGB	FLAGB

FPGA_IO5	R22	100R	LS_IO1
FPGA_IO4	R23	100R	LS_IO2
FPGA_IO3	R24	100R	LS_IO3
FPGA_IO2	R25	100R	LS_IO4
FPGA_IO1	R26	100R	LS_IO5
FPGA_IO0	R27	100R	LS_IO6

FPGA

FPGA_TEST_IO

LS_IO6	1	2	LS_IO4
LS_IO5	3	4	LS_IO3
LS_LED+	5	6	LS_IO1
LS_IO2	7	8	
LS_LED-	9	10	

GND — GND

Header 5X2

FPGA_3.3V — R21 50R — LS_LED+

LS_LED-

FPGA_IO6 — R28 10k — Q3 BC847C 100mA

GND

CLK_MAIN_OUT/TDIG1_BUF — CLK_MAIN_OUT/TDIG1_BUF

LVDS_CTR_N	LVDS_CTR_N
LVDS_CTR_P	LVDS_CTR_P
CLKOUT_N	CLKOUT_N
CLKOUT_P	CLKOUT_P
OUT0_TOP_N	OUT0_TOP_N
OUT0_TOP_P	OUT0_TOP_P
OUT1_TOP_N	OUT1_TOP_N
OUT1_TOP_P	OUT1_TOP_P
OUT2_TOP_N	OUT2_TOP_N
OUT2_TOP_P	OUT2_TOP_P
OUT3_TOP_N	OUT3_TOP_N
OUT3_TOP_P	OUT3_TOP_P
OUT4_TOP_N	OUT4_TOP_N
OUT4_TOP_P	OUT4_TOP_P
OUT5_TOP_N	OUT5_TOP_N
OUT5_TOP_P	OUT5_TOP_P
OUT6_TOP_N	OUT6_TOP_N
OUT6_TOP_P	OUT6_TOP_P
OUT7_TOP_N	OUT7_TOP_N
OUT7_TOP_P	OUT7_TOP_P
OUT8_TOP_N	OUT8_TOP_N
OUT8_TOP_P	OUT8_TOP_P
OUT9_TOP_N	OUT9_TOP_N
OUT9_TOP_P	OUT9_TOP_P
OUT10_TOP_N	OUT10_TOP_N
OUT10_TOP_P	OUT10_TOP_P
OUT11_TOP_N	OUT11_TOP_N
OUT11_TOP_P	OUT11_TOP_P
OUT12_TOP_N	OUT12_TOP_N
OUT12_TOP_P	OUT12_TOP_P
OUT13_TOP_N	OUT13_TOP_N
OUT13_TOP_P	OUT13_TOP_P
OUT14_TOP_N	OUT14_TOP_N
OUT14_TOP_P	OUT14_TOP_P
OUT15_TOP_N	OUT15_TOP_N
OUT15_TOP_P	OUT15_TOP_P

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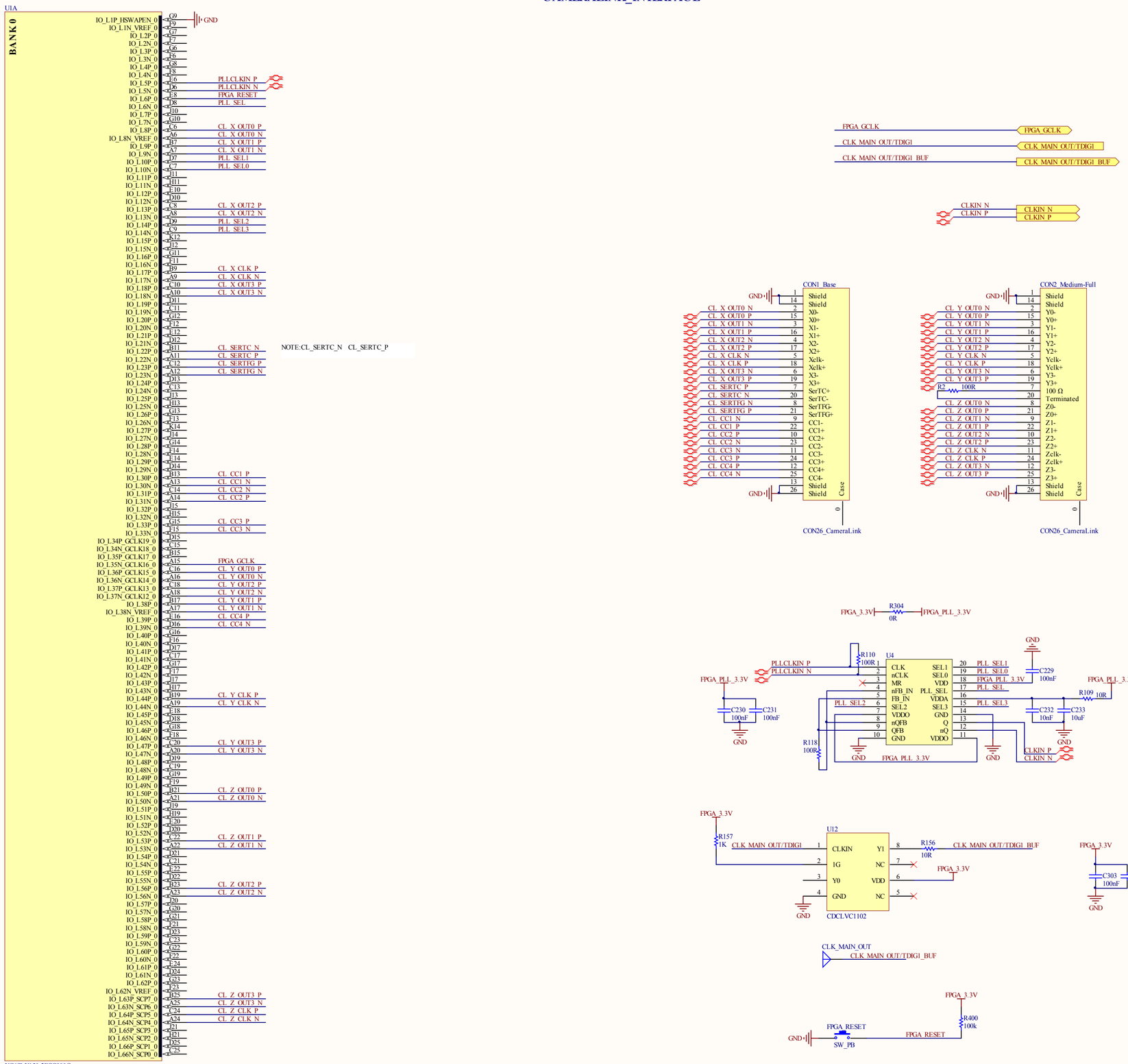

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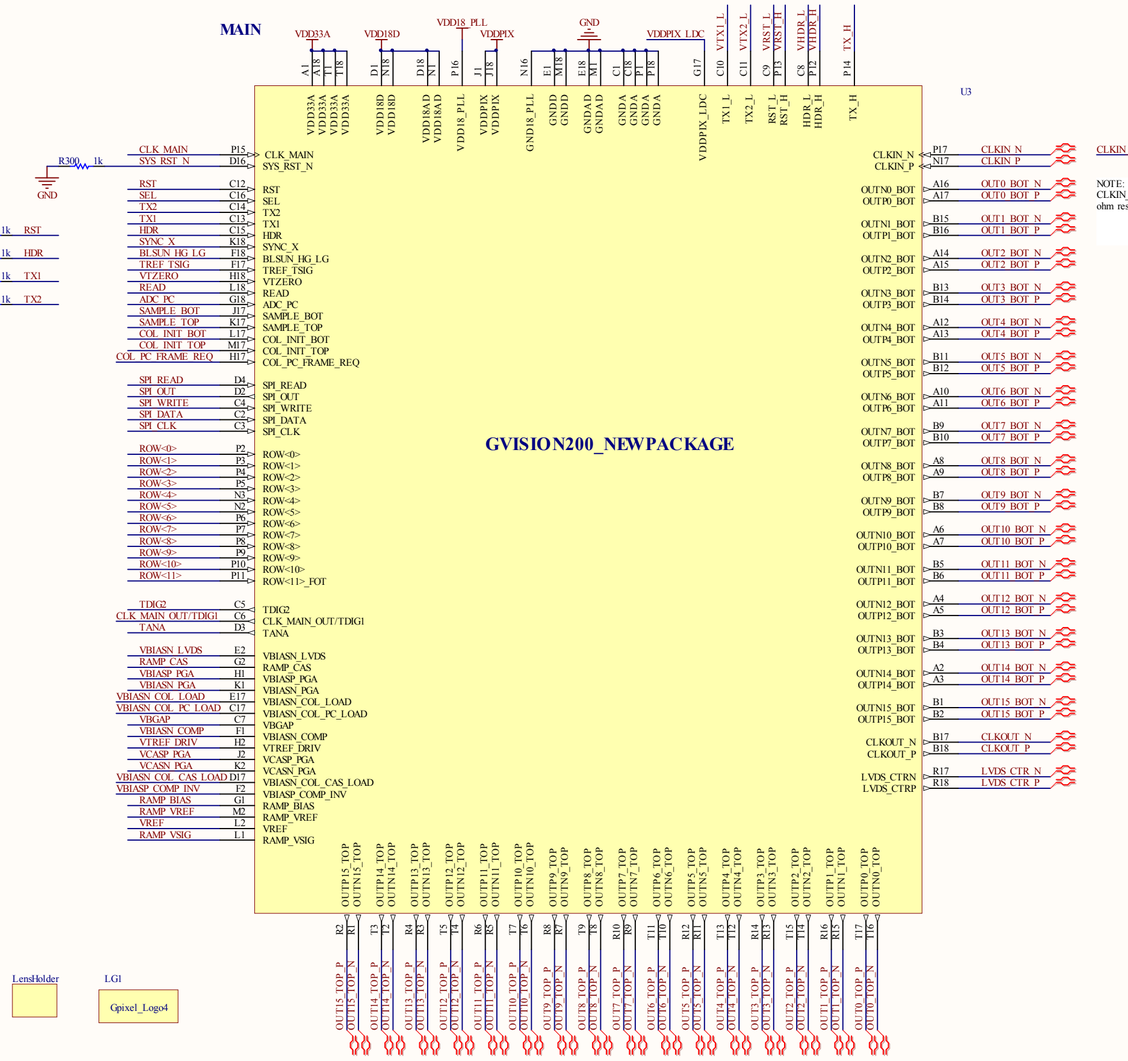
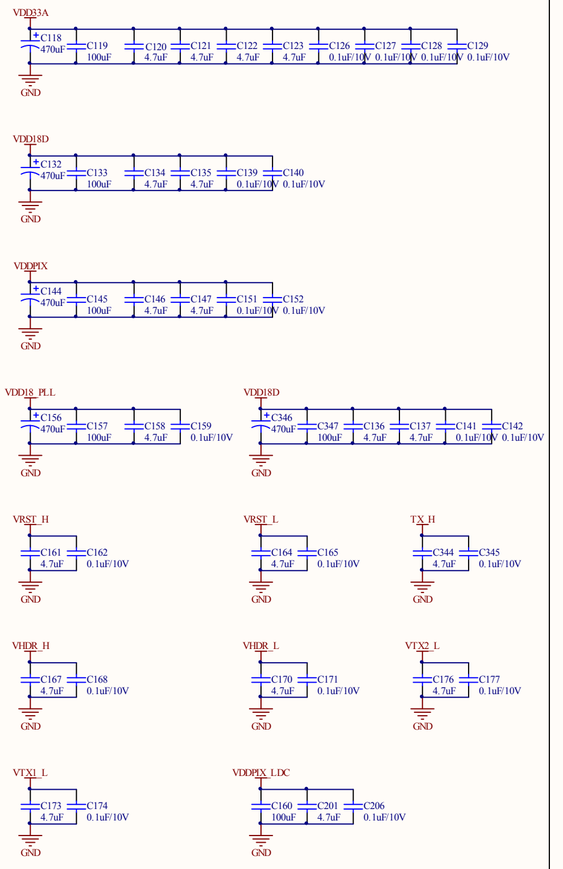


POWER_DECOUPLE



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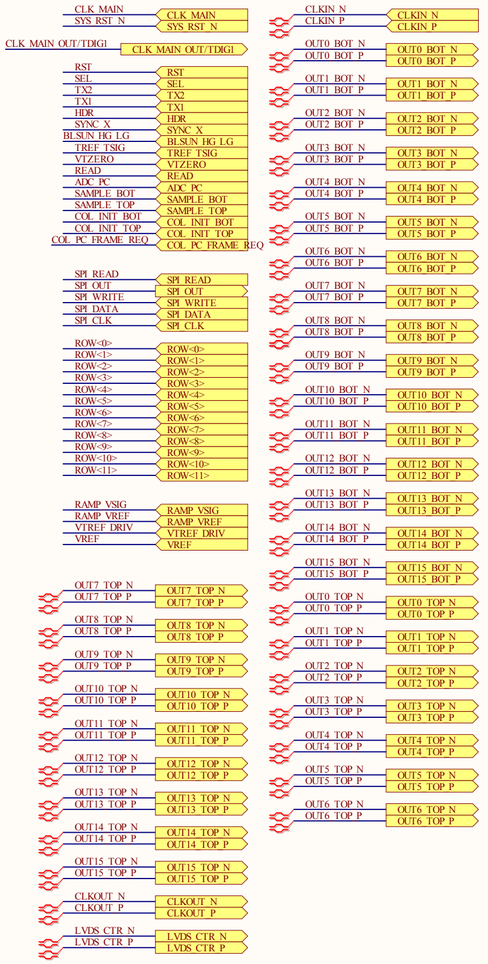

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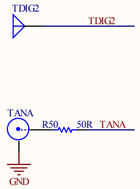

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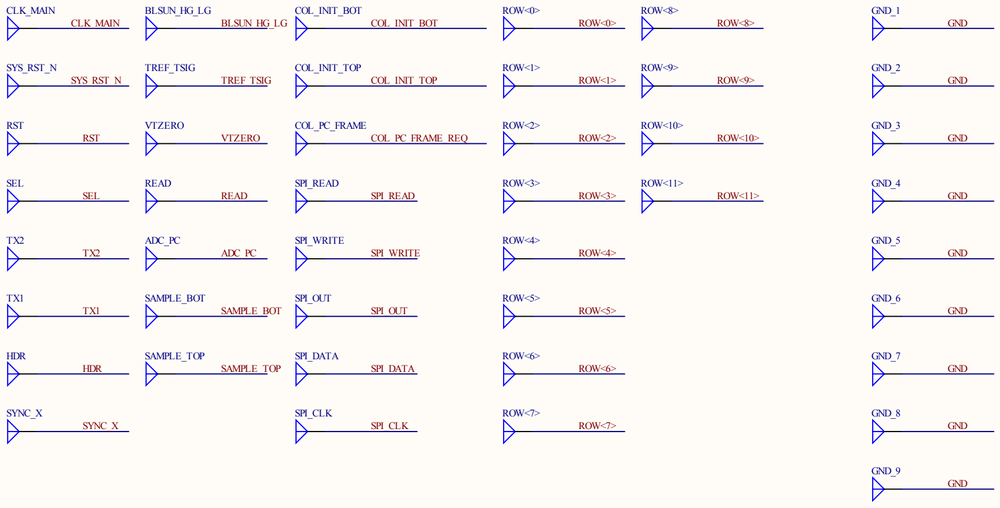

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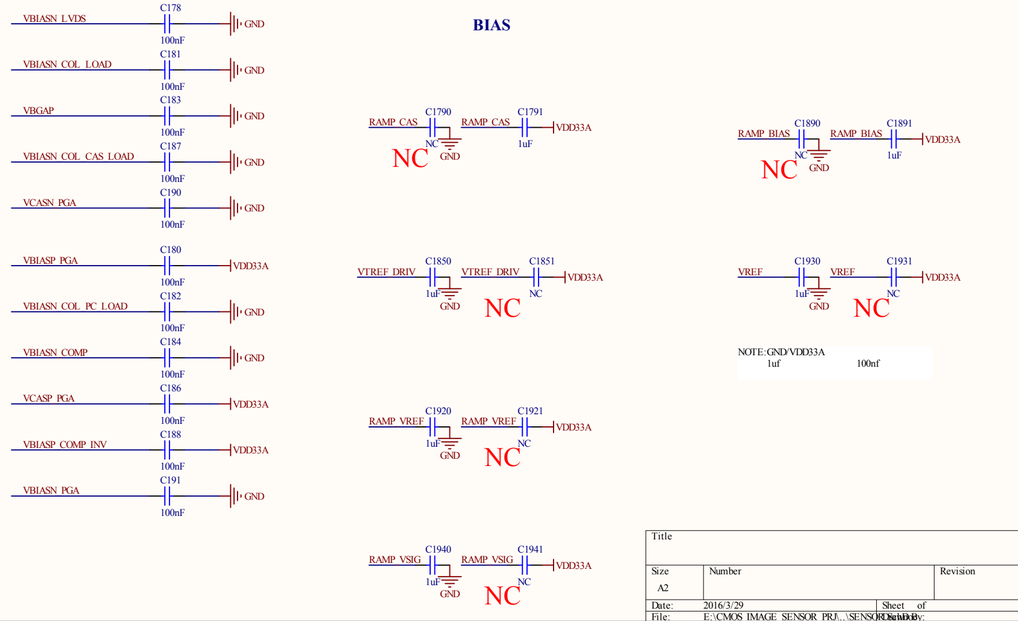

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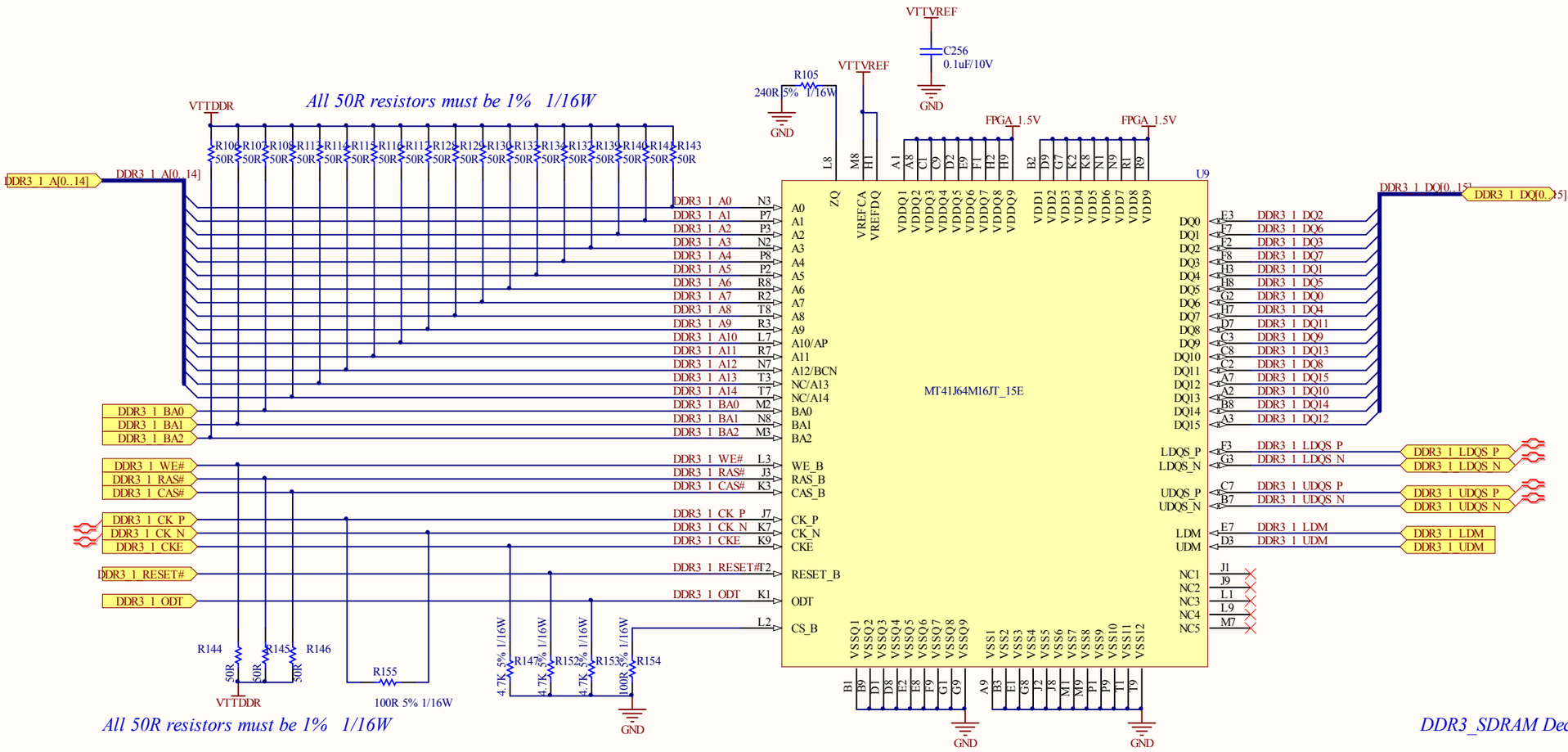
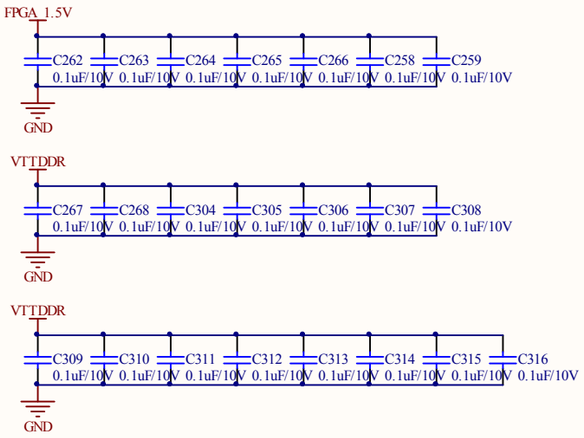
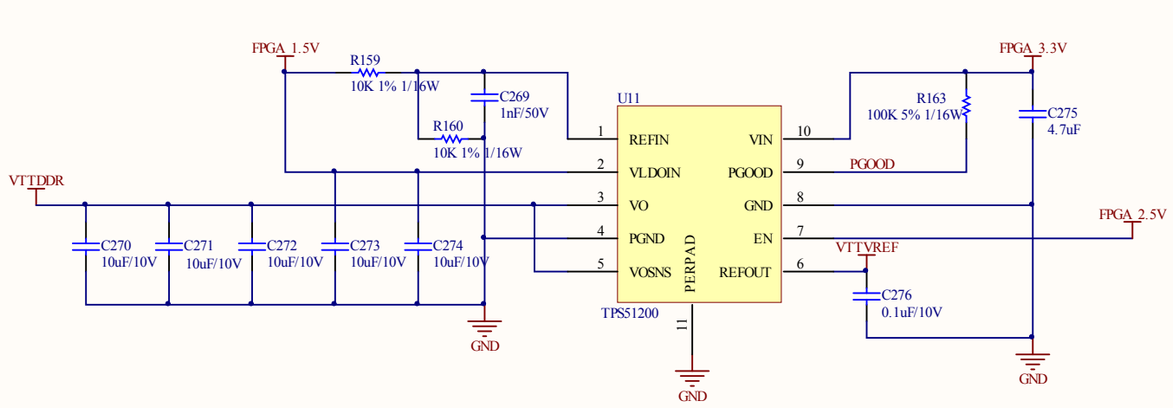
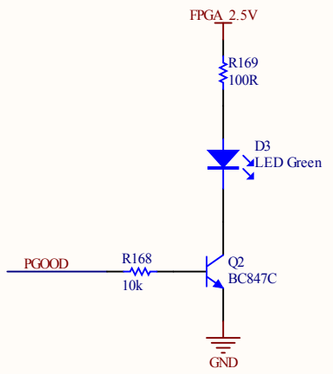
DDR3_1 SDRAM 1Gbit



DDR3_SDRAM Decoupling

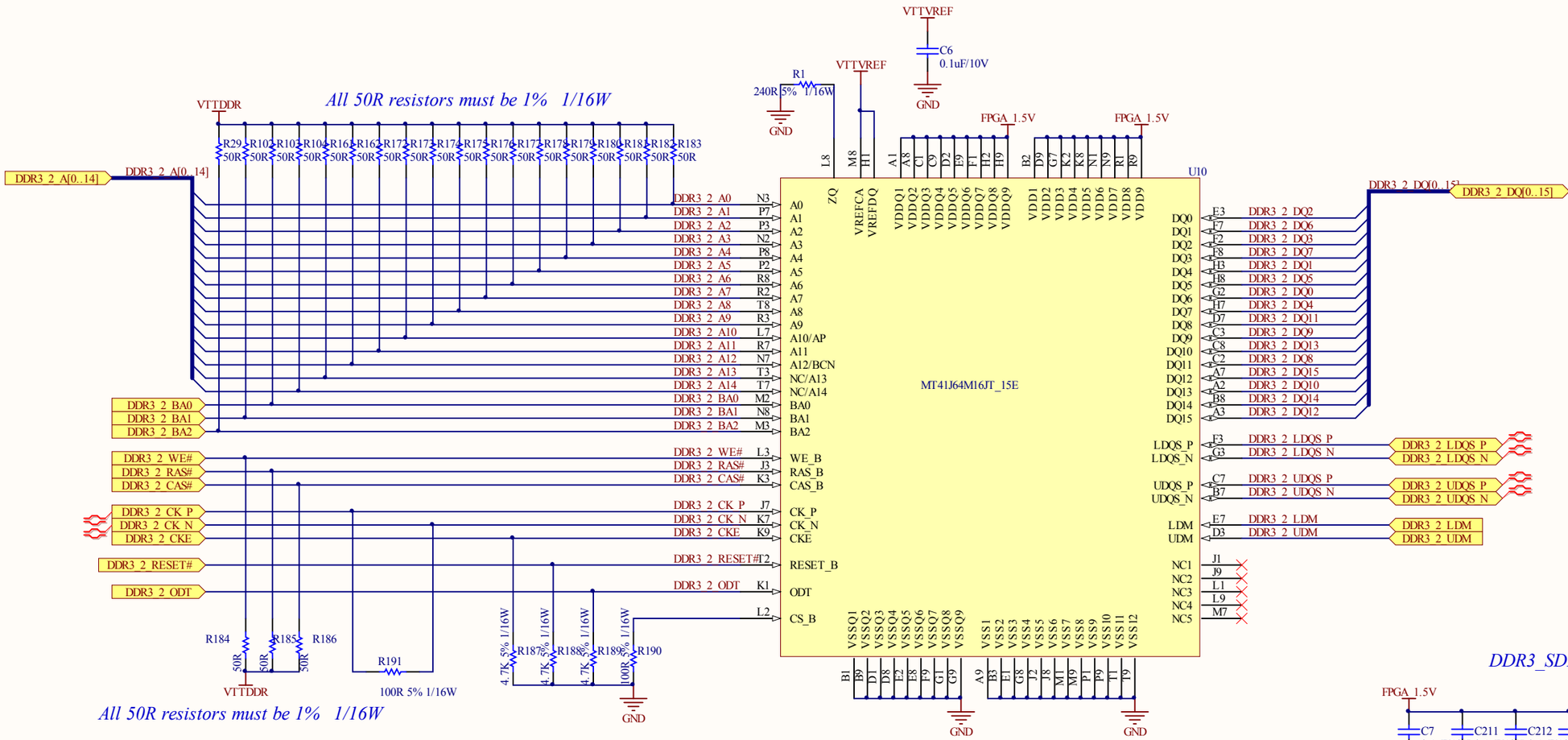




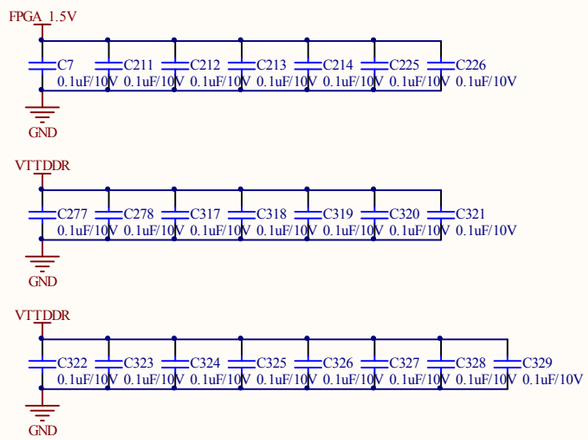


Cannot open file Z:\ \Altium Designer LIB\ \ LOGO \QQ 20140307111123.jpg	Title:		
	Coments:		
	Author:	Date:	Projects:
	Sheet of:	Version:	
Company: 长春长光辰芯光电技术有限公司 (Gpixelinc) www.gpixelinc.com			

DDR3_2 SDRAM 1Gbit



DDR3_SDRAM Decoupling



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Size: A3	Number	Revision
Date: 2016/3/29		Sheet of
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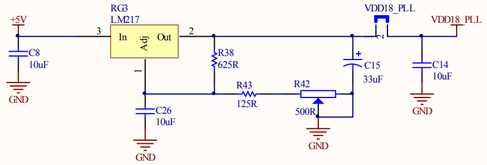
Revision History(Compared to V2.0 V3.0)

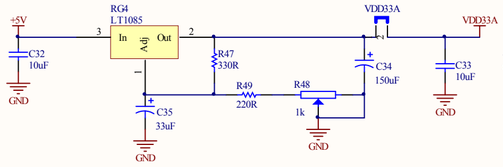
Data	Revision
2015 07 31	1 G200 image sensor socket 2 VDD18D VDD18D VDD18AD 1.8V 3 TX_H 4 Image lag Test IO, LED 5 Flash 1.8V LT_1761 LDO 6 PCB 246mm*185mm 7 FPGA_VBATT FPGA_2.5V 8 FPGA_1.2V USB_1.2V; 9 4.7uF 100nF 100uF
2015 08 13	1 J1--J6 2 CLKIN_P&CLKIN_N 100Ω 3 VTTDDR LVDS2 VCC
2016 01 30	1 VDD18 2 RST HDR TX1 TX2 1KΩ 3 +5V TVS LTM4628 LTM4616 4 ROW<011>

Gpixel.INC 长光辰芯光电	Title:		
	Coments:		
	Author:	Date:	Projects:
	Sheet of:	Version:	
Company: 长春长光辰芯光电技术有限公司 (Gpixelinc)		www.gpixelinc.com	

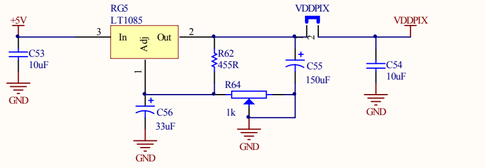
SENSOR_POWER_SUPPLY



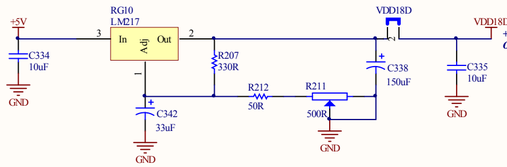
+1.8V for PLL
OUTPUT: 1.5V-2.5V



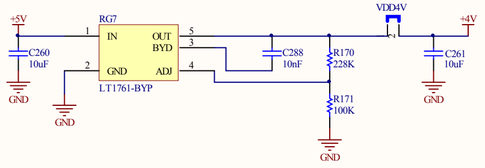
+3.3V for VDD33A
OUTPUT: 2.8V-4.2V

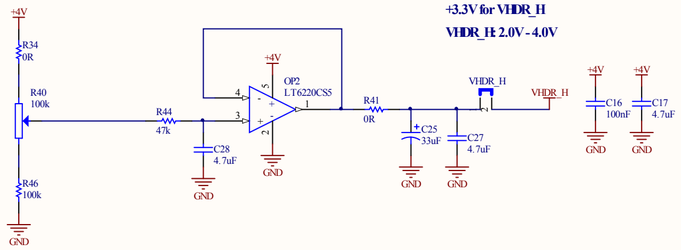


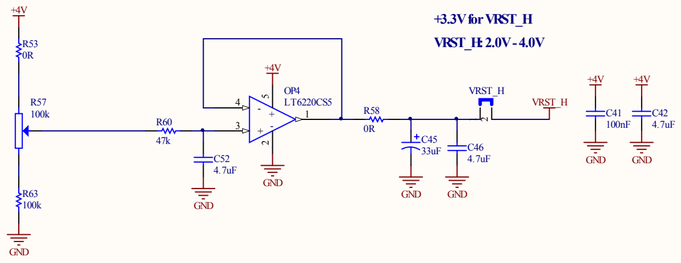
+3.0V for PIXEL
OUTPUT: 1.25V-4.0V

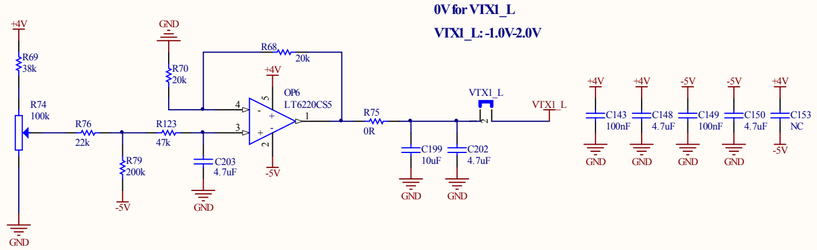


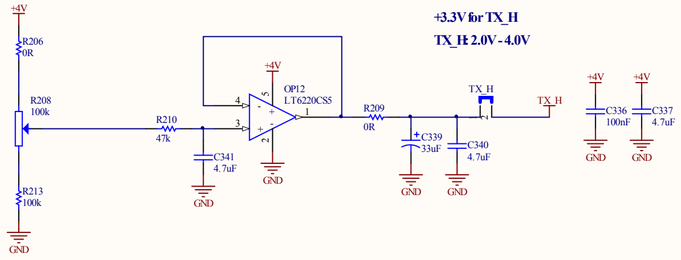
+1.8V for LVDS
OUTPUT: 1.5V-2.5V

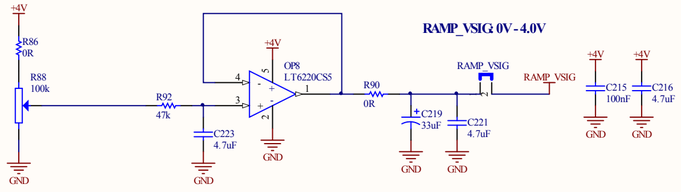


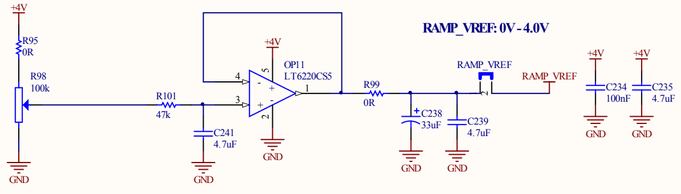


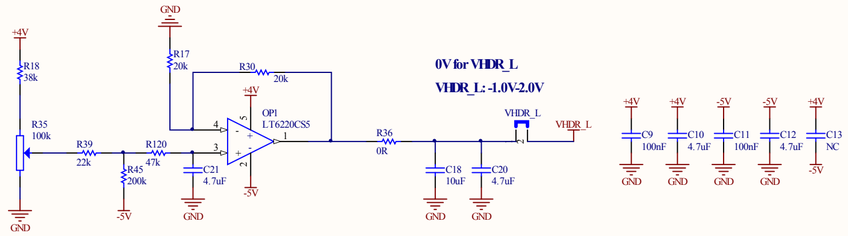


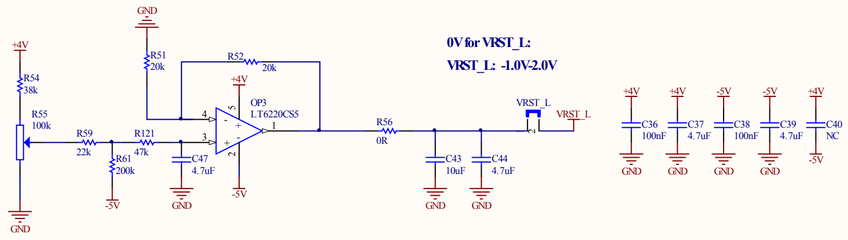


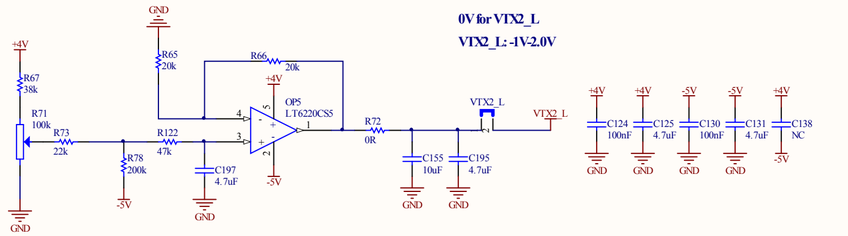


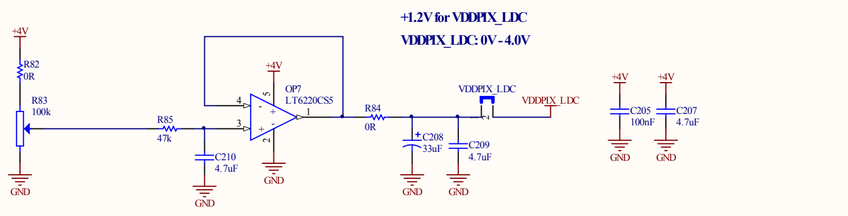


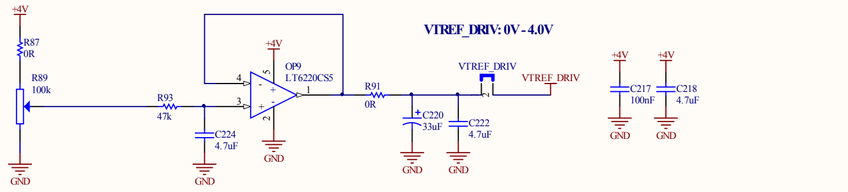


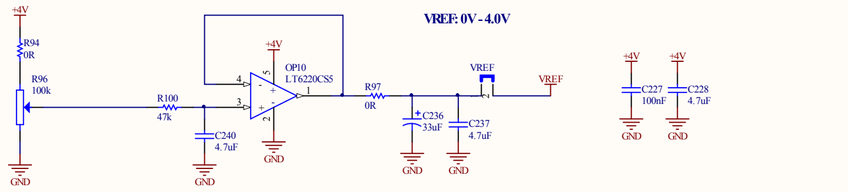












RAMP_VSIG → RAMP_VSIG
RAMP_VREF → RAMP_VREF
VTREF_DRIV → VTREF_DRIV
VREF → VREF

Gpixel.INC 长光辰芯光电	Title:	
	Coments:	
	Author:	Date: Projects:
	Sheet of:	Version:
Company: 长春长光辰芯光电技术有限公司 (Gpixelinc)		www.gpixelinc.com

USB3.0

FLAGA
FLAGB
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31
USB_GPIO0 USB_GPIO1
PCLK SLCS SLWR SLOE SLRD PKTEND CLKIN_FPGA INT USB_A0 USB_A1

USB_1.2V: C242 Cap 0.1uF/10V; C243 Cap 0.1uF/10V; C244 Cap 0.1uF/10V; C245 Cap 0.1uF/10V; C246 Cap 0.1uF/10V; C247 Cap 0.01uF
FPGA_3.3V: C248 Cap 0.01uF; C249 Cap 0.1uF/10V; C250 Cap 0.01uF

FPGA_3.3V: R125 Resl 10K; R126 Resl 10K; R127 Resl 10K
S1 SW DIP-3: PMODE0_DIP, PMODE1_DIP, PMODE2_DIP
MODE0 JUMPER → PMODE0; MODE1 JUMPER → PMODE1; MODE2 JUMPER → PMODE2

FPGA_3.3V → R132 DNP → RESET

S3 SW_PB: FPGA_3.3V → R135 Resl 100K; R136 Resl 10K; C257 Cap 100nF

USB_SCK_FPGA → R148 Resl 0R → SPI_SCK
USB_SSN_FPGA → R149 Resl 0R → SPI_SSN
USB_MISO_FPGA → R150 Resl 0R → SPI_MISO
USB_MOSI_FPGA → R151 Resl 0R → SPI_MOSI

FPGA_3.3V JP3 JUMPER; +5V
内核和模拟电压工作电流最大200mA
USB供电电压工作电流最大60mA

U6 CYUSB3014

DQ0	F10	GPIO[0]	
DQ1	F9	GPIO[1]	
DQ2	F7	GPIO[2]	
DQ3	G10	GPIO[3]	
DQ4	G9	GPIO[4]	
DQ5	F8	GPIO[5]	
DQ6	H10	GPIO[6]	
DQ7	H9	GPIO[7]	
DQ8	J10	GPIO[8]	
DQ9	J9	GPIO[9]	
DQ10	K11	GPIO[10]	
DQ11	L10	GPIO[11]	
DQ12	K10	GPIO[12]	
DQ13	K9	GPIO[13]	
DQ14	J8	GPIO[14]	
DQ15	G8	GPIO[15]	
PCLK	J6	GPIO[16]	
SLCS	K8	GPIO[17]	
SLWR	K7	GPIO[18]	
SLOE	J7	GPIO[19]	
SLRD	H7	GPIO[20]	
FLAGA	G7	GPIO[21]	
FLAGB	G6	GPIO[22]	
USB_GPIO0	K6	GPIO[23]	
PKTEND	H8	GPIO[24]	
USB_GPIO1	G5	GPIO[25]	
	H6	GPIO[26]	
	K5	GPIO[27]	
USB_A1	J5	GPIO[28]	
USB_A0	H5	GPIO[29]	
PMODE0	G4	GPIO[30]	
PMODE1	H4	GPIO[31]	
PMODE2	L4	GPIO[32]	
INT	L8	INT#	
RESET	C5	RESET#	
DQ16	K2	GPIO[33]	
DQ17	J4	GPIO[34]	
DQ18	K1	GPIO[35]	
DQ19	J2	GPIO[36]	
DQ20	J3	GPIO[37]	
DQ21	J1	GPIO[38]	
DQ22	H2	GPIO[39]	
DQ23	H3	GPIO[40]	
DQ24	F4	GPIO[41]	
DQ25	G2	GPIO[42]	
DQ26	G3	GPIO[43]	
DQ27	F3	GPIO[44]	
	F2	GPIO[45]	
	F5	GPIO[46]	DQ28
	E1	GPIO[47]	DQ29
	E5	GPIO[48]	DQ30
	E4	GPIO[49]	DQ31
	D1	GPIO[50]	
	D2	GPIO[51]	
	D3	GPIO[52]	
	D4	GPIO[53]	SPI_SCK
	C1	GPIO[54]	SPI_SSN
	C2	GPIO[55]	SPI_MISO
	D5	GPIO[56]	SPI_MOSI
	C4	GPIO[57]	
	D9	I2C_GPIO[58]	
	D10	I2C_GPIO[59]	
	E7	TDI	
	C10	TDO	
	B11	TRST#	
	E8	TMS	
	F6	TCK	
	D11	O[60]	

VDD: L5 J11 L7 H11 F11 E9 C3 B10
AVDD B7; AVSS A7
VBATT E10; VBUS E11; U3VSSQ A1; VIO1 H11; VIO1 L9; VIO2 F1; VIO3 E3; VIO4 B1; VIO5 C11; CVDDQ B6; U3TXVDDQ B5; U3RXVDDQ A2
VSS: D8 E2 G1 G11 L1 L6 L11 B8 B9 K4 L3 K3 L2 A8

U5
1 VBUS
2 D N
3 D P
4 D
7 GND
GND_DRAIN
5 SSRX N
6 SSRX P
8 SSTX N
9 SSTX P
SSRX
SSRX
SSTX
SSTX
USB3

U7 M25P40
D
Q
C
HOLD
S
W
VCC 8
VSS 4
SPI_MOSI 5
SPI_MISO 2
SPI_SCK 6
SPI_SSN 1
R111 100K
R112 4.7K
R119 4.7K
R124 4.7K
C251 Cap 100nF

OTG_ID A3
SSRXM A4
SSRXP A6
SSTXM A5
SSTXP
DP A9
DM A10
NC A11
SSRX N
SSRX P
C252 0.1uF/10V SSTX N
C253 0.1uF/10V SSTX P
D P
D N

U8 19.2MHz
1 GND
3 GND
2 GND
4 GND
XTALIN C6
XTALOUT C7
FSLC[0] B2
FSLC[1] B4
FSLC[2] E6
CLKIN D7
CLKIN_32 D6
C254 Cap 12pF
C255 Cap 12pF
R131 Resl 0R
CLKIN_FPGA

R_usb2 C8
R_usb3 B3
6.04K/1% R138 Resl
200R/1% R142 Resl

Title			
Size A3	Number		Revision
Date: 2016/3/29		Sheet of	
File: E:\CMOS_IMAGE_SENSOR_PRJ\...\USB3.0.SchDoc		Drawn By:	