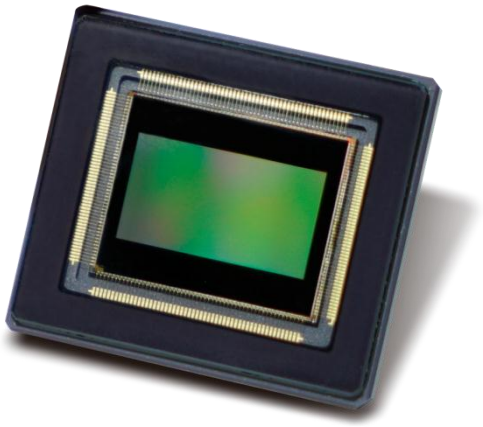
GSENSE2011s

6.5μm, 2MP Scientific CMOS Image Sensor



Datasheet V1.0

Release： Dec. 23th,2015

Features

- Resolution : 2048(H) x 1152(V)
- 6.5μm Square Pixels
- 1.0 inch Optical Format
- Frame Rate:
  - Max. 167 fps @ Rolling shutter
  - Max. 668 fps @ Global shutter (10-bit)
- Electronic Rolling and Global Shutter
- Readout noise:
  Rolling shutter: <2 e^-
  Global shutter: <6 e^-
- Sensitivity: 8.25x10^7 e^-/((W/m^2)·s)@ 625nm
- Dynamic Range : 88dB(Rolling HDR mode)
  70dB(Global HDR mode)
- Dark current: <6 e^-/s/pix @ 25°C@Rolling HDR
- On-chip 12-bit column-parallel ADC
- 32 LVDS output pairs
- On-chip temperature sensor
- On-chip SPI control
- On-chip PLL
- Power consumption :< 0.75 W @Rolling HDR,
  < 1.4W @ Global HDR

Applications

- Biometry and Medical
- Industrial and Machine Vision
- Security, Traffic and Surveillance
- Scientific Applications

Description

GSENSE2011s is a 2Mega pixel resolution scientific CMOS image sensor, capable of operating with either global or rolling shutter. Featured with six transistor (6T) pixel design on a 6.5μm pitch, the sensor has a very low readout noise of 1.9e^- in rolling shutter mode, and 5.7e^- in global shutter mode with external CDS. GSENSE2011s's max. frame rate is 167fps in rolling mode, and 668fps in 10bit global mode. These features make GSENSE2011s an ideal image sensor for various applications.

Specifications

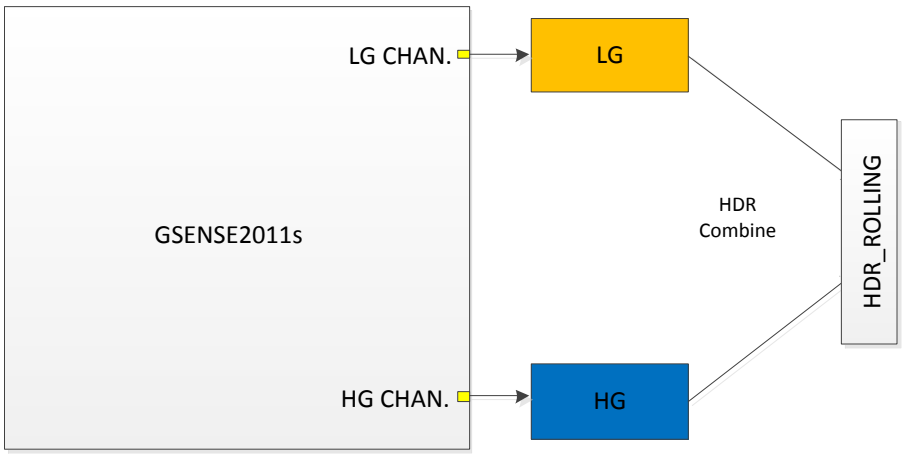
The table below lists the key specifications of GSENSE2011s. All the parameters are specified at 25°C chip temperature unless otherwise noted.

Parameter	Value
Photosensitive area	13.3mm x 7.5mm
Pixel size	6.5μm x 6.5μm
Number of active pixels	2048 (H) x 1152 (V)
Shutter type	Rolling shutter & Global shutter
Input clock rate	50MHz
Max Frame rate	83fps@ Rolling HDR 167fps@12-bit Rolling 167fps@ Global HDR 668fps@10-bit Global
Data rate	4.8Gbps @Rolling HDR; 19.2Gbps @Global HDR
Full well capacity(FWC)	48ke^- (Rolling HDR) 17ke^- (Global HDR)
Temporal noise	Rolling HDR: <2e^- Global HDR : < 6 e^-
Dynamic range	>88dB @Rolling HDR >70dB @Global HDR
Peak QE (with μLens)	62% @ 625nm
Supply voltage	3.3V for analog 1.8V for digital
Output format	32 pairs of LVDS driver
Power consumption	< 0.75W@ Rolling HDR < 1.4W @ Global HDR
Chroma	Mono and RGB
Package	153 pins μPGA

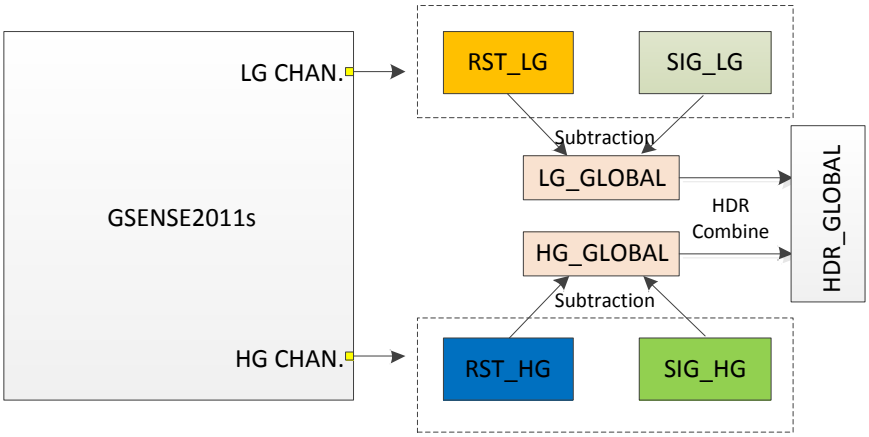
Sensor Operation Overview

GSENSE2011s sensor supports both rolling shutter HDR and global shutter HDR mode. Users need to combine both high gain (HG) and low gain (LG) images from the sensor to generate one HDR image off-chip. An intra-scene dynamic range of 88dB and 70dB can be achieved in rolling shutter and global shutter HDR respectively. The maximum frame rate is 83fps for rolling shutter HDR and 167fps in global shutter HDR mode. This document describes the sensor settings only in the two HDR modes. For applications that requires higher frame rate at the cost of lower dynamic range or higher noise, the sensor can be configured with double sampling on-chip to reach its max. speed, i.e. 668 fps in the 10-bit global shutter mode, or 167fps in the 12-bit rolling shutter mode. Please contact Gpixel Inc. for application notes that supports these operation modes.

In rolling shutter HDR mode, internal CDS are used to reduce the pixel KTC noise and offset. The LG image is optimized to reach max. full well capacity and the HG image is optimized for the low readout noise. In this mode, both HG and LG images are acquired with the same single exposure. The image signals are digitized with on-chip 12-bit ADC. After digitization, the two images are readout with in total 8 LVDS channels (4 out of the 16 LVDS channels from the top side and 4 out of the 16 LVDS from the bottom side of the sensor) at a maximum speed of 600Mbps per channel. Figure below shows the image sequence coming out from the sensor. Frame image signals of HG and LG images are readout simultaneously from both top and bottom side of the sensor line by line, users can use the pixel data from HG image and LG image to generate one HDR_ROLLING image.



In global shutter HDR mode, external CDS should be used to reduce the pixel KTC noise and offset. Therefore, instead of two images as in the rolling shutter mode, four images (RST_HG, RST_LG, SIG_HG, SIG_LG) are required to generate one HDR image. Image RST_HG is subtracted from the SIG_HG image to get a HG_GLOBAL image. RST_LG is subtracted from the SIG_LG image to generate a LG_GLOBAL image. Then the HG_GLOBAL and LG_GLOBAL images are used to generate one HDR image. In this mode, the images are digitized on-chip in 10 bits and then reading out from all the 32 LVDS channels (16 from top side of the sensor, and 16 from bottom side) at a maximum speed of 600Mbps. Figure below shows the image sequence coming out from the sensor in this mode. First RST_HG and RST_LG images are send out line by line, after the exposure, the SIG_HG and SIG_LG images are read out. Users need to combine these four images to generate the HDR image.


LG CHAN.
GSENSE2011s
HG CHAN.
RST_LG
SIG_LG
Subtraction
LG_GLOBAL
HDR
Combine
HG_GLOBAL
HDR_GLOBAL
Subtraction
RST_HG
SIG_HG

Revision History

Version	Date(dd/mm/yyyy)	Description
V1.0	23/12/2015	First release

CONTENTS

Package Outline

Units： mm

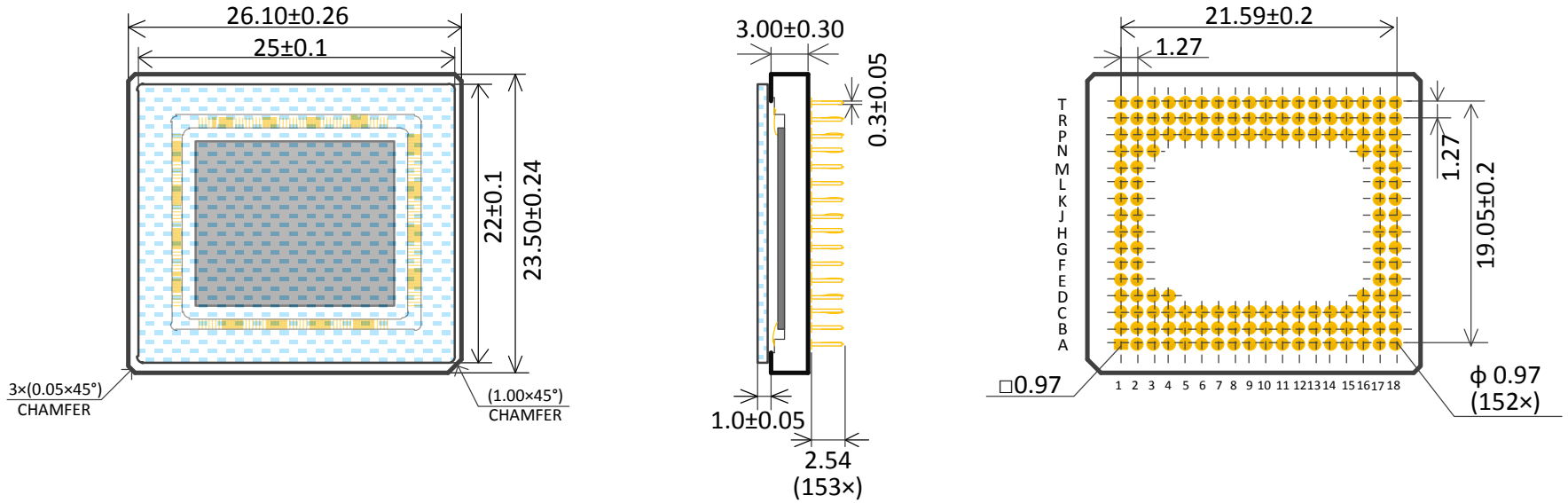


Figure 1: Package outline

Optical Center

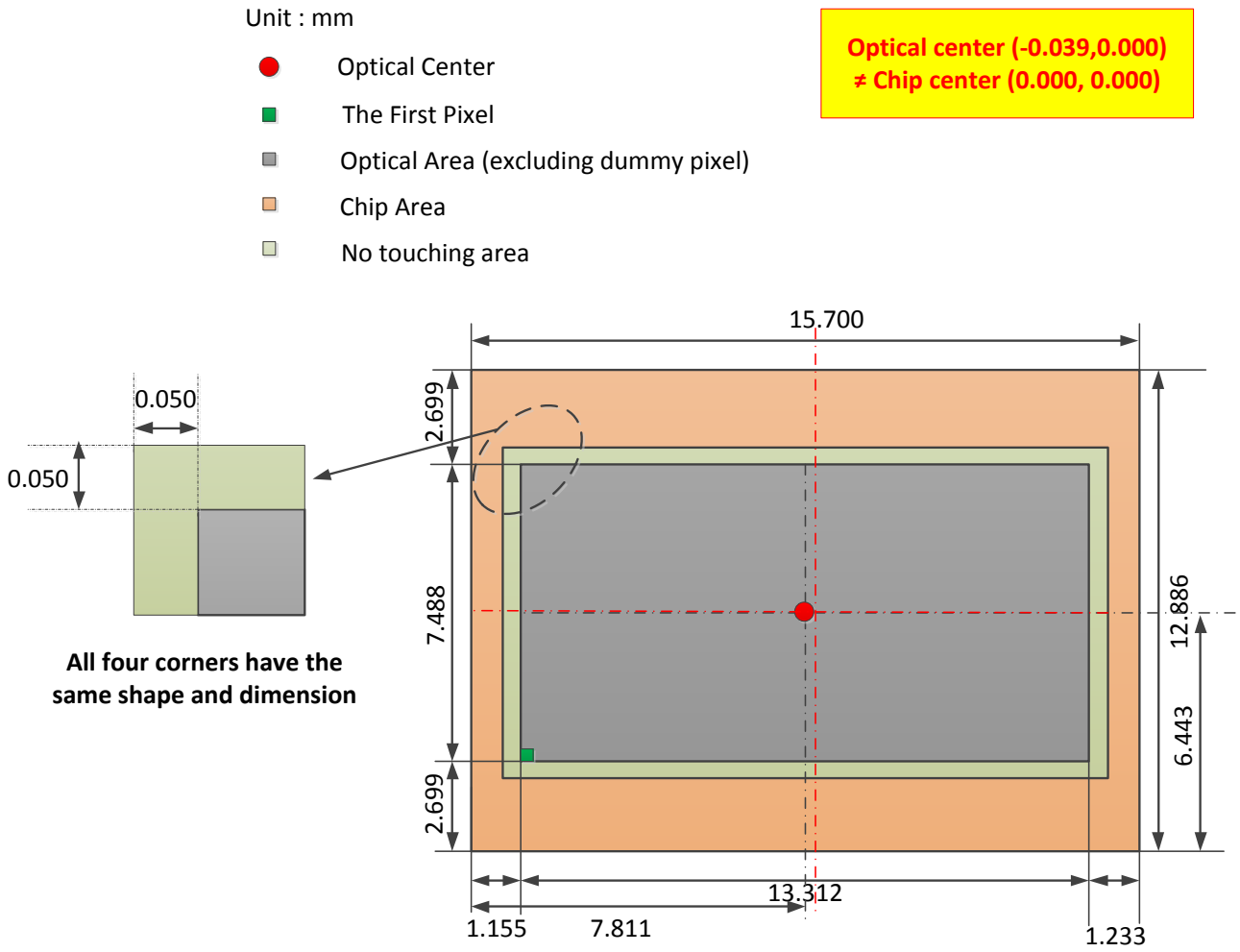


Figure 2: Optical center

Pixel Arrangement

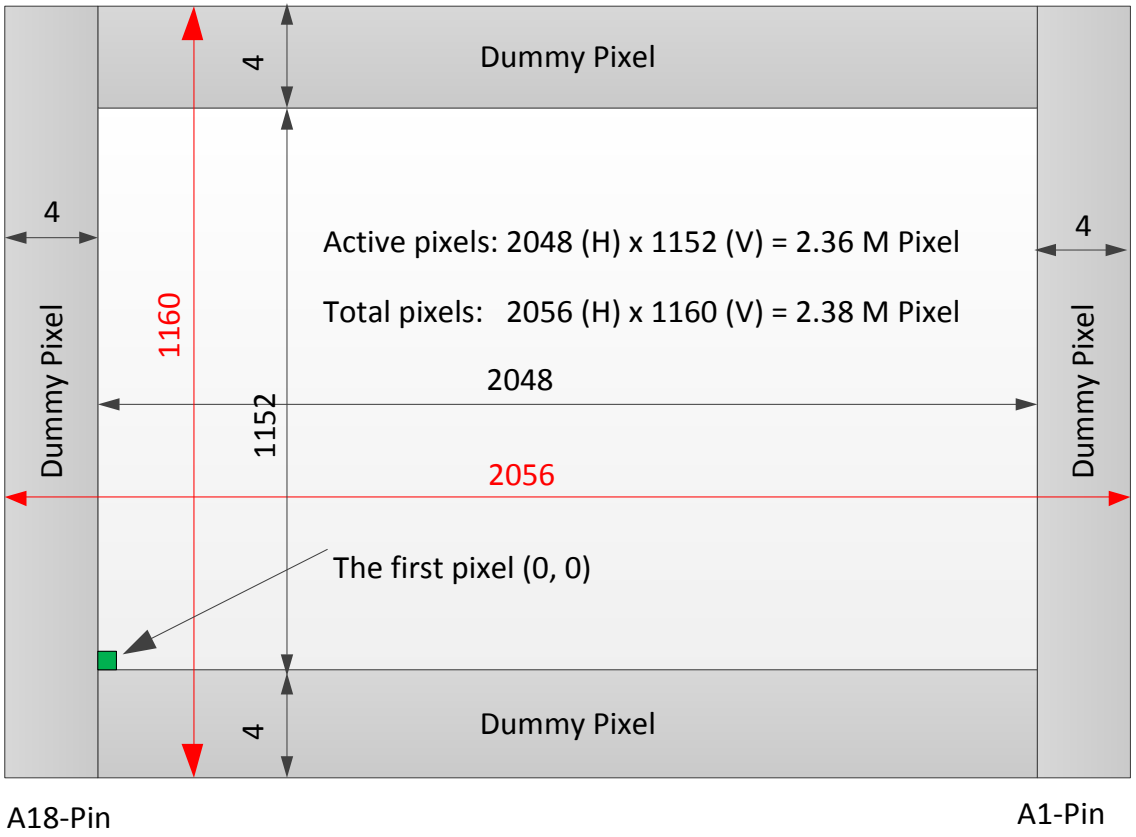


Figure 3: Pixel array

Bayer pattern on pixel array

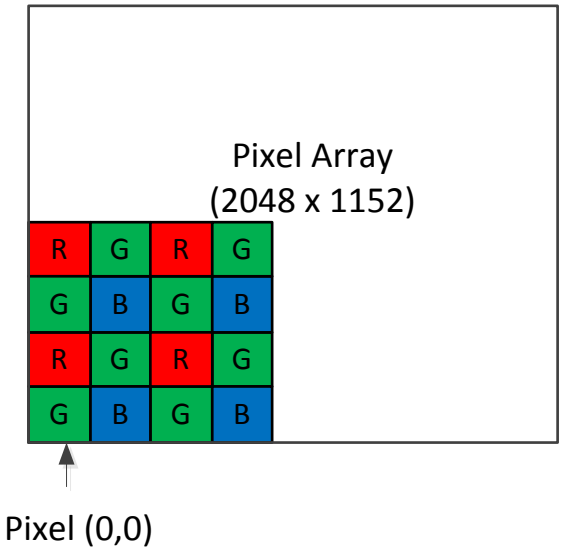


Figure 4: Bayer patter on top of pixel array

Internal Block Diagram and Pin Configuration

Internal Block Diagram

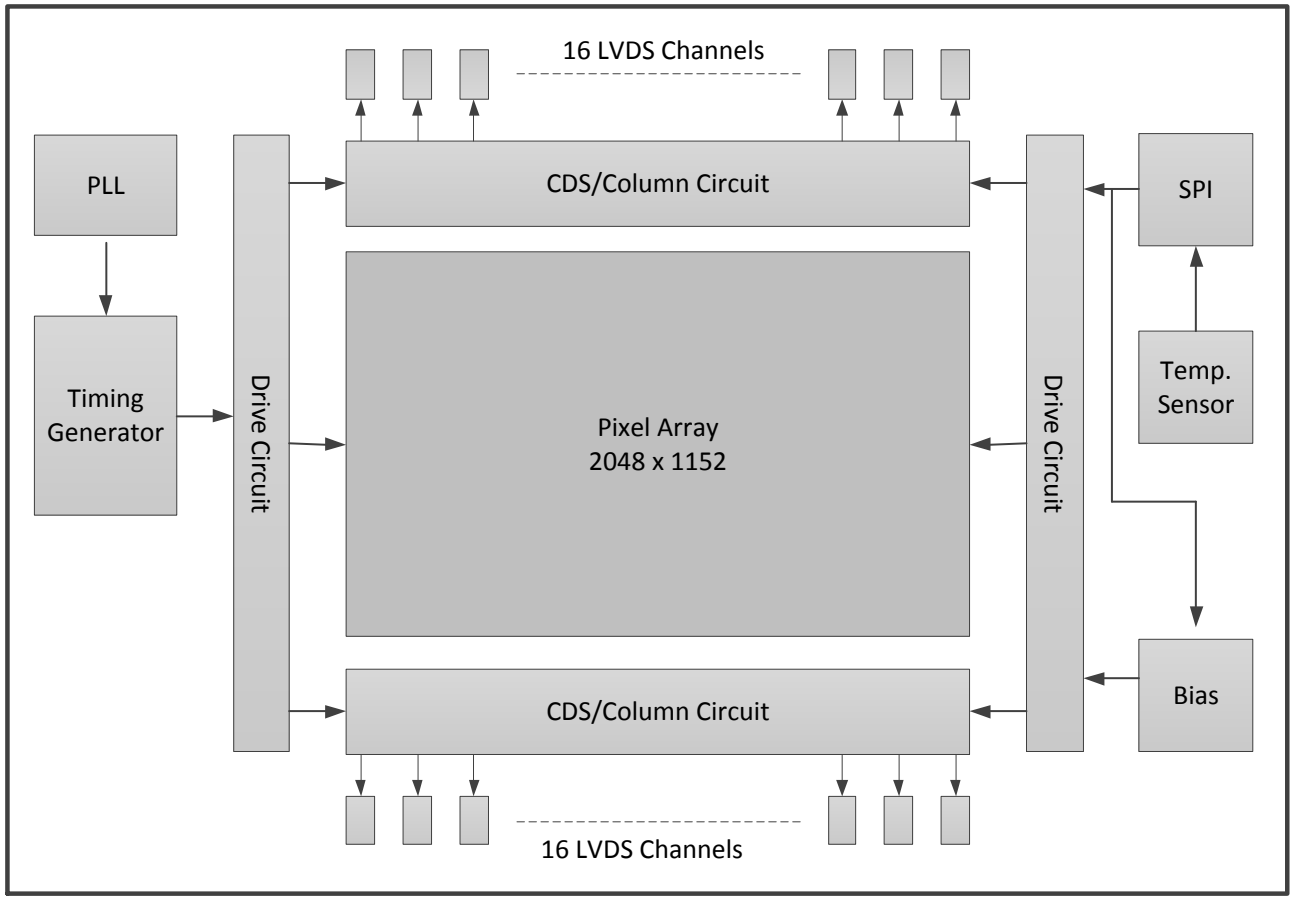


Figure 5: Block diagram

Pin Configuration

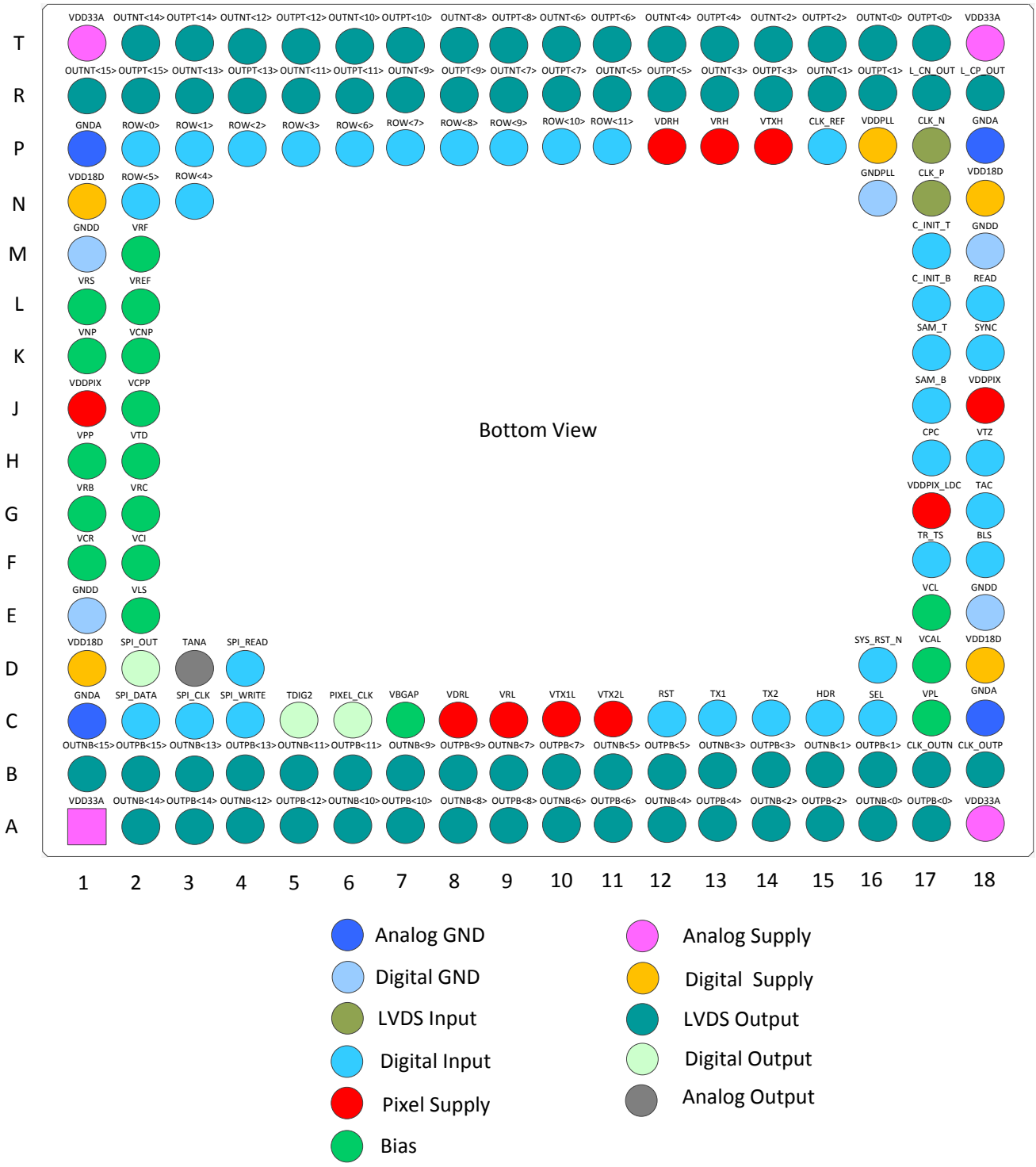


Figure 6: Pin configuration

Pin Description

No.	Pin No.	I/O	Symbol	Description	Type
1	A1	Power	VDD33A	3.3V analog supply	Supply
2	A2	O	OUTNB<14>	Bottom LVDS data negative channel 14	LVDS output
3	A3	O	OUTPB<14>	Bottom LVDS data positive channel 14	LVDS output
4	A4	O	OUTNB<12>	Bottom LVDS data negative channel 12	LVDS output
5	A5	O	OUTPB<12>	Bottom LVDS data positive channel 12	LVDS output
6	A6	O	OUTNB<10>	Bottom LVDS data negative channel 10	LVDS output
7	A7	O	OUTPB <10>	Bottom LVDS data positive channel 10	LVDS output
8	A8	O	OUTNB <8>	Bottom LVDS data negative channel 8	LVDS output
9	A9	O	OUTPB <8>	Bottom LVDS data positive channel 8	LVDS output
10	A10	O	OUTNB<6>	Bottom LVDS data negative channel 6	LVDS output
11	A11	O	OUTPB<6>	Bottom LVDS data positive channel 6	LVDS output
12	A12	O	OUTNB<4>	Bottom LVDS data negative channel 4	LVDS output
13	A13	O	OUTPB<4>	Bottom LVDS data positive channel 4	LVDS output
14	A14	O	OUTNB<2>	Bottom LVDS data negative channel 2	LVDS output
15	A15	O	OUTPB<2>	Bottom LVDS data positive channel 2	LVDS output
16	A16	O	OUTNB<0>	Bottom LVDS data negative channel 0	LVDS output
17	A17	O	OUTPB<0>	Bottom LVDS data positive channel 0	LVDS output
18	A18	Power	VDD33A	3.3V analog supply	Supply
19	B1	O	OUTNB<15>	Bottom LVDS data negative channel 15	LVDS output
20	B2	O	OUTPB<15>	Bottom LVDS data positive channel 15	LVDS output
21	B3	O	OUTNB<13>	Bottom LVDS data negative channel 13	LVDS output
22	B4	O	OUTPB<13>	Bottom LVDS data positive channel 13	LVDS output
23	B5	O	OUTNB<11>	Bottom LVDS data negative channel 11	LVDS output
24	B6	O	OUTPB <11>	Bottom LVDS data positive channel 11	LVDS output
25	B7	O	OUTNB <9>	Bottom LVDS data negative channel 9	LVDS output
26	B8	O	OUTPB <9>	Bottom LVDS data positive channel 9	LVDS output
27	B9	O	OUTNB<7>	Bottom LVDS data negative channel 7	LVDS output
28	B10	O	OUTPB<7>	Bottom LVDS data positive channel 7	LVDS output
29	B11	O	OUTNB<5>	Bottom LVDS data negative channel 5	LVDS output
30	B12	O	OUTPB<5>	Bottom LVDS data positive channel 5	LVDS output
31	B13	O	OUTNB<3>	Bottom LVDS data negative channel 3	LVDS output
32	B14	O	OUTPB<3>	Bottom LVDS data positive channel 3	LVDS output
33	B15	O	OUTNB<1>	Bottom LVDS data negative channel 1	LVDS output
34	B16	O	OUTPB<1>	Bottom LVDS data positive channel 1	LVDS output
35	B17	O	CLK_OUTN	LVDS clock negative output	LVDS output
36	B18	O	CLK_OUTP	LVDS clock positive output	LVDS output
37	C1	GND	GNDA	Analog ground	Ground

38	C2	I	SPI_DATA	Rigester data input pin	Digital input
39	C3	I	SPI_CLK	SPI clock in	Digital input
40	C4	I	SPI_WRITE	Digital control signal	Digital input
41	C5	O	TDIG2	Digital test pin	Digital output
42	C6	O	PIX_CLK*	Pixel clock out	Digital output
43	C7	I/O	VBGAP	Decouple with 100nF to GNDA	Bias
44	C8	Power	VDRL	Low voltage of pixel control signal (current sink)	Supply
45	C9	Power	VRL	Low voltage of pixel control signal (current sink)	Supply
46	C10	Power	VTX1L	Low voltage of pixel control signal (current sink)	Supply
47	C11	Power	VTX2L	Low voltage of pixel control signal (current sink)	Supply
48	C12	I	RST	Digital control signal	Digital input
49	C13	I	TX1	Digital control signal	Digital input
50	C14	I	TX2	Digital control signal	Digital input
51	C15	I	HDR	Digital control signal	Digital input
52	C16	I	SEL	Digital control signal	Digital input
53	C17	I/O	VPL	Decouple with 100nF to GNDA	Bias
54	C18	GND	GNDA	Analog ground	Ground
55	D1	Power	VDD18D	1.8V digital supply	Supply
56	D2	O	SPI_OUT	Read back internal register value	Digital output
57	D3	O	TANA	Analog test pin	Analog output
58	D4	I	SPI_READ	Digital control signal	Digital input
59	D16	I	SYS_RST_N	System reset signal	Digital input
60	D17	I/O	VCAL	Decouple with 100nF to GNDA	Bias
61	D18	Power	VDD18D	1.8V digital supply	Supply
62	E1	GND	GNDD	Digital ground	Ground
63	E2	I/O	VLS	Decouple with 100nF to GNDA	Bias
64	E17	I/O	VCL	Decouple with 100nF to GNDA	Bias
65	E18	GND	GNDD	Digital ground	Ground
66	F1	I/O	VCR	Decouple with 100nF to GNDA	Bias
67	F2	I/O	VCI	Decouple with 100nF to VDD33A	Bias
68	F17	I	TR_TS	Digital control signal	Digital input
69	F18	I	BLS	Digital control signal	Digital input
70	G1	I/O	VRB	Decouple with 1uF to VDD33A	Bias
71	G2	I/O	VRC	Decouple with 1uF to VDD33A	Bias
72	G17	Power	VDDPIX_LDC	Supply used to reduce dark cuttent	supply
73	G18	I	TAC	Digital control signal	Digital input
74	H1	I/O	VPP	Decouple with 100nF to VDD33A	Bias
75	H2	I/O	VTD	Decouple with 1uF to GNDA	Bias
76	H17	I	CPC	Digital control signal	Digital input
77	H18	I	VTZ	Digital control signal	Digital input
78	J1	Power	VDDPIX	Pixel array supply	Supply
79	J2	I/O	VCPP	Decouple with 100nF to VDD33A	Bias

80	J17	I	SAM_B	Digital control signal	Digital input
81	J18	Power	VDDPIX	Pixel array supply	Supply
82	K1	I/O	VNP	Decouple with 100nF to GNDA	Bias
83	K2	I/O	VCNP	Decouple with 100nF to GNDA	Bias
84	K17	I	SAM_T	Digital control signal	Digital input
85	K18	I	SYNC	Digital control signal	Digital input
86	L1	I/O	VRS	Decouple with 1uF to GNDA	Bias
87	L2	I/O	VREF	Decouple with 1uF to GNDA	Bias
88	L17	I	C_INIT_B	Digital control signal	Digital input
89	L18	I	READ	Digital control signal	Digital input
90	M1	GND	GNDD	Digital ground	Ground
91	M2	I/O	VRF	Decouple with 1uF to GNDA	Bias
92	M17	I	C_INIT_T	Digital control signal	Digital input
93	M18	GND	GNDD	Digital ground	Ground
94	N1	Power	VDD18D	1.8V digital supply	Supply
95	N2	I	ROW<5>	Digital control signal	Digital input
96	N3	I	ROW<4>	Digital control signal	Digital input
97	N16	GND	GNDPLL	PLL digital ground	Ground
98	N17	I	CLK_P	LVDS receiver input clock positive channel	LVDS input
99	N18	Power	VDD18D	1.8V digital supply	Supply
100	P1	GND	GNDA	Analog ground	Ground
101	P2	I	ROW<0>	Digital control signal	Digital input
102	P3	I	ROW<1>	Digital control signal	Digital input
103	P4	I	ROW<2>	Digital control signal	Digital input
104	P5	I	ROW<3>	Digital control signal	Digital input
105	P6	I	ROW<6>	Digital control signal	Digital input
106	P7	I	ROW<7>	Digital control signal	Digital input
107	P8	I	ROW<8>	Digital control signal	Digital input
108	P9	I	ROW<9>	Digital control signal	Digital input
109	P10	I	ROW<10>	Digital control signal	Digital input
110	P11	I	ROW<11>	Digital control signal	Digital input
111	P12	Power	VDRH	Supply of pixel control signal	Supply
112	P13	Power	VRH	Supply of pixel control signal	Supply
113	P14	Power	VTXH	Supply of pixel control signal	Supply
114	P15	I	CLK_REF	PLL input clock	Digital input
115	P16	Power	VDDPLL	PLL 1.8V supply	Supply
116	P17	I	CLK_N	LVDS receiver input clock negative channel	LVDS input
117	P18	GND	GNDA	Analog ground	Ground
118	R1	O	OUTNT<15>	Top LVDS data negative channel 15	LVDS output
119	R2	O	OUTPT<15>	Top LVDS data positive channel 15	LVDS output
120	R3	O	OUTNT<13>	Top LVDS data negative channel 13	LVDS output
121	R4	O	OUTPT<13>	Top LVDS data positive channel 13	LVDS output

122	R5	O	OUTNT<11>	Top LVDS data negative channel 11	LVDS output
123	R6	O	OUTPT<11>	Top LVDS data positive channel 11	LVDS output
124	R7	O	OUTNT<9>	Top LVDS data negative channel 9	LVDS output
125	R8	O	OUTPT<9>	Top LVDS data positive channel 9	LVDS output
126	R9	O	OUTNT<7>	Top LVDS data negative channel 7	LVDS output
127	R10	O	OUTPT<7>	Top LVDS data positive channel 7	LVDS output
128	R11	O	OUTNT<5>	Top LVDS data negative channel 5	LVDS output
129	R12	O	OUTPT<5>	Top LVDS data positive channel 5	LVDS output
130	R13	O	OUTNT<3>	Top LVDS data negative channel 3	LVDS output
131	R14	O	OUTPT<3>	Top LVDS data positive channel 3	LVDS output
132	R15	O	OUTNT<1>	Top LVDS data negative channel 1	LVDS output
133	R16	O	OUTPT<1>	Top LVDS data positive channel 1	LVDS output
134	R17	O	L_CN_OUT	LVDS control signal output negative channel	LVDS output
135	R18	O	L_CP_OUT	LVDS control signal output positive channel	LVDS output
136	T1	Power	VDD33A	3.3V analog supply	Supply
137	T2	O	OUTNT<14>	Top LVDS data negative channel 14	LVDS output
138	T3	O	OUTPT<14>	Top LVDS data positive channel 14	LVDS output
139	T4	O	OUTNT<12>	Top LVDS data negative channel 12	LVDS output
140	T5	O	OUTPT<12>	Top LVDS data positive channel 12	LVDS output
141	T6	O	OUTNT<10>	Top LVDS data negative channel 10	LVDS output
142	T7	O	OUTPT<10>	Top LVDS data positive channel 10	LVDS output
143	T8	O	OUTNT<8>	Top LVDS data negative channel 8	LVDS output
144	T9	O	OUTPT<8>	Top LVDS data positive channel 8	LVDS output
145	T10	O	OUTNT<6>	Top LVDS data negative channel 6	LVDS output
146	T11	O	OUTPT<6>	Top LVDS data positive channel 6	LVDS output
147	T12	O	OUTNT<4>	Top LVDS data negative channel 4	LVDS output
148	T13	O	OUTPT<4>	Top LVDS data positive channel 4	LVDS output
149	T14	O	OUTNT<2>	Top LVDS data negative channel 2	LVDS output
150	T15	O	OUTPT<2>	Top LVDS data positive channel 2	LVDS output
151	T16	O	OUTNT<0>	Top LVDS data negative channel 0	LVDS output
152	T17	O	OUTPT<0>	Top LVDS data positive channel 0	LVDS output
153	T18	Power	VDD33A	3.3V analog supply	Supply

**Recommend "PIX_CLK" to be the input reference clock of Field Programmable Gate Array (FPGA)*

Electrical Characteristics

DC Characteristics

Rolling HDR Mode

Item		Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog	VDD33A		3.0	3.3	3.6	V
	Digital	VDD18D		1.6	1.8	2	V
		VDDPLL		1.6	1.8	2	V
	Pixel	VDDPIX		2.4	2.6	3.6	V
		VDDPIX_LDC		0	0.8	1.0	V
		VDRH		2	3.0	3.6	V
		VDRL		0	0	1	V
		VRH		0	3.0	3.6	V
		VRL			-0.3	1	V
		VTXH*		**3.0**	**3.3**	**3.6**	**V**
		VTX1L		0	0	0	V
		VTX2L		0	0	0	V
Voltage reference	Analog	VTD		2	N/A	3.3	V
		VRF		0.8	1.15	1.5	V
		VREF		0.8	1	1.5	V
		VRS		0.8	1.15	1.5	V
Digital input voltage		CLK_REF ROW<10:0> ROW<11>_FOT RST SEL TX2 TX1 HDR SYNC	VIH	3.0	3.3	3.6	V
		BLS TR_TS VTZ READ C_INIT_B C_INIT_T TAC CPC	VIL	0	0	0.3	V

	SAM_B SAM_T SPI_DATA SPI_READ SPI_WRITE SPI_CLK SYS_RST_N					
	CLK_N CLK_P	VCM		1.25		V
		VOD	0.25	0.35	0.45	V
Digital output voltage	CLKN_OUT CLKP_OUT	VCM		1.25		V
	OUTNT<0:15> OUTPT<0:15> OUTNB<0:15> OUTPB<0:15>	VOD	0.25	0.35	0.45	V
	PIX_CLK	VOH	3.0	3.3	3.6	V
	SPI_OUT	VOL	0	0	0	

**Note: Supply voltage VTXH is added in sensor with this version of package. This supply may have influence on some functionality/performance. We are still waiting for new samples for the debug at this moment.*

Global HDR Mode

Item		Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Analog	VDD33A		3.0	3.3	3.6	V
	Digital	VDD18D		1.6	1.8	2	V
		VDDPLL		1.6	1.8	2	V
	Pixel	VDDPIX		2.4	2.6	3.6	V
		VDDPIX_LDC		0	0	0	V
		VDRH		2	3.0	3.6	V
		VDRL		0	0.5	1	V
		VRH		0	3.0	3.6	V
		VRL		0	0	1	V
		VTXH*		**3.0**	**3.3**	**3.6**	**V**
		VTX1L		0	0	0	V
		VTX2L		0	0	0	V
Voltage reference	Analog	VTD		2	2.2	3.3	V
		VRF		0.8	1.15	1.5	V
		VREF		0.8	1	1.5	V
		VRS		0.8	1.15	1.5	V
Digital input voltage		CLK_REF ROW<10:0> ROW<11>_FOT RST SEL TX2 TX1 HDR SYNC	VIH	3.0	3.3	3.6	V
		BLS TR_TS VTZ READ C_INIT_B C_INIT_T TAC CPC SAM_B SAM_T SPI_DATA SPI_READ SPI_WRITE	VIL	0	0	0.3	V

	SPI_CLK SYS_RST_N					
	CLK_N	VCM		1.25		V
	CLK_P	VOD	0.25	0.35	0.45	V
Digital output voltage	CLKN_OUT CLKP_OUT	VCM		1.25		V
	OUTNT<0:15> OUTPT<0:15> OUTNB<0:15> OUTPB<0:15>	VOD	0.25	0.35	0.45	V
	PIX_CLK	VOH	3.0	3.3	3.6	V
	SPI_OUT	VOL	0	0	0	

**Note: Supply voltage VTXH is added in sensor with this version of package. This supply may have influence on some functionality/performance. We are still waiting for new samples for the debug at this moment.*

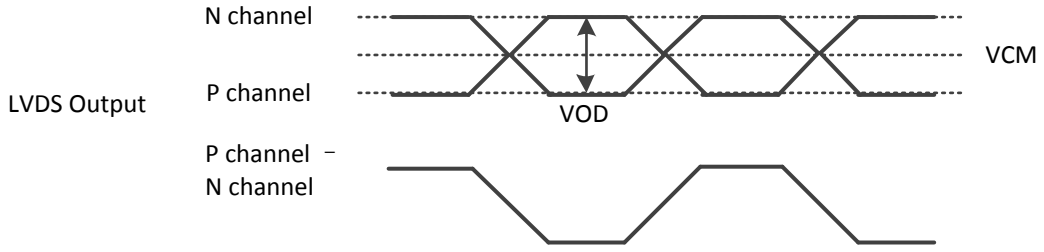


Figure 7: LVDS output

Analog Decouple

Pin number	Pin name	Description
E2	VLS	Decouple 100nF to GNDA
G2	VRC	Decouple with 1 uF to VDD33A
H1	VPP	Decouple with 100nF to VDD33A
E17	VCL	Decouple with 100nF to GNDA
C17	VPL	Decouple with 100nF to GNDA
C7	VBGAP	Decouple with 100nF to GNDA
F1	VCR	Decouple with 100nF to GNDA
H2	VTD	Decouple with 1uF to GNDA
J2	VCPP	Decouple with 100nF to VDD33A
F2	VCI	Decouple with 100nF to VDD33A
G1	VRB	Decouple with 1 uF to VDD33A
K2	VCNP	Decouple with 100nF to GNDA
K1	VNP	Decouple with 100nF to GNDA
M2	VRF	Decouple with 1 uF to GNDA
L2	VREF	Decouple with 1 uF to GNDA
L1	VRS	Decouple with 1 uF to GNDA

Power Consumption

In rolling HDR mode:

Supply source	Typical voltage(V)	Stand-by* current (mA)	Stand-by* (mW)	Max. current (mA)	Max. Power (mW)
VDDPIX	2.6	9	23.4	9	23.4
VDD18D	1.8	148	266.4	182	327.6
VDD33A	3.3	112	369.6	112	369.6
VDDPLL	1.8	4	7.2	4	7.2
Total power consumption (mW)	N/A	N/A	666.6	N/A	727.8

In global HDR mode:

Supply source	Typical voltage(V)	Stand-by* current (mA)	Stand-by* (mW)	Max. current (mA)	Max. Power (mW)
VDDPIX	2.6	6.73	17.50	13.37	34.76
VDD18D	1.8	286.38	515.48	370.67	667.21
VDD33A	3.3	191.53	632.05	194.86	643.04
VDDPLL	1.8	3.93	7.07	3.99	7.18
Total power consumption (mW)	N/A	N/A	1172.11	N/A	1352.19

"Stand-by" means the sensor has been ready to receive digital control signals. The power consumption is measured with the typical supply voltage.

AC Characteristics

1. Digital input reference clock (CLK_REF) waveform diagram

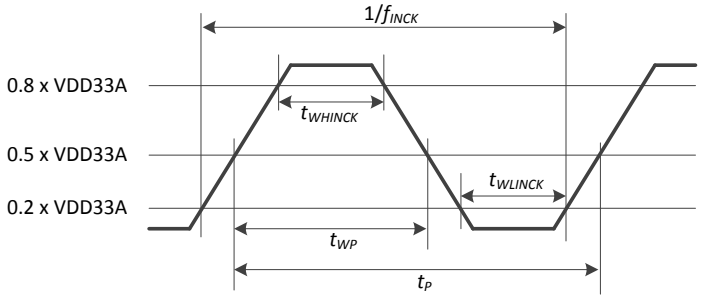


Figure 8: AC input reference clock

Duty Ratio = t_{WP} / t_P × 100

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
CLK_REF frequency	f_{INCK}	40	50	60	MHz	
CLK_REF Low level pulse width	t_{WLINCK}	8			ns	
CLK_REF High level pulse width	t_{WHINCK}	8			ns	
CLK_REF duty ratio		45	50	55	%	Define with 0.5 x VDD33A

2. Digital input control signal waveform diagram

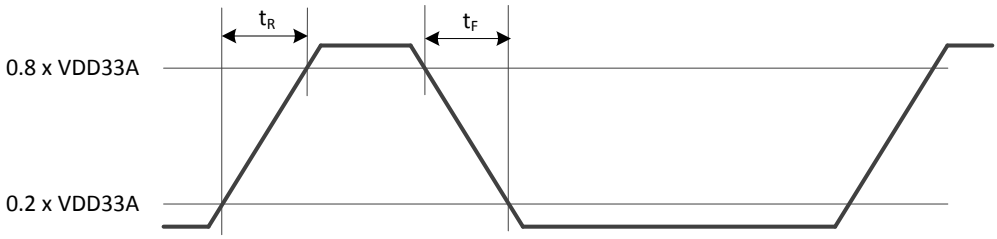


Figure 9: AC digital input control signal

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Control signal rising edge	t_R	—	2	4	ns	Define with 0.2 x VDD33A and 0.8 x VDD33A
Control signal falling edge	t_F	—	2	4	ns	Define with 0.2 x VDD33A and 0.8 x VDD33A

LVDS Driver Output

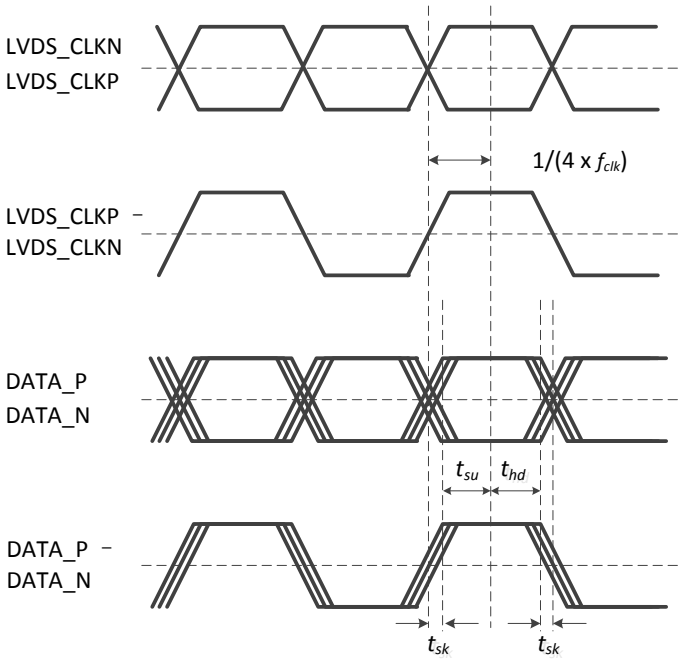


Figure 10: LVDS driver output

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
LVDS clock frequency	f_{clk}		300		MHz	Data rate 600MHz, DDR clock
LVDS clock duty		40	50	60	%	Data rate 600MHz
Data skew time	t_{sk}			400	ps	Data rate 600MHz
Data setup time	t_{su}	400			ps	Data rate 600MHz
Data hold time	t_{hd}	400			ps	Data rate 600MHz

Image Sensor Characteristics

Rolling HDR Mode

Key Specification

Measurement Item	1.7x PGA gain setting Low gain image			10.8x PGA gain setting High gain image			Unit	Note
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Conversion factor		0.08			2.15		DN/e^-	
FWC	40	48		1.6	1.8		ke^-	1
Linear FWC	40	47		1.6	1.7		ke^-	
Linear Error		0.5	0.8		0.7	0.8	%	
Max. SNR		46			32		dB	
Temporal noise		28	31		1.9	2	e^-	
Intra-scene Dynamic Range	62	63.7		58	60		dB	2
MAX. Dynamic Range	88						dB	
Sensitivity @625nm	$8.25x10^7$						$e^-/((W/m^2)\cdot s)$	
Peak QE @625nm	62						%	3
Dark Current	6						$e^-/s/pix$	4
DCNU	11						$e^-/s/pix$	4
Image Lag			2			1.6	e^-	
FPN		10	13		1.2	1.5	e^-	
PRNU		0.75	1		1.2	1.5	%	5

Notes

1. The FWC is calculated by dividing the saturation signal (DN) by the conversion factor (DN/e^-).
2. The intra-scene dynamic range is the ratio of FWC (e^-) to temporal noise (e^-) measured at the same system gain setting, the unit of dB is 20 x log(DR).
3. The measurement result equals to QE X FF (fill factor).
4. The dark current and DCNU are measured at room temperature of 25^{o}C.
5. The PRNU results are measured with full resolution.

Photon Response Curve

The curve below shows the photon response curve for the sensor. (1.7x PGA gain for low gain image and 10.8x PGA gain for high gain image)

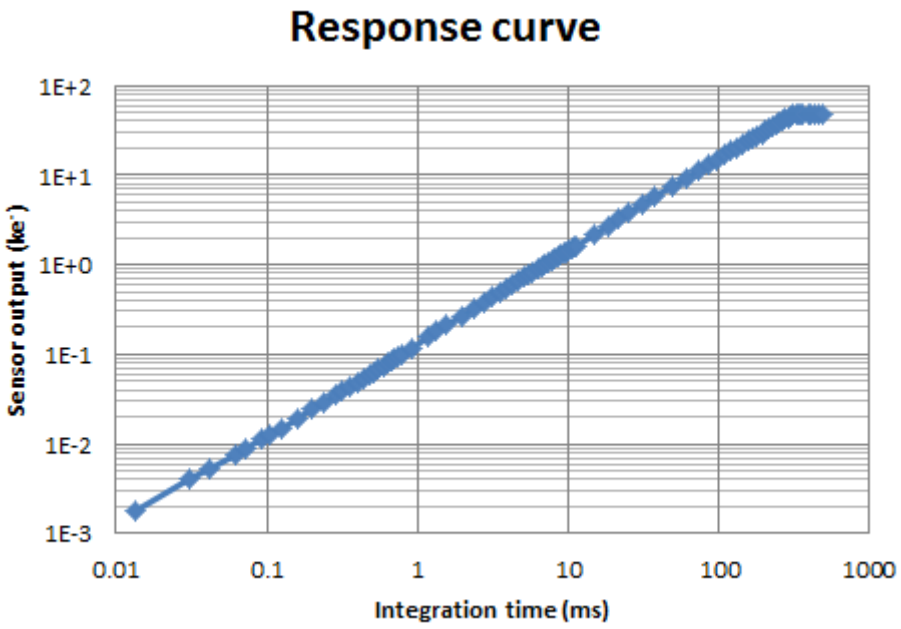


Figure 11: Photon response curve in rolling HDR mode

Temporal Noise Distribution

The curve below shows the temporal noise distribution (10.8x PGA gain for high gain image). As shown, the sensor temporal noise is around 1.9e$^-$.

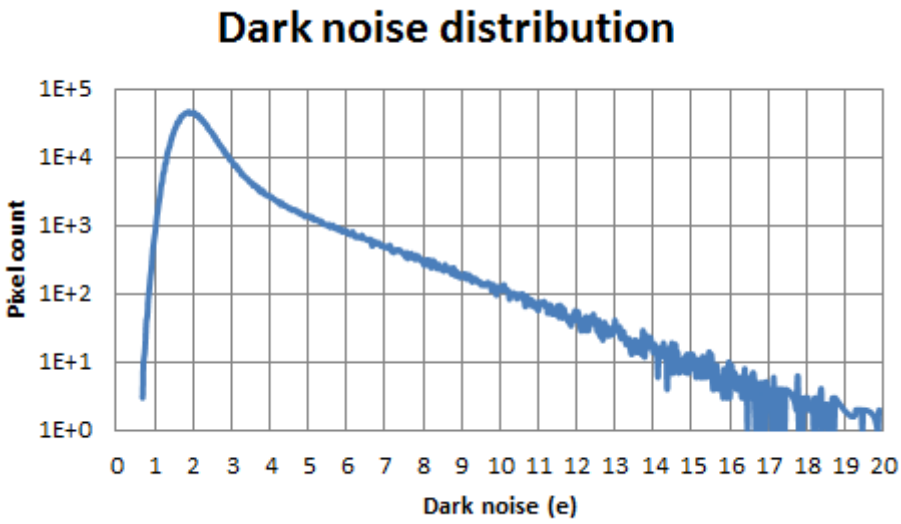


Figure 12: Temporal noise distribution in rolling HDR mode

Spectral Sensitivity Characteristics

The curve below displays the spectral response for visible spectrum (350-950nm). The measurement in graph below is done with the monochromatic sensor. As shown, the sensor peak QE is around 62%. The QE measurement result of the global HDR mode is same as that of the rolling HDR mode.

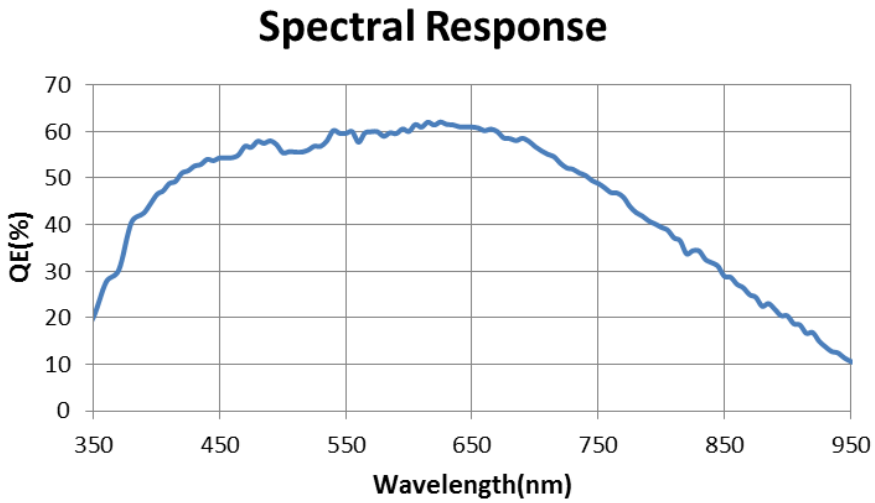


Figure 13: Spectral response for mono version in rolling HDR mode

The table below shows more details about the QE measurement results.

Wavelength(nm)	QE x FF (%)
350	20.19
400	46.42
500	55.44
600	60.00
625	62.05
700	56.77
800	39.44
900	20.43
950	10.67

The figure below shows the sensor color sensitivity with Bayer CFA pattern. Note there is no IR-cut filter on the glass lid of the sensor, so the user need a separate IR-cut filter for white balance.

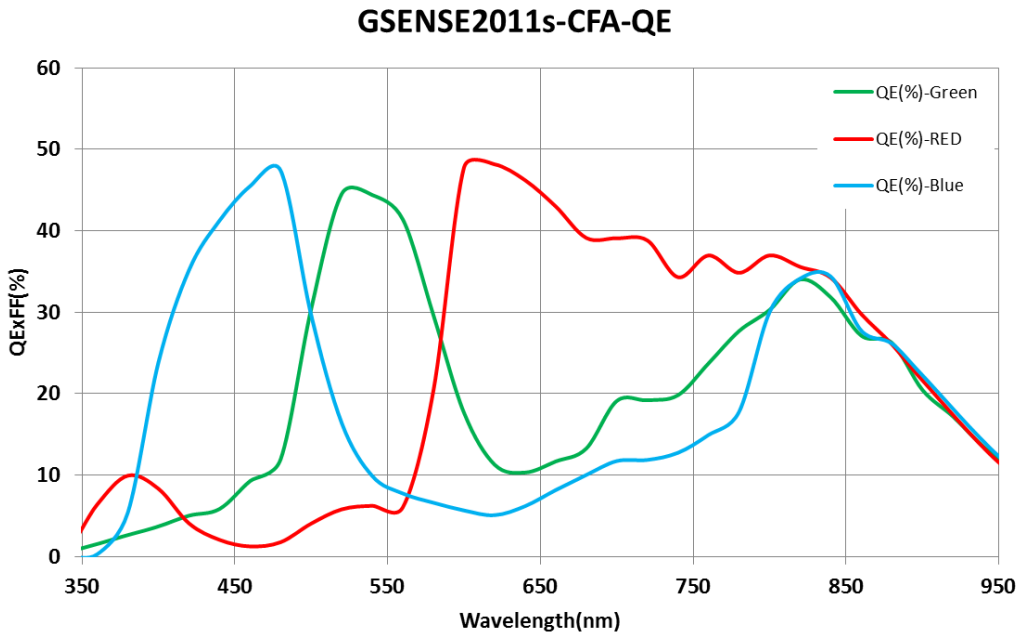


Figure 14: Spectral response curve for RGB version

Dark Signal Distribution

The curve below displays the dark signal distribution over the complete array (10.8x PGA gain for high gain image). The sensor FPN (DSNU) is around 1.2e$^-$.

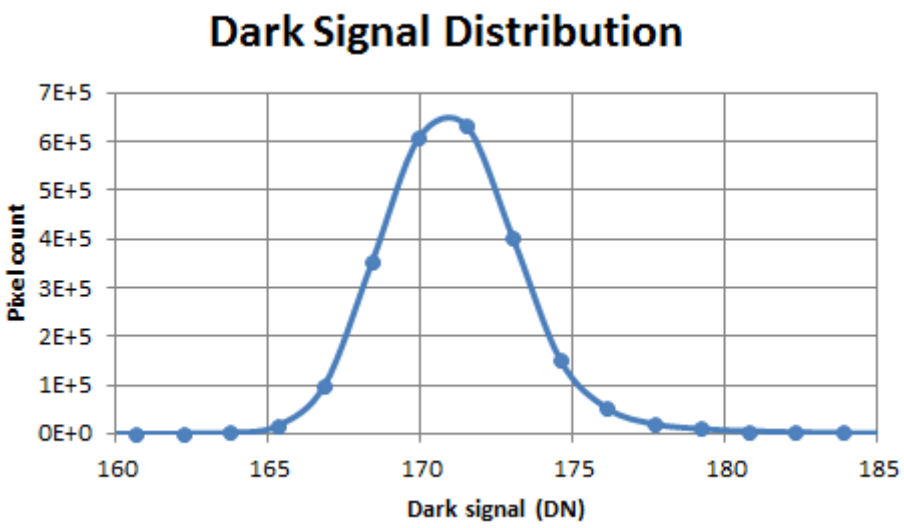


Figure 15: Dark signal distribution in rolling HDR mode

Photon Response Distribution

The graph below shows the photon response histogram at 50% of the sensor saturation level. The PRNU value of the sensor is about 0.75% (1.7x PGA gain for low gain image).

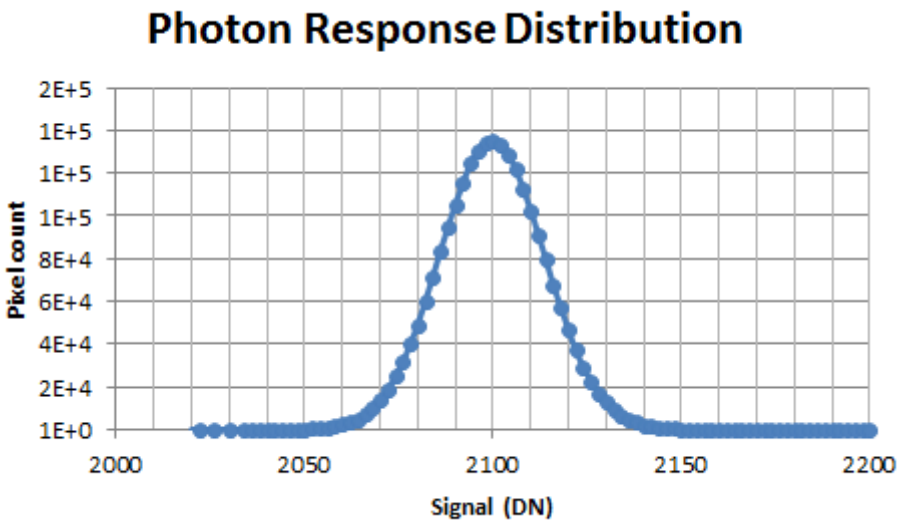


Figure 16: Photon response distribution in rolling HDR mode

Black Level Image

The figure below shows the black level high gain image with 10.8x PGA gain value, 5μs exposure time and complete dark condition. The image is obtained by subtracting the offset image and adding 50 DN for each pixel point in order to remove the negative level. The offset image is obtained by averaging 20 frames which are taken with the shortest exposure in complete dark condition. Therefore, all offset FPN had been removed from the image. The contrast of this image is defined that 25 DN is the absolutely black and 80 DN is the absolutely white. The sensor conversion factor in this mode is 2.15DN/e^- in this setting.

The noise of the complete image below is around 2.65e^- which is calculated by the standard deviation (stdev) of each pixel output, it consists of:

- Pixel-level temporal noise 1.9e^-(as in EMVA1288 definition)
- Row noise 0.13e^-
- Column noise 0.14e^-

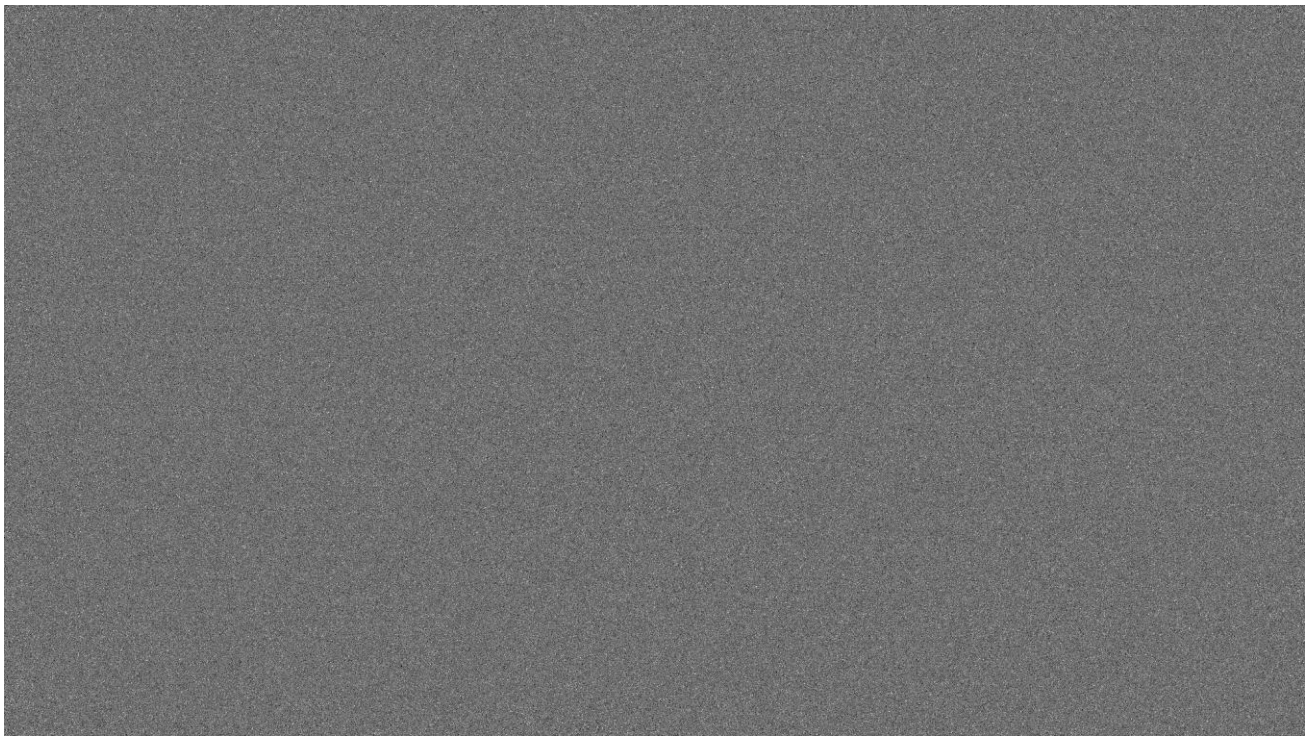


Figure 17: Dark image in rolling HDR mode

Dark current distribution at low temperature

The graph below shows the dark current distribution of the sensor at environment temperature of -40 °C. The DC value with most pixel counts is 0.05e^-/s/pixel (10.8x PGA gain for high gain image).

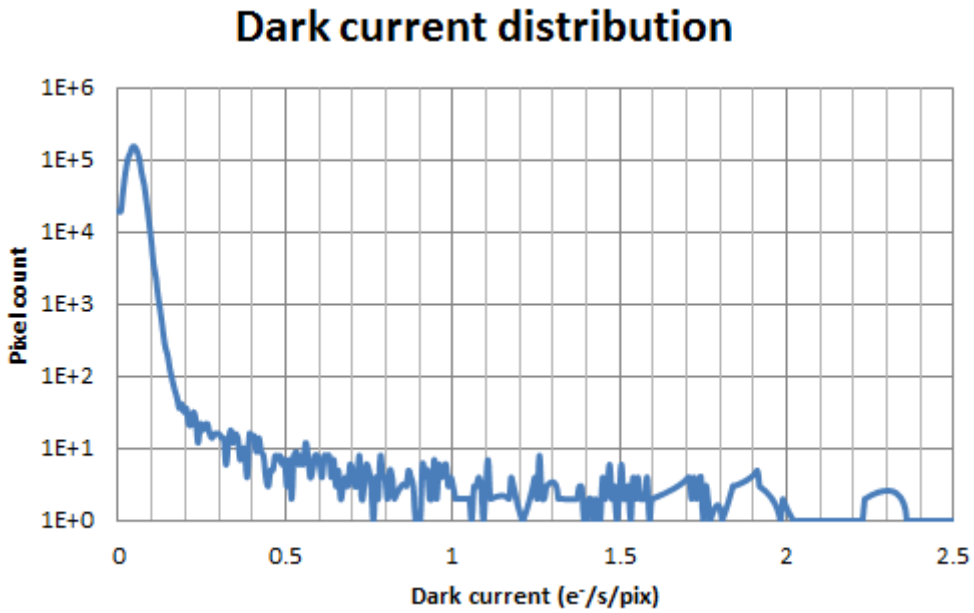


Figure 18: Dark current distribution at -40 °C

Note:

1. Around 1.05M pixels (in mid of the array) are chosen to calculate this distribution. This is because pixels at top and bottom side of the array have higher temperature with heat generated by the readout circuits.
2. The measurement results have been processed with all the negative value clipped to zero.

Global HDR Mode

Key Specification

Measurement Item	1.08x PGA gain setting Low gain image			7.0x PGA gain setting High gain image			Unit	Note
	Min.	Typ.	Max.	Min.	Typ.	Max.		
Conversion factor		0.04			0.3		DN/e^-	
FWC	17	17		2.3	2.5		ke^-	1
Linear FWC	15	16		1.4	1.5		ke^-	
Linear Error		0.75	0.90		0.40	0.76	%	
Max. SNR	41	42.3		31	31.8		dB	
Temporal noise		22.9	24		5.7	6.2	e^-	
Intra-scene Dynamic Range	57	58		51	52		dB	2
Max. Dynamic Range	69.2						dB	
Sensitivity @625nm	$8.25X10^7$						$e^-/((W/m^2)\cdot s)$	
Peak QE @625nm	62						%	3
Dark Current	TBD						$e^-/s/pix$	
DCNU	TBD						$e^-/s/pix$	
Image Lag			2			1	e^-	
FPN		6.27	6.5		3.15	3.4	e^-	
PRNU		1.31	1.4		1.10	1.2	%	4

Notes

1. The FWC is calculated by dividing the saturation signal level (DN) by the conversion factor (DN/e^-).
2. The intra-scene dynamic range is the ratio of FWC (e^-) to temporal noise (e^-) measured at the same system gain setting, the unit of dB is 20 x log(DR).
3. The measurement result equals to QE x FF (fill factor).
4. The PRNU results are measured with full resolution.

Photon Response Curve

The curve below shows the photon response curve for the sensor (1.1x PGA gain for low gain image and 7.0x PGA gain for high gain image).

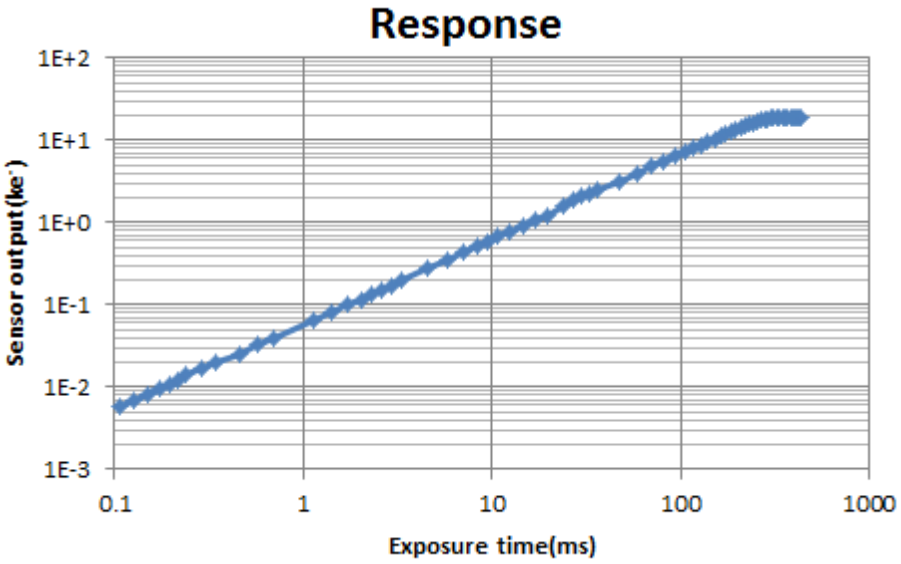


Figure 19: Photon response curve in global HDR mode

Temporal Noise Distribution

The curve below shows the temporal noise distribution (7.0x PGA gain for high gain image). As shown, the sensor temporal noise is around 5.7e$^-$.

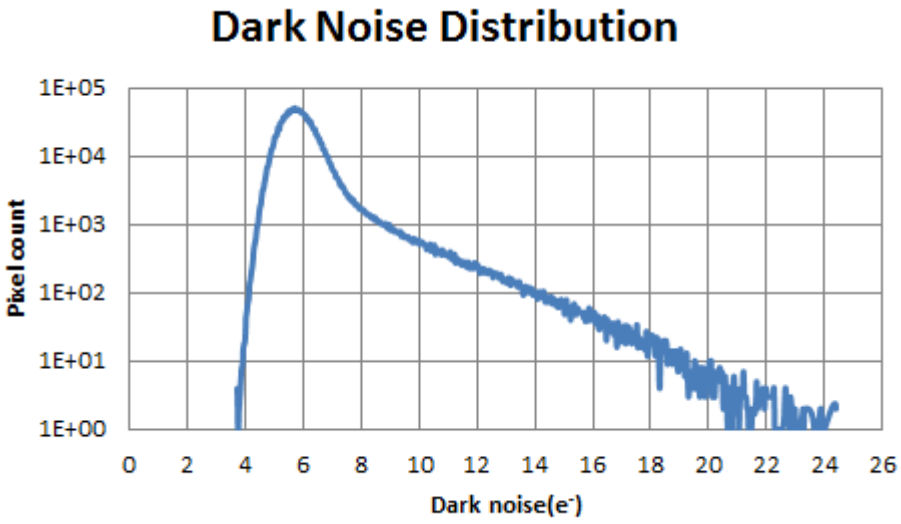


Figure 20: Temporal noise distribution in global HDR mode

Dark Signal Distribution

The curve below displays the dark signal distribution over the complete array (7.0x PGA gain for high gain image). The sensor FPN (DSNU) is around 3.1e$^-$.

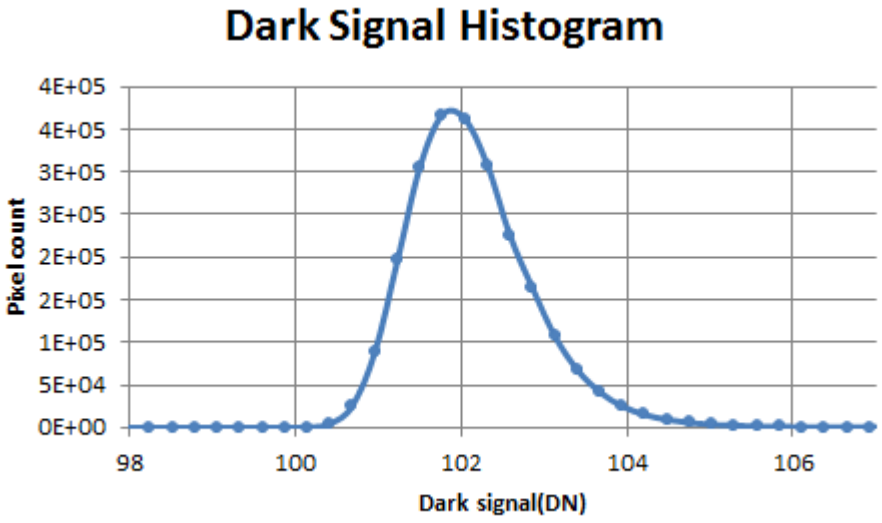


Figure 21: Dark signal histogram in global HDR mode

Photon Response Distribution

The graph below shows the photon response histogram at 50% of the sensor saturation level. The PRNU value of the sensor is around 1.1% (7.0x PGA gain for high gain image).

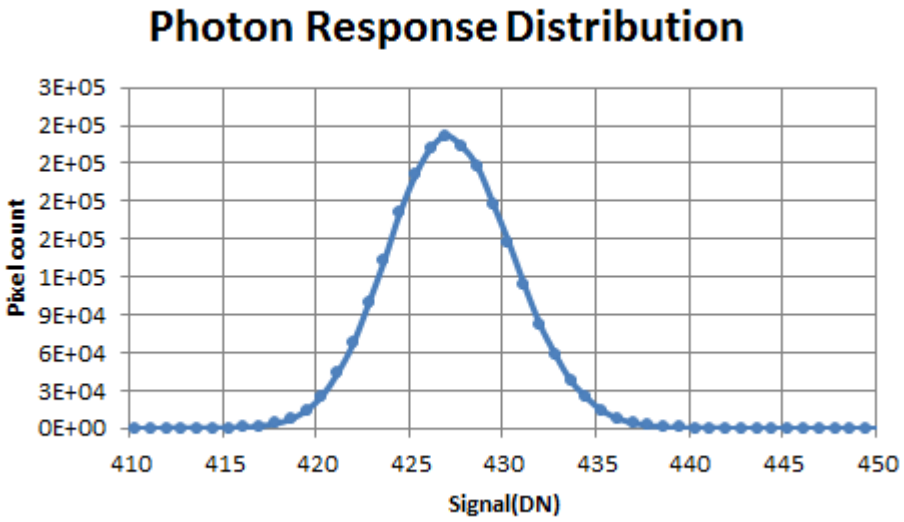


Figure 22: Photon response distribution in global HDR mode

Black Level Image

The figure below shows the black level high gain image with 7.0x PGA gain value, 19μs exposure time and complete dark condition. The contrast of this image is defined that 95 DN is the absolutely black and 105 DN is the absolutely white. The sensor conversion factor in this mode is 0.3DN/e^-.

The noise of this image below is around 6.3e^- which is calculated by the standard deviation (stdev) of each pixel output, it consists of:

- Pixel-level temporal noise 5.7e^-
- Row noise 0.72e^-
- Column noise 0.52e^-

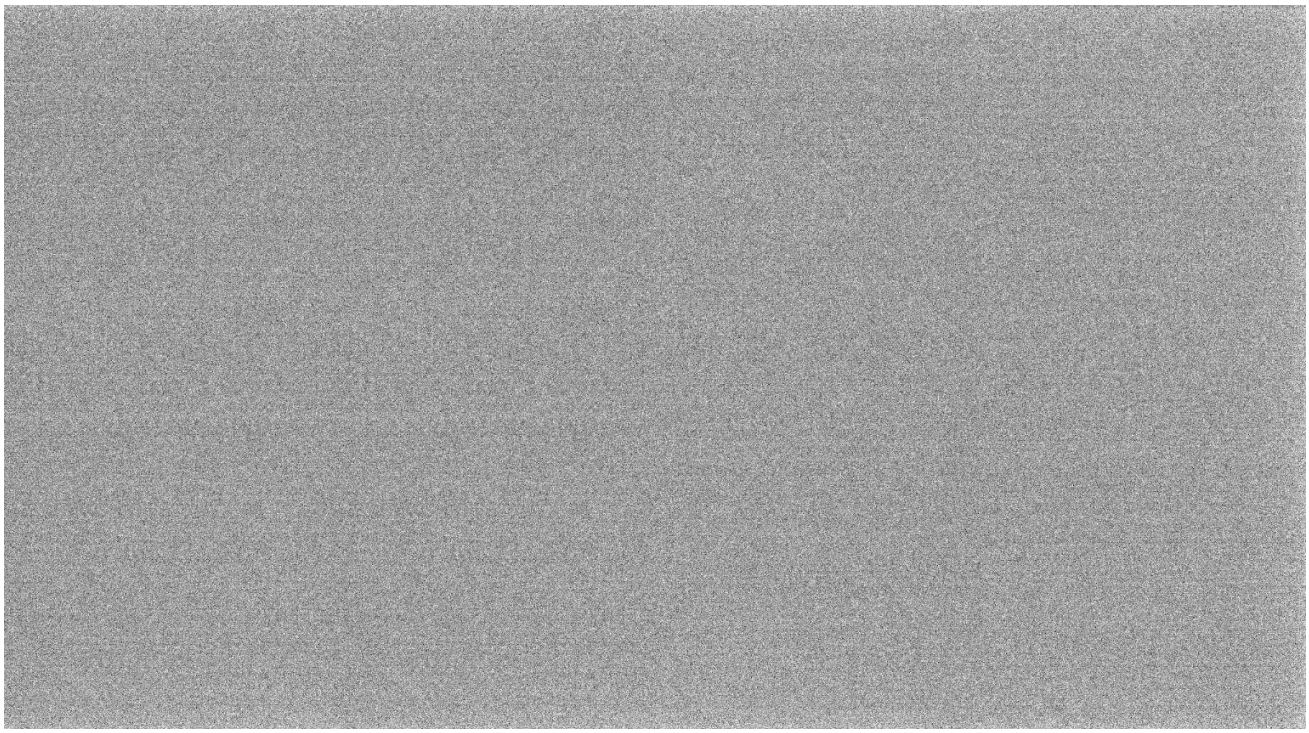


Figure 23: Dark image of GSENSE2011s image sensor

Image Sensor Characteristics Measurement Method

All measurement methods are based on the EMVA 1288 Standard[1].

Measurement Conditions

No.	Measurement Condition	Explanation
1	Constant illumination with variable exposure time	With this method, the light source is operated with constant radiance and the irradiation is changed by the variation of the exposure time. The non-uniformity of the light source is less than 2%.
2	Monochromatic light source	With this method, the light output of a monochromator which consists of a series of optical gratings (300-1000nm) is used.
3	Temperature operation	Room temperature: 25 degrees, no active cooling applied for the sensor.

Measurement Method

1. FWC

Set to measurement condition 1. At each exposure time, 50 grabbed images are averaged and the averaged resulting image is again averaged over all its pixels. The FWC is calculated by dividing the saturation signal (DN) by the conversion factor (DN/e^-).

2. Linear FWC and Linear Error

Set to measurement condition 1. The linearity is determined by computing a least-squares linear regression with the data points in the linear range of the response curve. Then the linear FWC is calculated by dividing the maximum signal (DN) in the linear region by the conversion factor (DN/e^-). The linear error is calculated by:

$$LE = MAX(LE(i)) = MAX(100 \cdot \frac{Y(i) - (a0 + a1 \cdot Exp(i))}{Y_{sat}})$$

Where

Item	Explanation
LE	Linear error
$LE(i)$	Linear error of data point i
$Y(i)$	The pixel signal (DN) at exposure time $Exp(i)$
Y_{sat}	The saturation signal
$a0 + a1 \cdot Exp(i)$	The linear fit value at exposure time $Exp(i)$

3. Temporal Noise

When the temporal noise is measured, the sensor is put in a completely dark environment. 50 full images are grabbed with shortest possible integration time. Based on these images, the noise on pixel level is counted by calculating the stdev value of these pixel output values of every pixel. From the histogram, the peak value can be obtained.

4. Dynamic Range

Typically, the dynamic range of an image sensor is calculated by dividing the FWC by the temporal noise, both in units of electrons.

$$DR = \frac{FWC}{temporal\ noise}$$

5. Sensitivity

Set to measurement condition 2. The power of the single-wavelength (600nm) light source is measured by the optical meter in unit of W/m^2. Then the response curve of the sensor is measured. The slope of the linear range of the response curve (e^-/(W/m^2)) is divided by the integration time (s) to calculate the sensitivity.

6. Dark Current and DCNU

For this measurement, at various exposure times and at room temperature of 25°C, multiple (5 frames) completely dark full images are grabbed. The dark current (DN/s) is the slope of the sensor output (DN) versus the exposure time (s). The dark current (e^-/s) is calculated by dividing this slope by the conversion factor (DN/e^-). The stdev of dark current at each pixel point is considered to be the DCNU.

7. FPN

This non-uniformity is calculated based on 50 full scale images taken in completely dark condition with shortest possible integration time as possible and these 50 images are averaged in order to reduce the influence of any temporal noise component. The stdev of such a resulting averaged image is considered to be the FPN.

8. PRNU

Set to measurement condition 1 and an exposure time until at least 50% of saturation is reached. 20 full scale images are grabbed in completely dark condition and uniform illumination. Mean and stdev values are calculated just like in the case of the FPN measurement.

$$PRNU(\%) = 100 \cdot \frac{\sqrt{S_{50}^2 - S_d^2}}{\overline{y_{50}} - \overline{y_d}}$$

Where s and $\overline{y}$ are respectively stdev and mean value of the average resulting image. Mark “50” and “d” are respectively 50% of saturation signal and dark signal.

Driving the Sensor

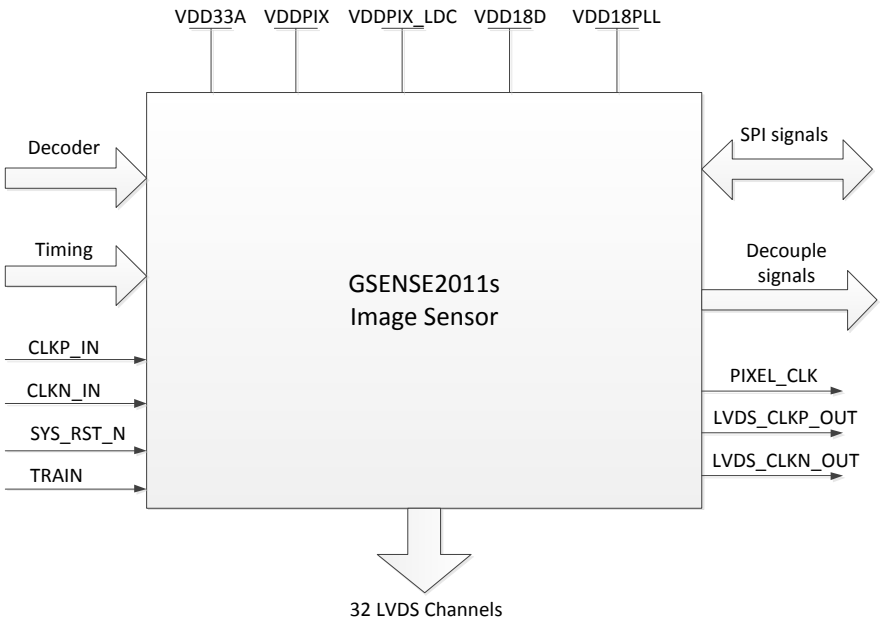


Figure 24: Driving the sensor

Figure 24 shows the necessary external signals to drive the image sensor. The user can find all the dc details of the inputs in the “DC Characteristics”.

1. Power supplies
   GSENSE2011s needs five power supplies: VDD33A, VDDPIX, VDDPIX_LDC, VDD18D and VDDPLL. Please refer to the “Power Consumption” for the details.

2. SPI signals
   GSENSE2011s uses five-pins SPI to program the sensor. After power-on or reset sequence, the sensor must be reprogrammed. The timing of the SPI signals is shown in the “Register Communication Timing”.

3. Decoder and timing signals
   Decoder is used to control the row logic address of the pixel array while timing signals are used to control the read out circuit of the sensor. The decoder and timing signals must be operated at the same time, please refer to the “Timing of Control Signals” for the control timing details.

4. Input clock
   The sensor needs a high speed clock to generate the internal control signals and two methods are provided to generate it: The first one is using the internal PLL and an external low speed clock (CLK_REF); The other is using the internal LVDS receiver and a pair of external high speed differential clock (CLK_N and CLK_P). The details of them are shown in “Input Clock Selection”.

5. Decouple signals

   Please refer to the “Analog Decouple” for the details of all the decouple signals. The table below shows the symbol of the external signals.

Power supplies	SPI signals	Decoder	Timing signals	Input clocks		LVDS driver outputs	System signals
				PLL	LVDS Receiver		
VDD33A	SPI_IN	ROW<11:0>	RST	CLK_REF	CLK_N	OUTNT<0:15>	SYS_RST_N
VDD18D	SPI_READ		SEL		CLK_P	OUTPT<0:15>	
VDDPLL	SPI_WRITE		TX2			OUTNB<0:15>	
VDDPIX	SPI_CLK		TX1			OUTPB<0:15>	
VDDPIX_LDC	SPI_OUT		HDR			CLKP_OUT	
			SYNC			CLKN_OUT	
			BLS				
			TR_TS				
			VTZ				
			READ				
			C_INIT_B				
			C_INIT_T				
			TAC				
			CPC				
			SAM_B				
			SAM_T				

Power-on Sequence

The power supplies should follow the power-on sequence as illustrated in Figure 25. It is necessary that the sensor power-on sequence follow the minimal time delays as specified in Figure 25. Otherwise, the sensor may be damaged.

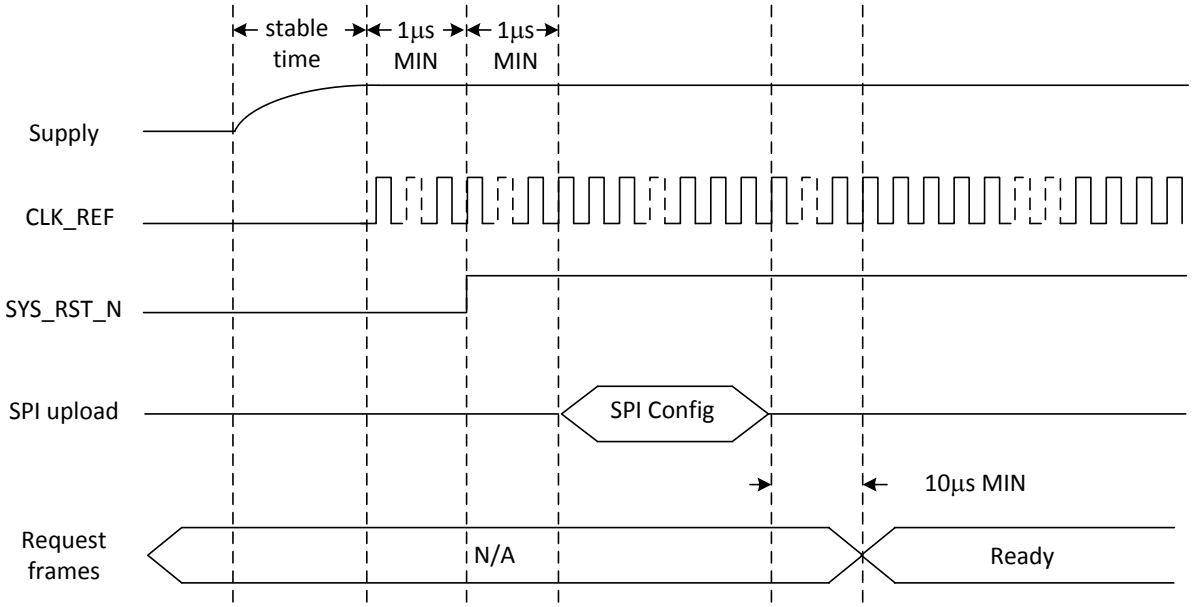


Figure 25: Power-up sequence

Reset Sequence

The reset sequence of GSENSE2011s is shown in Figure 26. The reset sequence should follow the corresponding minimal time delay as specified in Figure 26. All programming registers will be reset to ground when a falling edge is detected on the pin SYS_RST_N. It is necessary to upload a new SPI register after resetting the sensor. When different CLK_REF speed is desired while the sensor is running, the reset sequence must be executed.

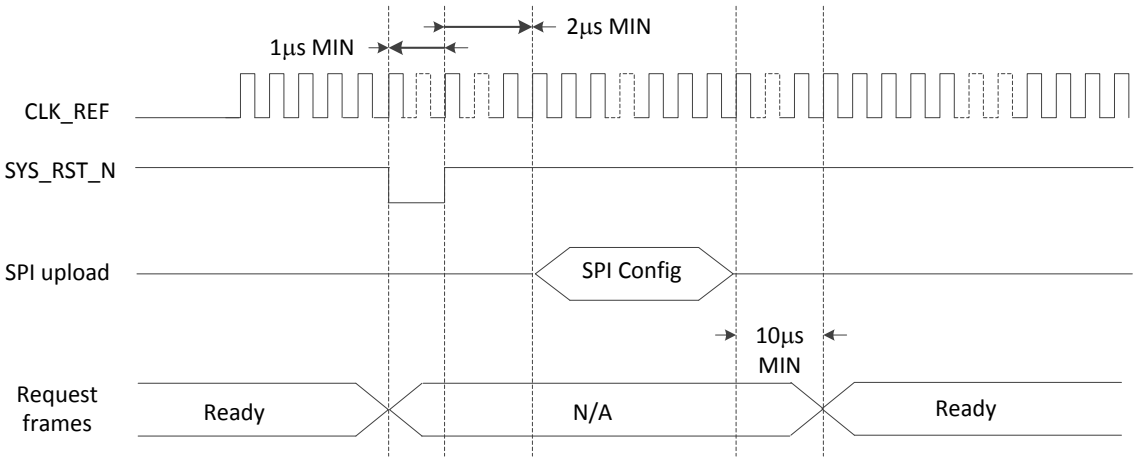


Figure 26: Sensor reset sequence

Register Communication Timing

After the power-up or reset sequence, the default values for all SPI registers are '0'. The SPI registers should be re-programmed via a serial-to-parallel interface (SPI) first. The maximum SPI_CLK is 25MHz.

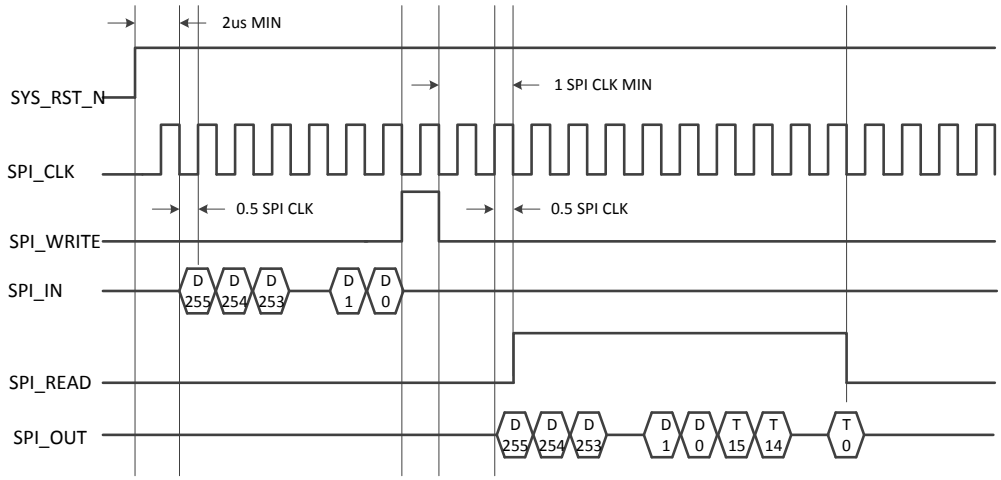


Figure 27: SPI write and read sequence

Figure 27 shows the SPI write and read sequence. The first data in SPI_IN should be sent at least 2 us after the SYS_RST_N is pulled high. The data on SPI_IN is loaded sequentially at each rising edge of SPI_CLK. At the 256th SPI_CLK falling edge, the SPI_WRITE should be set to '1', indicating one SPI write process is completed. The sensor operates at this setting until the next rising edge on SPI_WRITE is detected. The SPI clock may be continuously running or stopped after the writing is finished.

The data written to the SPI registers may be read out via the same interface. SPI_READ should be pulled high at a falling edge of the SPI_CLK. Then the SPI registers are read out sequentially at each rising edge of the SPI_CLK, together with the on-chip 16-bit temperature sensor data. Please note that SPI write sequence and the read sequence cannot be executed at the same time.

Input Clock Selection

Sensor needs a high speed clock (named CLK_INTER in the sensor) to generate the internal control signals. There are two selections (shown in Figure 28) to provide the high speed clock by programming the SPI registers.

1. When using the internal PLL (LVDSRECEN=”0”, LVDS receiver is disabled), the input reference clock (CLK_REF) must be provided. Then CLK_INTER is influenced by PLL,

$$f_{CLK\_INTER} = f_{clk\_ref} \times Mx / Dy \qquad 250MHz \leq f_{clk\_ref} \times Mx \leq 650MHz$$

f_{CLK_INTER} is the frequency of CLK_INTER, Mx is the internal PLL multiplication factor controlled by PLLDIV[3:0], Dy is the internal PLL dividing factor controlled by PLLCTRL[1:0]. Please see Figure 28 for details.

2. When using the LVDS receiver (LVDSRECEN=”1”, PLL is disabled), a pair of high speed differential LVDS input clock (CLK_P and CLK_N) must be provided. Then CLK_INTER is influenced by LVDS receiver,

$$f_{CLK\_INTER} = f_{clkp\_in}$$

f_{clkp_in} is the frequency of CLK_P or CLK_N

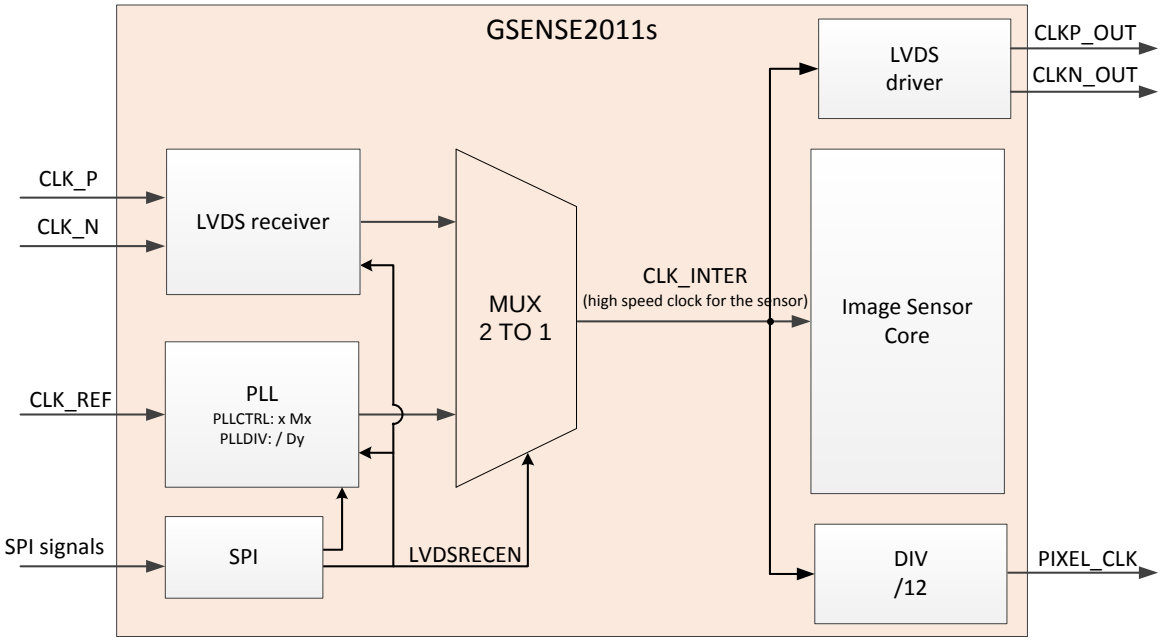


Figure 28: The block diagram of generating a high speed clock for the sensor

The table below shows the detailed information of the related register settings.

Address	Bit	Register Name	Description	Default value
17:16	1	PLLCTRL[1:0]	internal PLL dividing factor Dy: 00: /1 01: /2 10: /4 11: /8	0
	0			0
14:11	3	PLLDIV[3:0]	Internal PLL multiplication factor Mx: 0000: x1 0001: x2 … 1111: x16	1
	2			0
	1			1
	0			1
39	0	LVDSRECEN	LVDS receiver enable： 0: disable(enable internal PLL) 1: enable(disable internal PLL)	1

PIX_CLK Calculation

PIX_CLK is the digital output pin of the sensor and its frequency is one of the parameters in the formulas of calculating the line time and frame frequency. PIX_CLK is influenced by CLK_INTER.
If one PIX_CLK has a frequency of f_{pixel_clk}, then f_{pixel_clk} can be calculated as below:

$$f_{pixel\_clk} = f_{CLK\_INTER} /12$$

Operating Pixel Array

The GSENSE2011s sensor supports two pixel operation modes: Rolling HDR and Global HDR. GSENSE2011s uses a 12-bit decoder (Pin: ROW<11:0>) to operate the pixel array in rolling HDR mode and 11-bit decoder(Pin: ROW<10:0>) in global HDR mode. In rolling HDR mode, pin ROW<11>_FOT is treated as decoder address control ROW<11>, in global HDR mode, pin ROW<11>_FOT is treated as timing control FOT . The operation of these modes is described separately.

Rolling HDR Mode

In one line-time, the decoder has two phases: one is defined as a read phase and the other is defined as a reset phase. The read phase is always prior to the reset phase when they are in the same line-time.

Figure 29 shows the decoder phase definition.

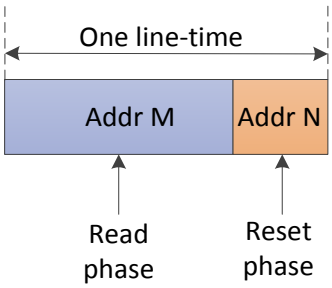


Figure 29: Decoder phase definition

The difference between these two addresses defines the exposure time (in the number of lines):

1. When exposure time is less than the number of selected rows, the exposure time is calculated as:

$$T_{exp,RHDR} = (K + N - M - 1)\%K$$

Where $T_{exp,RHDR}$ is the exposure time, K is the number of selected rows, M is the address of read row in one line time, N is the address of reset row in one line time.

2. When exposure time is equal to or larger than the number of selected rows, dummy rows must be inserted to increase the exposure time and the address of read row in one line time should be the same as the address of reset row in one line time, then the exposure time is calculated as:

$$T_{exp,RHDR} = K - 1 + N_{dummy}$$

Where N_{dummy} is the number of inserted dummy rows. Figure 30 shows the N_{dummy} definition.

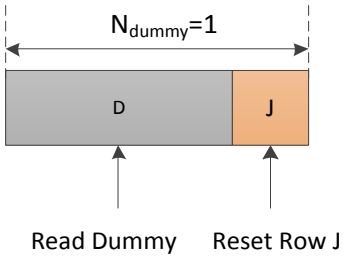


Figure 30: N_{dummy} definition

NOTE:

The N and M must be the addresses in the selected rows, for example, if the address range of the K selected rows is from X to $X+K-1$, then:

$$\begin{cases} X \le M \le (X+K-1) \\ X \le N \le (X+K-1) \end{cases}$$

Suppose in total L dummy rows are inserted for the required integration time, row address J in dummy rows inserted are calculated as:

No. of the dummy row inserted	J value(Address -1 and 1152 are treated as Address D(dummy address))
0	Max(X+K,1152)
1	Min(X-1,-1)
2	Max(X+K,1152)
3	Min(X-2,0)
...	...
L-1	Max(X+K+(L-1)/2, 1152) if L%2=1 Min(X-(L-1)/2, -1) if L%2 = 0

Figure 31 and Figure 32 show the moving of the address decoder when the sensor is working with different exposure time. By changing the address of reset row, read row in one line time and N_{dummy}, the user can easily modify the exposure time for GSENSE2011s sensor.

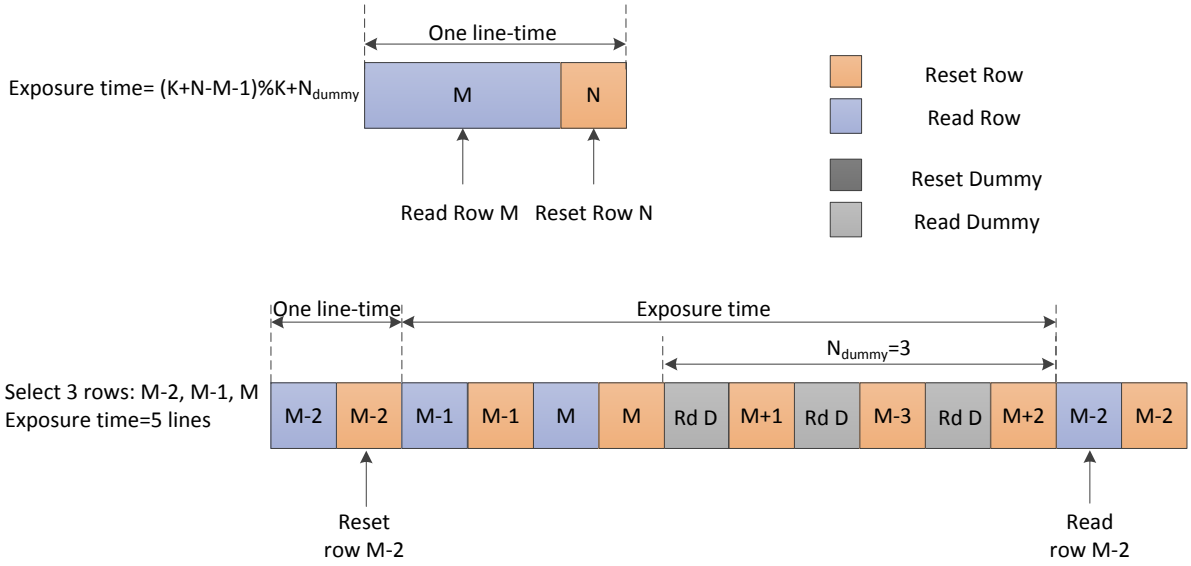


Figure 31: Exposure time is larger than selected rows in HDR Mode

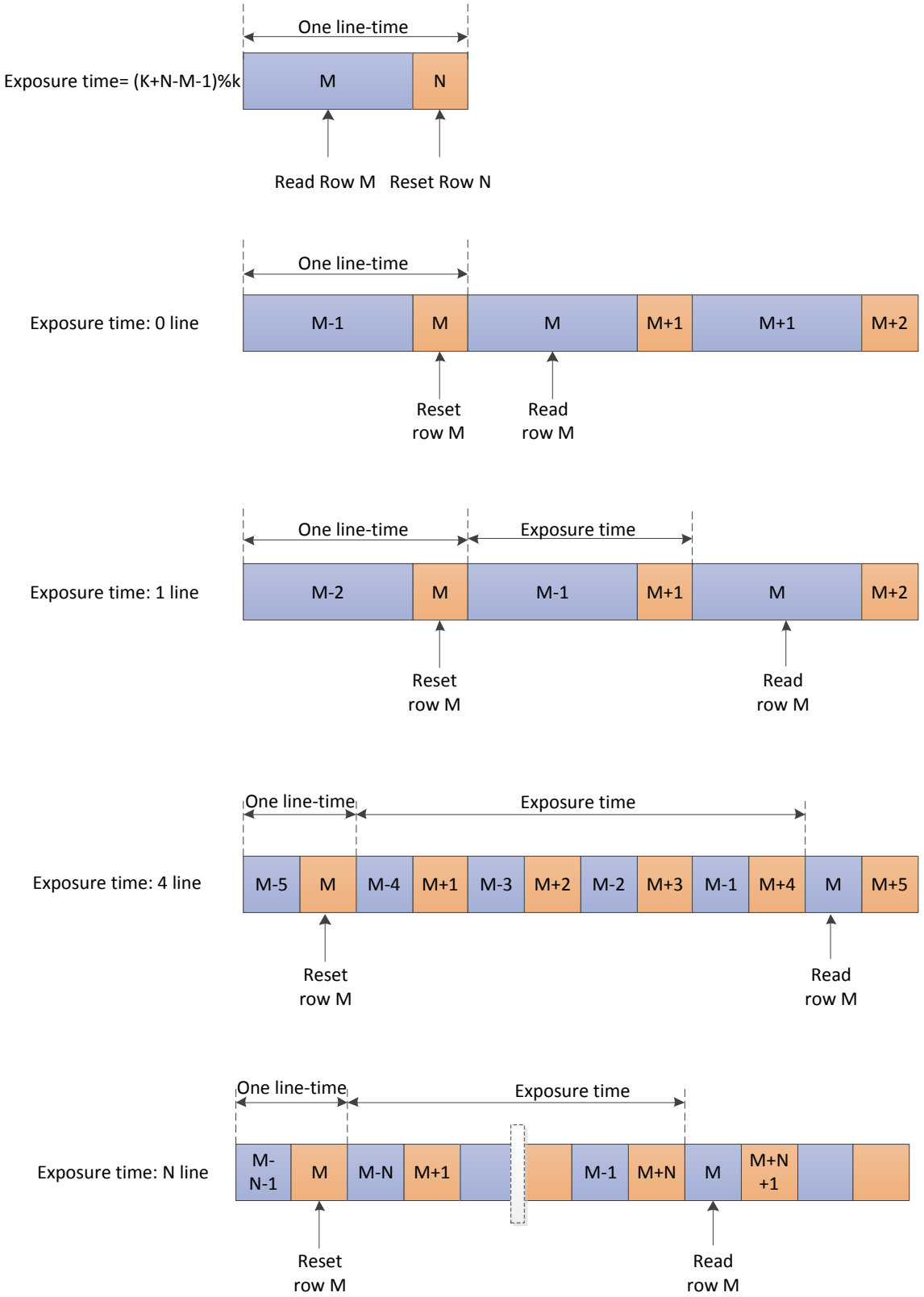


Figure 32: Setting exposure time in rolling HDR mode

Request a single frame

Figure 33 shows the sensor row operation of a full frame with the exposure time of two line-times. Figure 34 illustrates the decoder address in a full frame (same condition as above).

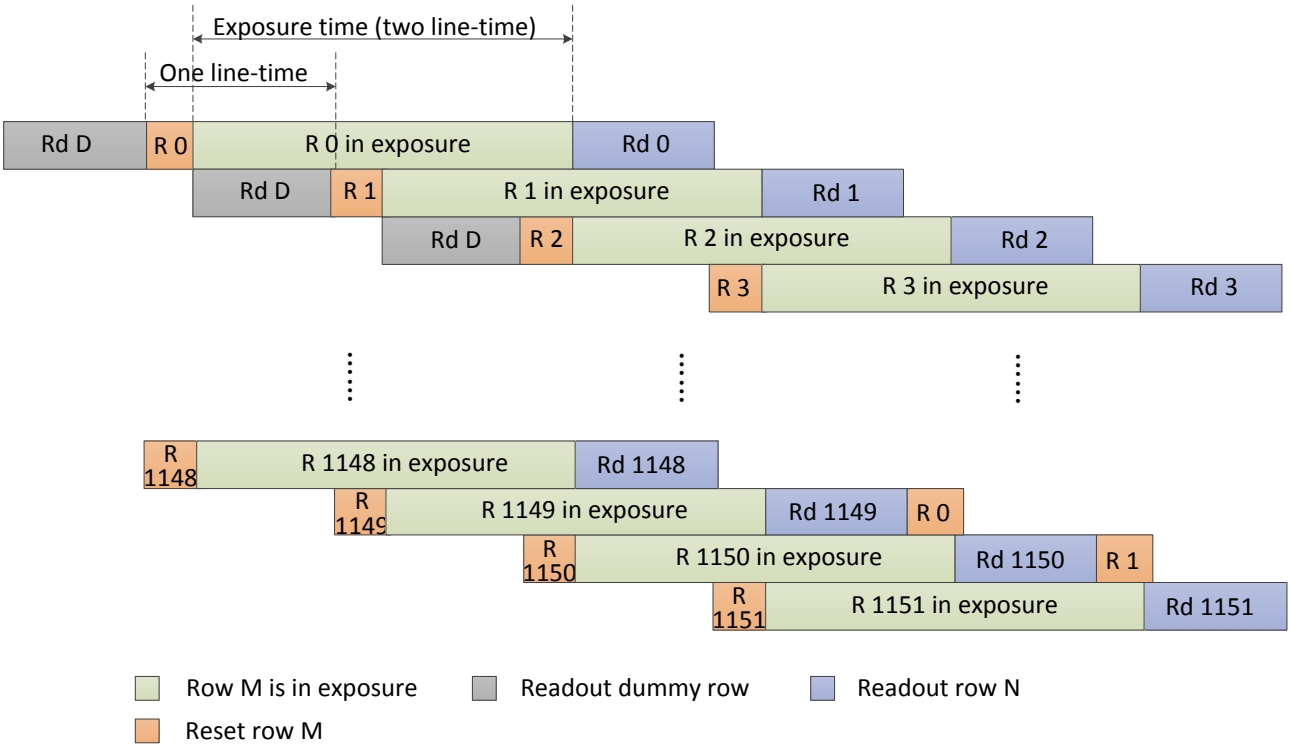


Figure 33: Row operation of a full image

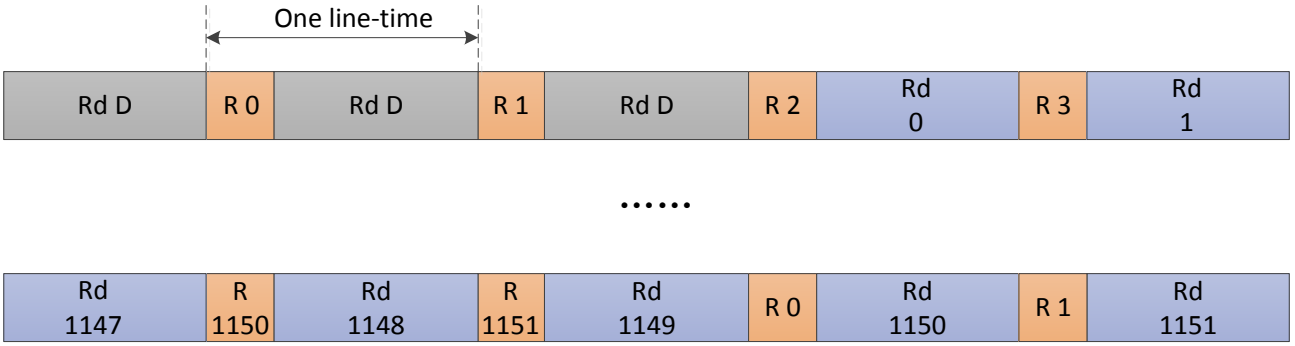


Figure 34: Movement of the decoder address in a full frame

A dummy address can be inserted to reduce the frame rate. In this case, the read operation does not address any physical pixel row, while reset operation continues resetting the pixel row as illustrated in Figure 33, it is actually meaningless to do the read operation before the exposure finished. The last two reset phases continue resetting pixel row 0 and 1 even they have already been readout. In GSENSE2011s sensor, it is recommended to use address “4000” as the dummy address in both read and reset phase.

Request multi-frame

If more frames are required, it is possible to start a new exposure during the previous frame readout. The decoder is shown in Figure 35 when two frames are required and the exposure time is two line-times.

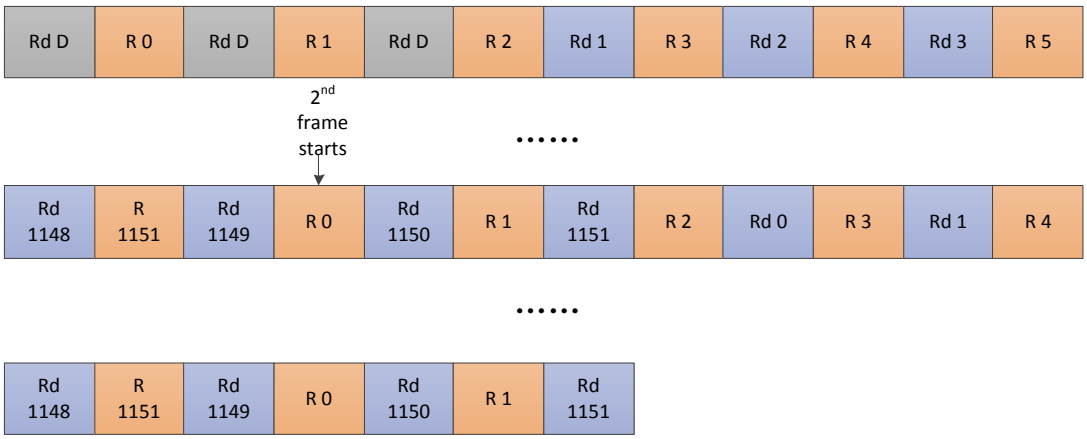


Figure 35: The decoder when two frames are requested

When the exposure time (using number of lines in description) is equal or larger than the number of selected rows, the movement of the decoder is shown in Figure 36. In the example, the exposure time is set to 1153 line time.

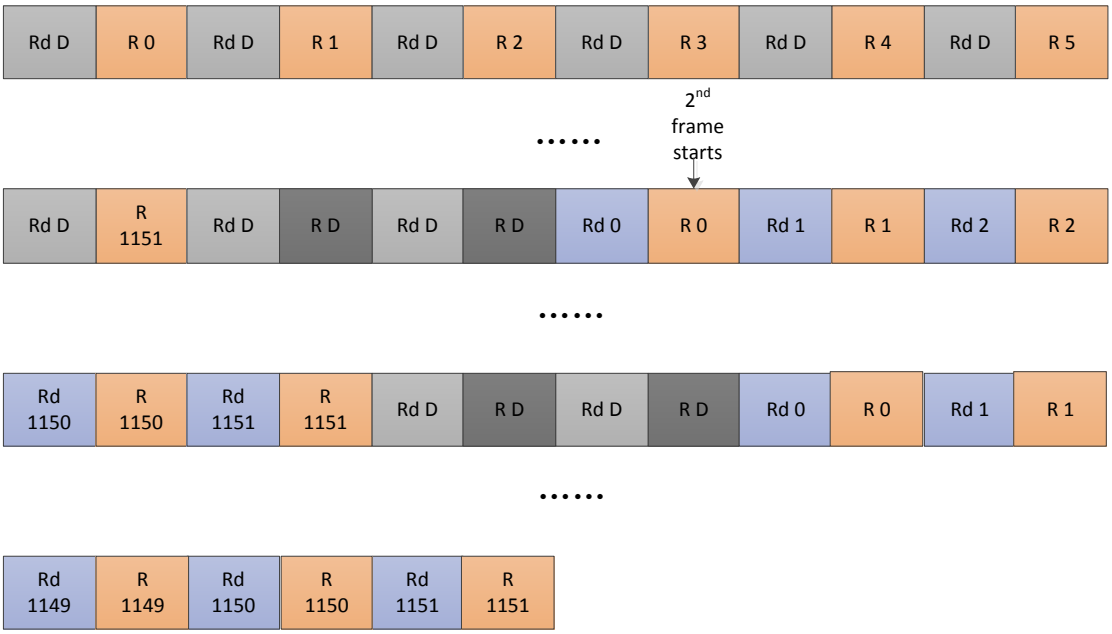


Figure 36: Movement of the decoder when exposure time is equal or larger than selected rows

In conclusion, when multi-frame is requested:

1) If the exposure time is less than the number of selected rows, the exposure of the first row in the second frame follows the exposure of the last row in the first frame (remember there is a read phase between two reset phases).
2) If the exposure time is equal or larger than the number of selected rows, the exposure of the first row in the second frame starts immediately after the readout of the first row in the first frame.

Global HDR Mode

In Global HDR mode, external CDS is incorporated to remove the in-pixel KTC noise and offset. Figure 37 shows the process to get one HDR image from GSENSE2011s sensor when it is operating in global shutter HDR mode. Two images for pixel reset(RST_HG and RST_LG) are first read-out and stored externally. After that, two images for pixel signal(SIG_HG and SIG_LG) are readout for processing. Image RST_HG should be subtracted from SIG_HG to get a HG_GLOBAL image. RST_LG should be subtracted from SIG_LG to get a LG_GLOBAL image. Then these two images are used to generate one HDR image(HDR_GLOBAL).

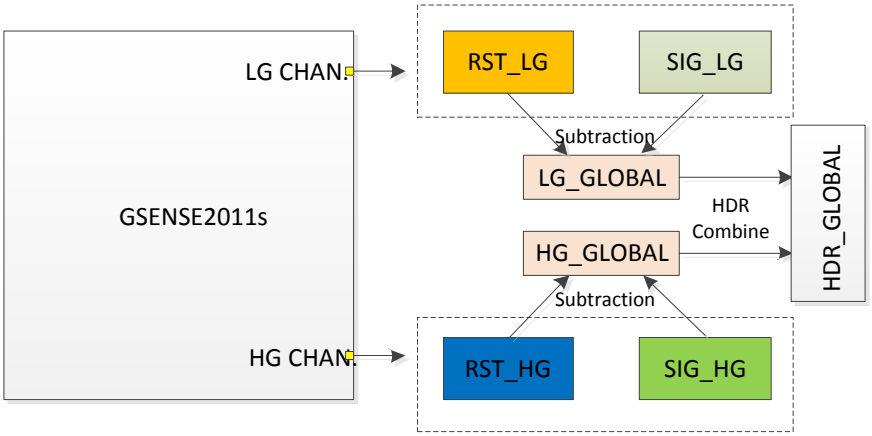


Figure 37: Process to generate one HDR image for global shutter

For the readout of the images, RST_HG and RST_LG are sent out from the sensor at the same time but from different channels, this also applies to image SIG_HG and SIG_LG. So in the later sections about GSENSE2011s working in this mode, we will describe the operation with only RST image and SIG image for simplicity.

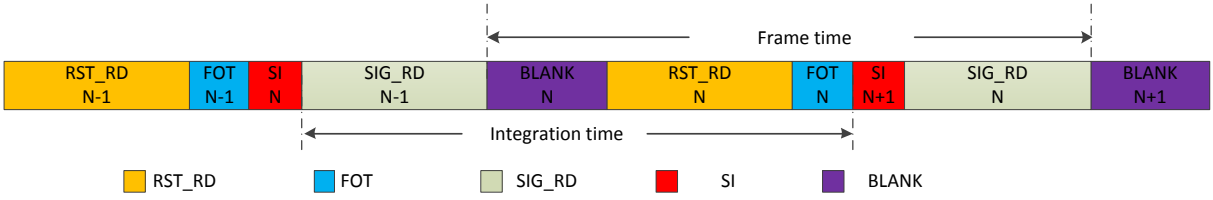


Figure 38: Operation sequence for GSENSE2011s in global HDR mode

Figure 38 shows the typical GSENSE2011s sensor operating sequence. It contains five phases(RST_RD, FOT, SIG_RD, SI,BLANK). In order to readout one frame, first RST image is reading out line by line in phase RST_RD, after that FOT phase is needed to store the collected charges in the pixel array, then the SIG image is again read out line by line in SIG_RD phase. SI(start integration) is needed to start the integration of the whole array,

depending on the integration time, SI can be inserted during the readout, or when the readout has finished. When it is inserted in RST_RD or SIG_RD phases, the frame readout should be stopped and restarted after the SI phase. When the integration time is longer than the readout time for RST image and SIG image, BLANK should be inserted as shown in the figure.

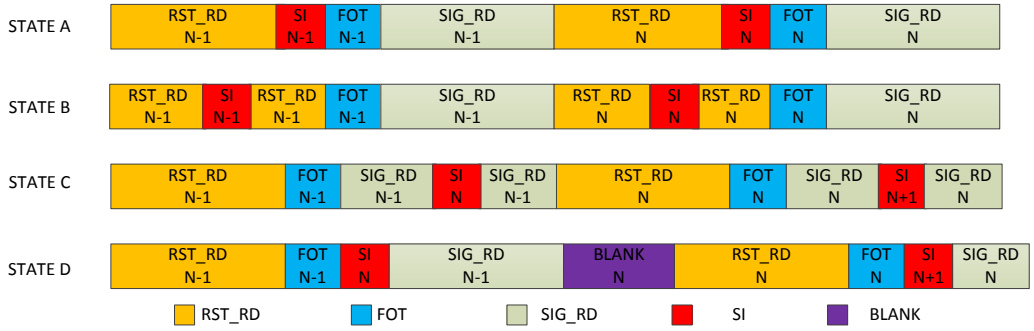


Figure 39: Different operation states for GSENSE2011s sensor

Depending on the integration time required, GSENSE2011s sensor should to be operated in four different operation states. This is shown in Figure 39. In STATE A, SI phase is in between phase RST_RD & FOT, integration time in this state is quite short. As the integration time increases, GSENSE2011s should be operated in state B, C and D. In state D, phase BLANK is inserted to increase the total integration time. The users should do calculations based on section “Frame rate calculation” to check which state the sensor need to be operated in.

GSENSE2011s sensor is in idle state when there is no image requested. In this state, the decoder address should be kept to row 0 and the control signal timing is the same as in phase RST_RD except that TX2 is constantly in logic ‘1’.

Decoder operation

Please be noted that pin “ROW<11>_FOT” is treated as FOT in global HDR mode.

RST_RD and SIG_RD phase

Pixel data from GSENSE2011s is readout row by row sequentially. For each line time, the decoder address keeps the same which is quite different as in rolling shutter mode. Users need to drive the control signals and row address decoder together in order to readout the correct row image.

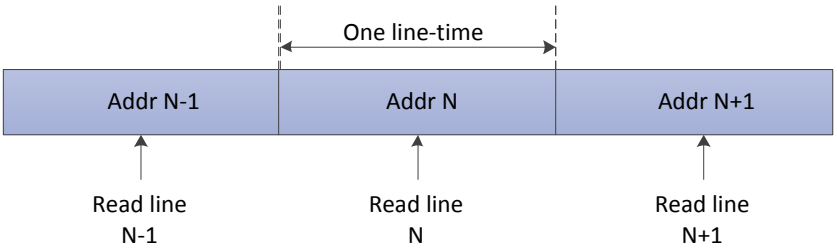


Figure 40: Decoder address during one line time of readout in RST_RD and SIG_RD phase

For GSENSE2011s sensor, one RST image and SIG image takes 1153 line-times to readout. Figure 41 shows the

decoder address for three line-times when the sensor is in phase RST_RD and SIG_RD phases. Figure 41 shows the exact decoder address in these two phases. In order to readout the total 1152 lines, 1153 line-times are needed. For the extra one line-time, the decoder address should keep it as it is (1151 as in Figure 41).

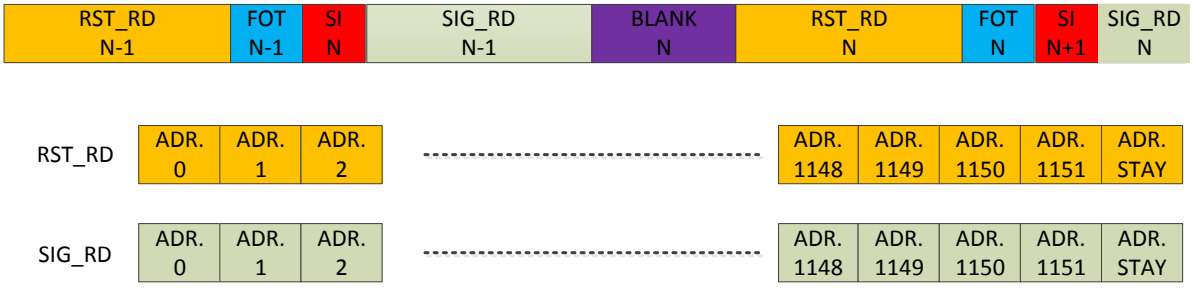


Figure 41: Decoder address during the frame readout for RST image and SIG image

FOT phase

In FOT phase, GSENSE2011s sensor will transfer all the integrated charges that collected in current frame to the in-pixel memory node. Six line-times are needed in this phase, the decoder address should keep the same as in last line-time, this is shown in Figure 42.

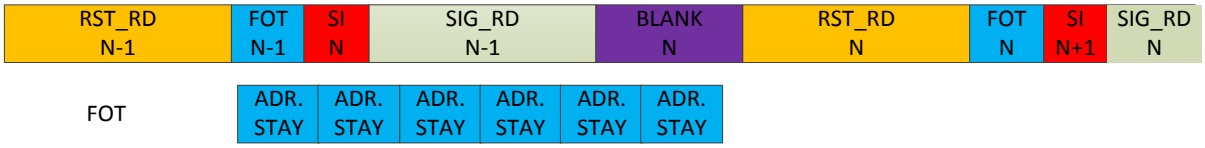


Figure 42: Decoder address during the FOT phase

SI phase

In SI phase, GSENSE2011s sensor will clear all the charges collected in the photodiode in each pixel and start a new integration. In total six line-times are needed in this phase, the decoder address should stay the same as last line-time before the sensor enter this phase. This is shown in Figure 43.

Figure 43: Decoder address during SI phase

BLANK phase

When the integration time is longer than the readout time of RST image and SIG image, GSENSE2011s need to enter the BLANK phase in order to increase the integration time. Depending on the total integration time required, This phase includes several line-times, the decoder address should stay the same as last line-time before the sensor enter this phase. This is shown in Figure 44.

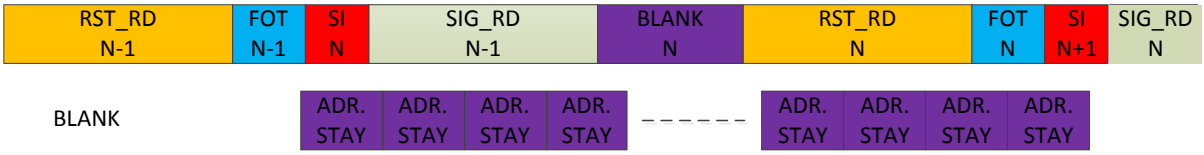


Figure 44: Decoder address during BLANK phase

Timing of Control Signals

In GSENSE2011s, All decoder signals and digital control signals should be synchronized to the rising edge of PIX_CLK (Digital output, pin D6).

Please refer to “PIX_CLK Calculation” for the details of PIX_CLK.

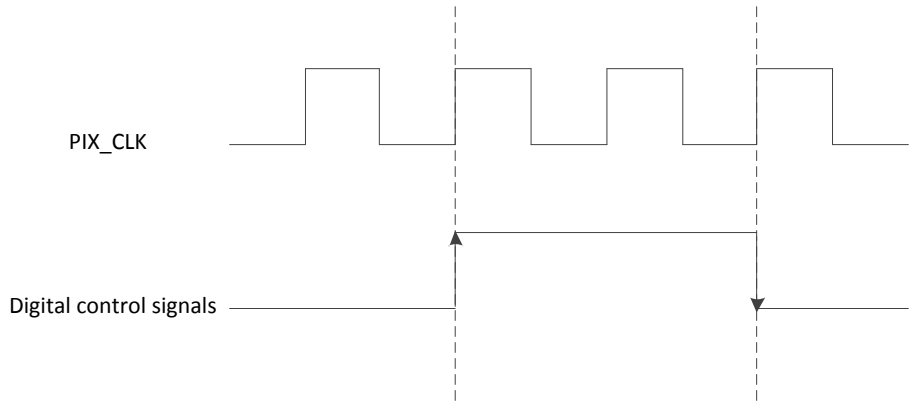


Figure 45：Synchronization

Rolling HDR Mode

In rolling HDR mode, one row is readout and another row is reset during one line-time. Control signals have a periodic of 534 PIX_CLKs (one line time) in this mode. Figure 46 shows the relationship between decoder address and control signals. The details of these signals in HDR mode are shown in Figure 47 and timing table of HDR mode. The figure and table include the same information but just in different view.

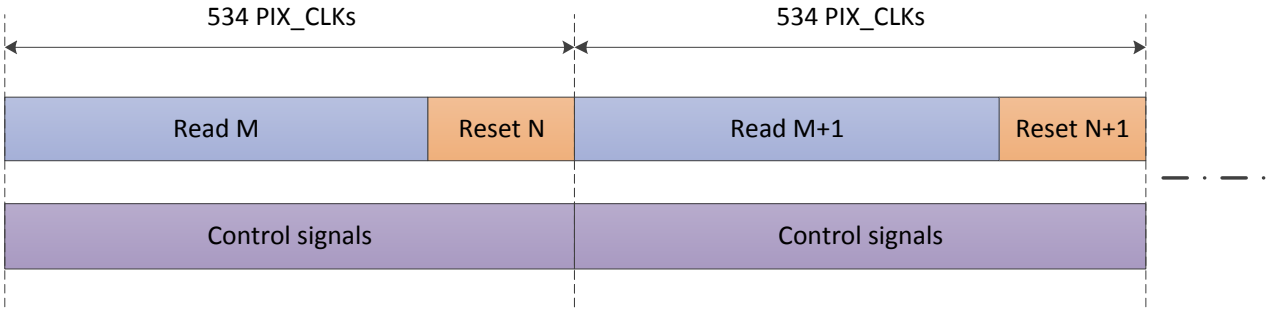


Figure 46: Relationship between decoder address and control signal

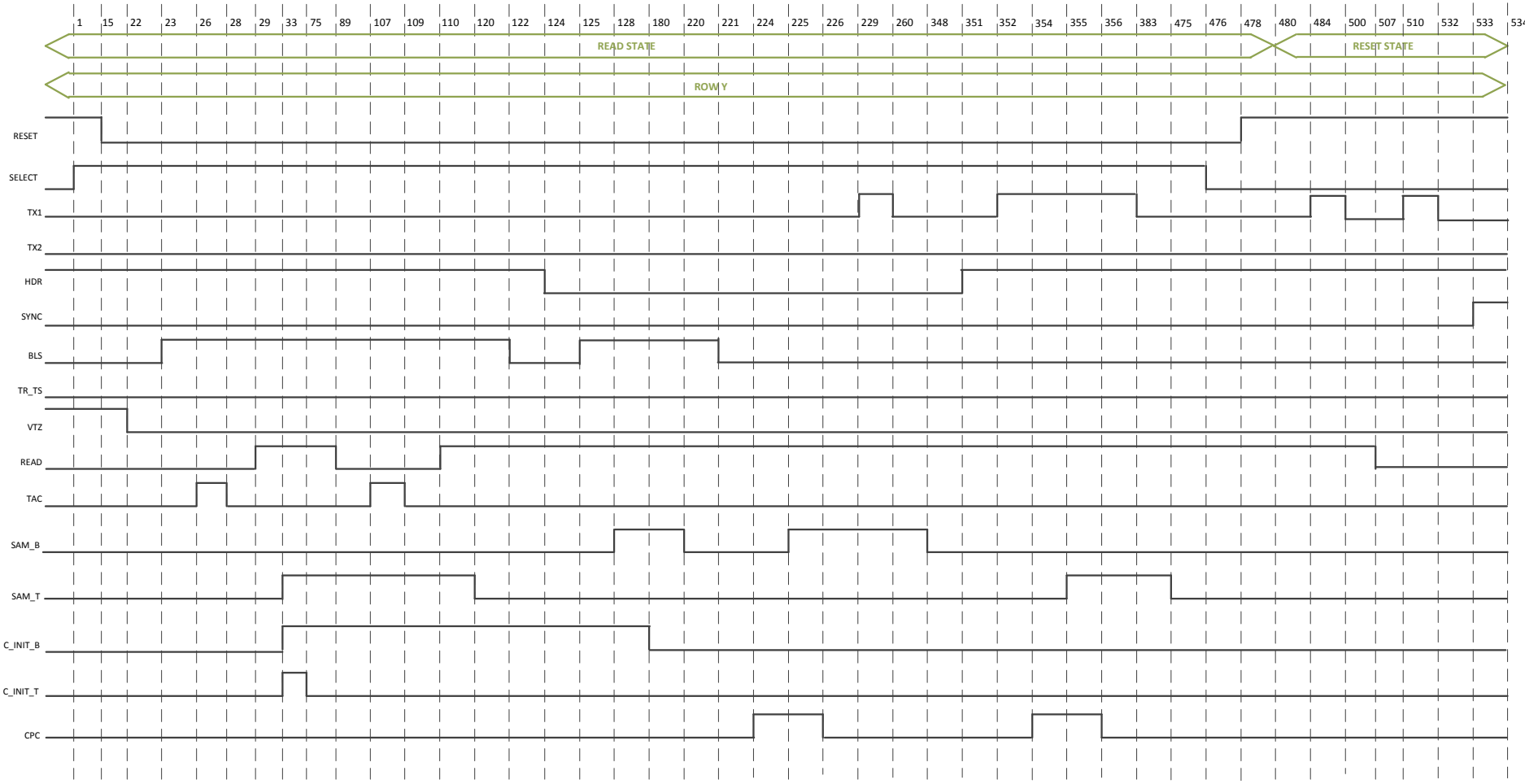


Figure 47: Timing for rolling HDR mode

Signal	Initial state	1st rising (falling) edge	Length	2nd rising (falling) edge	Length	3th rising (falling) edge	Length	4th rising (falling) edge	Length
RESET	1	15	463						
SELECT	0	1	475						
TX1	0	229	31	352	31	484	16	510	22
TX2	0	keep low							
HDR	1	124	227						
SYNC	0	533	1						
BLS	0	23	99	125	96				
TR_TS	0	Keep low							
VTZ	1	22	512						
READ	0	29	60	110	397				
TAC	0	26	2	107	2				
SAM_B	0	128	92	225	123				
SAM_T	0	33	87	355	120				
C_INIT_B	0	33	147						
C_INIT_T	0	33	42						
CPC	0	224	2	354	2				

Global HDR Mode

In global HDR mode, one row image data is reading out during one line-time. The decoder address stays the same in the complete line-time. Control signals need to drive the sensor together with decoder for the proper working of the sensor. Figure 48 shows the relationship between decoder address and control signals. Timing for control signals are different when the sensor is working in different phases. In below sections, this will be described in detail.

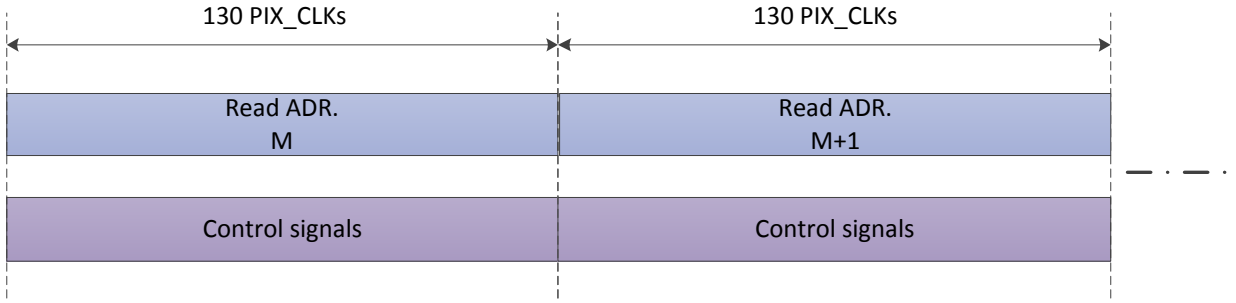


Figure 48: Relationship between decoder address and control signals in global HDR mode

RST _RD phase

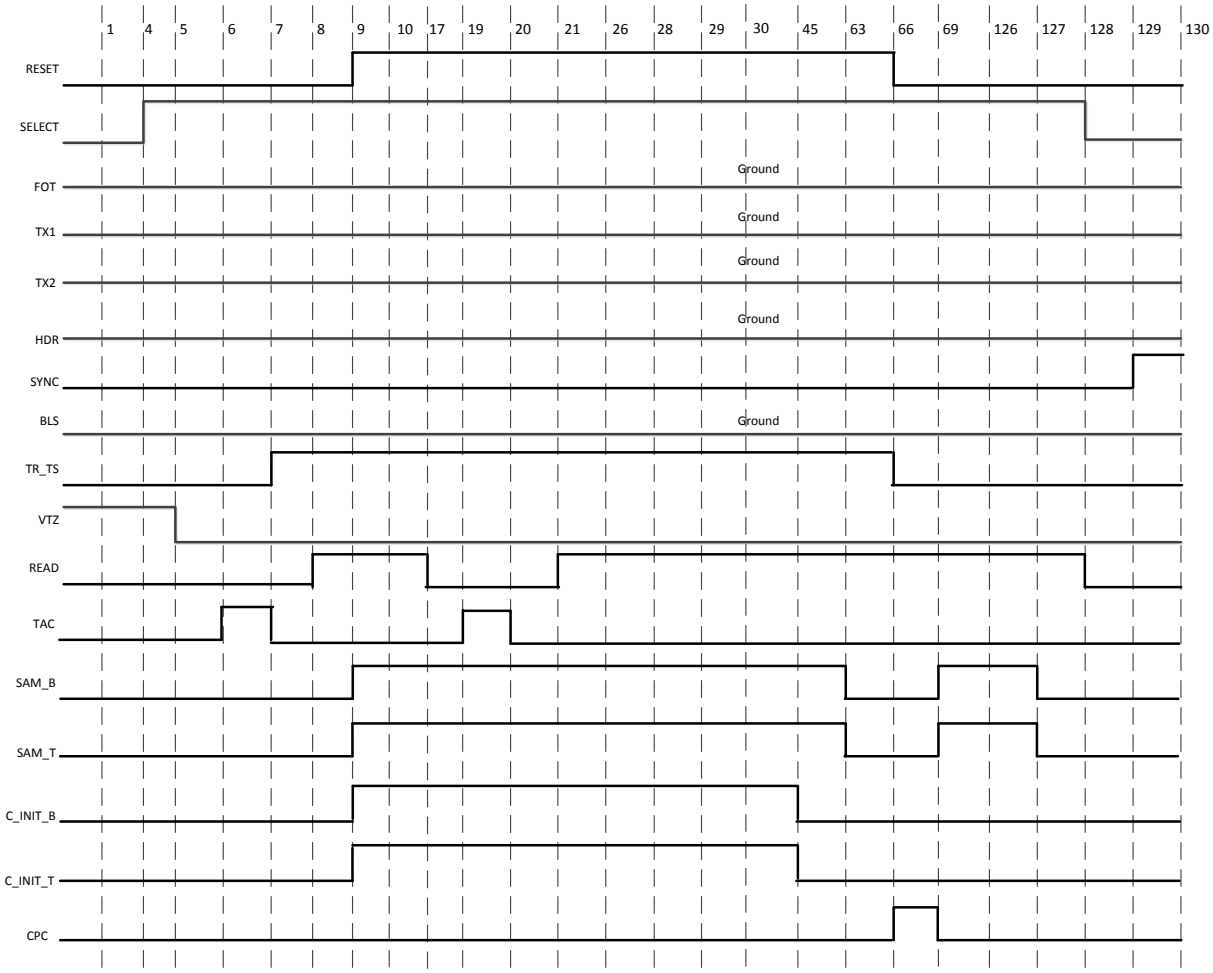


Figure 49: Control signals timing in RST_RD phase

Signal	Initial state	1st rising (falling) edge	Length	2nd rising (falling) edge	Length
RESET	0	9	57		
SELECT	0	4	124		
FOT	0	Keep low			
TX1	0	Keep low			
TX2	0	Keep low			
HDR	0	Keep low			
SYNC	0	129	1		
BLS	0	Keep low			
TR_TS	0	7	59		
VTZ	1	5	125		
READ	0	8	9	21	107
TAC	0	6	1	19	1
SAM_B	0	9	54	69	57
SAM_T	0	9	54	69	57
C_INIT_B	0	9	36		
C_INIT_T	0	9	36		
CPC	0	66	3		

SIG_RD phase

In this phase, the timing for control signals are the same as in RST_RD phase except for “Reset”, it keep to ground for the whole integration time.

FOT phase

GSENSE2011s will last 6 line-times in this phase. In the first line-time of this phase, the timing for all the control signals should be kept to ground except for “FOT” and “TX1”. In the last 5 line-times, the timing for all the control signals is the same as in SIG_RD phase.

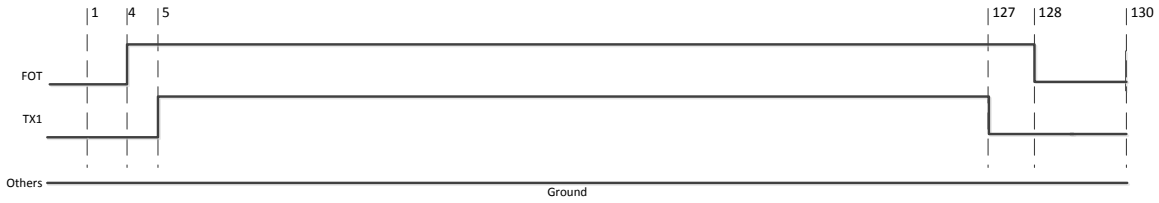


Figure 50: Control signals timing in the first line-time of FOT phase

SI phase

SI phase of GSENSE2011s sensor lasts for 6 line-times, the timing for control signals are the same as in RST_RD phase in state B and the same as in SIG_RD phase in in state A, C, D except for “TX2”. “TX2” pulses are different as

state A and state B-D in Figure 39. The pulse width for “TX2” is one line-time. Figure 52 shows the timing for control signals when the sensor enters SI phase in state A. In the last four line-times, TX2 should be kept ground. Figure 51 shows the timing for control signals when the sensor enters SI phase in state B-D. Users need to calculate how “TX2” are pulsed depending on the integration time. Please check section for more information.

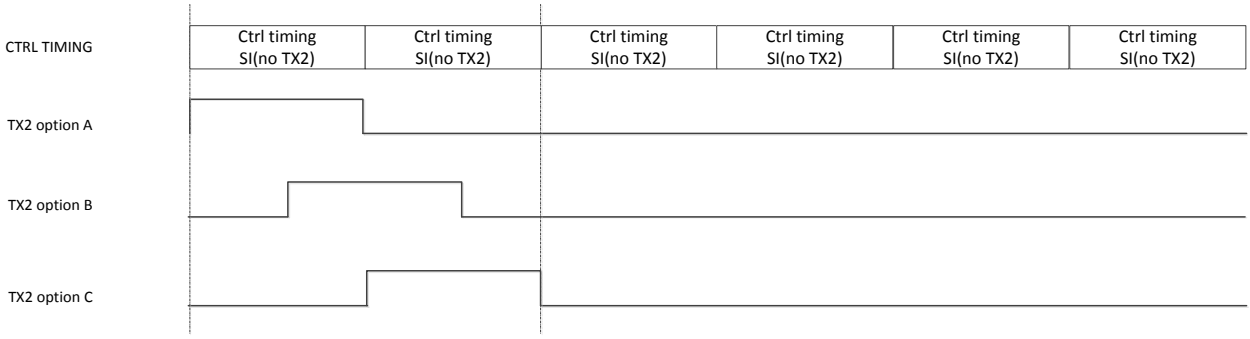


Figure 51: TX2 pulse in SI phase of GSENSE2011s(state B-D)

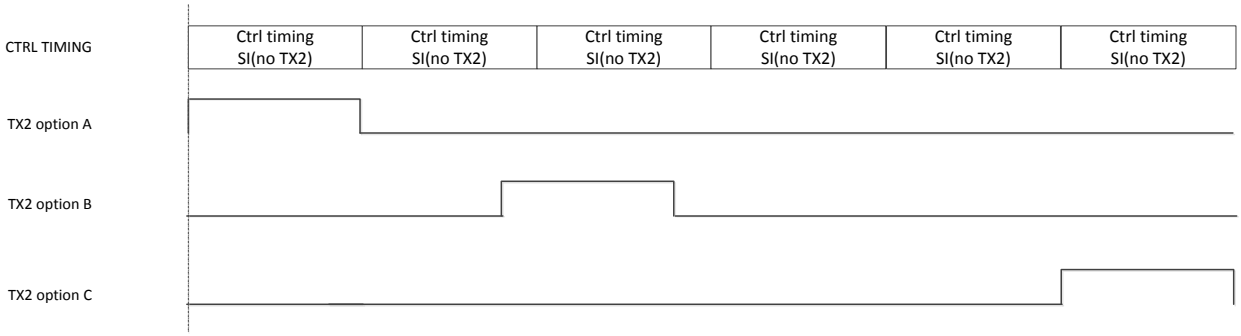


Figure 52: TX2 pulse in SI phase of GSENSE2011s(state A)

BLANK phase

BLANK phase for GSENSE2011s sensor can last several line-times depending on the integration time. The timing for control signals are the same as in RST_RD phase.

Exposure Time Calculation

The exposure time is influenced by the PIX_CLK's frequency. In the following calculation, T_{pixel_clk} is the period of PIX_CLK.

Rolling HDR mode

The line time T_{line} can be calculated as:

$$T_{line} = 534 \times T_{pixel\_clk}$$

In rolling HDR mode, exposure time:

$$T_{exp,RHDR} = N \times T_{line} + 385 \times T_{pixel\_clk}$$

N is the number of line-times, which is controlled by the decoder operation. N is an integer and can vary from '0' to any value in principle.

Global HDR mode

The line time T_{line} can be calculated as:

$$T_{line} = 130 \times T_{pixel\_clk}$$

The exposure time for the pixel is defined by the falling edge of TX2 in SI phase and the falling edge of TX1 in FOT phase. For different states that the sensor is operated, the exposure time has the following restriction, with k the number of selected rows for windowing.

State	Restrictions
A	$127 \times T_{pix\_clk} \le T_{exp,GHDR} \le 5 \times T_{line} + 127 \times T_{pix\_clk}$
B	$5 \times T_{line} + 127 \times T_{pix\_clk} \le T_{exp,GHDR} \le (k+6) \times T_{line} + 127 \times T_{pix\_clk}$
C	$(k+6) \times T_{line} + 127 \times T_{pix\_clk} \le T_{exp,GHDR} \le (2 \times k + 6) \times T_{line} + 127 \times T_{pix\_clk}$
D	$(2 \times k + 6) \times T_{line} + 127 \times T_{pix\_clk} \le T_{exp,GHDR}$

Frame Rate Calculation

Rolling HDR mode

Frame time is calculated as:

$$T_{frame,RHDR} = \begin{cases} K \times T_{line}, & N \le (K-1) \\ N \times T_{line}, & N > (K-1) \end{cases}$$

Where $T_{frame,RHDR}$ is the time used to get one frame (windowing or not windowing), N is the exposure time in number of line-times, K is the number of selected rows and must be less than 1152.

The frame rate is:

$$Frame\ rate\ =\ 1/T_{frame,RHDR}$$

Global HDR mode

Frame time in global HDR mode is calculated as:

$$T_{frame,GHDR} = \begin{cases} (2 \times K + 14) \times T_{line}, & state\ A\ B\ and\ C \\ (2 \times K + 14 + M_{BLANK}) \times T_{line} & state\ D \end{cases}$$

With K the number of selected rows, M_{BLANK} the number of line times inserted in phase BLANK.

The frame rate is:

$$Frame\ rate\ =\ 1/T_{frame,GHDR}$$

Register Map

Address	Bit	Register Name	Rolling HDR mode	Global HDR mode
255-250	5	V_BLSUN_BOT	0	1
	4		1	1
	3		0	0
	2		1	1
	1		1	1
	0		0	0
249-244	5	V_BLSUN_TOP	0	1
	4		0	1
	3		1	1
	2		0	0
	1		1	1
	0		0	0
243-238	5	ADC_GAIN	0	1
	4		1	0
	3		1	0
	2		1	0
	1		0	0
	0		0	0
237-234	3	I_RAMP_OTA	0	0
	2		1	1
	1		1	1
	0		1	1
233-230	3	I_ROWLOGIC	0	0
	2		1	1
	1		1	1
	0		1	1
229-226	3	I_TESTDRIV	0	0
	2		1	0
	1		1	0
	0		1	0
225-222	3	TANA	1	1
	2		1	1
	1		1	1
	0		1	1
221	0	LC_LVDS_EN	0	0
220-217	3	I_LVDS_DRIV	0	0
	2		1	1

	1		1	0
	0		1	0
216-213	3	I_COL_PC	0	1
	2		1	1
	1		1	0
	0		1	0
212-209	3	I_COL_LOAD	1	0
	2		1	1
	1		0	1
	0		0	1
208-205	3	INTERNAL_DRIV	0	0
	2		0	0
	1		0	0
	0		0	0
204-201	3	I_COMPINV	0	0
	2		1	1
	1		1	1
	0		1	1
200-197	3	I_COMP	1	0
	2		0	1
	1		0	1
	0		0	1
196-193	3	I_AMP	1	1
	2		0	1
	1		0	1
	0		1	0
192-187	5	V_VREF	0	0
	4		1	1
	3		1	1
	2		1	1
	1		1	1
	0		0	0
186-181	5	V_VTREF	1	1
	4		1	1
	3		0	1
	2		0	1
	1		1	0
	0		0	0
180-175	5	V_VTSIG	1	1
	4		0	1
	3		1	1

	2		0	1
	1		1	0
	0		1	0
174	0	VRAMP_EN	0	0
173-168	5	V_VRAMP	1	1
	4		0	0
	3		0	0
	2		0	0
	1		0	0
	0		0	0
167-158	9	DIG_10MSB_OFFSET	1	1
	8		1	1
	7		1	1
	6		1	1
	5		0	0
	4		1	0
	3		0	1
	2		0	1
	1		1	0
	0		0	1
157-152	5	DIG_6LSB_TOP_OFFSET	0	1
	4		0	0
	3		0	1
	2		0	1
	1		0	0
	0		0	0
151-146	5	DIG_6LSB_BOT_OFFSET	1	1
	4		1	0
	3		1	0
	2		1	1
	1		1	0
	0		1	0
145-142	3	TDIG_2	1	1
	2		0	1
	1		0	1
	0		1	1
141-138	3	TDIG_1	0	0
	2		0	0
	1		0	0
	0		1	1
137-132	5	PGA_GAIN_BOT	1	1

	4		1	0
	3		0	0
	2		1	0
	1		1	1
	0		0	0
131-126	5	PGA_GAIN_TOP	0	0
	4		0	0
	3		1	0
	2		1	1
	1		0	1
	0		1	0
125-114	11	TRAIN_PATTERN	1	1
	10		0	0
	9		0	0
	8		1	1
	7		1	1
	6		0	0
	5		0	0
	4		0	0
	3		1	1
	2		1	1
	1		1	1
	0		0	0
113	0	MUX_TO_4_EN	1	0
112	0	DELAY_SAMPLE_EN	0	0
111	0	DIG_READ_PL	0	0
110	0	FULL_ADDER_EN	1	1
109	0	ADC_10BIT_EN	0	1
108	0	FLIP_EN	0	0
107	0	LP_ADC_EN	1	1
106	0	ADC_CALI	1	1
105	0	PGA_NOISE_EN	1	1
104	0	PGA_CALI	0	1
103	0	COL_BIN	0	0
102	0	PIX_LDC_EN1	0	0
101	0	BOT_ANA_EN	1	1
100	0	TOP_ANA_EN	1	1
99	0	PIX_BIN_EN	0	0
98	0	PIX_HG_EN	0	1
97	0	GRST_EN	0	0
96	0	HDR_EN	0	0

95	0	DEC_10BIT_EN	0	0
94	0	DIRECTION_11BIT	1	1
93	0	SEQ_EN	0	0
92	0	GS_EN	0	1
91-64	27	SEQ_EXP_TIME	0	0
	26		0	0
	25		0	0
	24		0	0
	23		0	0
	22		0	0
	21		0	0
	20		0	0
	19		0	0
	18		0	0
	17		0	0
	16		0	0
	15		0	0
	14		0	0
	13		0	0
	12		0	0
	11		0	0
	10		0	0
	9		0	0
	8		0	0
	7		0	0
	6		0	0
	5		0	0
	4		0	0
	3		1	1
	2		1	1
	1		1	1
	0		0	0
63-52	11	SEQ_START_ADDR	0	0
	10		0	0
	9		0	0
	8		0	0
	7		0	0
	6		0	0
	5		0	0
	4		0	0
	3		0	0

	2		1	1
	1		1	1
	0		1	1
51-40	11	SEQ_ROW_NUM	0	0
	10		0	0
	9		0	0
	8		0	0
	7		0	0
	6		0	0
	5		0	0
	4		0	0
	3		0	0
	2		1	1
	1		0	0
	0		1	1
39	0	LVDS_REC_EN	0	0
38-35	3	I_LVDS_REC	0	0
	2		1	1
	1		1	1
	0		1	1
34	0	TEST_EN	0	0
33-18	15	SEQ_FRAME_NUM	0	0
	14		0	0
	13		0	0
	12		0	0
	11		0	0
	10		0	0
	9		0	0
	8		0	0
	7		0	0
	6		0	0
	5		0	0
	4		0	0
	3		0	0
	2		1	1
	1		1	1
	0		1	1
17-16	1	PLL_CTRL_BIT	0	0
	0		0	0
15	0	PLL_CPC	0	0
14-11	3	PLL_DIV	1	1

	2		0	0
	1		1	1
	0		1	1
10	0	TRAIN_CTR	0	0
9	0	SEQ_EXP_MODE	1	1
8	0	RAMP_CTR_DELAY_EN	0	0
7	0	DELAY_LOAD_E	0	0
6	0	ADC_CLK_GATE_EN	1	1
5	0	TOP_DIG_EN	1	1
4	0	BOT_DIG_EN	1	1
3	0	PIX_LDC_EN2	0	0
2	0	RAMP_DOWN_EN	0	0
1-0		NO USE		

Reading out the Sensor

LVDS Output

The GSENSE2011s sensor uses LVDS outputs to transport the image data to the surrounding system. In total there are 32 LVDS data pairs (DP) to output the image data. Next to the bottom left DPs, the sensor has one LVDS clock pair (CP) for the LVDS clock output which can be used to sample the image data. In total, GSENSE2011s has 33 LVDS output channels:

- 32 DPs
- 1 CP

LVDS Training

In order to synchronize the data from the DP in GSENSE2011s sensor, a known data pattern can be used as a reference on the output LVDS DPs. This reference pattern can be set by the user and used to “train” each LVDS receiver channel individually in the system. Such LVDS training is needed to avoid LVDS data misalignment due to the mismatch in the LVDS output channel design (both on chip and in electronic system).

Setting SPI register TRAIN_EN (Address<10>) to ‘1’ can make the sensor work in the training mode. In this mode, all DPs will output training pattern (Programmed through SPI register TRAIN_PATTERN (Address<125:114>).

For simplicity, the below example shows the training method of only four DPs. In GSENSE2011s, the maximum phase shift of different DPs is less than 3-bit (only the sensor part, the surrounding systems are not taken into account).

It is recommended to align all DPs to the DP which has a maximum delay (in the below figure, since the DP1 has the maximum delay, after word correction all DPs are aligned with DP1). The shift time (Tdelay0 to Tdelay31) of all

DPs should be recorded in this step. In GSENSE2011s, DP with pin OUTPB<15> and OUTNB<15> has the maximum delay.

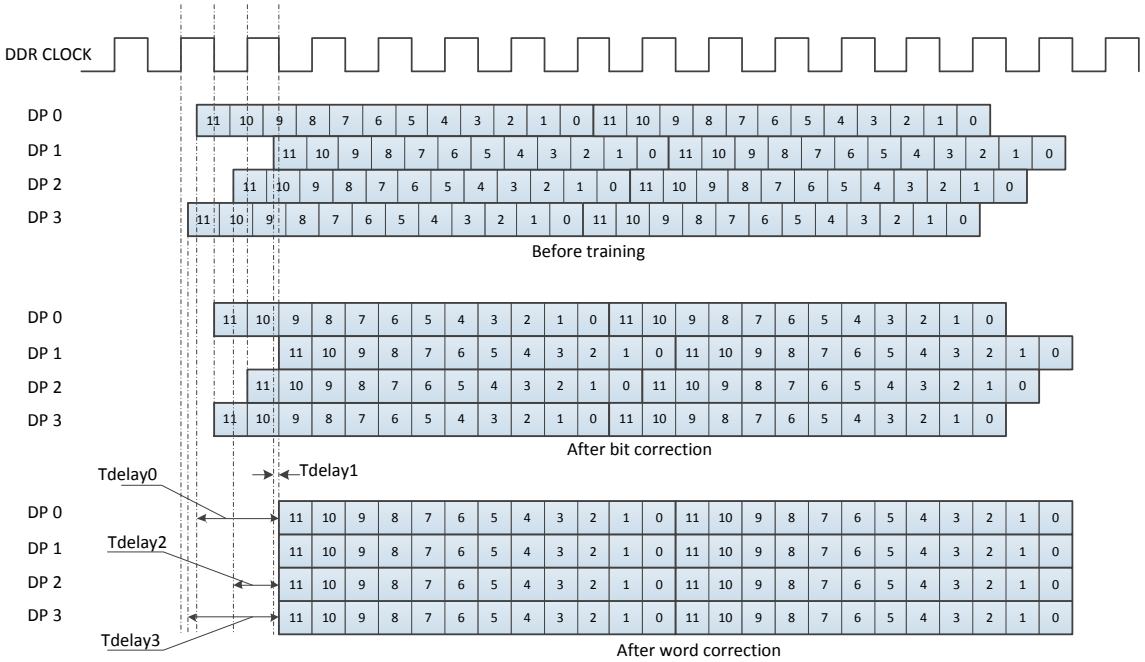


Figure 53: LVDS training

Data Receiving

In digital control signals, the SYNC is X-axis synchronization signal. The following figure illustrates the data receiving principle. As mentioned in "LVDS Training" section, a delay time "T_{delay}" should be taken into account. Compared to the rising edge of SYNC signal, the first effective column data appearing on the LVDS receiver has a delay T_{SYNC} calculated as:

$$T_{SYNC} = T_{delay} + T_{pixel\_clk}$$

Where T_{delay} is the same delay time measured in LVDS training procedure, T_{pixel_clk} is the period of one PIX_CLK cycle.

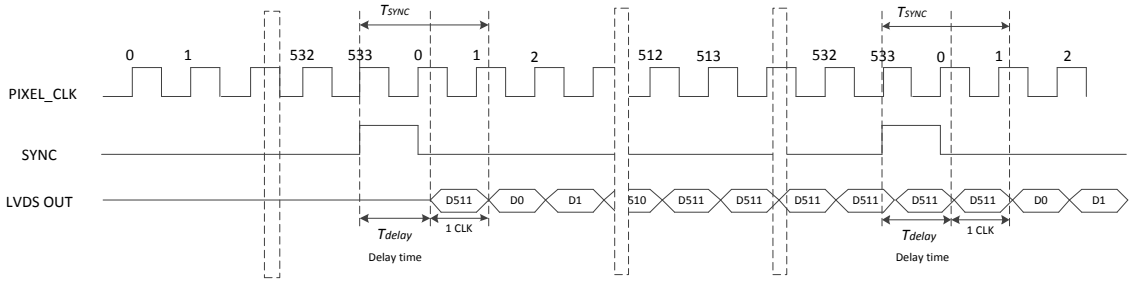


Figure 54：Data receiving for rolling shutter mode

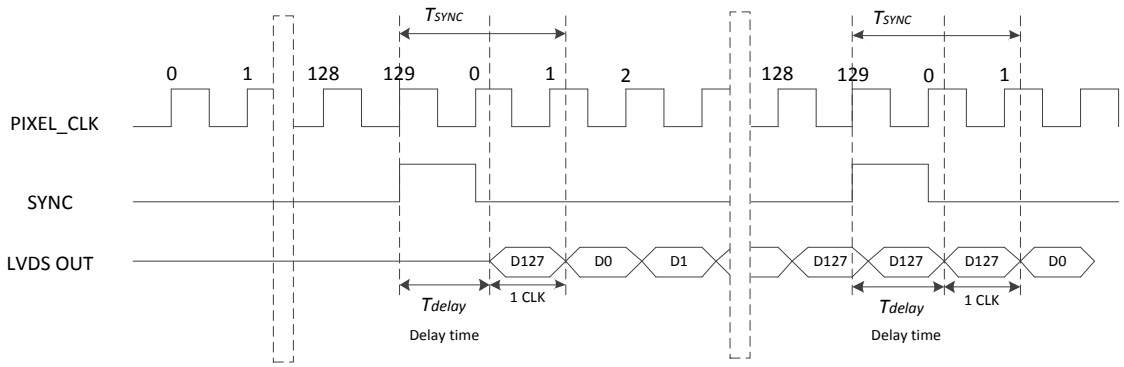


Figure 55: Data receiving for global shutter mode

Image Data Output Format

Rolling HDR Mode

Because of pipeline readout structure there is a delay between the pixel reading and data output.

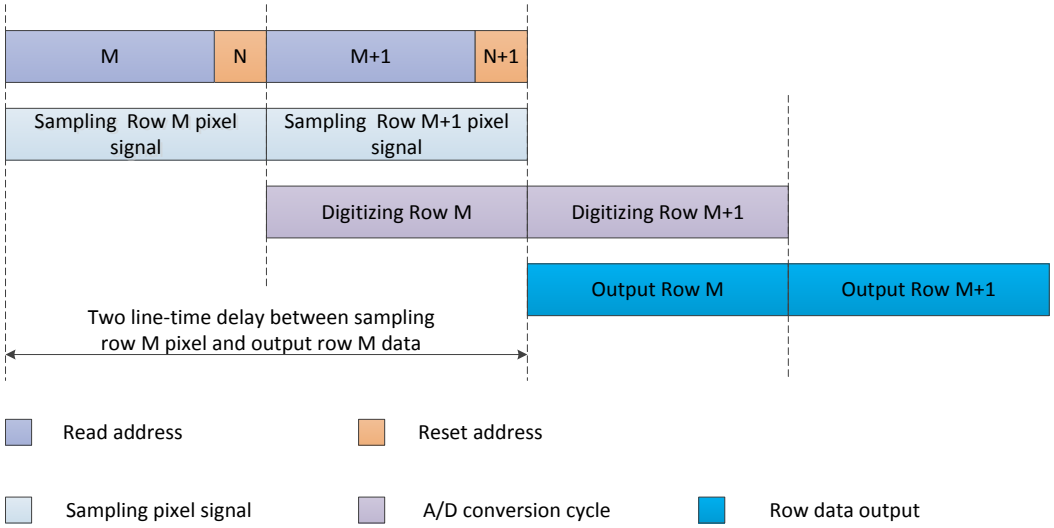


Figure 56: Pipeline readout structure in HDR mode

*Set exposure time to 2 lines.

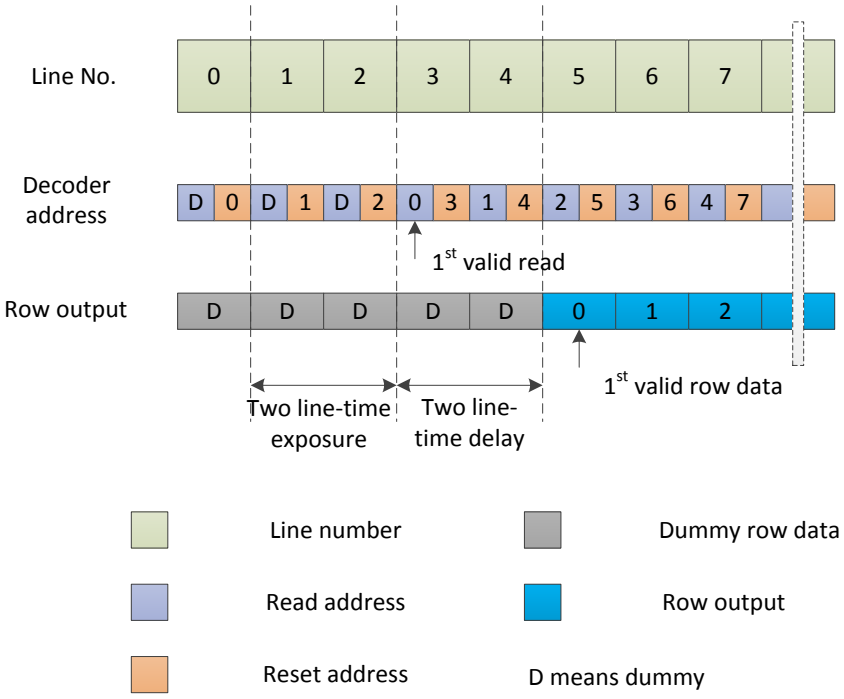


Figure 57: Delay between the first valid read address and the first valid data output

Figure 58: Data output of rolling HDR mode (Exposure time is set to two lines)

Global HDR Mode

Because of pipeline readout structure there is a delay between the pixel reading and data output. Figure 59 shows the relationship.

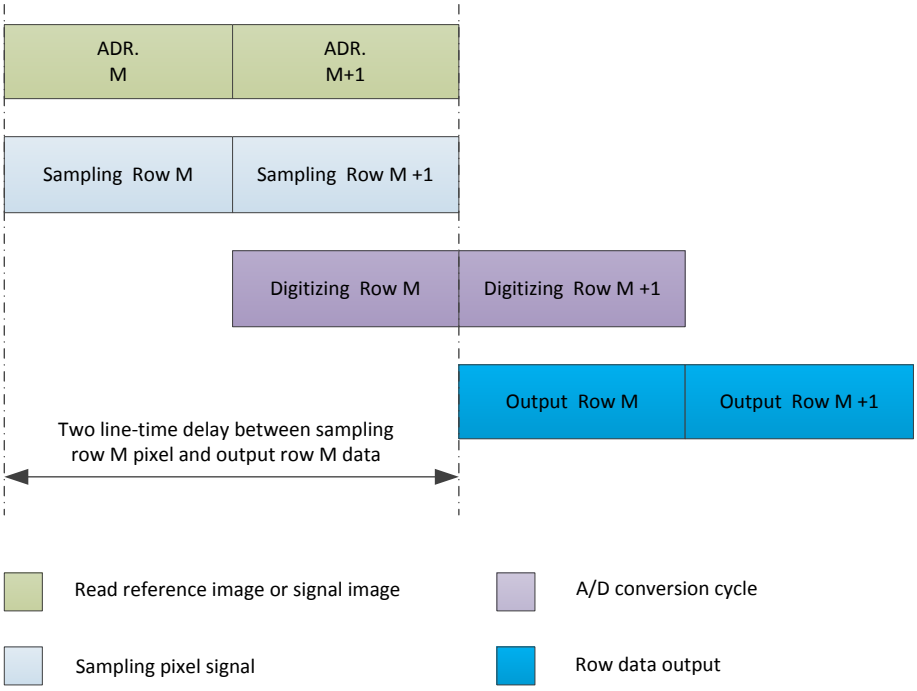


Figure 59: Pipeline readout structure in global shutter mode

Figure 60 illustrates the output data format of global shutter mode operation in state D mode. Top figure shows the row data output relationship with the decoder address. Bottom figure shows the pixel data output in each row time. Figure 61-63 shows the output data format of global shutter mode in state A, B and C respectively. Only the row data output vs. decoder address are shown as the pixel output sequence inside each row are the same with state D.

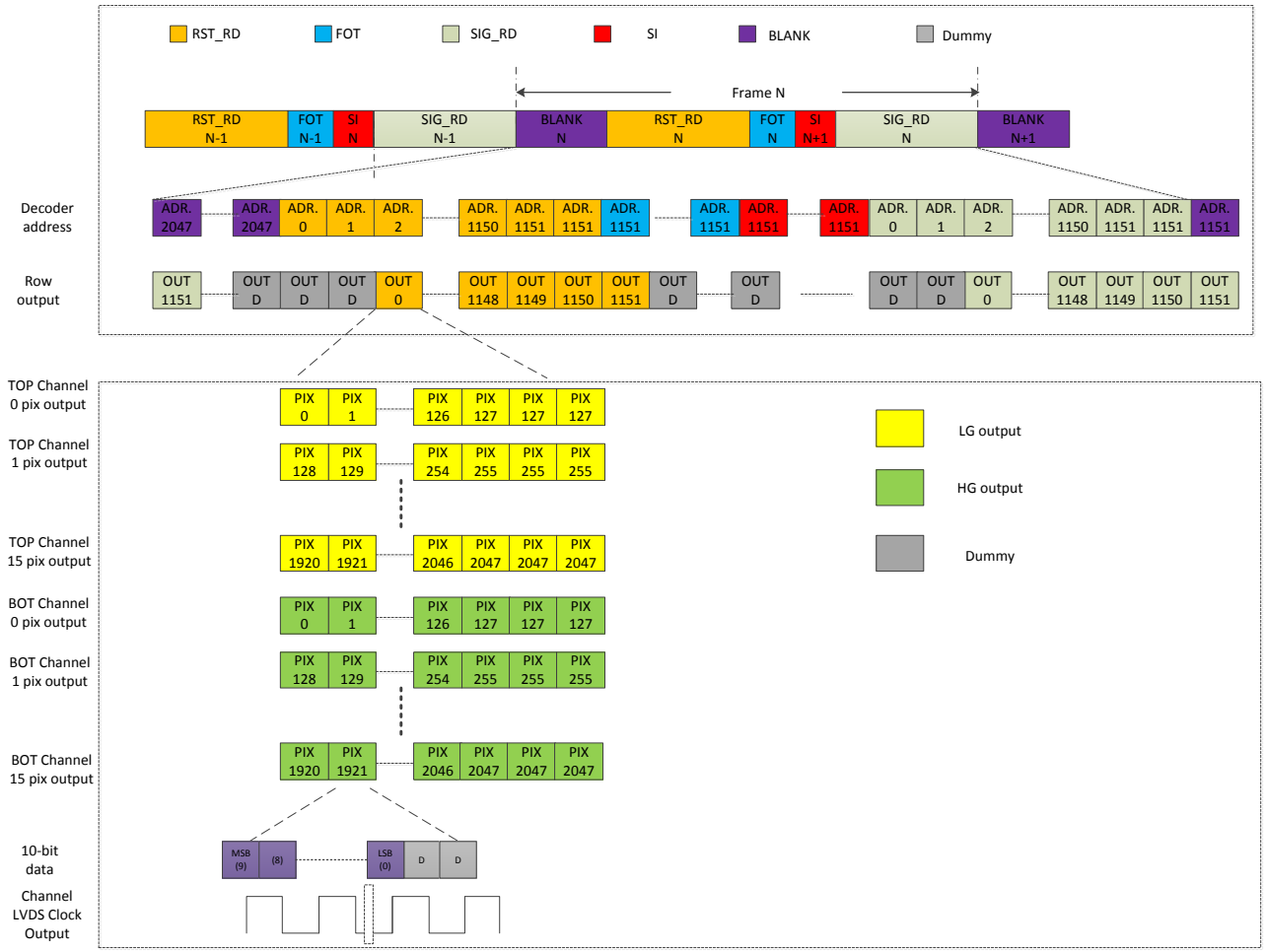


Figure 60: Data output of global HDR mode in state D

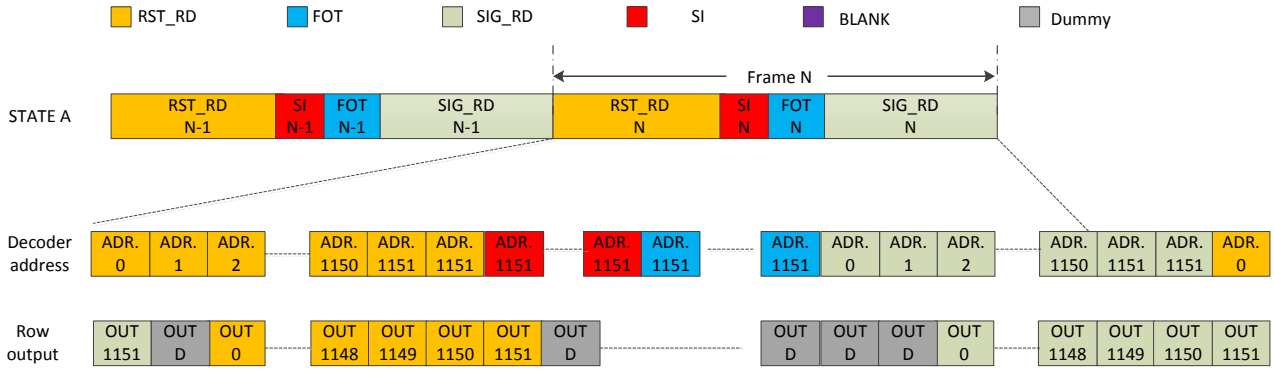


Figure 61: Data output of global HDR mode in state A

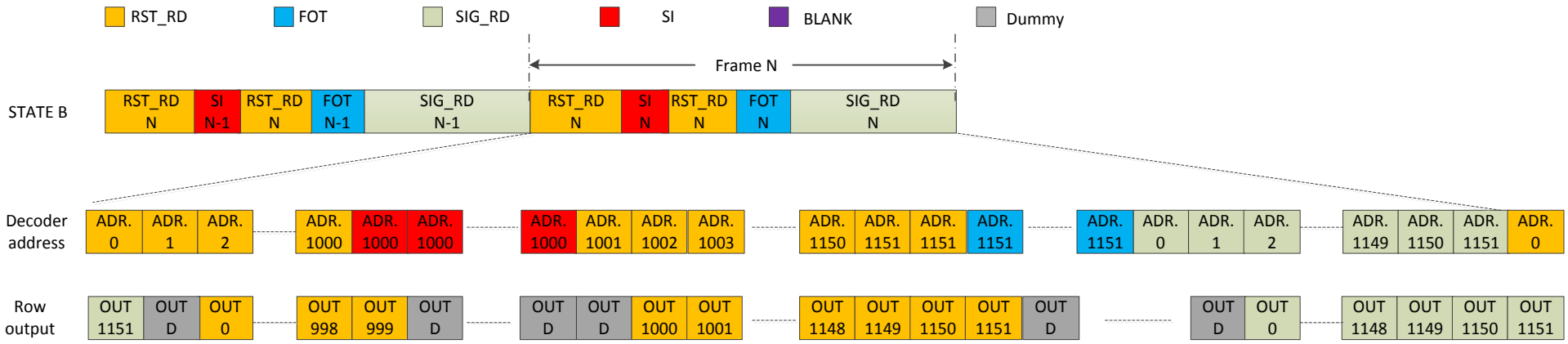


Figure 62: Data output of global HDR mode in state B

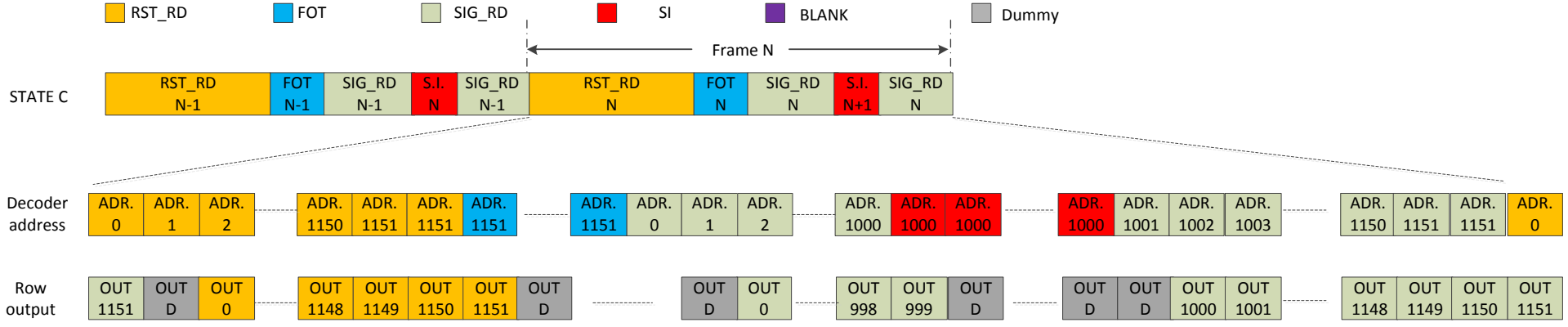


Figure 63: Data output of global HDR mode in state C

High Dynamic Range Image Construction

A high dynamic range image can be constructed by the low gain image and high gain image for HDR mode. A simple HDR image construction method is described in this document. The users can also choose other methods to combine the HDR image.

The method for a HDR image construction is basically according to the function below.

$$Y_{HDR} = \begin{cases} Y_H \ (Y_H \le T_H) \\ aY_L - b \ (Y_H > T_H) \end{cases}$$

Where

Item	Explanations
Y_{HDR}	Pixel output of the HDR image
Gain ratio	$a = \frac{K_H}{K_L}$
Compensation value	$\mathrm{b} = \frac{K_H}{K_L} O_L - O_H$
Y_H (DN) K_H (DN/e$^-$) O_H (DN)	Pixel output of high gain image Conversion factor for high gain image Black level offset of high gain image
Y_L (DN) K_L (DN/e$^-$) O_L (DN)	Pixel output of low gain image Conversion factor for low gain image Black level offset of low gain image
T_H (DN)	The threshold value for conversion between low gain image and high gain image

Construction method:

1) The response curves for low gain output and high gain output are obtained using the same optical condition.
2) The parameter *a* is calculated by the ratio of the slopes of the linear region of these two curves.

$$a = \frac{slope_{HG}}{slope_{LG}}$$

3) The parameter *b* is usually calculated by the black level offset of low gain image and high gain image.

$$b = offset_{LG} \cdot a - offset_{HG}$$

Note: The result by calculating this formula is absolute value of the compensation value $|b|$, this value would be minus for the HDR image construction.

4) The parameter TH (DN) is usually set to 3600 DN which is around the maximum value of the linear region of the response curve for high gain image.

Note:

1. When the difference between the PGA gain for low gain image and the high gain image is increased, the SNR dip will be larger, but the dynamic range of the HDR image will be enlarged. For gain adjustment description see the *gain adjustment function*. The figure below explains the SNR dip.
2. The parameter TH (DN) is usually set to 3600 DN at rolling HDR mode, and 400 DN at global HDR mode for this sensor.

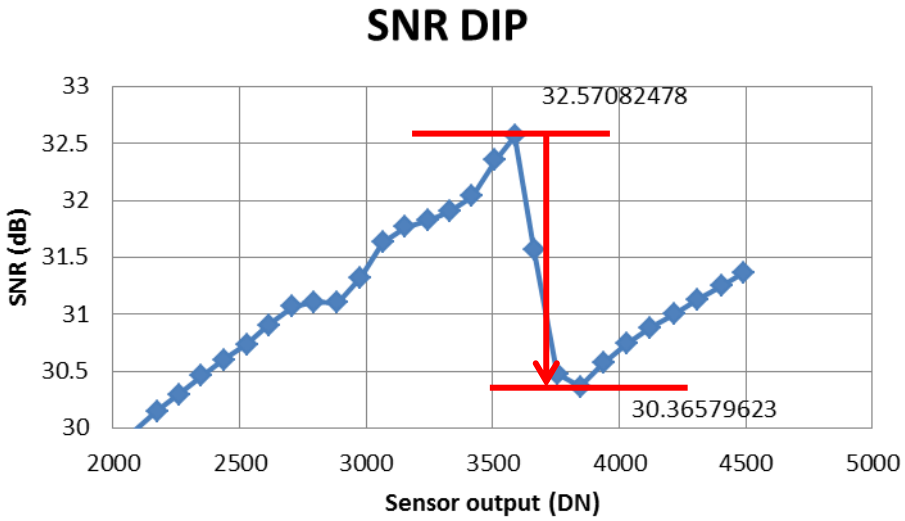


Figure 64: SNR dip

Description of Various Functions

Gain Adjustment Function

The PGA gain value of this sensor can be adjusted by the PGA_GAIN_BOT and PGA_GAIN_TOP register settings. The PGA gain for low gain image can be set by the PGA_GAIN_TOP register setting. The PGA gain for high gain image can be set by the PGA_GAIN_BOT register setting. The table below shows the register setting of PGA gain and the corresponding gain value.

PGA gain value	Address 137-132 or 131-126	Register setting
0.3162	000000	0
0.458	000001	1
0.501	000010	2
0.684	000100	4
0.8616	001000	8
0.9846	000011	3

0.9904	000101	5
1.0834	000110	6
1.228	001100	12
1.2474	001001	9
1.3644	001010	10
1.7766	001101	13
1.943	001110	14
2.126	000111	7
2.454	010000	16
2.676	001011	11
2.818	010100	20
2.99	011000	24
3.352	011100	28
3.548	010001	17
3.806	001111	15
3.878	010010	18
4.068	010101	21
4.32	011001	25
4.442	100000	32
4.446	010110	22
4.724	011010	26
4.802	100100	36
4.842	011101	29
4.976	101000	40
5.292	011110	30
5.334	101100	44
6.408	100001	33
6.536	110000	48
6.892	110100	52
6.924	100101	37
7.002	100010	34
7.06	111000	56
7.174	101001	41
7.418	111100	60
7.564	010011	19
7.564	100110	38
7.686	101101	45
7.836	101010	42
8.394	101110	46
8.662	010111	23
9.208	011011	27
9.404	110001	49

9.91	110101	53
10.154	111001	57
10.26	110010	50
10.3	011111	31
10.658	111101	61
10.816	110110	54
11.082	111010	58
11.63	111110	62
13.558	100011	35
14.62	100111	39
15.132	101011	43
16.18	101111	47
19.674	110011	51
20.68	110111	55
21.18	111011	59
22.18	111111	63

The table below shows the register address for the gain setting.

Address	Bit	Register Name	Description
137-132	5	PGA_GAIN_BOT	PGA gain setting for high gain readout chain
	4		
	3		
	2		
	1		
	0		
131-126	5	PGA_GAIN_TOP	PGA gain setting for low gain readout chain
	4		
	3		
	2		
	1		
	0		

ADC Gain Adjustment Function

The ADC gain value of the sensor can be adjusted by the ADC_GAIN register setting. The smaller the register setting value, the greater the gain is. The table below shows the register address for the ADC gain setting.

Address	Bit	Register Name	Description
243-238	5	ADC_GAIN	ADC gain setting
	4		
	3		
	2		
	1		
	0		

Black Level Adjustment Function

In rolling shutter mode, the black level offset can be adjusted by the DIG_10MSB_OFFSET($D_{15}D_{14}…D_7D_6$), DIG_6LSB_TOP_OFFSET($D_{5T}D_{4T}…D_{1T}D_{0T}$) and DIG_6LSB_BOT_OFFSET($D_{5B}D_{4B}…D_{1B}D_{0B}$) register settings.
D_7D_6 is constantly kept to ’10’. The black level for top(LG) and bottom(HG) readout is set with the following algorithm.

	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8						
+							D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
=	B_{13}	B_{12}	B_{11}	B_{10}	B_9	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0

The table below displays the register address for the black level offset.

Address	Bit	Register Name	Description
167-158	9	DIG_10MSB_OFFSET	10 MSB ADC count setting.Note that the low two bits should always be set to ‘10’
	8		
	7		
	6		
	5		
	4		
	3		
	2		
	1		
	0		
157-152	5	DIG_6LSB_TOP_OFFSET	6 LSB ADC count setting for top(LG) readout line
	4		
	3		
	2		
	1		
	0		
151-146	5	DIG_6LSB_BOT_OFFSET	6 LSB ADC count setting for bottom(HG) readout line
	4		
	3		
	2		
	1		
	0		

In global shutter mode, the black level is set by playing with the subtraction function in Figure 37. Register settings for DIG_10MSB_OFFSET ($D_{15}D_{14}…D_7D_6$), DIG_6LSB_TOP_OFFSET ($D_{5T}D_{4T}…D_{1T}D_{0T}$) and DIG_6LSB_BOT_OFFSET ($D_{5B}D_{4B}…D_{1B}D_{0B}$) should be kept to the default value.

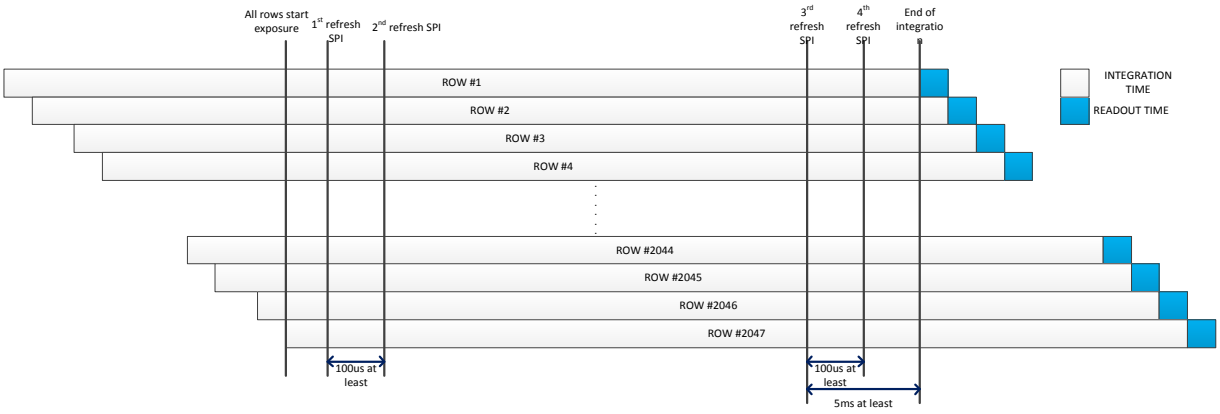
Low Dark Current Feature at Low Sensor Temperature

In rolling shutter mode, lower dark current mode can be achieved by switching off pixel supply during exposure, and then power it back immediately before sensor readout. This is done by SPI updating. Due to the limitation on SPI speed, a minimum of 100ms exposure time is recommended if this working mode is enabled.

The sequence of the SPI setting is shown below.

Sequence	Point in time	PIX_LDC_EN1 setting	PIX_LDC_EN2 setting	Remarks
1st	Start integration	0	0	Original state
2nd	After all rows start integration	1	0	The 1st time to refresh SPI setting
3rd		1	1	The 2nd time to refresh SPI setting
4th	5ms before end of the integration	1	0	The 3rd time to refresh SPI setting
5th		0	0	The 4th time to refresh SPI setting
6th	End of integration	0	0	Normal timing for read out
Note: Min. 100us time interval must be kept between each refresh of SPI.				

The diagram below explains this operation in more details.



When GSENSE2011s is working in this mode, the voltage of supply VDDPIX_LDC is set to 0.8V.

The measurement result for dark current versus chip temperature is shown in the graph below.

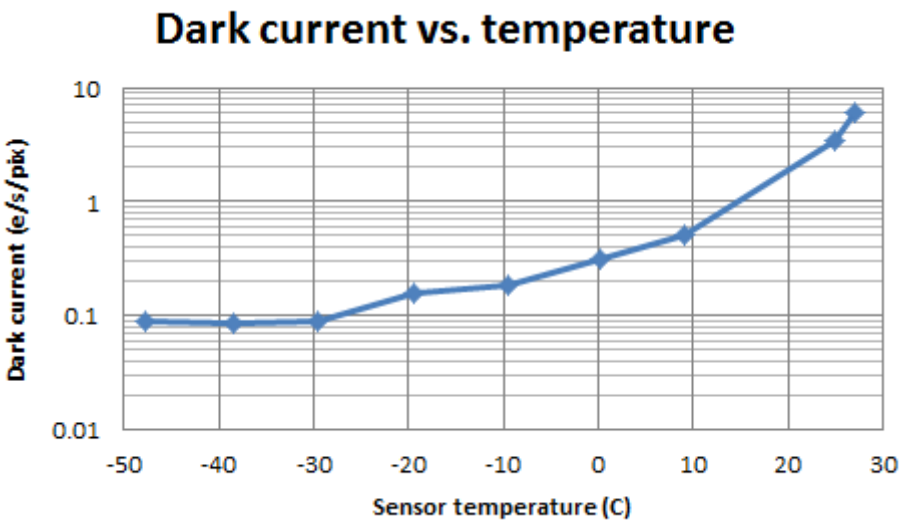


Figure 65: Dark current vs. sensor temperature

Image Inverted Operation

The sensor readout in vertical direction (normal/inverted) can be switched by the DIRECTION_11BIT register setting. Register address for image inverted operation is shown in the table below.

Address	Bit	Register Name	Description
94	0	DIRECTION_11BIT	Readout direction setting 1: normal operation 0: invert operation

The figure below shows the normal and inverted readout operation in vertical direction. (TOP VIEW)

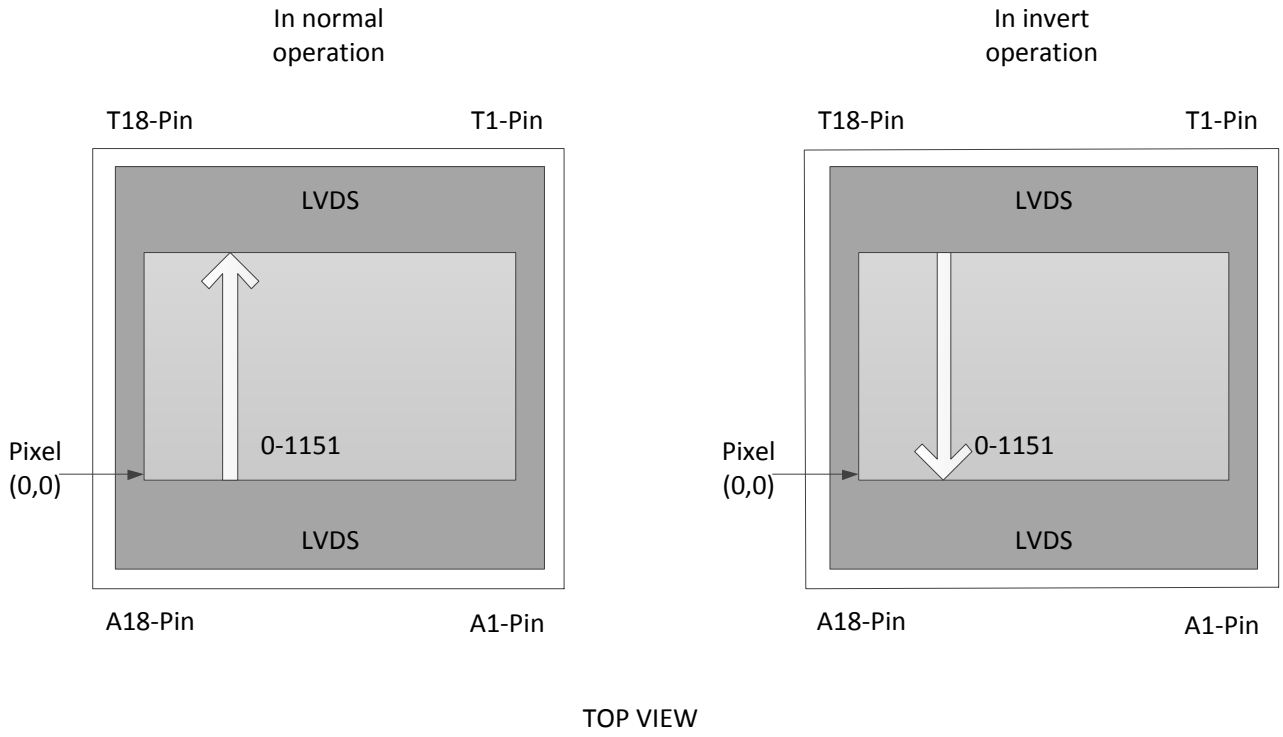


Figure 66: Normal and inverted readout operation in vertical direction (TOP VIEW)

Windowing Operation

To limit the amount of data, windowing in vertical direction is possible. The number of lines and start address can be set for the windowing operation. The figure below shows the windowing operation.

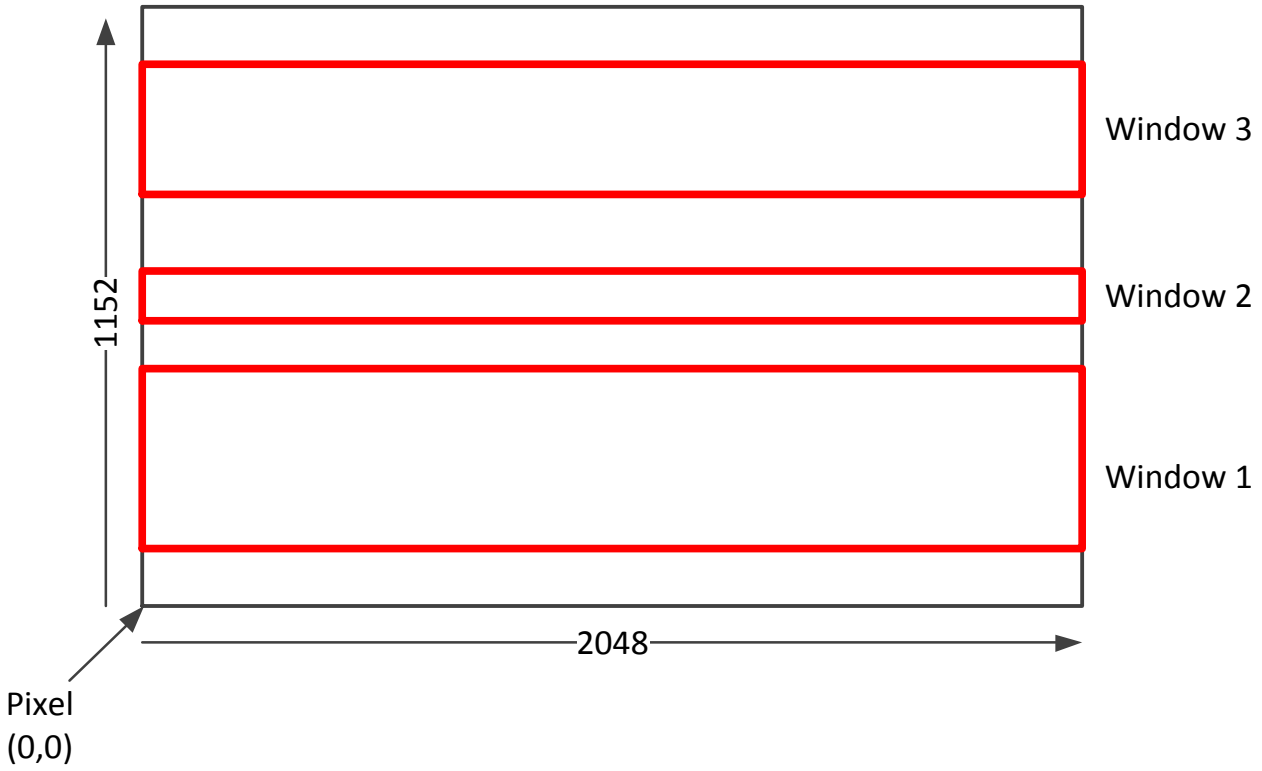


Figure 67: The windowing operation

Black Sun Calibration Function

The sensor supports a black sun calibration function. This function is already switched on by default settings.

Temperature Sensor

There is a temperature sensor integrated in the sensor in order to obtain the temperature of the sensor. An example for the output of this temperature sensor (DN) versus the chip temperature is shown in the graph below. The temperature of the sensor is usually obtained by using this fit line.

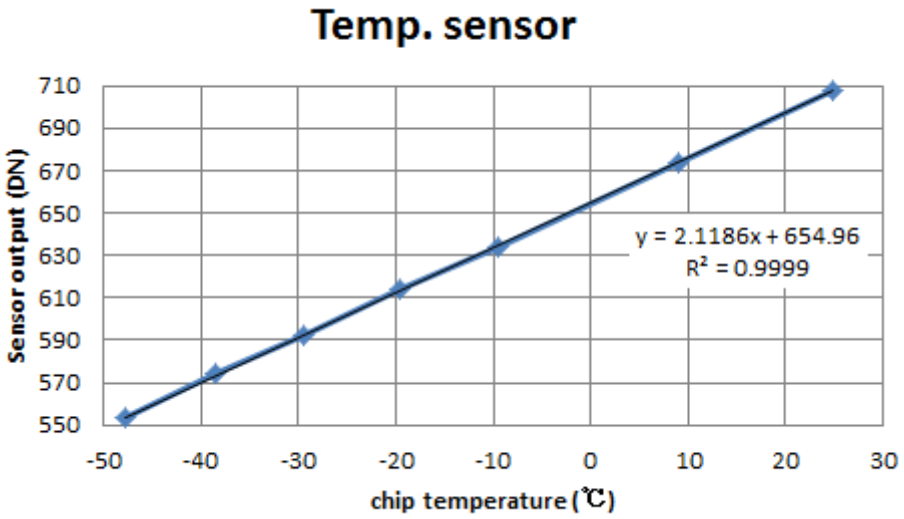


Figure 68: Temperature sensor

Note: The fitting of the temperature output curve may be slightly different from sensor to sensor, the user is advised to do individual characterization of the temperature sensor on each sensor for best accuracy.

Blemish Specification

Test Images

- The test images are generated using GSENSE2011s evaluation system with a light source of uniformity better than 98%. GSENSE2011s is configured in Rolling shutter HDR 12bit mode with default settings
- Test images of “Dark”, ”Grey”, and “Saturation” are generated by averaging a certain number of images taken at dark, half-saturation and saturation conditions. With each exposure, one image in the HG channel and one image in the LG channel are grabbed. No image correction algorithm is applied.
- Three images of “Half-saturation images in HG and LG channels” and “saturation image” are constructed from the test images, and used for blemish definition.

The table below explains the imaging conditions for the test images and the three constructed images.

Image Level	Definition
Dark	In dark environment and with exposure time of 1 line time, 20 images are grabbed and averaged, for HG and LG channel individually.
Grey	20 images at half-saturation are grabbed and averaged, for HG and LG channel individually.
Saturation	20 images at saturation are grabbed and averaged, for LG channel only
Half-saturation images in HG and LG channels	The half-saturation image for HG channel is constructed by subtracting the HG Dark image from the HG Grey image, and the half-saturation image for LG channel is constructed by subtracting the LG Dark image from the LG Grey image.
Saturation image	Saturation images is constructed by subtracting the LG Dark image from the LG Grey image

Blemish Definitions

The table below explains the definition of blemishes.

Defect Name	Detail
Bad pixel in half-saturation images	Any pixel deviates more than 15% from the mean value of the half-saturation images (either HG or LG channel)
Bad pixel in saturation image	Any pixel deviates more than 10% from the mean value of the saturation image (LG channel)
Total defect pixels	The total number of non-overlapping bad pixels in half-saturation images and in saturation image
Cluster	The defect pixels that are adjacent (horizontal, vertical or diagonal) are considered a cluster.
Cluster (3x3)	Any cluster with size of 2-9 pixels is considered cluster (3x3).
Cluster (5x5)	Any cluster with size of 10-25 pixels is considered cluster (5x5).
Defect Row	Any row with its mean value deviating more than 5% from the mean value of the

	half-saturation images (either HG or LG channel) Any row with its mean value deviating more than 5% from saturation image of the LG channel; Or a row with more than 100 defect pixels;
Defect Column	Any column with its mean value deviating more than 5% from the mean value of the half-saturation images (either HG or LG channel) Any column with its mean value deviating more than 5% from saturation image of the LG channel; Or a column with more than 100 defect pixels.

Defect limits

Maximum allowed defect levels are indicated below.

Item	GSENSE2011s	
	Grade 1	Grade 2
Defect pixel	30	80
Cluster (3x3)	0	2
Cluster (5x5)	0	1
Cluster (>5x5)*	0	0
Defect row/column (total)	0	3
2 Adjacent rows/columns (total)	0	0
>2 Adjacent rows/columns (total)	0	0

* Any cluster with size >25 pixels is considered cluster (>5x5).

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Publication Ordering Information

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