



Optimization of thermo-optic phase-shifter design and mitigation of thermal crosstalk on the SOI platform

MAXIME JACQUES,^{1,*} ALIREZA SAMANI,¹ ESLAM EL-FIKY,^{1,2} DAVID PATEL,¹ ZHENPING XING,¹ AND DAVID V. PLANT¹

¹Department of Electrical and Computer Engineering, McGill University, Montreal, H3A 0E9, Canada

²Electrical Engineering Department, Alexandria University, Alexandria, 21544, Egypt

*maxime.jacques@mail.mcgill.ca

Abstract: We first optimize the design and compare the performance of thermo-optic phase-shifters based on TiN metal and N₊₊ doped silicon, in the same SOI process. The designs don't require special material processing, show negligible loss, and have very stable power consumption. The optimum TiN design has a switching power $P_{\pi} = 21.4$ mW and a time constant $\tau = 5.6$ μ s, whereas $P_{\pi} = 22.8$ mW and $\tau = 2.2$ μ s for the best N₊₊ Si design, enabling 2.5x faster switching compared to the metal heater. Doped-Si-based heaters are therefore the most practical and efficient on standard SOI. In addition, to optimize the layout density of highly integrated dies, we experimentally characterize internal and external thermal crosstalk for tunable Mach-Zehnder interferometers (MZIs) based on both heater designs for various power, distances, and etching patterns. Deep trenches are the best structures not involving special fabrication techniques to mitigate heat leakage affecting phase-sensitive devices close to heaters. Given the numerous applications of thermal tuners, this work is relevant to almost all silicon photonics designers.

© 2019 Optical Society of America under the terms of the [OSA Open Access Publishing Agreement](#)

1. Introduction

Integrated thermo-optic phase-shifters (TOPS), or optical waveguide heaters, have become widely employed in applications ranging from sensing to switching, advanced communications and neural networks [1–4], and on various platforms [5,6]. On silicon-on-insulator (SOI), increasingly popular for its compact devices, large wafers, low cost, high yields and complementary metal oxide semiconductor (CMOS) compatibility [7,8], heaters are now routinely embedded in the design of more complex devices and sub-systems such as ring resonators/modulators [9,10], Mach-Zehnder interferometers (MZIs) and Mach-Zehnder modulator (MZM) arrays [11]. Active ring-based devices typically have small footprint and low power consumption, and several SOI TOPS designs targeted at these devices were proposed lately [12–18]. However, the wavelength selectivity, thermal sensitivity and poor fabrication tolerance of ring structures explain why MZI-based (or other interferometric) designs are often preferred [19].

A summary of recently published SOI TOPS designs embedded in interferometric structures is presented in Table 1 [19–24]. MI and MZI are respectively Michelson and Mach-Zehnder interferometers, V_{π} and P_{π} are the voltage and electrical power leading to the temperature change ΔT_{π} required in the optical waveguide for a π -shift, and τ is the $1/e$ limiting time constant of heat diffusion (rise or fall). The figure of merit (FOM) $P_{\pi} \cdot \tau$, to be minimized, is accepted as a global heater performance measure [19,20]. The two best published designs in terms of this FOM employ respectively a doped-Si heater embedded directly in the optical waveguide [19] and a metal heater with substrate undercut [23]. However, undercuts are usually not part of standard processes or imply extra cost, same for the silicidation used in [22].

Moreover, TOPS designs based on direct doping of the Si waveguide [19,20] involve optical attenuation, which is a significant problem if several switches are cascaded, such as in switch networks.

Table 1. Recent SOI Thermo-Optic Phase-Shifters Implemented in Interferometric Structures

	Foundry	Heater	Tuned device	Cladding	Under-cut	L [μm]	Loss [dB]	P_π [mW]	V_π [V]	τ^b [μs]	$P_\pi \cdot \tau$ [mW · μs]
[21]	IME ^a	Ti	MI	oxide	no	~600	-	10.6	4.9	15.9	168.2
[22]	IBM	NiSi	MZI	air	no	200	5	20	1	2.8	56
[23]	IME ^a	TiN	MZI	air	yes	1000	0.3	0.5	0.9	65.5	32.1
[19]	Sandia ^a	N Si	MZI	air	no	>9.4	0.5	12.7	12.0	2.4	30.5
[20]	OpSIS	P Si	MZI	SiO ₂	no	61.6	0.23	24.8	4.4	2.7	66.9
[24]	IME	N ₊₊ Si	MZI	SiO ₂	no	~120	-	25	0.6	2.3	56.8

^aAssumed from reference. ^bWe used $\tau = \tau_{10\%-90\%} / 2.2$ and $\tau = 0.35 / f_{3dB}$ when necessary.

Thus, the practical TOPS designs on SOI, i.e., low-cost and not involving waveguide doping, can be split into two main groups: those based on a metal heater layer above the waveguide [21,23], and those based on doped-Si strips laid out on both sides of the waveguide [24]. Unfortunately, since the designs reported in Table 1 were built at different foundries, implying different materials, layer thickness and doping levels, it is not clear which of the two approaches performs best. This question has partly been studied in [25] for the IMEC SOI process, however the designs are not optimized, and the doped-Si heater is lossy due to waveguide doping.

At the die level, the higher density of recent SOI photonic integrated circuits (PICs), such as advanced transceivers for digital communications [3], makes them more sensitive to heater thermal leakage [6]. Although thermal crosstalk on SOI has partly been studied in [13,20,21], we have not found a comparison of crosstalk between different heater types, nor across the different etches and trenches available in standard CMOS.

In this paper, we first optimize metal-based (TiN) and doped-Si based (N₊₊ Si) TOPS designs with thermal and optical simulations based on the finite element method (FEM). We then experimentally compare their performance at DC and for switching. Both TOPS designs are fabricated on the same die in the IME process (now AMF), and neither requires special fabrication steps such as undercuts, post-processing or small feature size. We also measure the thermal crosstalk between the two arms of a MZI switch for both TOPS types, for various heater powers and various pitches between the arms. Furthermore, we compare the thermal isolation provided by the default cladding oxide, cladding etches and deep trenches, by measuring the crosstalk between an aggressor heater and a nearby victim MZI, again for various power levels and aggressor-victim gaps. This paper thus reports comprehensively on heater design optimization and crosstalk mitigation on a standard SOI process, which to the best of our knowledge had not been presented in the literature.

2. Heater design

2.1 Theory

We start with a brief review of core concepts guiding heater design. Based on [19], to define heater efficiency and speed, we have $P_\pi = \Delta T_\pi G$, where G is the thermal conductance between the heated waveguide and the heat sink (Si substrate), and $\tau = H / G$, where H is the heat capacity of the heated arm. However, the formulas should include the area A traversed by the heat flow, i.e. the waveguide cross-section perpendicular to heat flux:

$$P_\pi = \Delta T_\pi \cdot G \cdot A, \quad (1)$$

$$\tau = H / (G \cdot A), \quad (2)$$

where G is in, [W/m²·K], A is in [m²] and H is in [J/K]. Note that these formulas neglect any gap or finite thermal conductance between the heat source and the waveguide. While a gap may be used to avoid optical loss through metal or carrier absorption, the conductance between the heater and waveguide should always be maximized. If efficiency and speed are the main heater metrics to be co-optimized, it is readily seen from Eqs. (1) and (2) that

$$\text{FOM} = P_\pi \cdot \tau = \Delta T_\pi \cdot H \quad (3)$$

is a fit choice of figure of merit, since it accounts for the opposite impact of G on both metrics. For example, as seen in Table 1 [23], substrate undercuts can drastically improve P_π via a substantial decrease of G , but at the expense of a proportionally larger τ . To detail Eq. (3) further, the temperature-dependent phase change in the heated waveguide is:

$$\Delta\Phi = \frac{2\pi L}{\lambda_0} \frac{dn}{dT} \Delta T, \quad (4)$$

where L is the TOPS length, λ_0 is the free-space wavelength, dn/dT is the thermo-optic coefficient, ~1.8E-04 K⁻¹ at $\lambda_0 = 1550$ nm and T = 300 K for silicon [26], and ΔT is the temperature change. Therefore, for a π phase shift we have:

$$\Delta T_\pi = \frac{\lambda_0}{2L dn/dT}. \quad (5)$$

Increasing L effectively lowers ΔT_π , which reduces lateral crosstalk. However the device footprint, propagation loss and V_π all increase proportionally to L (assuming the TOPS resistance $R_{eq.,TOPS} \propto L$). Therefore, in practice L is usually made small. Importantly, note from Eqs. (1) and (2) that in theory L impacts neither P_π nor τ , since in general both A and H are $\propto L$. In addition, since dn/dT is a fixed material property, the only way to truly improve the heater FOM in Eq. (3) is to reduce the heat capacity H , or in other words to decrease the thermal energy required to increase the waveguide temperature [19]. This is typically achieved by bringing the heat source as close as possible to the waveguide while limiting optical loss, especially if a low thermal conductivity material (oxide) separates the resistor and waveguide. Finally, the resistive conductors available on SOI are usually limited to one dedicated metal layer and doped silicon. Both are compared in Section 2.2.

2.2 FEM simulations

A cross-sectional view of the two configurations, i.e. metal and doped-Si resistors, are shown in Fig. 1(a) [14,16]. In both cases, the current flow is through the page, parallel to the waveguide. Since we exclude TOPS designs involving direct doping of the waveguide due to cascaded optical losses, as mentioned in introduction, Fig. 1(a) is a rather general picture of ‘lossless’ heater implementation on SOI. In our simulations and experiments, the buried oxide (BOX) thickness is 2 μm. The material for the BOX and cladding is SiO₂.

The heater metal is titanium nitride (TiN), and is located 2 μm above the Si strip waveguide [23]. The strip waveguide height and width are 220 nm and 500 nm to support a single TE mode at $\lambda_0 = 1550$ nm. For the doped-Si heater, a 90 nm high Si slab is added to create a rib waveguide structure and connect it to the N₊₊ Si resistors on either side, which also have to be defined on 90 nm Si. The rib structure improves heater efficiency, as the thermal conductivity of silicon

(148 W/m·K) is much higher than that of SiO₂ (~1.4 W/m·K) [15]. Note that all height values are constrained here by the fabrication process, but different Si slab heights could allow for further design optimization [15]. For the N₊₊ Si design, a 0.8 μm wide lateral buffer between the waveguide and the resistors is used to prevent free-carrier absorption of light. The strongest doping concentration available, 1E20 cm⁻³ [27], is chosen to reduce electrical resistance and for better ohmic heating [24]. The choice of N (phosphorus) versus P (boron) doping for the resistors is arbitrary since their specific heat is not expected to differ significantly. For both the TiN and N₊₊ Si heaters, the resistor width is the smallest allowed by fabrication: 2.0 μm for the TiN strip and 1.0 μm for each doped-Si strip. The TOPS total lengths L is arbitrarily set to 320 μm, and should impact neither P_π nor τ as discussed in Section 2.1.

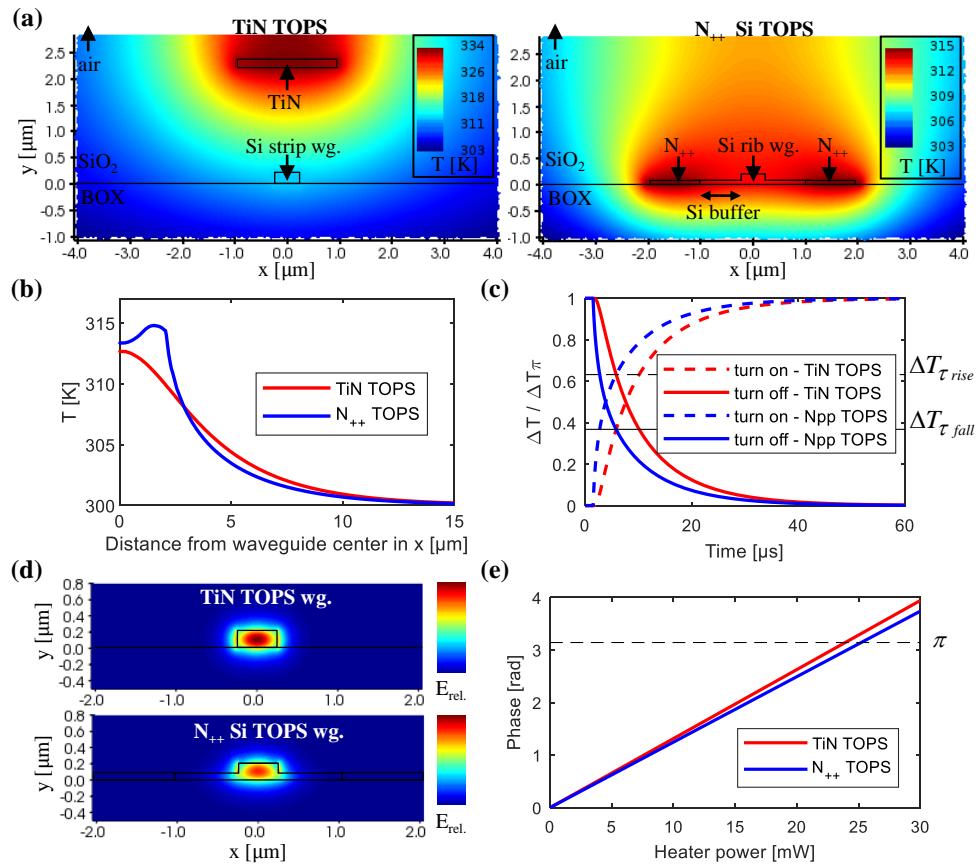


Fig. 1. Thermal and optical simulation of the TiN and N₊₊ Si designs with the finite element method (FEM). (a) Temperature distribution at P_π for both heaters. 23.9 mW is applied on the TiN resistor (left) and 25.2 mW in total is applied on the N₊₊ Si resistors (right). (b) Temperature at P_π as a function of lateral distance, at mid-waveguide height ($y = 0.11 \mu\text{m}$). (c) Transient analysis: temperature vs. time at the waveguide core for heater power turn-on and turn-off ($0 \rightarrow P_\pi$ and $P_\pi \rightarrow 0$). Dashed and full lines represent $1/e$ temperature changes for turn-on and turn-off. (d) Optical E field distribution (relative amplitude) for the fundamental mode at $\lambda_0 = 1550 \text{ nm}$ in the TiN (top) and N₊₊ Si (bottom) designs. (e) Optical phase vs. total heater power for a 320 μm long TOPS.

The cross-section of the TiN-based and the N₊₊ Si-based TOPS designs are simulated with the combination of a thermal solver and an optical mode solver in Lumerical Device, to

compare their heat distribution, efficiency and transient response. The thermal and optical FEM engines respectively solve the Heat Diffusion equation in a wide area ($40 \mu\text{m}$ wide $\times 18 \mu\text{m}$ high) around the heater, and Maxwell's equations at $\lambda_0 = 1550 \text{ nm}$ in the optical waveguide area. The temperature at the bottom of the thermal simulation region (in the Si substrate) is fixed to the ambient temperature of 300 K , and fixed convection of $10 \text{ W/m}^2\text{-K}$ is defined between the oxide layer and air above it. The thermal and electromagnetic properties used for the different materials and layer thicknesses are listed in Table 3 in Appendix [28–38]. Key parameters include the strong dependence of the silicon thermal conductivity on layer thickness and doping, and free carrier dispersion and absorption in doped-Si. For each TOPS design, the simulation procedure is as follows:

1. With solvers in steady-state and mesh locked, sweep heater power $P_{el.}$ and record the temperature change profile $\Delta T_{wg}(x, y, P_{el.})$ in the waveguide cross-section.
2. With dn/dT_{Si} , convert to index perturbation: $\Delta T_{wg}(x, y, P_{el.}) \rightarrow \Delta n_{wg}(x, y, P_{el.})$.
3. Solve for the fundamental mode index $\Delta n_{eff}(P_{el.})$; convert to phase shift with Eq. (4).
4. Retrieve P_π from Step 3 and set the heater to this power. Turn heater on/off with heat solver in transient mode, and retrieve $\Delta T(t)$ in the waveguide center to extract τ .

For the TiN design, a single rectangular temperature monitor covering the strip waveguide was used to simulate the thermo-optic effect. For the N₊₊ Si design, two additional monitors overlapping the adjacent 90-nm-high Si slab sections were added.

Results are summarized in Figs. 1(a)–1(e). In Fig. 1(a), the temperature distribution is shown at P_π for both heaters. A temperature shift $\Delta T \approx +13^\circ \text{K}$ in the waveguide core is necessary in both designs to induce a π shift over a $320 \mu\text{m}$ length. However, at P_π , the TiN resistor reaches a much higher temperature than the N₊₊ Si resistors, because of its greater distance from the waveguide and bad oxide thermal conductivity. In Fig. 1(b), we show the lateral heat distribution at P_π and $y = 0.11 \mu\text{m}$ (mid-waveguide height) for both heaters. The two designs show a similar thermal decay profile, with substantial residual heat $>10 \mu\text{m}$ away from the waveguide center. The corresponding crosstalk induced in waveguides laid out at various distances from the heater is studied experimentally in Section 3.1. In Fig. 1(c), the simulated transient response of both heaters is shown. The limiting $1/e$ time constants are $\sim 10.2 \mu\text{s}$ and $\sim 5.8 \mu\text{s}$ for the TiN and N₊₊ Si designs respectively. For each, the rise and fall times are similar. The faster response of the N₊₊ Si TOPS is due to the proximity of the heat source and the waveguide: a more compact design decreases the heated arm heat capacity H and therefore τ , per Eq. (2). The fundamental TE mode at $\lambda_0 = 1550 \text{ nm}$ in the strip and rib waveguides of the TiN and N₊₊ Si designs are shown in Fig. 1(d). The relatively tight optical confinement and the weak thermo-optic coefficient of silica, $\partial n/\partial T_{SiO_2} = 1.0E-05 \text{ K}^{-1}$ [15], ~ 18 times weaker than silicon, justify neglecting the thermo-optic effect in the cladding in our simulations. We also retrieve from optical simulations the complex effective index $n = n + i\kappa$. The attenuation, $\alpha = 4\pi\kappa/\lambda_0$ [39], where λ_0 is the free-space wavelength, is found to be negligible for the TiN design ($\alpha \approx 0$), meaning the metal is high enough above the waveguide. However, $\alpha = 0.26 \text{ dB/cm}$ for the N₊₊ Si design, which translates to a small $\sim 0.008 \text{ dB}$ loss for a $320 \mu\text{m}$ long TOPS. Finally, in Fig. 1(e), the optical phase versus heater power is shown for the TiN and N₊₊ Si designs. The extracted P_π are 23.9 mW and 25.5 mW respectively, in the same range as literature measurements for metal-based [40] and doped-Si-based [20,24] designs. In

addition to geometry, the lower specific heat of TiN (598 J/kg·K) versus Si (711 J/kg·K) also explains its slightly better efficiency.

We now investigate the impact of resistor width on the performance of the designs. Figures 2(a)–2(c) show the efficiency, time constant (at P_π) and heater FOM from Eq. (3) for different resistive TiN and N₊₊ Si strip widths. The efficiency of both designs intuitively decreases as the resistor width increases, due to a larger fraction of the heat being diffused inefficiently. However, for both designs the lowest time constant is achieved for a total resistive width of 2.5 μm, or +0.5 μm versus the minimum widths allowed by fabrication. In terms of the FOM, the optimal TiN strip width is 2.5 μm, and the optimal width of each N₊₊ Si strip is 1.0 μm. The FOM is significantly better for the N₊₊ Si design compared to the TiN design, due to its considerably faster response.

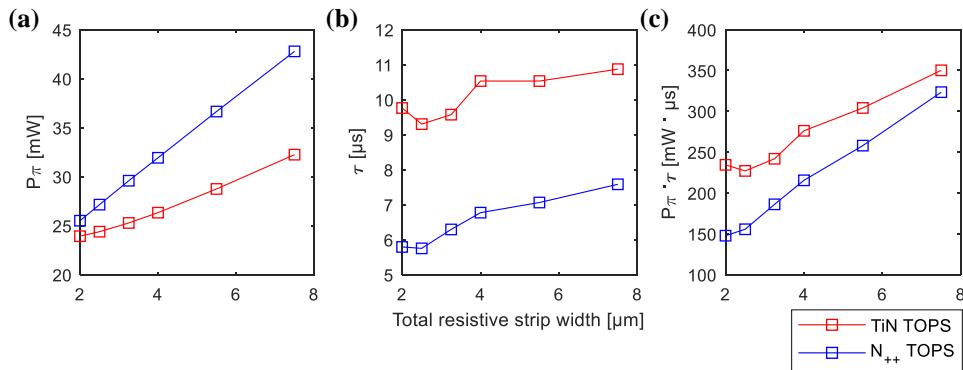


Fig. 2. Simulated impact of resistor width on the performance of both TOPS designs. (a) Switching power P_π , (b) limiting time constant τ ($0 \rightarrow P_\pi$ or $P_\pi \rightarrow 0$), and (c) $P_\pi \cdot \tau$ FOM vs. total resistive strip width (sum of the 2 strips for the N₊₊ Si design).

To finalize the optimization of the N₊₊ Si TOPS design, the last handle available is the width of the intrinsic silicon slab buffer between the heaters and the waveguide, W_{buffer} , shown in Fig. 1(a). The efficiency, optical loss, limiting time constant and heater FOM as a function of W_{buffer} are shown in Figs. 3(a)–3(d). In Figs. 3(a) and 3(b), P_π and τ expectedly decrease as W_{buffer} decreases and the heaters are brought closer to the waveguide. However, as seen in Fig. 3(c), decreasing W_{buffer} also drastically increases loss. This was expected from Fig. 1(d), where the optical field almost reaches the highly-doped (highly-attenuating) heater regions when $W_{buffer} = 0.8\mu\text{m}$. Considering the FOM/loss tradeoff just described, we propose a modified, more complete figure of merit for heater design:

$$\text{FOM}_{mod} = P_\pi \cdot \tau / I_r = \Delta T_\pi \cdot H / e^{-\alpha L}, \quad [\text{mW} \cdot \mu\text{s}] \quad (6)$$

where $I_r = I_{out} / I_{in} = e^{-\alpha L}$ is the relative optical intensity after propagation in the TOPS. FOM_{mod} must also be minimized. This figure of merit is similar to the one reported in [41] for the evaluation of switches. Note that in the case of negligible attenuation ($\alpha \rightarrow 0$), FOM_{mod} reduces to FOM from Eq. (3). Both figures of merit are plotted in Fig. 3(d). Whereas FOM suggests that W_{buffer} should be reduced to increase performance, FOM_{mod} shows that the optimal width is $W_{buffer} = 0.6\mu\text{m}$. This design would allow for optimal P_π and τ while limiting attenuation below 2.9 dB/cm (~0.09 dB for a 320 μm long TOPS). Note that since α is very small for $W_{buffer} > 0.8\mu\text{m}$, FOM_{mod} is expected to grow monotonically, i.e., get worse, past that point.

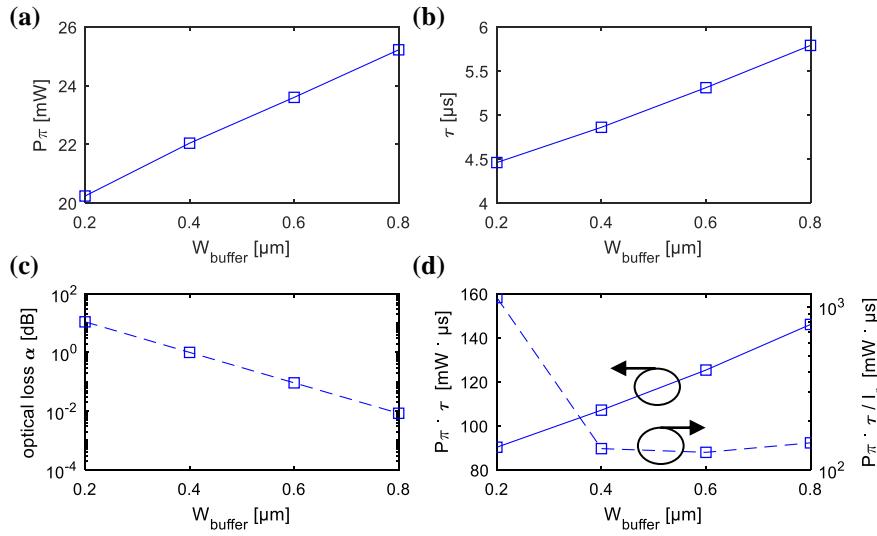


Fig. 3. Simulated impact of the intrinsic Si slab width W_{buffer} , shown in Fig. 1 (a), on the performance of the N_{++} Si TOPS design. (a) P_π , (b) limiting τ , (c) α , and (d) $P_\pi \cdot \tau$ and $P_\pi \cdot \tau / I_r$ FOMs vs. W_{buffer} .

2.3 Layout and fabrication

Figure 4 shows the fabricated SOI TOPS designs. Since layout space was limited and a large fraction was dedicated to crosstalk test structures (described in Section 3), not all simulations of Section 2.2 could be verified experimentally. To validate the accuracy and robustness of our simulation method, we implemented the TiN design with a $7.5 \mu\text{m}$ wide resistor (widest simulated in Fig. 2), and the N_{++} Si design with $1 \mu\text{m}$ wide N_{++} Si strips (narrowest allowed). To make the N_{++} Si design approximately lossless (<0.01 dB optical attenuation), W_{buffer} is set to $0.8 \mu\text{m}$, based on Fig. 3(c). The cross-section of the two final TOPS designs are shown in Fig. 4(a). In the longitudinal direction, the TiN TOPS is implemented as a single resistive strip. Since the expected sheet resistance of the N_{++} Si layer is several times that of TiN (Foundry data), the N_{++} Si TOPS is instead implemented as 6 resistors connected in parallel [24]. This lowers the equivalent resistance of the design and the required voltage. The total length of both TOPS designs L is $320 \mu\text{m}$ to match simulations. The top view of both designs is shown in Fig. 4(b). Both were fabricated on the same die in a multi-project wafer at A*STAR's Institute of Microelectronics (IME) Foundry.

3. Experimental results

The typical test structure for heater characterization is shown in Fig. 5(a), and is comprised of a thermally-tuned MZI next to which is laid out a passive victim MZI. As the extinction ratio of a $(1 \times n)$ MZI switch is primarily function of the splitter/combiner design (outside the scope here), the tuned MZI has only one output. Light is coupled in and out of both MZIs with grating couplers, and a probe is landed on aluminum pads to contact the two heater leads. The pitch between the arms of the tunable MZI, d_{intra} , the gap between both MZIs, d_{inter} , and the material in-between are varied between test structures. A total of 15 structures like Fig. 5(a) are laid out, all in C-band. Measurements are presented in two parts: DC (resistance, stability, efficiency and thermal crosstalk), and AC (bandwidth and switching). For the first part, a constant-voltage signal is sent through a precision multi-meter then applied to the heater. The optical signal out of the device under test (DUT) is sent to a variable optical attenuator (VOA) and power-meter.

For the second part, the electrical pattern generator signal is split to the heater and directly to an oscilloscope. The tunable MZI output is sent to a commercial photodetector AC-coupled to an oscilloscope. The experimental setup is shown in Fig. 5(b).

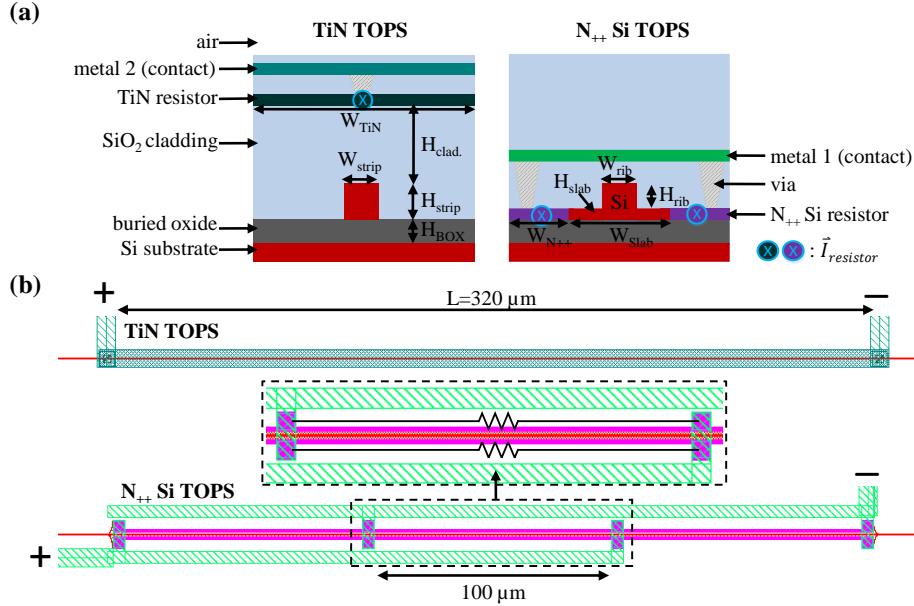


Fig. 4. Final heater layouts. (a) Cross-section (not to scale) and (b) top view of the TiN and N₊₊ Si TOPS designs, plus metal contacts. $W_{strip} = 0.5 \mu\text{m}$, $W_{TiN} = 7.5 \mu\text{m}$, $H_{clad.} = 2 \mu\text{m}$, $H_{strip} = 0.22 \mu\text{m}$, $H_{BOX} = 2 \mu\text{m}$ (TiN TOPS); $W_{N_{++}} = 1.0 \mu\text{m}$, $W_{Slab} = 2.1 \mu\text{m}$, $W_{rib} = 0.5 \mu\text{m}$, $H_{rib} = 0.13 \mu\text{m}$, $H_{slab} = 0.09 \mu\text{m}$ (N₊₊ Si TOPS). Layer colors match in (a) and (b). Current direction is arbitrary.

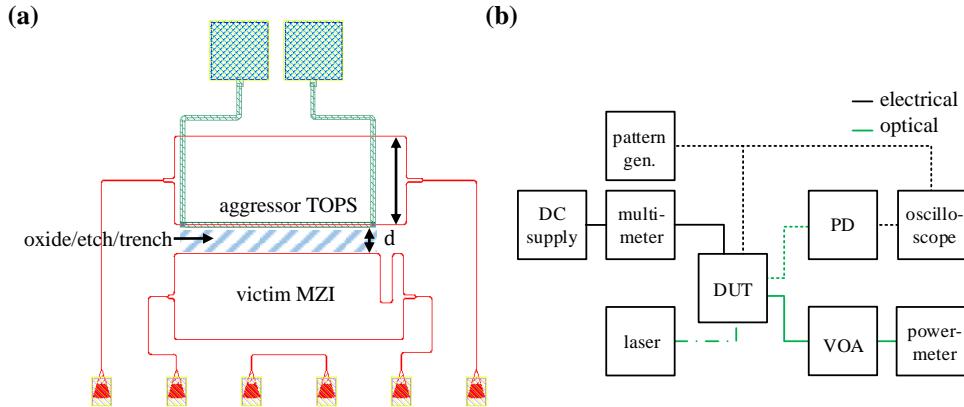


Fig. 5. (a) Typical test structure for performance and crosstalk characterization of TOPS designs. d_{intra} and d_{inter} are respectively the intra- and inter-MZI pitch. (b) Experimental setup. Solid lines and dashed lines are respectively used for DC and AC characterization.

3.1 DC characterization

Figure 6 shows the basic electrical characterization of the TiN and N₊₊ Si heaters. In Fig. 6(a), the measured IV curves allow to extract total resistance values (<4 V) of 0.54 kΩ and 1.02 kΩ, respectively. From previous experience, the voltage drop across the cables and probe can be neglected. Since the voltage drop across the aluminum heater leads can also be neglected – aluminum resistivity is 2-3 orders of magnitude smaller than the resistor materials – the

resistance values extracted are approximately those of the heaters alone. The small glitch at 6.5 V for the TiN IV curve is due to the power supply. The IV linearity of the TiN design is observed to be much better than the N₊₊ Si design. In Fig. 6(b), we show the evolution of the electrical power consumed by the heaters over 10 minutes for a fixed applied voltage. For both heaters, the decrease in power is limited to <0.1 mW over the test duration. The corresponding change in optical phase is negligible, masked by the ± 0.2 dBm caused by the random fiber array unit (FAU) drift. The probe drift, although lesser than the FAU drift due to the contact with the pads, hinders stability measurements >10 min.

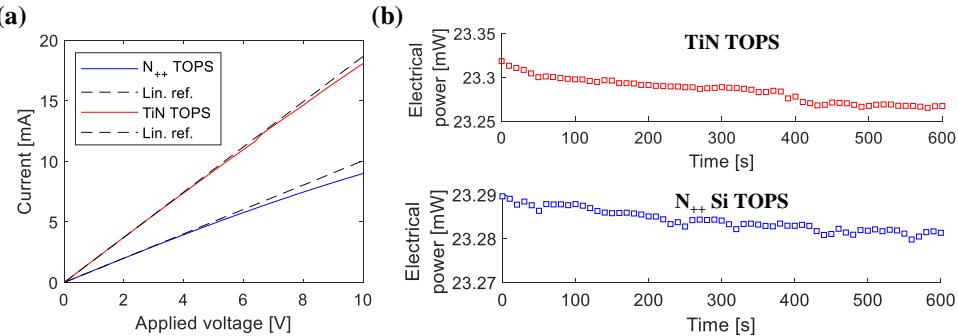


Fig. 6. Electrical characterization of the fabricated TiN and N₊₊ Si TOPS designs. (a) IV curves. Linear references are extrapolated from the [0-1] V segments. (b) Measured electrical power consumption over 10 minutes for a constant applied voltage.

The optical loss in a simple heated waveguide segment between two grating couplers, when compared to back-to-back grating couplers, is below the effective measurement resolution due to the FAU drift, but from simulations of Section 2.2 should be very small (<0.01 dB) for both designs. No voltage dependence is measured.

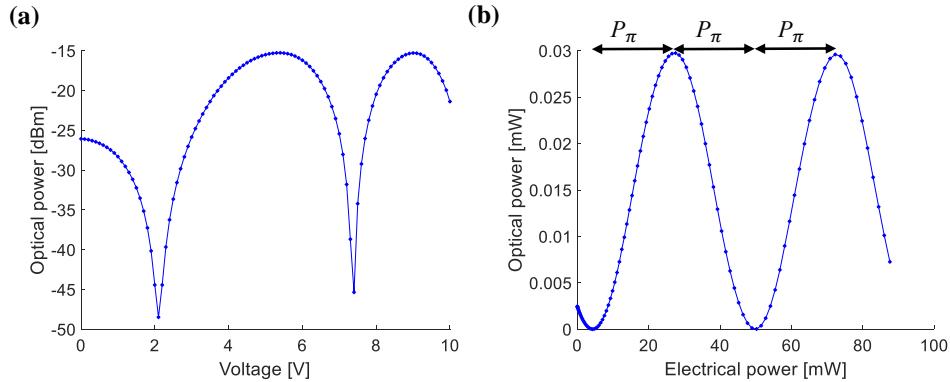


Fig. 7. Tunable MZI transfer function for the N₊₊ Si heater ($d_{intra} = 200 \mu\text{m}$). Optical power is shown vs. heater voltage in (a) and vs. heater power in (b). $P_{\pi,1} = (23.2 \pm 0.7) \text{ mW}$, $P_{\pi,2} = (22.7 \pm 1.1) \text{ mW}$, $P_{\pi,3} = (22.1 \pm 1.4) \text{ mW}$.

Figure 7 shows the raw transfer function (TF) for a tunable MZI based on the N₊₊ Si TOPS swept from 0 to 10 V. Similar data is obtained for the TiN TOPS. The same TF is shown vs. voltage in Fig. 7(a) and vs. electrical power in 7(b), to show the impact of the heater bias point on efficiency. From Fig. 7(a), biasing the heater at a high potential reduces V_π , however from

Fig. 7(b) P_π remains approximately the same regardless of bias. Hence, strongly biasing a TOPS is useless, unless the V_{pp} budget for switching is limited.

After TF normalization, the optical phase φ is extracted from the measured intensity I with $I = 0.5 + 0.5 \cos(\varphi)$. In Fig. 8, the relative phase $\Delta\varphi$ is plotted against heater power for both types of TOPS and 4 pitches d_{intra} between the two arms of the tunable MZI, of 50 μm , 100 μm , 150 μm and 200 μm . The extracted P_π are 29.2 mW - 31.5 mW for MZIs based on the TiN TOPS and 22.8 mW - 23.3 mW for those based on the N₊₊ Si TOPS. Reducing d_{intra} from 200 μm , to 50 μm increases P_π by 2.3 mW for tunable MZIs based on the TiN TOPS and by 0.6 mW for those based on the N₊₊ Si TOPS. This is due to enhanced heat crosstalk between the two arms, which partially cancels out $\Delta\varphi$ in the active arm. Hence, these results quantify the footprint (d_{intra})-efficiency tradeoff in doped-Si and metal-based thermo-optic switches on SOI. Moreover, comparing with Fig. 2(a), efficiency measurements closely match and validate our simulations: $P_{\pi,sim} = +3.0$ mW vs. $P_{\pi,meas.}$ for the 7.5 μm wide TiN resistor, and $P_{\pi,sim} = +2.7$ mW vs. $P_{\pi,meas.}$ for the 2.0 μm wide (total) N₊₊ Si resistor. For both heaters, $P_{\pi,meas.}$ for the widest d_{intra} pitch is taken for the comparisons since crosstalk effects were absent from simulations. Finally, the good agreement between measurements and simulations suggests that a fabricated 2.0 μm wide TiN heater, the most efficient in simulations, could achieve a ~21 mW P_π , or ~1.8 mW better than the N₊₊ Si design.

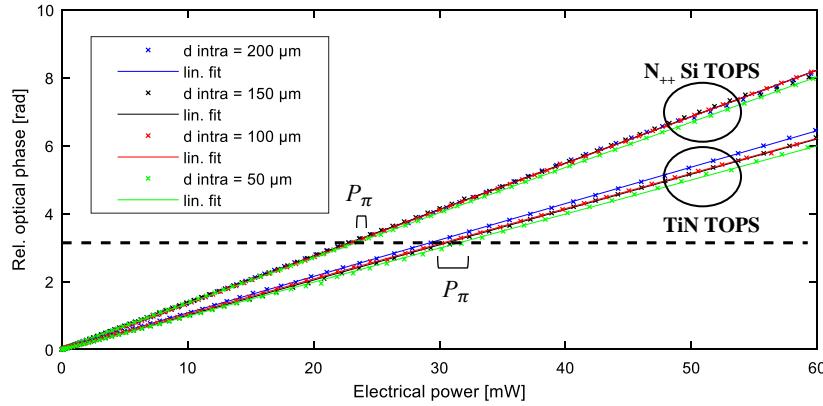


Fig. 8. De-embedded phase change and linear fit as a function of heater power for 4 pitches d_{intra} between the two arms of the tunable MZI, for the N₊₊ Si and TiN heaters. $\Delta P_{\pi,N_{++}} = 0.6$ mW

$$\text{and } \Delta P_{\pi,TiN} = 2.3 \text{ mW.}$$

Next, we characterize heat crosstalk between the heater (aggressor) and the unbalanced MZI (victim) shown in Fig. 5(a). Wavelength is set to bias the victim MZI at quadrature, to maximize its output optical power change for small parasitic heat flux and to better discriminate from noise. Figure 9 shows the de-embedded relative phase of the victim MZI as a function of heater power, for $d_{inter} = 5 \mu\text{m}$, 15 μm , 45 μm and 135 μm , after sinusoidal fits are applied to the normalized TFs. Note that the phase measured should be independent of the total heater length L , per Eqs. (4) and (5). Three material processing patterns between the aggressor and victim are tested, to investigate layout-based approaches to mitigate parasitic heat flux on the die. In Figs. 9(a) and 9(b), the default SiO₂ cladding fills the aggressor-victim gap, for TiN and N₊₊ Si heaters respectively. The phase change in the victim MZI is similar for both heaters at all d_{inter} values. Moreover, as simulated in Fig. 1(d), significant residual heat is present 5 μm away from

the waveguide, and most of heat is scattered at 15 μm . However, depending on the heater power and the victim function in practice, the parasitic phase shift can still be significant – and is easily measurable – as far as 135 μm away from the heater. In Figs. 9(c) and 9(d), only the N₊₊ Si heater is tested. In Fig. 9(c), the SiO₂ cladding is etched across the heater/victim gap. In Fig. 9(d), the gap is a deep trench cutting through the SiO₂ cladding, 220 nm Si, BOX and Si substrate layers (partially). Comparing Fig. 9(c) with 9(b), etching the cladding has little impact on heat crosstalk. However, comparing Fig. 9(d) with 9(b), the deep trench reduces the phase change in the victim MZI by a factor of ~3, or by 0.31 rad ($\pi/10$), 0.11 rad, 0.08 rad and 0.02 rad for gap widths of 5 μm , 15 μm , 45 μm and 135 μm , versus the default SiO₂ cladding when the N₊₊ Si heater power is ~ 23 mW (P_π). Deep trenches can therefore provide significant thermal insulation, and should advantageously be used in tight PIC layouts between heaters and other phase-sensitive devices such as resonators, MZIs, arrayed-waveguide de-multiplexers or coherent receiver hybrids. As noted in Section 2.1 and verified in [21], if using trenches very close to the heated waveguide, the $P_\pi \cdot \tau$ heater performance tradeoff will also be affected.

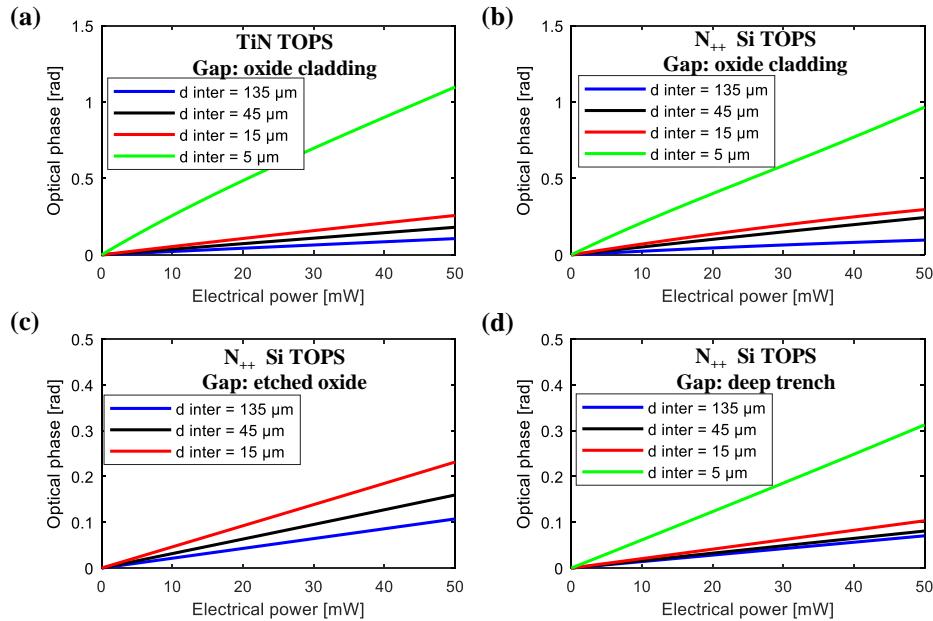


Fig. 9. Measured phase change at quadrature in the victim MZI vs heater power for different aggressor/victim gap widths d_{inter} . (a) TiN heater and default oxide in the gap. (b) N₊₊ Si heater, default oxide in the gap. (c) N₊₊ Si heater, etched oxide in the gap ($d_{\text{inter}} = 5 \mu\text{m}$ is absent because of layout rules). (d) N₊₊ Si heater, deep trench in the gap.

3.2 AC characterization

Figures 10(a) and 10(b) show the measured bandwidth and time-domain switching of the TiN and N₊₊ Si TOPS. In Fig. 10(a), the pattern generator produces a variable frequency sine wave with $V_\pi / 2$ amplitude, and the amplitude response is read on the oscilloscope. The -3dB bandwidth is 33 kHz for the TiN TOPS and 85 kHz for the N₊₊ Si TOPS. In Fig. 10(b), a 5 kHz square wave with $V_\pi / 2$ amplitude and the required offset to switch between the two first extrema of optical transmission is applied to both heaters. The $1/e$ rise and fall time constants are measured directly with the oscilloscope, and are [$\tau_{\text{rise}} = 3.7 \mu\text{s}$, $\tau_{\text{fall}} = 7.2 \mu\text{s}$] for the TiN TOPS, and [$\tau_{\text{rise}} = 2.2 \mu\text{s}$, $\tau_{\text{fall}} = 2.0 \mu\text{s}$] for the N₊₊ Si TOPS. For the TiN TOPS, the asymmetric time constants, i.e., significantly slower fall time, can be explained by the bad thermal

conductance between the heater and the heat drain [21], itself arising from the relatively thick oxide layer and air surrounding the metal.

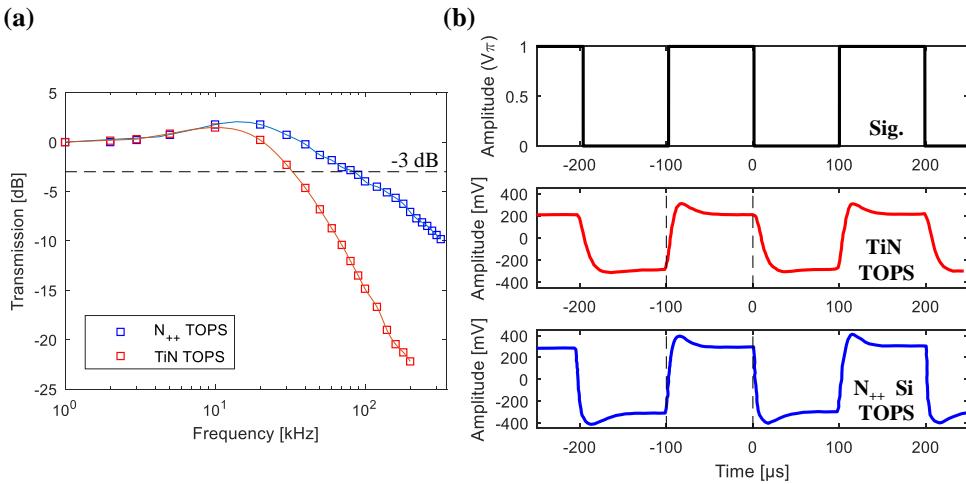


Fig. 10. AC measurements of the N₊₊ Si and TiN heaters ($d_{intra} = 200 \mu\text{m}$). (a) Frequency-domain: optical amplitude normalized to 1 kHz vs. frequency of the sine wave. (b) Time-domain: 5 kHz square electrical drive signal (top), and optical response of the TiN (middle) and N₊₊ (bottom) heaters. Exact response amplitude depends on FAU coupling.

From Fig. 2(b), the simulated time constant is offset by exactly $+3.6 \mu\text{s}$ versus the measured limiting τ , for both TOPS designs. Again, this correlation suggests that a fabricated $2.5 \mu\text{m}$ wide TiN heater, the fastest in simulations, would achieve a limiting τ of $\sim 5.6 \mu\text{s}$. For optimized designs (in terms of the $P_\pi \cdot \tau$ FOM from Fig. 2(c)), the limiting time constant is thus roughly 2.5 times better for the N₊₊ Si TOPS. Note that several pulse-shaping approaches have been suggested to improve time constants of heaters on SOI [42–47].

Lastly, the frequency response of both heaters in Fig. 10(a) features noticeable peaking, around 13 kHz and 17 kHz for the TiN and N₊₊ Si heaters. This peaking is believed to be the cause of the time-domain overshoot in Fig. 10(b), since the square wave modulation frequency is only 5 kHz. To quickly verify this assumption, Fig. 11 shows the filtering (in simulation) of an ideal square wave with the measured heater transfer functions from Fig. 10(a). In Fig. 11(a), the Fourier transform of an ideal 5 kHz square signal and the filter definitions are shown. In Fig. 11(b), time-domain square signals of 2 kHz, 5 kHz and 10 kHz are shown after multiplication with the filters in the frequency domain. It is readily seen that the peaking is the cause of the observed overshoot, since it disappears when the modulation frequency approaches the peaks in Fig. 10(a). These basic simulations don't account for the physical directionality of time propagation, explaining the overshoot in both directions in Fig. 11(b). Note that heater 'overdriving' is not related to overshoot here, as it is still visualized experimentally at $V_{pp} = V_\pi / 2$ (not shown). The response of both the TiN and the N₊₊ Si heaters is thus typical of second-order systems [48,49]. From a circuit perspective, both heaters are analogous to under-damped RLC circuits, where the induction comes from the long metal traces (heaters and leads), and the capacitance is dominated by thermal diffusion. Note that overshoot is absent from transient simulations of Fig. 1(c) because the (longitudinal) inductance traces cannot be modeled.

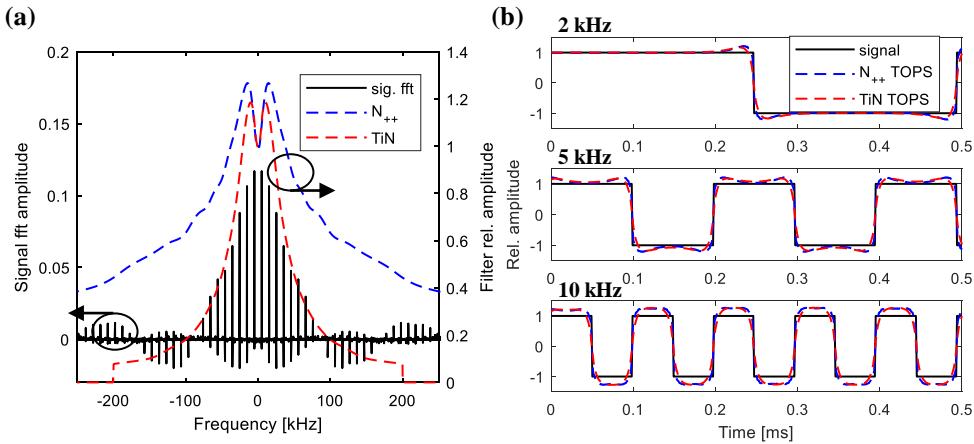


Fig. 11. Switch overshoot characterization. (a) Ideal 5 kHz square signal fast Fourier transform (FFT), and measured filter response of the N_{++} Si and TiN heaters. The FFT extends beyond 250 kHz, and filter definitions are extended (zero padding) to match the FFT length. (b) Ideal and filtered time domain signals (simulation) at 2 kHz, 5 kHz and 10 kHz. Modulation is done with a full V_π swing.

4. Heater comparison summary

Table 2 summarizes the performance of optimal TiN and N_{++} Si TOPS designs (320 μm long), based on simulations and experiments. V_π and heater resistance are excluded due to the dependence on the length.

Table 2. Comparison Summary between Optimal TiN-Based and Doped-Si-Based TOPS on SOI

Resistor material	Resistor width ^a [μm]	Heater loss [dB]	P_π ^b [mW]	El. power variation (10 min)	Limiting τ [μs]	$P_\pi \cdot \tau$ [mW \cdot μs]
TiN	2.5	<0.4	~21.4	<0.1 mW	~5.6	~119.8
N_{++} Si	2.0	<0.4	22.8	<0.1 mW	2.2	50.2

^aFor optimal $P_\pi \cdot \tau$ FOM and respecting layout rules. Width is the sum of the 2 resistors for the N_{++} design.

^bAssuming a 200 μm pitch between the arms of the thermally-tuned MZI.

In Table 2, P_π and τ could slightly be decreased for the N_{++} Si design if the intrinsic Si slab width was decreased to 0.6 μm (instead of 0.8 μm), for an added \sim 0.1 dB loss according to Fig. 3. Also, $P_\pi \cdot \tau \approx P_\pi \cdot \tau / I_r$ since loss is small. Overall then, the TiN and N_{++} Si TOPS designs have very similar efficiencies, but the latter shows significantly better speed, making it in our opinion the most practical and scalable TOPS on SOI among the ‘lossless’ (without waveguide doping) and fully CMOS-compatible designs. Furthermore, this design only requires 1 metallization layer, for electrical contacts.

Finally, in terms of the $P_\pi \cdot \tau$ FOM, the two designs summarized in Table 2 compare advantageously with TOPS designs of [21] and [24], both detailed in Table 1. Those are respectively metal-based and doped-Si based devices also built at IME, both avoiding direct waveguide doping and substrate undercuts. Our TiN design beats [21] by \sim 48.4 mW \cdot μs , and our N_{++} Si design beats [24] by \sim 6.6 mW \cdot μs .

5. Conclusion

We optimized and compared the two main approaches to build thermo-optic phase-shifters on the SOI platform with negligible optical attenuation. Only standard and widely available fabrication steps were used. We first reviewed TOPS theory, and discussed implementation tradeoffs. We then optimized the design of metal-based and doped-Si-based TOPS for the IME process with thermal and optical FEM simulations. To minimize the $P_\pi \cdot \tau$ FOM, the resistor widths must be $\sim 2.5 \mu\text{m}$ for TiN and $\sim 1.0 \mu\text{m}$ for N₊₊ Si (each resistor). In simulations the TiN design has approximately no optical loss, and the width of the intrinsic Si slab for the N₊₊ Si design has to be $>0.8 \mu\text{m}$ to contain loss $<0.01 \text{ dB}$ (loss was too small to be measured for both designs). Optimal TOPS designs have P_π and limiting τ of $\sim 21.4 \text{ mW}$ and $\sim 5.6 \mu\text{s}$ using a TiN resistor, and 22.8 mW and $2.2 \mu\text{s}$ using N₊₊ Si resistors. Peaking in the frequency response of both heaters, likely caused by the inductive traces, causes overshoot in the time domain when the modulation frequency is low. Both designs show very good power consumption stability, $<0.1 \text{ mW}$ over 10 minutes. In summary, the two optimized designs have similar phase-shifting efficiencies, but the doped-Si design is best suited for switching applications due to its better speed. Both designs outperform comparable designs from the literature in terms of the $P_\pi \cdot \tau$ FOM.

Furthermore, it was experimentally shown that P_π is increased by up to a few mW if the pitch between the arms of a thermo-optic switch is reduced from $200 \mu\text{m}$ to $50 \mu\text{m}$ in an effort to reduce footprint. In addition, we showed that except substrate undercuts (requiring special processing), deep trenches are the best structures to limit parasitic thermal phase shifts in sensitive devices at short distances from heaters. This phase shift is reduced by 0.31 rad, 0.11 rad, 0.08 rad and 0.02 rad for distances of $5 \mu\text{m}$, $15 \mu\text{m}$, $45 \mu\text{m}$ and $135 \mu\text{m}$, versus the default SiO₂ cladding when heater power is P_π .

Appendix

Table 3 lists material constants used in FEM simulations. Properties are taken at 300 K. It is assumed that silicon specific heat is negligibly affected by layer thickness and doping. The electrical conductivity of intrinsic silicon is assumed constant for all film thicknesses as it is $\sim 10^9$ times smaller than for N₊₊ Si. The optical attenuation and refractive index of N₊₊ Si are computed using relations of [30] and the doping dosage information provided by the Foundry. Attenuation is reported as the imaginary part of the refractive index, $\kappa = \alpha \lambda_0 / 4\pi$, where α is the linear attenuation coefficient and λ_0 is the free-space wavelength. Properties without explicit references are part of the Software database.

Table 3. Thermal and Electromagnetic Properties of Materials Used in FEM Simulations

Material	Thickness [μm]	Density [kg/m ³]	Specific heat [J/kg·K]	Thermal conductivity [W/m·K]	Electrical conductivity [S/m]	n _{λ = 1550 nm}	K _{λ = 1550 nm}
Si (bulk)	>>5	2330	711	148 [32]	4.3E-4 [28]	-	-
Si (wg)	0.22	2330	711	90 [32]	4.3E-4	3.476	0
Si (slab)	0.09	2330	711	55 [32]	4.3E-4	3.476	0
N ₊₊ Si ^a	0.09	2330	711	25 [29,38]	1.0E + 5 [33]	3.072 [30]	0.137 [30]
TiN	(withheld)	5240 [34]	598 [36]	28 [34]	2.3E + 6 [35]	-	-
SiO ₂	(withheld)	2203	709	1.38	1E-11	1.55	0
air	>>5	1.177	1006	0.026	1E-12	-	-

^aHighest doping dosage available.

Acknowledgments

We acknowledge the support of the Natural Sciences and Engineering Research Council of Canada (NSERC), the Fonds de recherche du Québec – Nature et technologies (FRQNT), CMC Microsystems, Lumerical Solutions and Advanced Micro Foundry (AMF).

References

1. M. S. Rasras and O. Al Rayat, "Lab-on-Chip Silicon Photonic Sensor," in *The IoT Physical Layer*, I. Elfadel, M. Ismail, eds. (Springer, Cham, 2019).
2. G. Coppola, L. Sirleto, I. Rendina, and M. Iodice, "Advance in thermo-optical switches: principles, materials, design, and device structure," *Opt. Eng.* **50**(7), 071112 (2011).
3. C. Doerr, L. Chen, T. Nielsen, R. Aroca, L. Chen, M. Banaee, S. Azemati, G. McBrien, S. Y. Park, J. Geyer, and B. Guan, "O, E, S, C, and L band silicon photonics coherent modulator/receiver," in *Optical Fiber Communications Conference and Exhibition*, (Optical Society of America, 2016), paper Th5C.4.
4. A. N. Tait, T. F. de Lima, E. Zhou, A. X. Wu, M. A. Nahmias, B. J. Shastri, and P. R. Prucnal, "Neuromorphic photonic networks using silicon photonic weight banks," *Sci. Rep.* **7**(1), 7430 (2017).
5. H. Yagi, T. Kaneko, N. Kono, Y. Yoneda, K. Uesaka, M. Ekawa, M. Takechi, and H. Shoji, "InP-based monolithically integrated photonic devices for digital coherent transmission," *IEEE J. Sel. Top. Quantum Electron.* **24**(1), 1–11 (2018).
6. W. Bogaerts and L. Chrostowski, "Silicon photonics circuit design: methods, tools and challenges," *Laser Photonics Rev.* **12**(4), 1700237 (2018).
7. D. Thomson, A. Zilkie, J. E. Bowers, T. Komljenovic, G. T. Reed, L. Vivien, D. Marrs-Morini, E. Cassan, L. Virot, J. M. Fédeli, J. M. Hartmann, J. H. Schmid, D.-X. Xu, F. Boeuf, P. O'Brien, G. Z. Mashanovich, and M. Nedeljkovic, "Roadmap on silicon photonics," *J. Opt.* **18**(7), 073003 (2016).
8. C. Doerr, "Silicon photonic integration in telecommunications," *Front. Phys.* **3**, 37 (2015).
9. W. Bogaerts, P. De Heyn, T. Van Vaerenbergh, K. De Vos, S. Kumar Selvaraja, T. Claes, P. Dumon, P. Bienstman, D. Van Thourhout, and R. Baets, "Silicon microring resonators," *Laser Photonics Rev.* **6**(1), 47–73 (2012).
10. P. Dong, "Silicon photonic integrated circuits for wavelength-division multiplexing applications," *IEEE J. Sel. Top. Quantum Electron.* **22**(6), 370–378 (2016).
11. A. Samani, V. Veerasubramanian, E. El-Fiky, D. Patel, and D. V. Plant, "A silicon photonic PAM-4 modulator based on dual-parallel Mach-Zehnder interferometers," *IEEE Photonics J.* **8**(1), 1–10 (2016).
12. M. R. Watts, W. A. Zortman, D. C. Trotter, G. N. Nielson, D. L. Luck, and R. W. Young, "Adiabatic resonant microrings (ARMs) with directly integrated thermal microphotonics," in *Conference on Lasers and Electro-Optics*, (OSA, 2009), paper CPDB10.
13. P. Dong, W. Qian, H. Liang, R. Shafiiha, D. Feng, G. Li, J. E. Cunningham, A. V. Krishnamoorthy, and M. Asghari, "Thermally tunable silicon racetrack resonators with ultralow tuning power," *Opt. Express* **18**(19), 20298–20304 (2010).
14. K. Xiong, X. Xiao, X. Li, Y. Hu, Z. Li, T. Chu, Y. Yu, and J. Yu, "CMOS—compatible reconfigurable microring demultiplexer with doped silicon slab heater," *Opt. Commun.* **285**(21–22), 4368–4371 (2012).
15. P. Pintus, C. Manganelli, F. Gambini, F. Di Pasquale, M. Fournier, O. Lemonnier, C. Kopp, and C. J. Oton, "Optimization of integrated silicon doped heaters for optical microring resonators," in *ECOC 2016; 42nd European Conference on Optical Communication*, (VDE, 2016), pp. 1–3.
16. A. Masood, M. Pantouvaki, D. Goossens, G. Lepage, P. Verheyen, D. Van Thourhout, P. Absil, and W. Bogaerts, "CMOS-compatible tungsten heaters for silicon photonic waveguides," in *9th International Conference on Group IV Photonics (GFP)*, (IEEE, 2012), pp. 234–236.
17. L. Yu, Y. Yin, Y. Shi, D. Dai, and S. He, "Thermally tunable silicon photonic microdisk resonator with transparent graphene nanoheaters," *Optica* **3**(2), 159–166 (2016).
18. N. J. Martinez, C. T. DeRose, R. Jarecki, A. L. Starbuck, A. T. Pomerene, D. C. Trotter, and A. L. Lentine, "Substrate removal for ultra efficient silicon heater-modulators," in *IEEE Optical Interconnects Conference*, (IEEE, 2017), pp. 15–16.
19. M. R. Watts, J. Sun, C. DeRose, D. C. Trotter, R. W. Young, and G. N. Nielson, "Adiabatic thermo-optic Mach-Zehnder switch," *Opt. Lett.* **38**(5), 733–735 (2013).
20. N. C. Harris, Y. Ma, J. Mower, T. Baehr-Jones, D. Englund, M. Hochberg, and C. Galland, "Efficient, compact and low loss thermo-optic phase shifter in silicon," *Opt. Express* **22**(9), 10487–10493 (2014).
21. J. Song, Q. Fang, S. H. Tao, T. Y. Liow, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Fast and low power Michelson interferometer thermo-optical switch on SOI," *Opt. Express* **16**(20), 15304–15311 (2008).
22. J. Van Campenhout, W. M. Green, S. Assefa, and Y. A. Vlasov, "Integrated NiSi waveguide heaters for CMOS-compatible silicon thermo-optic devices," *Opt. Lett.* **35**(7), 1013–1015 (2010).
23. Q. Fang, J. F. Song, T.-Y. Liow, H. Cai, M. B. Yu, G. Q. Lo, and D.-L. Kwong, "Ultralow power silicon photonics thermo-optic switch with suspended phase arms," *IEEE Photonics Technol. Lett.* **23**(8), 525–527 (2011).

24. D. Patel, V. Veerasubramanian, S. Ghosh, W. Shi, A. Samani, Q. Zhong, and D. V. Plant, "A 4×4 fully non-blocking switch on SOI based on interferometric thermo-optic phase shifters," in *Optical Interconnects Conference*, (IEEE, 2014), TuD5.
25. A. Masood, M. Pantouvaki, G. Lepage, P. Verheyen, J. Van Campenhout, P. Absil, D. Van Thourhout, and W. Bogaerts, "Comparison of heater architectures for thermal control of silicon photonic circuits," in *10th International Conference on Group IV Photonics (GFP)*, (IEEE, 2013), pp. 83–84.
26. J. Komma, C. Schwarz, G. Hofmann, D. Heinert, and R. Nawrodt, "Thermo-optic coefficient of silicon at 1550 nm and cryogenic temperatures," *Appl. Phys. Lett.* **101**(4), 041905 (2012).
27. A. Samani, M. Chagnon, D. Patel, V. Veerasubramanian, S. Ghosh, M. Osman, Q. Zhong, and D. V. Plant, "A low-voltage 35-GHz silicon photonic modulator-enabled 112-Gb/s transmission system," *IEEE Photonics J.* **7**(3), 1–13 (2015).
28. G. Eranna, *Crystal Growth and Evaluation of Silicon for VLSI and ULSI* (CRC, 2014).
29. M. Asheghi, K. Kurabayashi, R. Kasnavi, and K. Goodson, "Thermal conduction in doped single-crystal silicon films," *J. Appl. Phys.* **91**(8), 5079–5088 (2002).
30. M. Nedeljkovic, R. Soref, and G. Z. Mashanovich, "Free-Carrier Electrorefraction and Electroabsorption Modulation Predictions for Silicon Over the 1–14 μm Infrared Wavelength Range," *IEEE Photonics J.* **3**(6), 1171–1180 (2011).
31. X. Zhang and C. P. Grigoropoulos, "Thermal conductivity and diffusivity of free-standing silicon nitride thin films," *Rev. Sci. Instrum.* **66**(2), 1115–1120 (1995).
32. M. Asheghi, M. Touzelbaev, K. Goodson, Y. Leung, and S. Wong, "Temperature-dependent thermal conductivity of single-crystal silicon layers in SOI substrates," *J. Heat Trans.* **120**(1), 30–36 (1998).
33. B. Van Zeghbroeck, "Semiconductor Fundamentals," in *Principles of electronic devices* (University of Colorado, 2011).
34. J. F. Shackelford, Y.-H. Han, S. Kim, and S.-H. Kwon, *CRC materials science and engineering handbook* (CRC, 2016).
35. P. Patsalas, C. Charitidis, S. Logothetidis, C. Dimitriadis, and O. Valassiatades, "Combined electrical and mechanical properties of titanium nitride thin films as metallization materials," *J. Appl. Phys.* **86**(9), 5296–5298 (1999).
36. M. W. Chase, Jr., "NIST-JANAF thermochemical tables, Monograph 9," in *J. Phys. Chem. Ref. Data*, D. R. Burgess Jr, A. H. Harvey, eds. (American Chemical Society, 1998).
37. H. O. Pierson, *Handbook of refractory carbides and nitrides* (Elsevier, 1996).
38. W. Liu, K. Etessam-Yazdani, R. Hussin, and M. Asheghi, "Modeling and data for thermal conductivity of ultrathin single-crystal SOI layers at high temperature," *IEEE Trans. Electron Dev.* **53**(8), 1868–1876 (2006).
39. E. Hecht, "The propagation of light," in *Optics, 4th Edition*, Addison-Wesley, ed. (Pearson Education, 2002).
40. A. Masood, M. Pantouvaki, D. Goossens, G. Lepage, P. Verheyen, J. Van Campenhout, P. Absil, D. Van Thourhout, and W. Bogaerts, "Fabrication and characterization of CMOS-compatible integrated tungsten heaters for thermo-optic tuning in silicon photonics devices," *Opt. Mater. Express* **4**(7), 1383–1388 (2014).
41. K. Liu, C. Zhang, S. Mu, S. Wang, and V. J. Sorger, "Two-dimensional design and analysis of trench-coupler based Silicon Mach-Zehnder thermo-optic switch," *Opt. Express* **24**(14), 15845–15853 (2016).
42. A. H. Atabaki, A. A. Eftekhar, S. Yegnanarayanan, and A. Adibi, "Sub-100-nanosecond thermal reconfiguration of silicon photonic devices," *Opt. Express* **21**(13), 15706–15718 (2013).
43. D. Hohlfeld and H. Zappe, "Thermal and optical characterization of silicon-based tunable optical thin-film filters," *J. Microelectromech. Syst.* **16**(3), 500–510 (2007).
44. T. T. Aalto, M. Kapulainen, S. Yliniemi, P. Heimala, and M. J. Leppihalme, "Fast thermo-optical switch based on SOI waveguides," in *Integrated Optics: Devices, Materials, and Technologies VII*, S. S. Yakov, A. Tervonen, eds. (International Society for Optics and Photonics, 2003), 149–160.
45. H. Matsuura, S. Suda, K. Tanizawa, K. Suzuki, K. Ikeda, H. Kawashima, and S. Namiki, "Accelerating switching speed of thermo-optic MZI silicon-photonic switches with "Turbo Pulse" in PWM Control," in *Optical Fiber Communication Conference*, (Optical Society of America, 2017), paper W4E. 3.
46. M. Harjanne, M. Kapulainen, T. Aalto, and P. Heimala, "Sub-us switching time in silicon-on-insulator Mach-Zehnder thermooptic switch," *IEEE Photonics Technol. Lett.* **16**(9), 2039–2041 (2004).
47. M. J. Brinkman, W. K. Bischel, T. Kowalczyk, D. R. Main, and L. L. Huang, "Thermo-optic switch having fast rise-time," US 6,351,578 B1 (2002).
48. K. J. Aström and R. M. Murray, *Feedback systems: an introduction for scientists and engineers* (Princeton University, 2010).
49. R. H. Cannon, "Damped second-order systems," in *Dynamics of physical systems*, McGraw-Hill, ed. (Courier Corporation, 1967).