A Heterogeneously Integrated Wafer-level Processed Co-Packaged Optical Engine for Hyper-scale Data Centres

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***Abstract*— The amount of IP traffic in data centers has been doubling approximately every 2-3 years and high-performance optical transceivers are required to handle such data. We propose a heterogeneous packaging of Optical Engines with edge optical coupling for hyper-scale data center application demonstrated using an 800Gbps test vehicle. This platform allows the integration of ICs from diverse technologies such as CMOS, SiGe, SOI, III-V, etc. in small form factor, through wafer-scale electronics-photonics packaging on 300mm wafers. The package offers short electrical interconnects between the photonic integrated circuit and electronic integrated circuit components and the package substrate with minimal signal loss. This high-performance compact OE can be integrated with Application Specific Integrated Circuits, making the package suitable for use in hyper-scale data centres and high-performance computing applications.**

Keywords- Hyperscale Data Centers, High-performance computing, Electronic Photonic Package, Silicon photonics, Heterogeneous Integration, Optical Transceivers, Optical Engine, Fan-out wafer-level packaging.

I. INTRODUCTION

Optical communications have replaced electrical I/O for applications requiring very high data transfer rates such as hyper-scale datacenters (HDC) [1]. With data transmission between servers within the data center constituting about 70% of the total traffic, the demand for optical links that can be used effectively within or between data centers is on the rise [2-4]. The growing internet traffic in cloud service providers and hyperscale data centers is leading to increasing demand for higher data rates and bandwidth. To keep up with this trend, Switch Application Specific Integrated Circuits (ASICs) have been doubling their bandwidth every two years [5]. However, to stay relevant, optical transceivers must also provide higher bandwidth rates in each new generation of ASICs, while maintaining similar form factors and costs [6]. To achieve this there is a need for integrating photonics and electronics together addressing integration incompatibility and design incompatibility issues. Components in photonic ICs (PIC) often have large footprints, making it extremely cost-inefficient to utilize the expensive wafer area of high-speed electronics (<22 nm) for photonic components.

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In this work, an electronic-photonic heterogeneous packaging, which is a promising technique to realize a high-speed Optical Engine (OE) for HDC, is enabled by advanced Fan-out wafer-level packaging (FOWLP), which integrates individually optimized chiplets.

II. DESIGN AND FABRICATION

A. OE Package Features

Packaging based on FOWLP is employed in work which is compatible with the high-speed signal application. A Mold-first approach is followed to fabricate the OE package (Fig. 1) through a robust process integration flow. The key challenges addressed during packaging include encapsulation of the PIC without impacting its functions such as edge and vertical optical coupling; redistribution layer (RDL) and Through Mold Via (TMV) development for 100Gbps/lane applications and managing mechanical integrity such as package and wafer warpage. The packaging is realized on a 300mm FOWLP line equipped to undertake the whole assembly and fabrication process development.

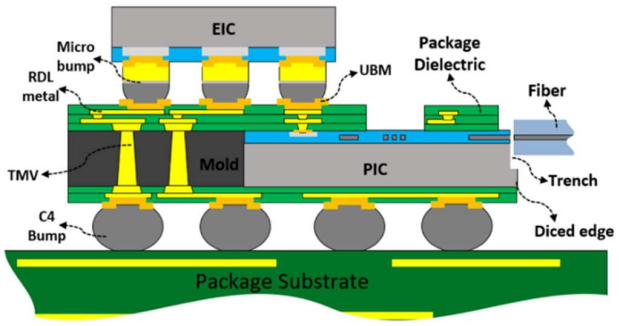

Fig. 1. The cross-sectional layout of the optical engine is realized by fan-out wafer-level packaging. The package contains photonic integrated circuit chips that are encased within an epoxy mold compound and EICs mounted on the surface. The mold area that surrounds the PIC enables electrical routing to the substrate.

The package has a footprint of 9.5mmx13mm and consists of a PIC and multiple electronic ICs (EICs). The PIC die contains high-speed 100Gbps/lane silicon modulators,

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waveguided germanium photodetectors together with other passive photonic circuits and thermo-optic components. The 800Gbps OE demonstrator package is designed in such a way that the PIC die is embedded in the mold compound, while the EICs are assembled on the package surface. In this demonstration, the EIC used are passive devices with only the interconnects. The PIC is designed with suspended optical couplers at one edge of the chip, facilitating edge coupling to external optical I/O during module packaging. A specially designed silicon buffer structure is used to preserve the optical coupling structures of the PIC from any contamination and damage while performing FOWLP molding for chip reconstitution [7]. For high-speed connections, RDL metal with 15µm line/space and TMV provides fine line width interconnects that can reduce the parasitic components with good impedance control. EICs are placed on the package surface bridging the fanout area and PIC with their I/Os sit directly above the bond pads of the photonic IC modulator in the case of the driver and those of the Photodetector in the case of the Transimpedance amplifier (TIA) where the TMVs provide the interconnections to the package substrate through backside RDL.

B. *Package design*

Interconnects carrying high-speed signals between the EIC and PIC are designed with low propagation loss to enable high data rates and low power consumption. EIC and PIC are connected such that the shortest path is formed between them by placing the micro bump of the EICs directly above the PIC modulator or PD pads. The frequency response of the differential transmission lines is modelled using a 3D electromagnetic simulator (ANSYS HFSS). The EIC microbump has a pitch of 150um and a diameter of 70um. The frequency response can be seen in Fig. 2. The link provides an insertion loss of 0.04dB and 0.14 dB at 28 GHz and 56 GHz respectively. The return loss is >15dB at 28 GHz and 56 GHz. The above indicates that our platform provides low loss for high-speed signals.

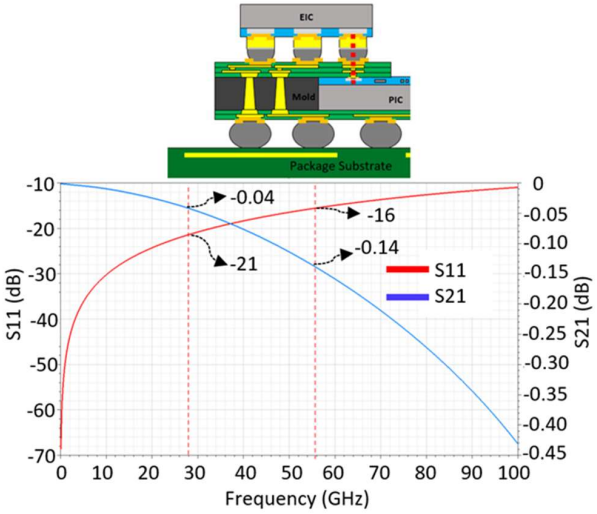

Fig. 2. Plot showing the frequency response of the interconnects connecting EIC to PIC

The performance of the differential interconnects connecting the EIC to the substrate through the package can be seen in Fig. 3. The package provides two frontside metal layers, and backside metal layers in addition to the UBM. The front side and back side metal are connected by TMV that has a diameter, height and pitch of 150um, 300um and of 300um respectively. The dielectric constant and loss tangent of the mold compound are 3.42 and 0.008. The package is connected to the substrate through a controlled collapsed chip connection (C4 bump) that has a diameter of 120um and a pitch of 250um. The electrical signal insertion loss introduced by interconnects from package substrate to EICs including C4 bump, TMV, and the RDL metal is 0.87dB at 56GHz and return loss greater than 20dB. By adding 2mm of substrate transmission line the total insertion loss is predicted to be 1.2dB. The performance of TMV is such that it contributes an insertion loss of 0.24dB at 56GHz. Hence, the package interconnect has a wide bandwidth that can support 100Gbps/lane and even 200Gbps/lane high-speed digital signals.

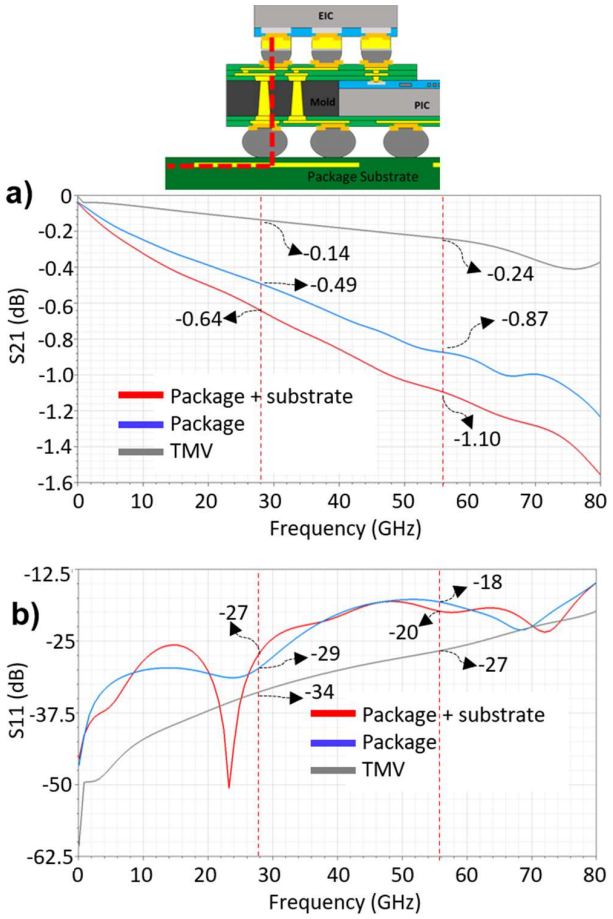

Fig. 3. a) Plot showing the frequency response of the differential transmission interconnects connecting the substrate to the input of the EIC (driver) including the µbump, front side RDL, TMV, backside RDL, c4 bump and substrate a) insertion loss b) reflection loss.

The warpage of the package is estimated through thermo-mechanical simulation. Figure 4 shows a 3D Finite Element

Analysis (FEA) model that was developed for the optical engine fan out-level package. PIC silicon die is modelled encased inside the 300µm mold that has a coefficient of thermal expansion (CTE) of 7 ppm/ºC and 22 ppm/ºC before and after glass transition temperature respectively. The package has dielectric layers with a total thickness of 30µm on its frontside and 20um at the backside with a CTE of 65ppm/ºC. Two EICs are flip-chip bonded to the surface through bumps. Epoxy mold compound is cured at a temperature of 150ºC and therefore, its stress-free reference temperature. Dielectric polyimide layers are cured at 225ºC and solder reflow at 220ºC. The embedded PIC warpage is calculated to be 17um and the predicted package warpage of <30um is within the acceptable range for assembly.

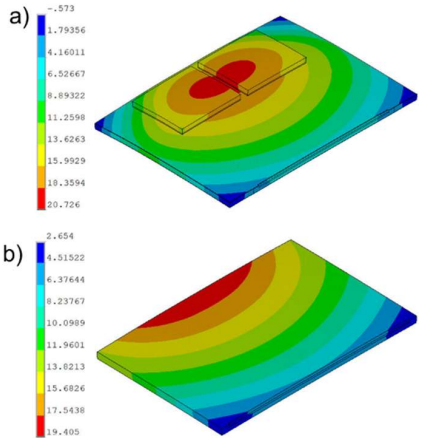

Fig. 4. a) Warpage (um) of optical engine package. b) Warpage (um) of PIC die embedded in the mold.

C. PIC Features

Figure 5 illustrates the schematic of the PIC designed for the 800G OE demonstration. Each PIC die contains 8 high-speed silicon modulators and 8 waveguided germanium photodetectors.

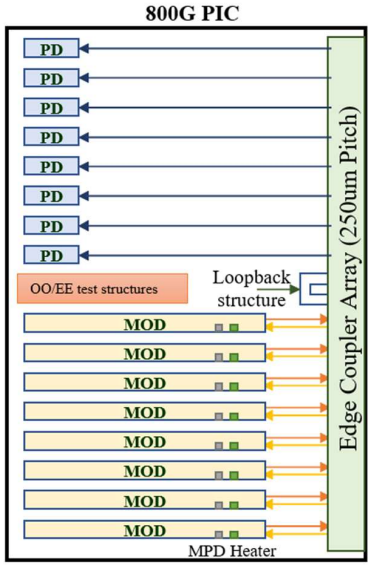

Fig. 5. Schematic of the 800G PIC.

The high-speed modulators exhibit over 32GHz 3dB EO bandwidth (Fig. 6a), supporting 100Gbps/lane data transmissions using 4-level pulse amplitude modulation (PAM-4). The silicon modulator also achieves high modulation efficiency, and it can be driven by commercially available 100Gbps/lane drivers. Figure 6b shows the optical eye diagram of an SSPRQ PAM-4 signal at 53.125Gbaud when the modulator is driven by a commercial 100G differential driver. The average optical power is 0.15dBm (after factoring in CDR splitting and connection losses) with an extinction ratio (ER) of 4.5dB at the driver's highest gain setting. The measured transmitter dispersion eye closure quaternary (TDECQ) is 1.25dB. The 100G optical signal meets IEEE 400GBASE-DR4 and 800GBASE-DR8 standard. Thermal optical phase shifters and monitor photodetectors (MPDs) are used for modulator biasing control and monitoring and the electrical connections are provided by the FOWLP. Figure 6c shows the OE frequency response of the germanium photodetectors with over 30GHz bandwidth achieved.

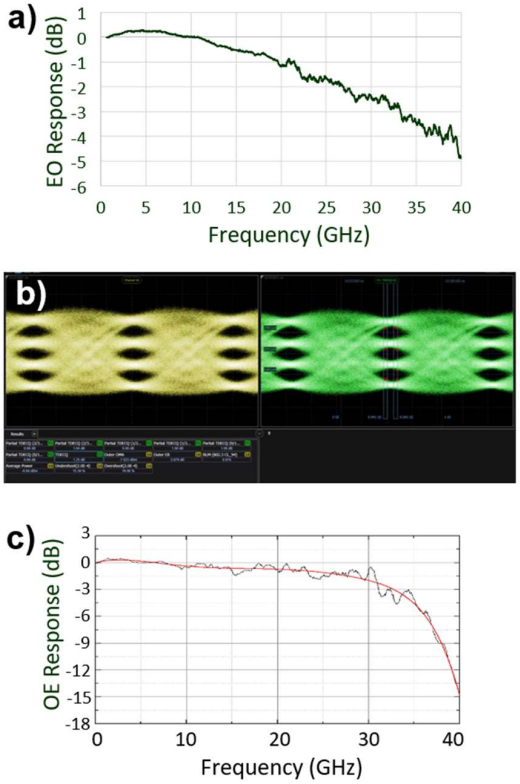

Fig. 6. a) Modulator EO bandwidth b) 100Gbps PAM-4 eye diagrams c) Waveguide germanium photodetector OE bandwidth.

The light sources, modulated optical transmitter signals and received optical signals are coupled to the PIC using an edge coupler array. The edge coupler array has a pitch of 250um, which is compatible with a standard fiber array. Furthermore, U-shaped loopback waveguides are integrated to facilitate the fiber array coupling. Moreover, vertical grating couplers provide optical access and support wafer-level testing. PIC dies can be tested at wafer level and only known-good-dies are

selected for the FOWLP process. As there are optical windows in the FOWLP dielectric film stack, wafer-level testing can also be performed on the FOWLP wafer.

D. Package Processing

A mold-first FOWLP process flow is utilized for integrating the optical engine package. The key steps in the package processing are depicted in Fig. 7. It starts with reconstituting the molded wafer from silicon dies. Here, the PIC is initially picked and placed face down on the adhesive mold plate, then undergoes compression molding to encapsulate them in resin (Fig. 8a, 8b). After the molding the measured warpage of wafers is below 200um (Fig. 8c). The wafers, after being reconstituted, are separated from the mold plate and undergo front-side RDL metal and dielectric processing (Fig. 9). The front side consists of 2 metal layers for routing and an under bump metallization (UBM) layer with exposed bond pads on which the EICs are bonded.

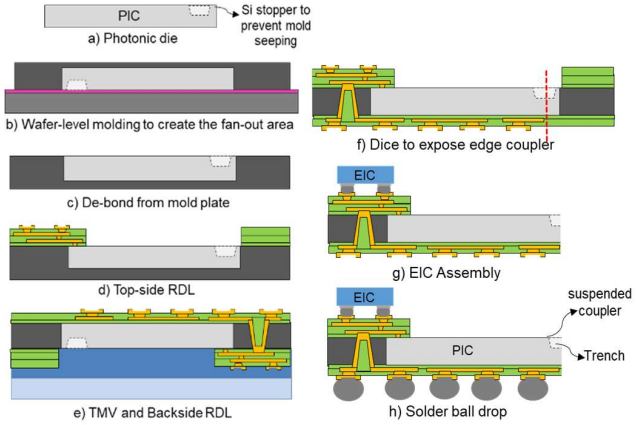

Fig. 7. Process flow to integrate the optical engine package with PIC embedded in the mold with edge optical coupling and EIC flip-chipped on its surface.

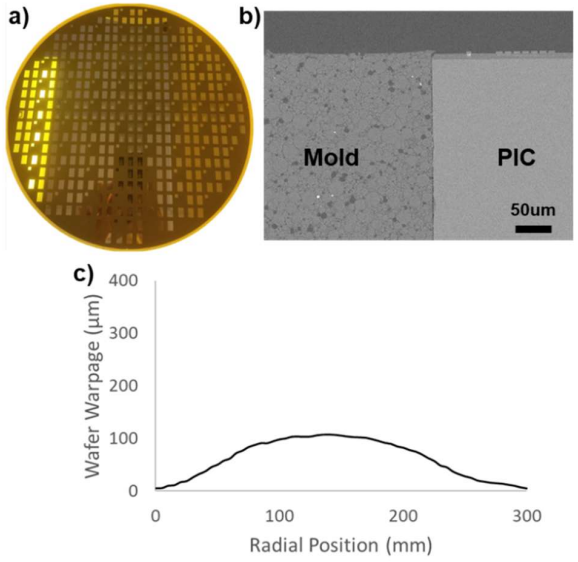

Fig. 8. a) Reconstituted wafer after molding where the PIC are embedded inside the mold compound. b) Cross-sectional image of a reconstituted wafer showing the PIC and mold. c) Warpage Plot of the wafer after molding process.

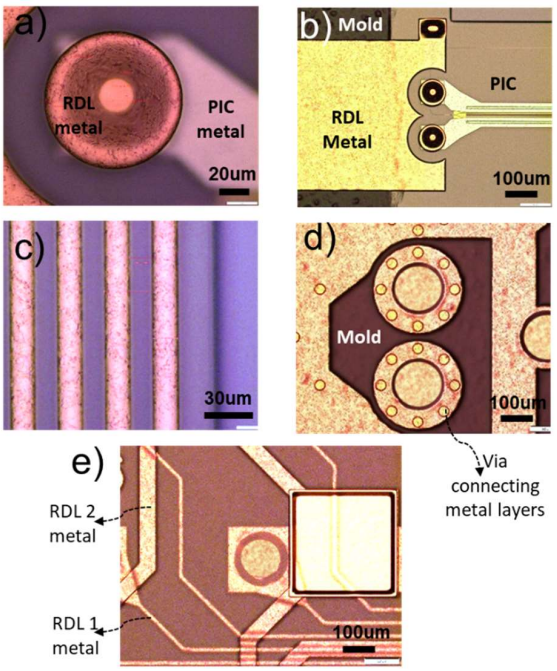

Fig. 9. Images of package RDL processing a) via connecting PIC metal to package RDL metal. b) Metal connecting PIC to the fanout area. c) Package metal interconnects with line/space of 15um/15um d) high-speed metal interconnects from modulators on mold area. e) image showing RDL 1 and RDL 2 metal.

After the front-side processing, the wafer thickness is reduced to 300um or less through back grinding before proceeding with TMV and back-side RDL processing. TMVs serve as vertical metal interconnects connecting the package's front side to its backside (Fig. 10). Backside RDL consists of one metal layer and UBM.

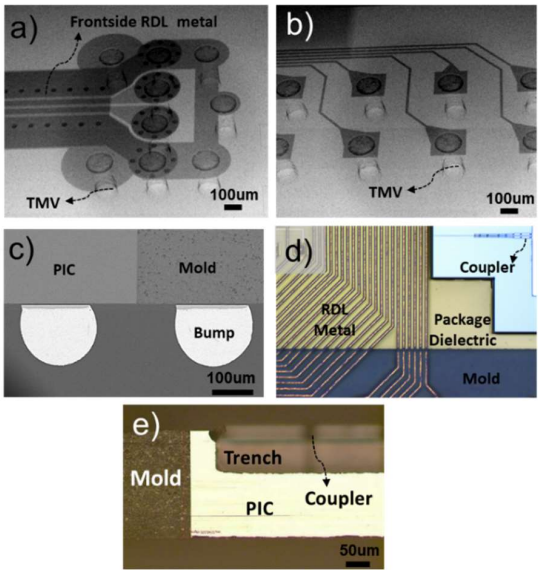

Fig. 10. Vertical interconnects, through mold vias a) for high-speed I/O b) for DC. c) Cross-sectional image of package backside bumps. d) Front side of the package showing optical coupler at package edge e) Optical I/O side diced to expose couplers

For a contamination-free coupler, a specially designed silicon buffer structure around the trench is added to the PIC design [8, 9]. This structure protects the optical couplers during the molding process by acting like a dam-like structure that prevents the mold from entering the deep trench. The wafer is diced along deep trenches to reveal the edge optical couplers (Fig. 10d) before being assembled with solder balls and EICs.

E. OE coupling efficiency

Suspended optical couplers employed in this work provide better coupling performance compared to vertical grating couplers or edge couplers without cantilever structures exhibiting good chip facet to fiber coupling losses. To examine the optical connection of the edge couplers, U-shaped loopback waveguides with a 250um pitch are integrated at the PIC edge and evaluated using an external fiber optic array. Optical connection tests showed <2dB/facet loss after packaging (Fig. 11).

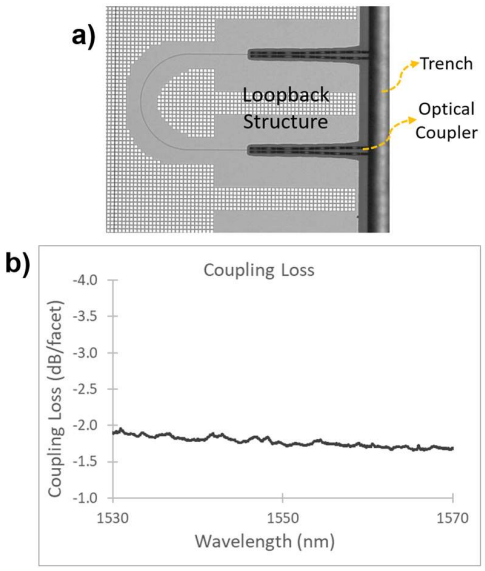

Fig. 11. a) Loopback structures through which the fibre-to-optical engine package coupling loss is measured. b) Measured optical coupling loss.

III. CONCLUSIONS

For modern data center infrastructure, higher capacity, low power and cost-efficient optical transceivers are required. This paper presents a new electronic-photonic integration platform demonstrated using a compact high-performance 800Gbps OE test vehicle suitable for hyperscale data centers. It is based on fan-out wafer-level packaging that can be mass-produced cost-effectively compared to other platforms such as those based on monolithic solutions. It covers critical aspects such as photonic IC, OE package processing, the integration of edge couplers, and its testing. Being able to be integrated at wafer scale, makes it a low-cost, manufacturable versatile package platform that can meet the requirements of modern data center infrastructure.

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REFERENCES

[1] H. Hsia et al., "Heterogeneous Integration of a Compact Universal Photonic Engine for Silicon Photonics Applications in HPC," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2021, pp. 263-268, doi: 10.1109/ECTC32696.2021.00052.

[2] Cisco, Annual internet report (2018–2023). Cisco (2020)

[3] A. V. Krishnamoorthy et al., "Progress in Low-Power Switched Optical Interconnects," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 17, no. 2, pp. 357-376, March-April 2011, doi: 10.1109/JSTQE.2010.2081350.

[4] N. D. Heidel, N. G. Usechak, C. L. Dohrman and J. A. Conway, "A Review of Electronic-Photonic Heterogeneous Integration at DARPA," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 22, no. 6, pp. 482-490, Nov.-Dec. 2016, Art no. 8300209, doi: 10.1109/JSTQE.2016.2577541.

[5] J. Xue et al., "Trends and Challenges in Advanced Packaging Development for Silicon Photonics Beyond 400Gbps in Hyperscale Data Center Networking Applications," 2022 6th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), Oita, Japan, 2022, pp. 148-150, doi: 10.1109/EDTM53872.2022.9798331.

[6] Minkenberg, C., Krishnaswamy, R., Zilkie, A. and Nelson, D. (2021), Co-packaged datacenter optics: Opportunities and challenges. IET Optoelectron, 15: 77-91. https://doi.org/10.1049/ote2.12020

[7] S. B. N. Gourikutty et al., "A Novel Packaging Platform for High-Performance Optical Engines in Hyperscale Data Center Applications," 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), San Diego, CA, USA, 2022, pp. 422-427, doi: 10.1109/ECTC51906.2022.00074.

[8] Lim et al., 'Photonic integrated circuit package and method of forming the same', US Patent 10,989,887 B2, 2021.

[9] S. B. N. Gourikutty et al., "Towards Heterogeneous Integrated Electronic-Photonic Packages for Hyperscale Data Centers," 2021 IEEE 23rd Electronics Packaging Technology Conference (EPTC), Singapore, Singapore, 2021, pp. 37-41, doi: 10.1109/EPTC53413.2021.9663971.