Alexandria University
Faculty of Engineering
Computer and Systems Engineering Dept.
Third Year



Computer Architecture Spring 2019 Assigned: 11th April 2019

Due: 25th April 2019

Cache Simulator

Overview

In this assignment, you will use a cache simulator to simulate different types of caches. The purpose of this assignment is to directly involve you in the different factors affecting cache performance. You are provided with a working version of a cache simulator, your job is to simulate the output for several important cache measurements.

Background

In this assignment, you'll use the cache simulator provided by the University of Massachusetts Amherst:

http://www.ecs.umass.edu/ece/koren/architecture/Cache/frame1.htm

The simulator provides the following functionalities:

- 1. The simulator reads-in a memory access pattern.
- 2. Customizable the cache size and the number of sets.
- 3. Customize the replacement policy: LRU (least recently used), FIFO (first in, first out), RAND (random replacement).
- 4. The ability to report the total number of cache queries, total misses, miss rate, cache hits, and hit rate, as well as the cache query sequence trace.

Requirements

Using the provided cache simulator, you should run the following tests:

- For the block addresses in the attached file, graph the total hit rate and miss rate for a cache of size 256 blocks for the following number of sets: 1, 2, 4, 8, 16, 32, 64, 128 and 256.
- Repeat the previous experiment for caches of size 128, 64, and 32 blocks (update the number of sets such that the maximum number of sets is less than or equal the total number of blocks in the cache).
- Suppose a computer has a 4-way set associative cache, and the cache size is 64 blocks, show the final cache contents and state the number of hits and misses for the following sequence of block addresses: 2, 16, 24, 32, 16, 24, 64, 48, 6 (Assume LRU replacement policy).

• Show the hits and misses and final cache contents for a two-way set-associative cache with one-word blocks and a total size of 16 words, Assume LRU replacement. Assume the word addresses are: 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6, 9, 17.

Submission Instructions

Please submit a report including the results for the tests above with your name as well as your student ID.