CENTER OF NANOELECTRONICS & DEVICES

CND 211: Advanced Digital Design

Complete ASIC Flow of I2C communication protocol

Section #: 19

Submitted by:

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Date: 19/5/2024

I2C protocol Introduction :

- The I2C (Inter-Integrated Circuit) protocol is a serial communication protocol that allows multiple “peripheral” digital integrated circuits (“chips”) to communicate with one or more “controller” chips
- I2C is a two wire serial communication protocol using a serial data line (SDA) and a serial clock line (SCL)
- Ideal for applications needing occasional communication over short distances
- Enables communication between multiple devices as a true multi-master bus.

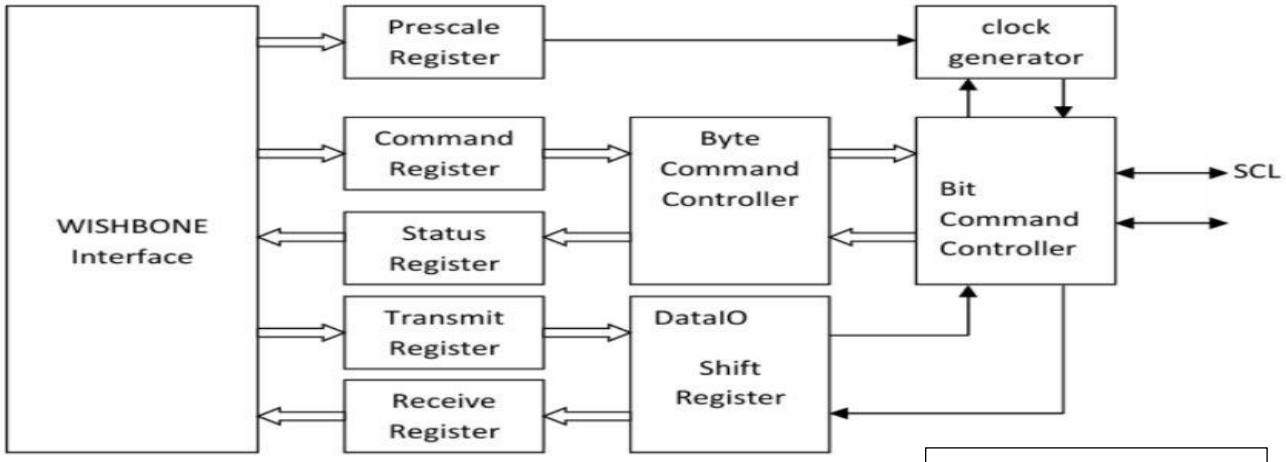
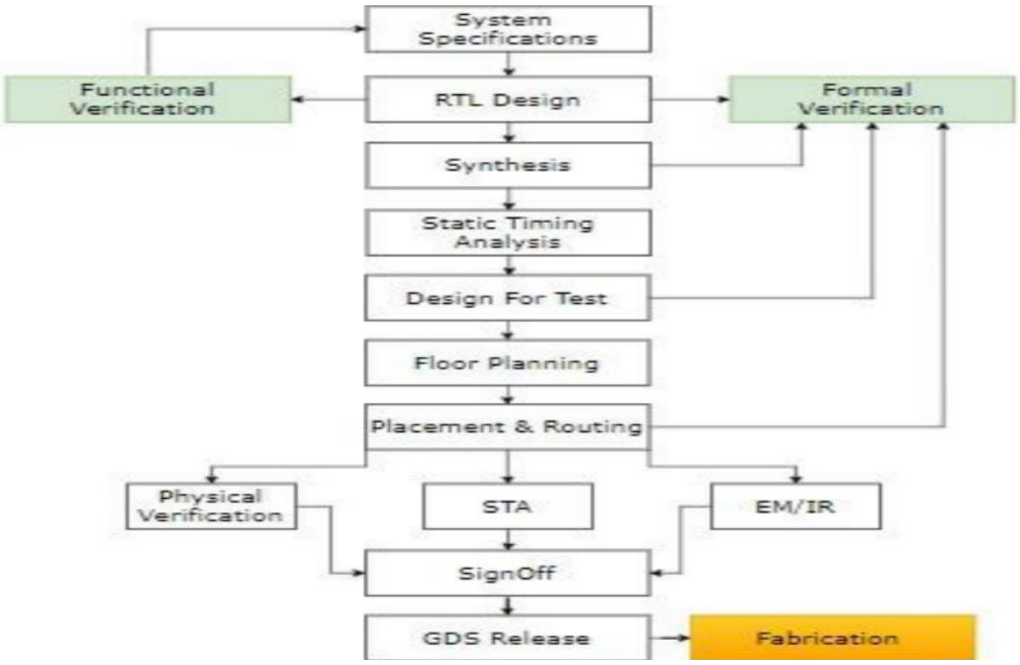


Figure_1:Internal structure of I2C

Full flow:



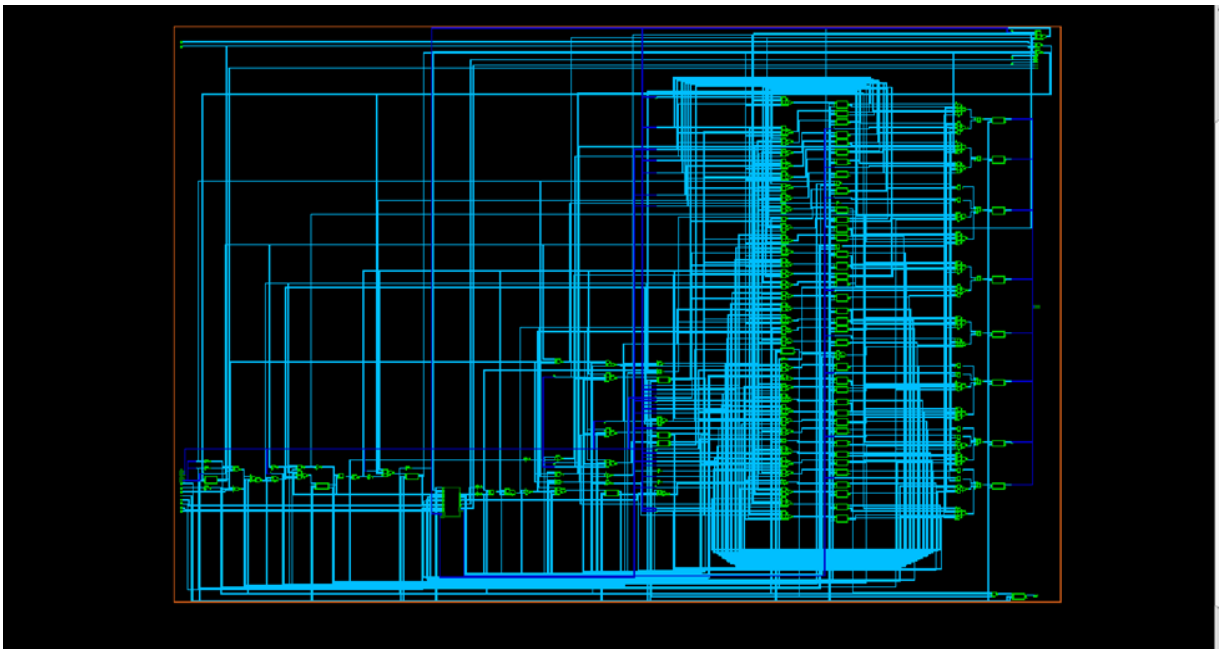
Synthesis flow:

In this stage, the high-level RTL code is transformed into an optimized gate-level representation using a standard cell library and design constraints , reports on timing, power, and area are generated during this step

Required Constraints:

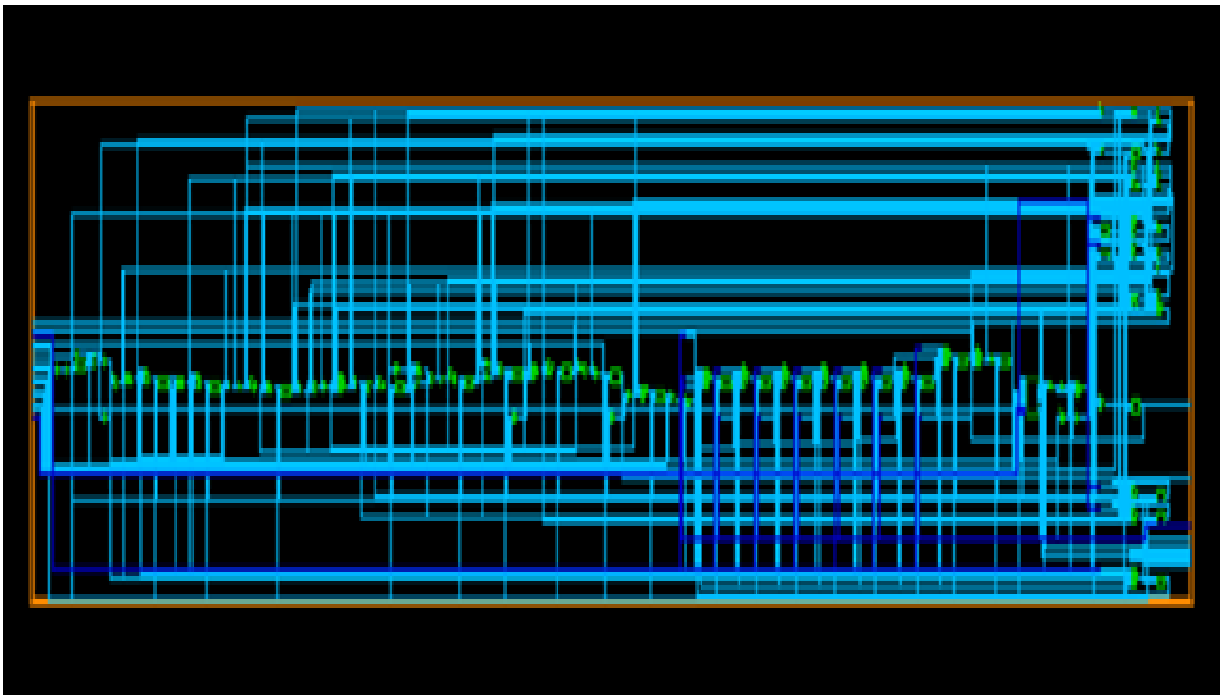
Parmeter	Value
Clock_Uncertainty	0.3
Transition	0.2
Clock_latency	0.25
Input_delay	10 % Clk_period
Output_delay	10 %Clk_period

The Top module RTL after synthesis :

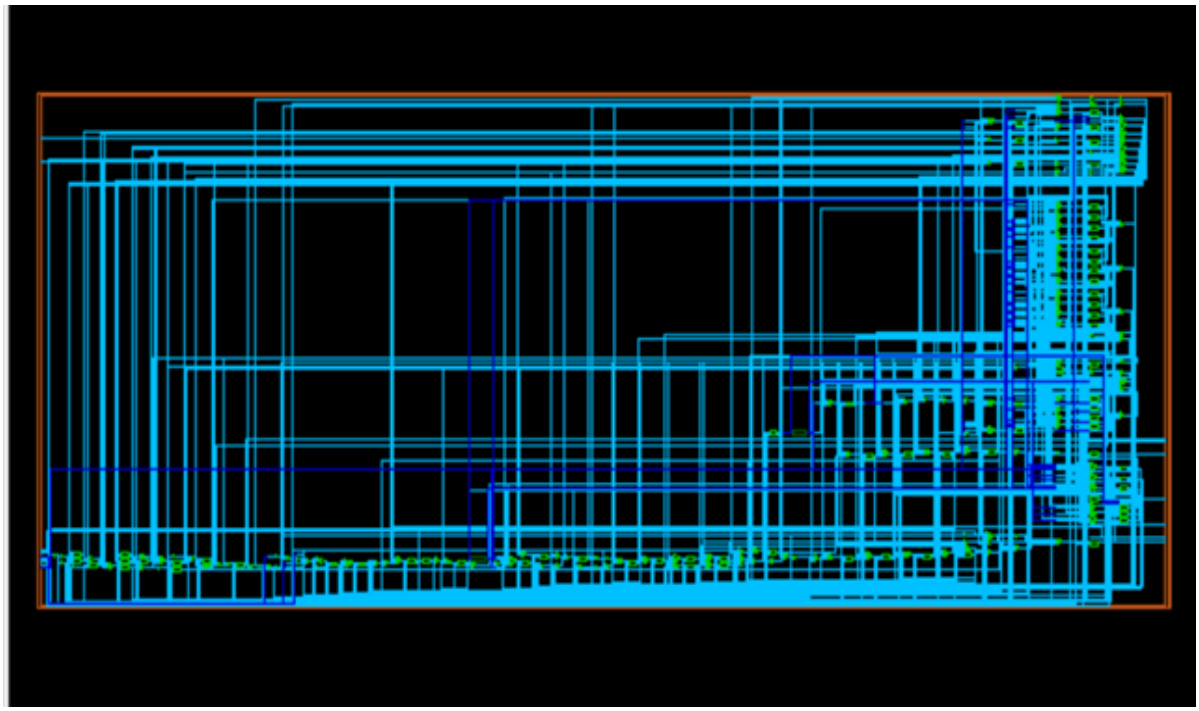


Blocks :

Byte block:



Bit block :



Timing Reports

Worst-case Setup path after synthesis:

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Open setup.rpt ~/logic_project/syn/syn_results/syn_reports Save

```
Point                                                  Fanout       Cap      Trans      Incr       Path
-------------------------------------------------------------------------------------------------------
clock clk (rise edge)                                                                   0.00       0.00
clock network delay (ideal)                                                             0.00       0.00
input external delay                                                                    2.00       2.00 r
wb_rst_i (in)                                                                 0.20      0.00       2.00 r
wb_rst_i (net)                                          25        64.90               0.00       2.00 r
byte_controller/rst (i2c_master_byte_ctrl)                                              0.00       2.00 r
byte_controller/rst (net)                                         64.90               0.00       2.00 r
byte_controller/bit_controller/rst (i2c_master_bit_ctrl)                                0.00       2.00 r
byte_controller/bit_controller/rst (net)                          64.90               0.00       2.00 r
byte_controller/bit_controller/U7/INP (INVX0)                                 0.20      0.16       2.16 r
byte_controller/bit_controller/U7/ZN (INVX0)                                  0.15      0.10       2.27 f
byte_controller/bit_controller/n38 (net)                9         18.33               0.00       2.27 f
byte_controller/bit_controller/U43/IN4 (NAND4X0)                              0.15      0.09       2.35 f
byte_controller/bit_controller/U43/QN (NAND4X0)                               0.34      0.19       2.55 r
byte_controller/bit_controller/N66 (net)               19         40.11               0.00       2.55 r
byte_controller/bit_controller/U49/IN2 (NOR2X0)                               0.34      0.16       2.71 r
byte_controller/bit_controller/U49/QN (NOR2X0)                                0.28      0.20       2.91 f
byte_controller/bit_controller/n4 (net)                17         31.99               0.00       2.91 f
byte_controller/bit_controller/U27/IN1 (NOR2X0)                               0.28      0.13       3.05 f
byte_controller/bit_controller/U27/QN (NOR2X0)                                0.35      0.20       3.24 r
byte_controller/bit_controller/n6 (net)                16         34.61               0.00       3.24 r
byte_controller/bit_controller/U34/IN4 (AO222X1)                              0.35      0.13       3.37 r
byte_controller/bit_controller/U34/Q (AO222X1)                                0.05      0.13       3.50 r
byte_controller/bit_controller/n183 (net)               1          1.49               0.00       3.50 r
byte_controller/bit_controller/cnt_reg_0_/D (DFFARX1)                         0.05      0.03       3.54 r
data arrival time                                                                                  3.54

clock clk (rise edge)                                                                  20.00      20.00
clock network delay (ideal)                                                             0.00      20.00
clock uncertainty                                                                      -0.30      19.70
byte_controller/bit_controller/cnt_reg_0_/CLK (DFFARX1)                                 0.00      19.70 r
library setup time                                                                     -0.07      19.63
data required time                                                                                 19.63
-------------------------------------------------------------------------------------------------------
data required time                                                                                 19.63
data arrival time                                                                                  -3.54
-------------------------------------------------------------------------------------------------------
slack (MET)                                                                                        16.10
```

Best-case Setup path after synthesis:

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Open hold.rpt ~/logic_project/syn/syn_results/syn_reports Save

setup.rpt hold.rpt

```
Design : i2c_master_top
Version: O-2018.06-SP1
Date   : Mon May 20 01:41:27 2024
****************************************

Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: enclosed

  Startpoint: byte_controller/bit_controller/scl_oen_reg
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: byte_controller/bit_controller/dscl_oen_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  i2c_master_top     16000                 saed90nm_typ

  Point                                   Fanout       Cap     Trans      Incr       Path
  ----------------------------------------------------------------------------------------
  clock clk (rise edge)                                                    0.00       0.00
  clock network delay (ideal)                                              0.00       0.00
  byte_controller/bit_controller/scl_oen_reg/CLK (DFFASX1)          0.20       0.00       0.00 r
  byte_controller/bit_controller/scl_oen_reg/Q (DFFASX1)            0.03       0.22       0.22 f
  byte_controller/bit_controller/scl_oen (net)     3      3.43                0.00       0.22 f
  byte_controller/bit_controller/dscl_oen_reg/D (DFFX1)             0.03       0.04       0.26 f
  data arrival time                                                                     0.26

  clock clk (rise edge)                                                    0.00       0.00
  clock network delay (ideal)                                              0.00       0.00
  clock uncertainty                                                        0.30       0.30
  byte_controller/bit_controller/dscl_oen_reg/CLK (DFFX1)                  0.00       0.30 r
  library hold time                                                        0.02       0.32
  data required time                                                                    0.32
  ----------------------------------------------------------------------------------------
  data required time                                                                    0.32
  data arrival time                                                                    -0.26
  ----------------------------------------------------------------------------------------
  slack (VIOLATED)                                                                     -0.06
```

- We can proceed with negative hold slack until CTS step

Clock report:

Open clocks.rpt ~/logic_project/syn/syn_results/syn_reports Save

```
****************************************
Report : clocks
Design : i2c_master_top
Version: O-2018.06-SP1
Date   : Mon May 20 01:41:27 2024
****************************************

Attributes:
    d - dont_touch_network
    f - fix_hold
    p - propagated_clock
    G - generated_clock
    g - lib_generated_clock

Clock          Period   Waveform           Attrs     Sources
------------------------------------------------------------------------------
clk             20.00   {0 10}                       {wb_clk_i}
------------------------------------------------------------------------------
1
```

Area report after synthesis:

Open | *area.rpt ~/logic_project/syn/syn_results/syn_reports | Save

setup.rpt | hold.rpt | *area.rpt

```
****************************************

Library(s) Used:

    saed90nm_typ (File: /home/ICer/logic_project/DB/saed90nm_typ.db)

Number of ports:                          185
Number of nets:                           825
Number of cells:                          583
Number of combinational cells:            422
Number of sequential cells:               157
Number of macros/black boxes:               0
Number of buf/inv:                         69
Number of references:                      21

Combinational area:               3771.187194
Buf/Inv area:                      390.758410
Noncombinational area:            4827.340860
Macro/Black Box area:                0.000000
Net Interconnect area:             514.908246

Total cell area:                  8598.528054
Total area:                       9113.436300

Hierarchical area distribution
------------------------------

                                  Global cell area          Local cell area
                                  ------------------  ----------------------------
Hierarchical cell                 Absolute   Percent  Combi-     Noncombi-  Black-
                                  Total      Total    national   national   boxes   Design
--------------------------------  ---------  -------  ---------  ---------  ------  ------------------------------
i2c_master_top                    8598.5281    100.0  1117.9008  1660.7232  0.0000  i2c_master_top
byte_controller                   5819.9040     67.7   695.8080   806.4000  0.0000  i2c_master_byte_ctrl
byte_controller/bit_controller    4317.6960     50.2  1371.3408  2360.2176  0.0000  i2c_master_bit_ctrl
byte_controller/bit_controller/sub_228  314.2656     3.7  314.2656    0.0000 0.0000 i2c_master_bit_ctrl_DW01_dec_1
byte_controller/bit_controller/sub_260  271.8720     3.2  271.8720    0.0000 0.0000 i2c_master_bit_ctrl_DW01_dec_0
--------------------------------  ---------  -------  ---------  ---------  ------  ------------------------------
Total                                                  3771.1872  4827.3409  0.0000

1
```

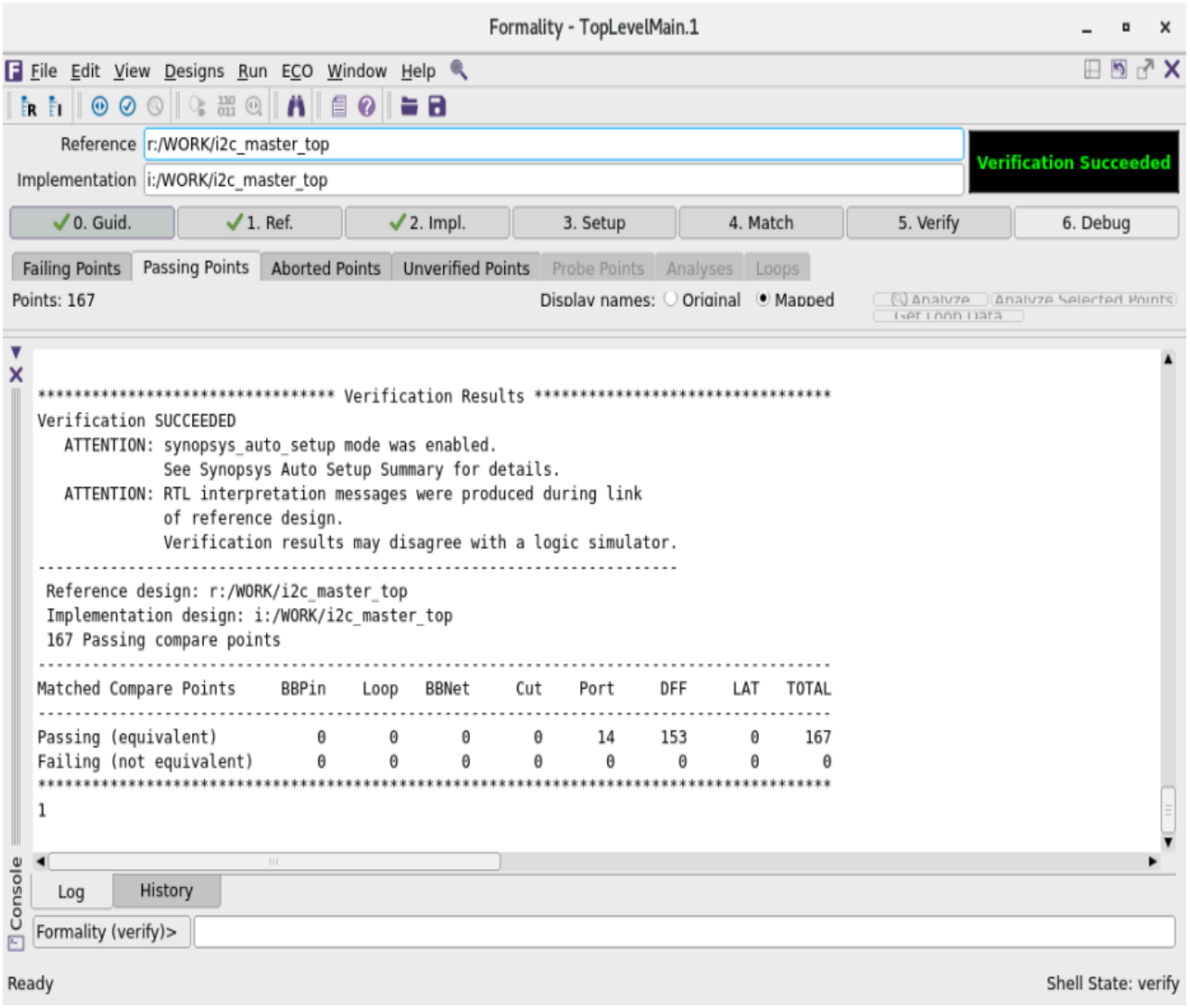
Plain Text | Tab Width: 8 | Ln 1, Col 1 | INS

Power report after synthesis:

```
Library(s) Used:

    saed90nm_typ (File: /home/ICer/logic_project/DB/saed90nm_typ.db)


Operating Conditions: TYPICAL   Library: saed90nm_typ
Wire Load Model Mode: enclosed

Design        Wire Load Model            Library
------------------------------------------------
i2c_master_top         16000             saed90nm_typ
i2c_master_byte_ctrl   8000              saed90nm_typ
i2c_master_bit_ctrl    8000              saed90nm_typ
i2c_master_bit_ctrl_DW01_dec_0 8000      saed90nm_typ
i2c_master_bit_ctrl_DW01_dec_1 8000      saed90nm_typ


Global Operating Voltage = 1.2
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000ff
    Time Units = 1ns
    Dynamic Power Units = 1uW    (derived from V,C,T units)
    Leakage Power Units = 1pW


--------------------------------------------------------------------------------
                                    Switch   Int      Leak     Total
Hierarchy                           Power    Power    Power    Power    %
--------------------------------------------------------------------------------
i2c_master_top                        4.879    5.949 3.38e+07   44.611 100.0
  byte_controller (i2c_master_byte_ctrl)    3.545    4.060 2.31e+07   30.672  68.8
    bit_controller (i2c_master_bit_ctrl)    2.729    3.595 1.74e+07   23.738  53.2
      sub_228 (i2c_master_bit_ctrl_DW01_dec_1)    0.406    0.530 1.16e+06    2.093   4.7
      sub_260 (i2c_master_bit_ctrl_DW01_dec_0) 6.43e-03 1.05e-02 8.67e+05    0.884   2.0
1
```

Formality:

- In this step the RTL description is compared against the synthesized netlist using formal verification tools like Synopsys Formality



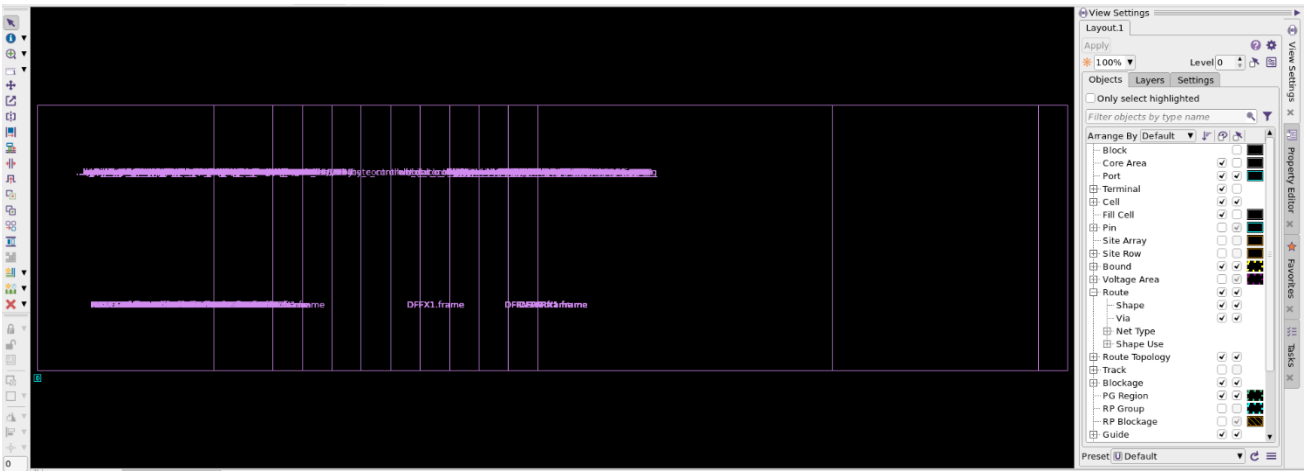
PnR Flow:

Library manager

- in this step we prepare the library files that ICC2 required to start PnR flow (.ndm) through using our technology files (.lib , .lef, .db,.tech)

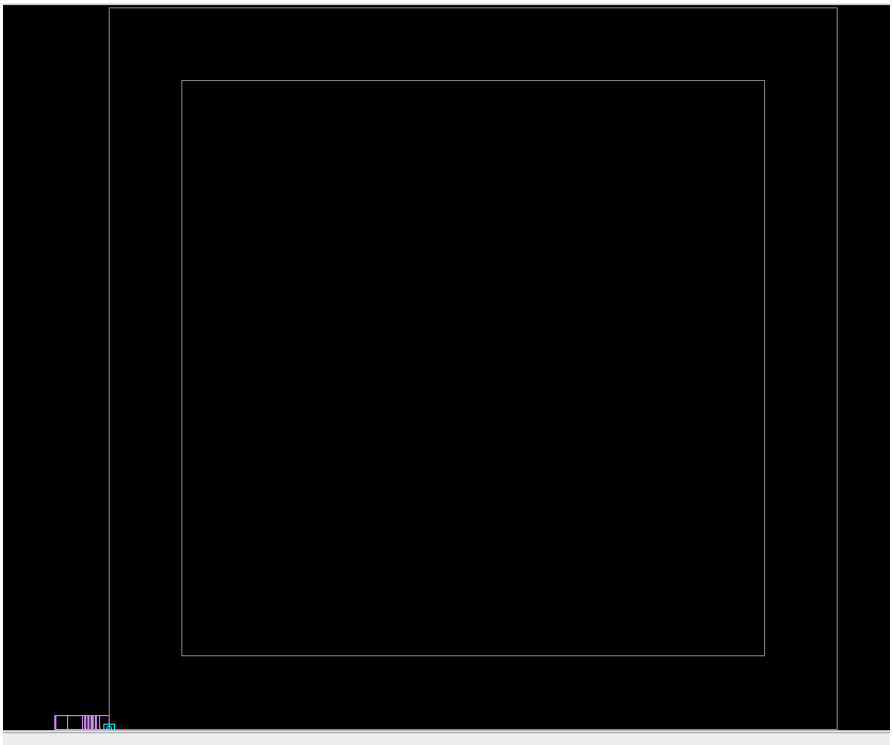
Design setup:

- in this step we only set all search paths we will need and create our library “which is .ndm library we created in the previous step” then reading our netlist from synthesis and link all this



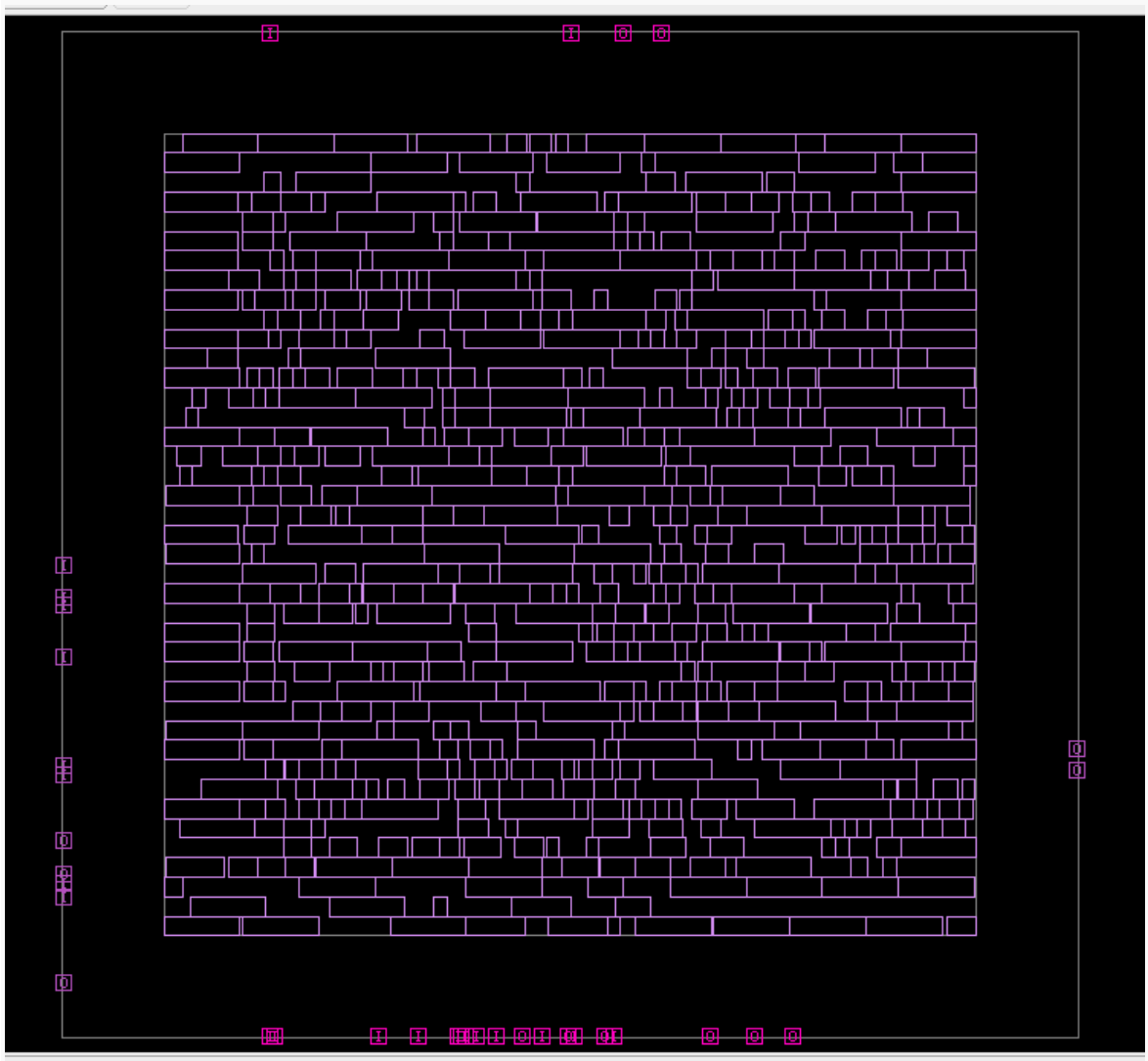
Floor_Planning:

- Floor planning is a critical step in the physical design process. It establishes the overall chip layout During the data set up and floor planning, the output of the icc2 from the GUI
- Utilization = 0.6



Initial _ placement:

- Initial placement, also known as global placement, is a crucial step in the physical design of an ASIC. It involves placing standard cells (the building blocks of the chip) within the core boundary.
- The goal is to find an optimal location for each standard cell, considering factors like timing, congestion, and area utilization.



Worst-case setup path after initial placement:

Open | setup_initial_placement.rpt — ~/logic_project/PnR/report | Save

Point	Fanout	Cap	Trans	Incr	Path
clock clk (rise edge)				0.00	0.00
clock network delay (ideal)				0.00	0.00
input external delay				2.00	2.00
wb_rst_i (in)			0.20	0.00	2.00 r
wb_rst_i (net)	25	108.19			
byte_controller/bit_controller/U7/INP (INVX0)			0.20	0.01	2.01 r
byte_controller/bit_controller/U7/ZN (INVX0)			0.23	0.15	2.16 f
byte_controller/bit_controller/n380 (net)	9	35.28			
byte_controller/bit_controller/U43/IN4 (NAND4X0)			0.23	0.00	2.16 f
byte_controller/bit_controller/U43/QN (NAND4X0)			0.52	0.29	2.45 r
byte_controller/bit_controller/N66 (net)	19	63.84			
byte_controller/bit_controller/U49/IN2 (NOR2X0)			0.52	0.00	2.45 r
byte_controller/bit_controller/U49/QN (NOR2X0)			0.45	0.32	2.77 f
byte_controller/bit_controller/n4 (net)	17	53.52			
byte_controller/bit_controller/U27/IN1 (NOR2X0)			0.45	0.00	2.77 f
byte_controller/bit_controller/U27/QN (NOR2X0)			0.53	0.30	3.07 r
byte_controller/bit_controller/n6 (net)	16	54.23			
byte_controller/bit_controller/U14/IN4 (AO222X1)			0.53	0.00	3.07 r
byte_controller/bit_controller/U14/Q (AO222X1)			0.07	0.16	3.23 r
byte_controller/bit_controller/n173 (net)	1	4.29			
byte_controller/bit_controller/cnt_reg_10_/D (DFFARX1)			0.07	0.00	3.23 r
data arrival time					3.23
clock clk (rise edge)				20.00	20.00
source latency				0.00	20.00
wb_clk_i (in)			0.20	0.00	20.00 r
wb_clk_i (net)	153	366.14			
byte_controller/bit_controller/cnt_reg_10_/CLK (DFFARX1)			0.20	0.00	20.00 r
clock uncertainty				-0.30	19.70
library setup time				-0.07	19.63
data required time					19.63
data required time					19.63
data arrival time					-3.23
slack (MET)					16.40

Worst-case hold path after synthesis:

Open | hold_initial_placement.rpt ~/logic_project/PnR/report | Save

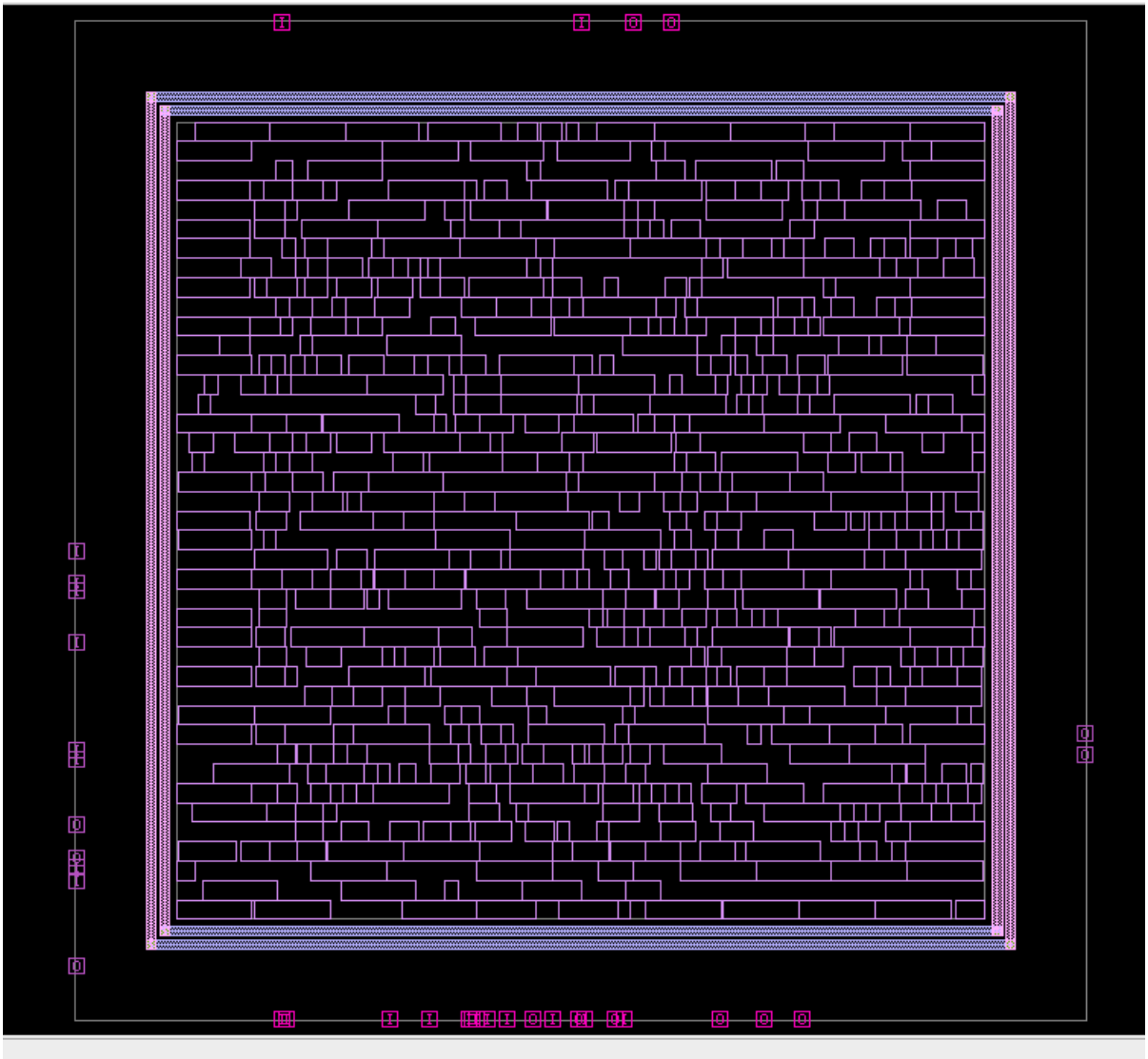
```
  Startpoint: wb_ack_o_reg (rising edge-triggered flip-flop clocked by clk)
  Endpoint: wb_ack_o_reg (rising edge-triggered flip-flop clocked by clk)
  Mode: default
  Corner: default
  Scenario: default
  Path Group: clk
  Path Type: min

  Point                                    Fanout     Cap      Trans      Incr      Path

-------------------------------------------------------------------------------------------
  clock clk (rise edge)                                                  0.00      0.00
  source latency                                                         0.00      0.00
  wb_clk_i (in)                                           0.20           0.00      0.00 r
  wb_clk_i (net)                             153    366.14
  wb_ack_o_reg/CLK (DFFX1)                                0.20           0.00      0.00 r

  wb_ack_o_reg/CLK (DFFX1)                                0.20           0.00      0.00 r
  wb_ack_o_reg/QN (DFFX1)                                 0.05           0.14      0.14 f
  n4 (net)                                     1      2.38
  U112/IN2 (AND3X1)                                       0.05           0.00      0.14 f
  U112/Q (AND3X1)                                         0.03           0.07      0.22 f
  N15 (net)                                    1      2.24
  wb_ack_o_reg/D (DFFX1)                                  0.03           0.00      0.22 f
  data arrival time                                                                0.22

  clock clk (rise edge)                                                  0.00      0.00
  source latency                                                         0.00      0.00
  wb_clk_i (in)                                           0.20           0.00      0.00 r
  wb_clk_i (net)                             153    397.74
  wb_ack_o_reg/CLK (DFFX1)                                0.20           0.00      0.00 r

  clock uncertainty                                                      0.30      0.30
  library hold time                                                      0.02      0.32
  data required time                                                               0.32

-------------------------------------------------------------------------------------------
  data required time                                                               0.32
  data arrival time                                                               -0.22

-------------------------------------------------------------------------------------------
  slack (VIOLATED)                                                                -0.10
```

- We will proceed with negative hold slack

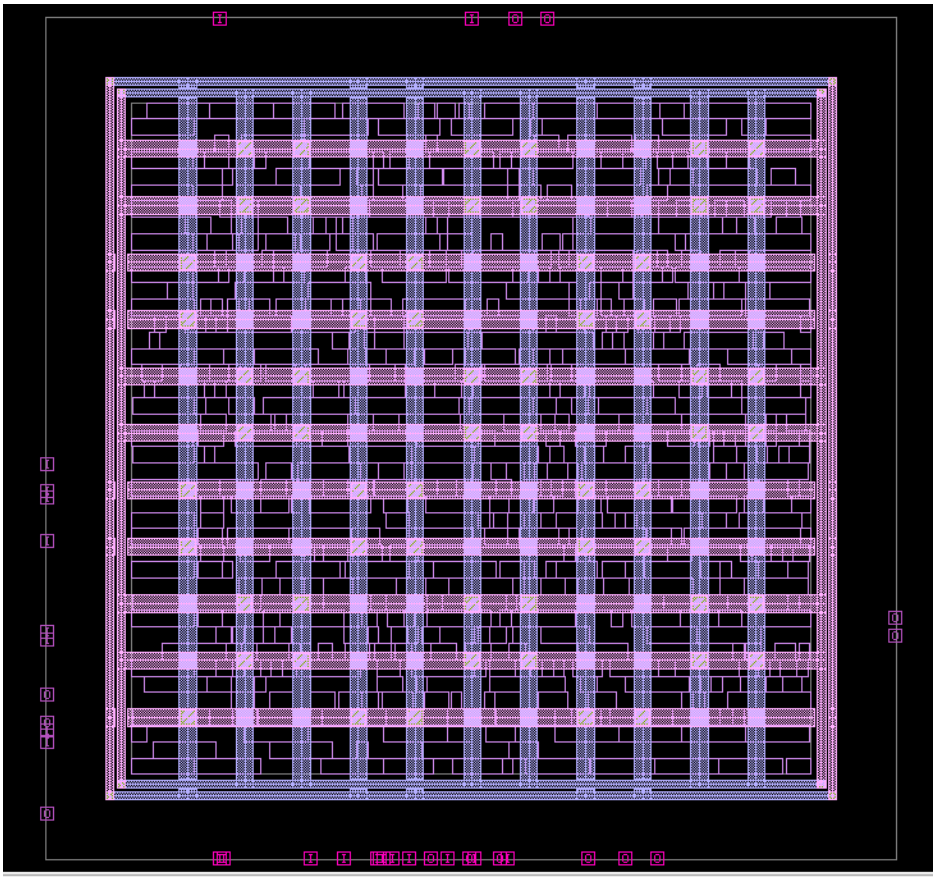
Power Planning:

- Power planning focuses on managing power distribution within the chip. It ensures that power and ground connections are robust and that the chip operates reliably.
- Metal used for power planning : M9&M8
- M1 is used for rails

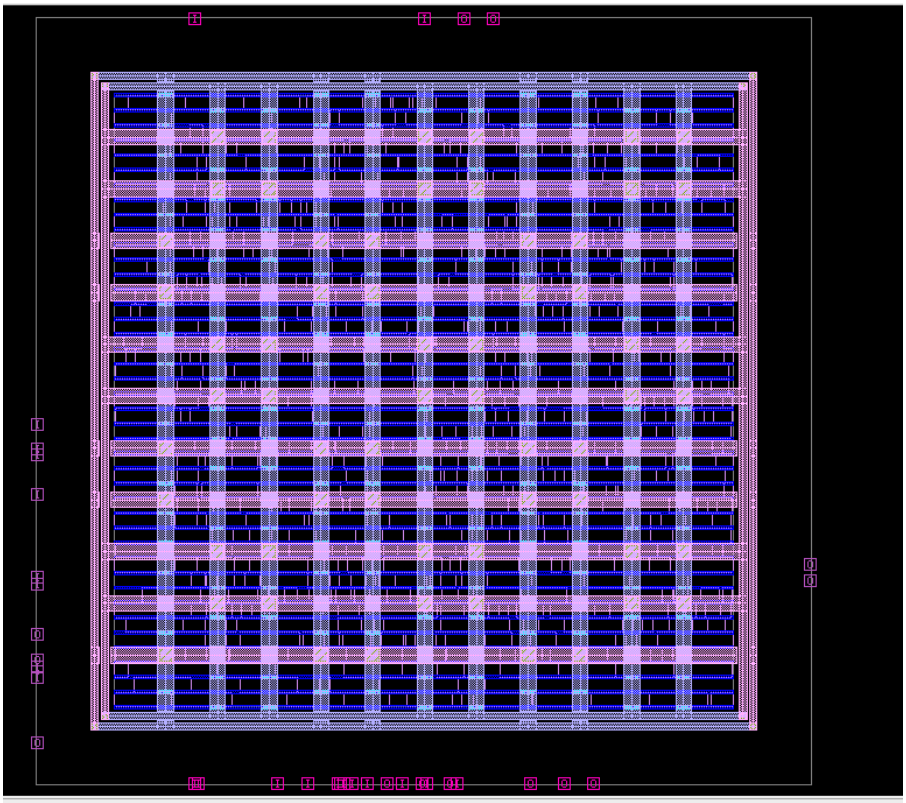
After Power Ring



After Mesh of power straps



After standard cell rail insertion



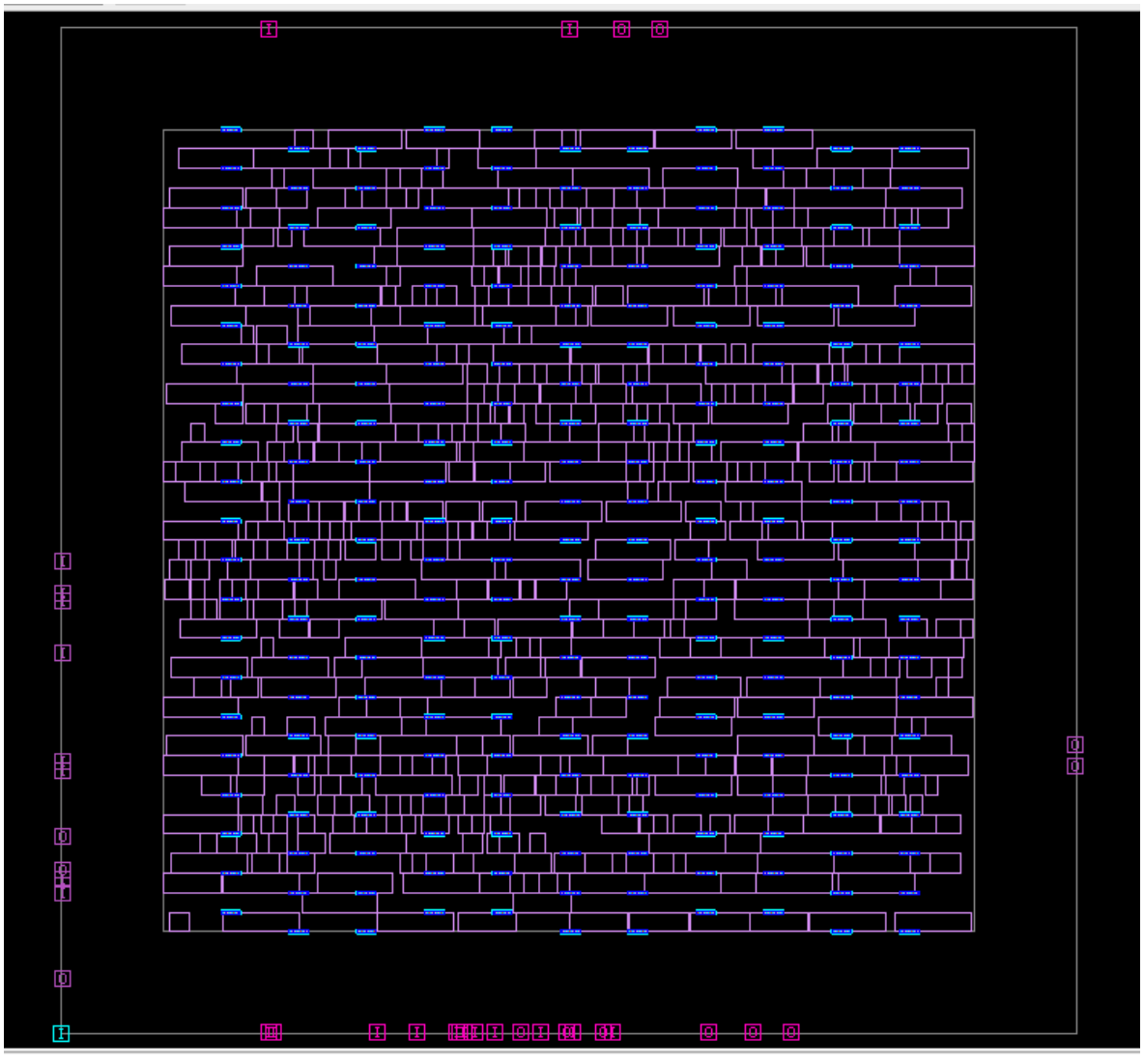
Place Opt.:

- We are hiding metals : M1,M8 and M9

- The place_opt command is used in the physical design flow of VLSI ASIC design, specifically during the placement and optimization stage. Here's a brief explanation of the commands:

  1. place_opt -from initial_place -to initial_place: This command performs coarse placement, high fanout net synthesis (HFNS), optimization, and legalization1. The tool determines an approximate location for each cell according to the timing, congestion, and multi-voltage constraints.

  2. place_opt -from initial_place -to initial_drc: This command likely performs the same operations as the previous command but with an additional step of Design Rule Checking (DRC). DRC is a process where the physical layout of a chip is checked for compliance with a series of manufacturing rules.

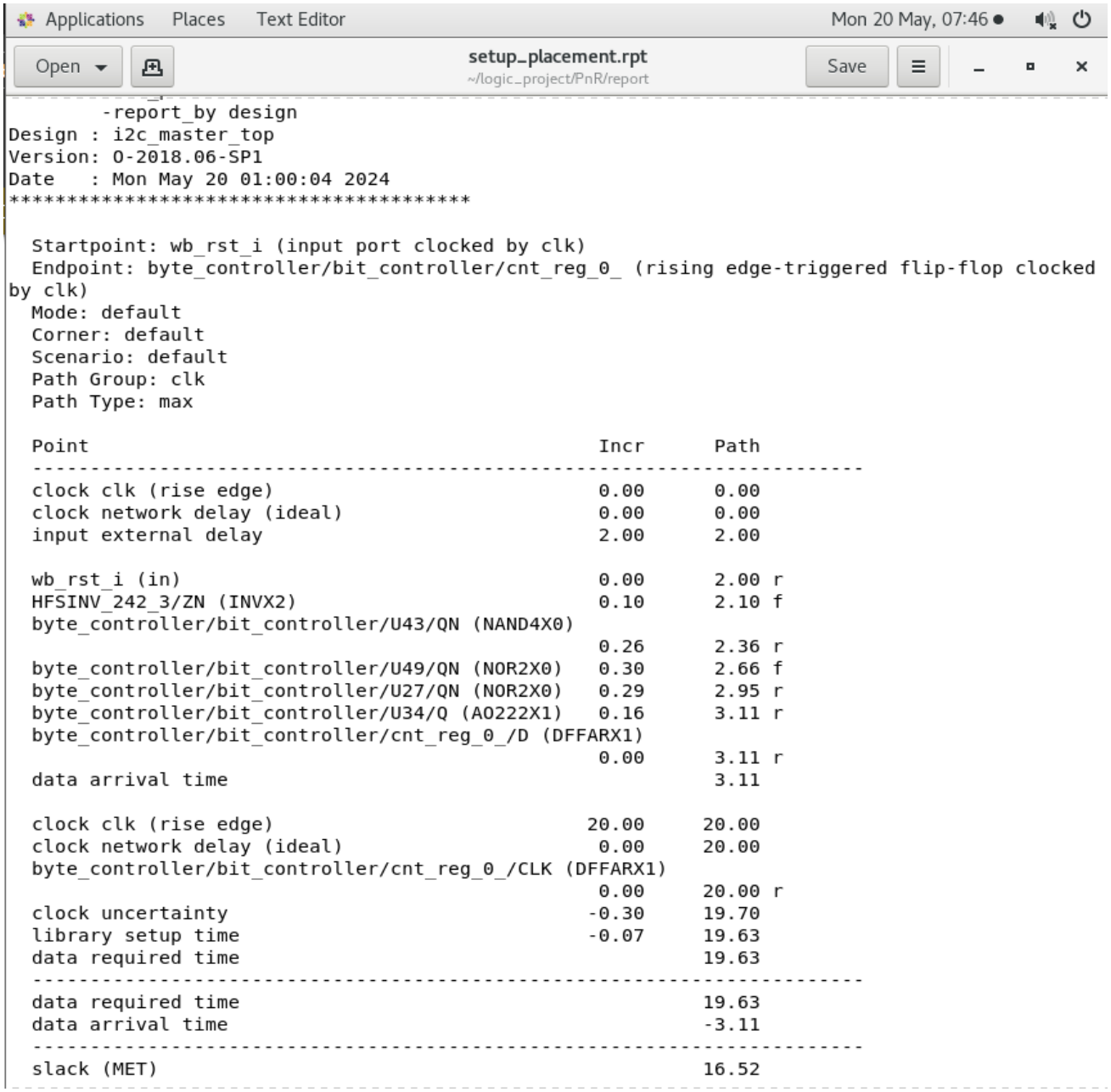


3. place_opt -from initial_drc -to initial_opto: This command takes the design from the initial DRC stage to the initial optimization stage. It likely involves further optimization of the design to improve timing, power, and area.

4. place_opt -from initial_opto -to final_place: This command takes the design from the initial optimization stage to the final placement stage. It likely involves final adjustments to the placement of cells to meet design constraints.

5. place_opt -from final_place -to final_opto: This command takes the design from the final placement stage to the final optimization stage. It likely involves final optimization of the design to meet all design constraints.

Worst-case setup path after place_opt. :




```
        -report_by design
Design : i2c_master_top
Version: O-2018.06-SP1
Date   : Mon May 20 01:00:04 2024
****************************************

  Startpoint: wb_rst_i (input port clocked by clk)
  Endpoint: byte_controller/bit_controller/cnt_reg_0_ (rising edge-triggered flip-flop clocked
by clk)
  Mode: default
  Corner: default
  Scenario: default
  Path Group: clk
  Path Type: max

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock clk (rise edge)                              0.00       0.00
  clock network delay (ideal)                        0.00       0.00
  input external delay                               2.00       2.00

  wb_rst_i (in)                                      0.00       2.00 r
  HFSINV_242_3/ZN (INVX2)                            0.10       2.10 f
  byte_controller/bit_controller/U43/QN (NAND4X0)
                                                     0.26       2.36 r
  byte_controller/bit_controller/U49/QN (NOR2X0)     0.30       2.66 f
  byte_controller/bit_controller/U27/QN (NOR2X0)     0.29       2.95 r
  byte_controller/bit_controller/U34/Q (AO222X1)     0.16       3.11 r
  byte_controller/bit_controller/cnt_reg_0_/D (DFFARX1)
                                                     0.00       3.11 r
  data arrival time                                             3.11

  clock clk (rise edge)                             20.00      20.00
  clock network delay (ideal)                        0.00      20.00
  byte_controller/bit_controller/cnt_reg_0_/CLK (DFFARX1)
                                                     0.00      20.00 r
  clock uncertainty                                 -0.30      19.70
  library setup time                                -0.07      19.63
  data required time                                           19.63
  -----------------------------------------------------------------------
  data required time                                           19.63
  data arrival time                                            -3.11
  -----------------------------------------------------------------------
  slack (MET)                                                  16.52
```

Worst-case hold path after place_opt. :

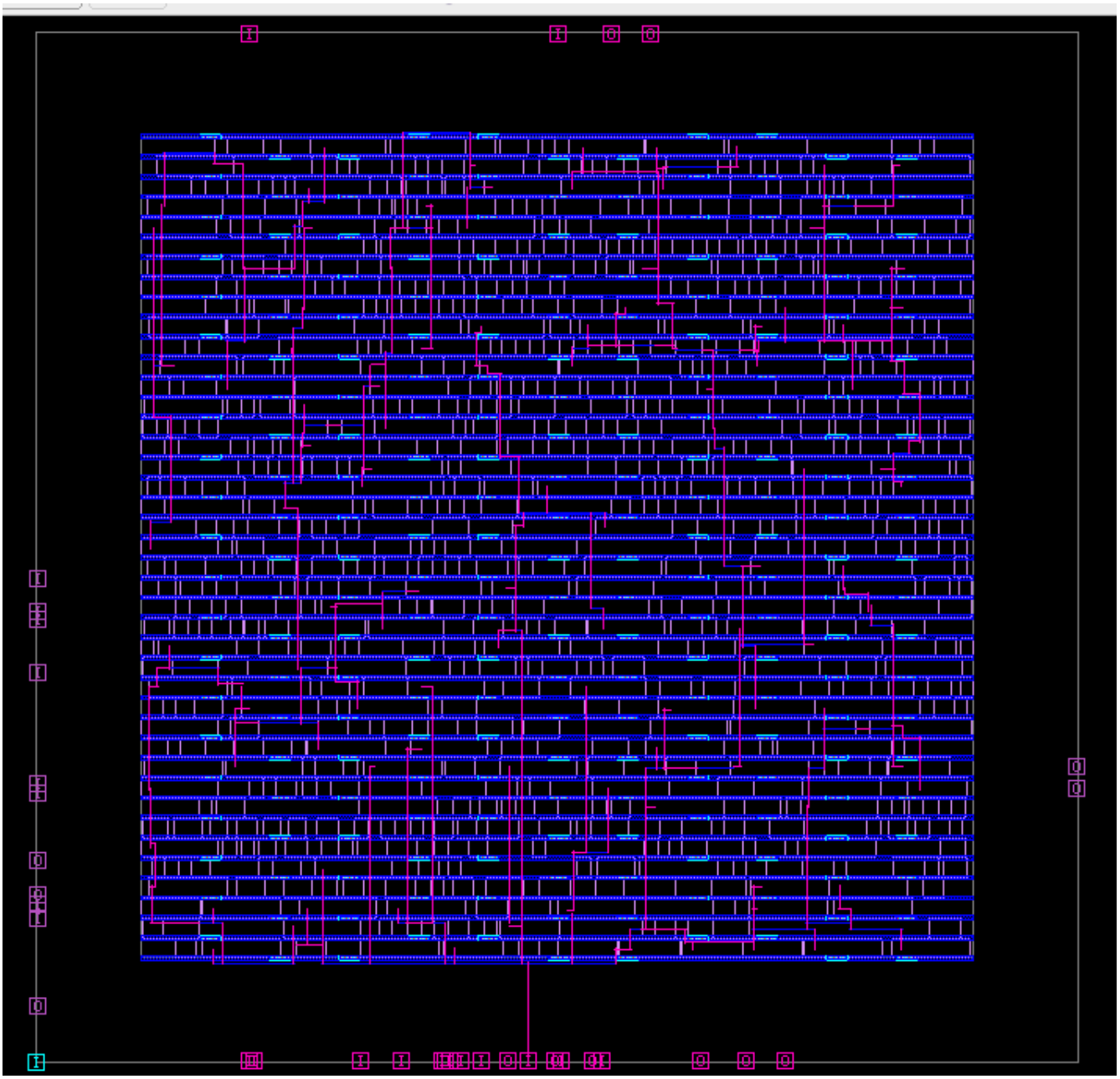
```
        -max_paths 100
        -report_by design
Design : i2c_master_top
Version: O-2018.06-SP1
Date   : Mon May 20 01:00:04 2024
****************************************

  Startpoint: byte_controller/bit_controller/cSDA_reg_0_ (rising edge-triggered flip-flop
clocked by clk)
  Endpoint: byte_controller/bit_controller/cSDA_reg_1_ (rising edge-triggered flip-flop
clocked by clk)
  Mode: default
  Corner: default
  Scenario: default
  Path Group: clk
  Path Type: min

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00

  byte_controller/bit_controller/cSDA_reg_0_/CLK (DFFARX1)
                                                          0.00       0.00 r
  byte_controller/bit_controller/cSDA_reg_0_/QN (DFFARX1)
                                                          0.16       0.16 r
  byte_controller/bit_controller/U87/QN (NOR2X0)          0.04       0.20 f
  byte_controller/bit_controller/cSDA_reg_1_/D (DFFARX1)
                                                          0.00       0.20 f
  data arrival time                                                  0.20

  clock clk (rise edge)                                   0.00       0.00
  clock network delay (ideal)                             0.00       0.00
  byte_controller/bit_controller/cSDA_reg_1_/CLK (DFFARX1)
                                                          0.00       0.00 r
  clock uncertainty                                       0.30       0.30
  library hold time                                       0.01       0.31
  data required time                                                 0.31
  ---------------------------------------------------------------------------
  data required time                                                 0.31
  data arrival time                                                 -0.20
  ---------------------------------------------------------------------------
  slack (VIOLATED)                                                  -0.11
```

- We will proceed with negative hold slack

CTS:

● Clock Tree Synthesis (CTS) is a crucial step in the physical design flow of VLSI ASIC design. It involves the automatic insertion of buffers/inverters along the clock paths of the ASIC design to balance the clock delay to all clock inputs.

● Purpose: ○ The main goal of CTS is to ensure that all the clock elements present in the design switch at the same time ○ This is achieved by balancing the clock paths, which helps to maintain minimum insertion delay and balance the skew.



Worst-case setup path after CTS :

Applications Places Text Editor Mon 20 May, 08:04

Open | setup_CTS.rpt ~/logic_project/PnR/report | Save

Point	Fanout	Cap	Trans	Incr	Path
clock clk (rise edge)				0.00	0.00
clock network delay (ideal)				0.29	0.29
input external delay				2.00	2.29
wb_rst_i (in)			0.20	0.00	2.29 r
wb_rst_i (net)	37	158.80			
HFSINV_242_3/INP (INVX0)			0.20	0.00	2.29 r
HFSINV_242_3/ZN (INVX0)			0.39	0.25	2.54 f
HFSNET_3 (net)	17	69.85			
byte_controller/bit_controller/U43/IN4 (NAND4X0)			0.39	0.00	2.54 f
byte_controller/bit_controller/U43/QN (NAND4X0)			0.57	0.34	2.88 r
byte_controller/bit_controller/N66 (net)	19	65.50			
byte_controller/bit_controller/U49/IN2 (NOR2X0)			0.57	0.00	2.88 r
byte_controller/bit_controller/U49/QN (NOR2X0)			0.45	0.32	3.21 f
byte_controller/bit_controller/n4 (net)	17	52.11			
byte_controller/bit_controller/U27/IN1 (NOR2X0)			0.45	0.00	3.21 f
byte_controller/bit_controller/U27/QN (NOR2X0)			0.53	0.30	3.51 r
byte_controller/bit_controller/n6 (net)	16	53.84			
byte_controller/bit_controller/U4/IN4 (AO222X1)			0.53	0.00	3.51 r
byte_controller/bit_controller/U4/Q (AO222X1)			0.07	0.16	3.67 r
byte_controller/bit_controller/n168 (net)	1	4.40			
byte_controller/bit_controller/cnt_reg_15_/D (DFFARX1)			0.07	0.00	3.67 r
data arrival time					3.67
clock clk (rise edge)				20.00	20.00
source latency				0.00	20.00
wb_clk_i (in)			0.63	0.25	20.25 r
wb_clk_i (net)	153	419.27			
byte_controller/bit_controller/cnt_reg_15_/CLK (DFFARX1)			0.63	0.01	20.25 r
clock reconvergence pessimism				0.00	20.25
clock uncertainty				-0.30	19.95
library setup time				-0.09	19.87
data required time					19.87
data required time					19.87
data arrival time					-3.67
slack (MET)					16.20

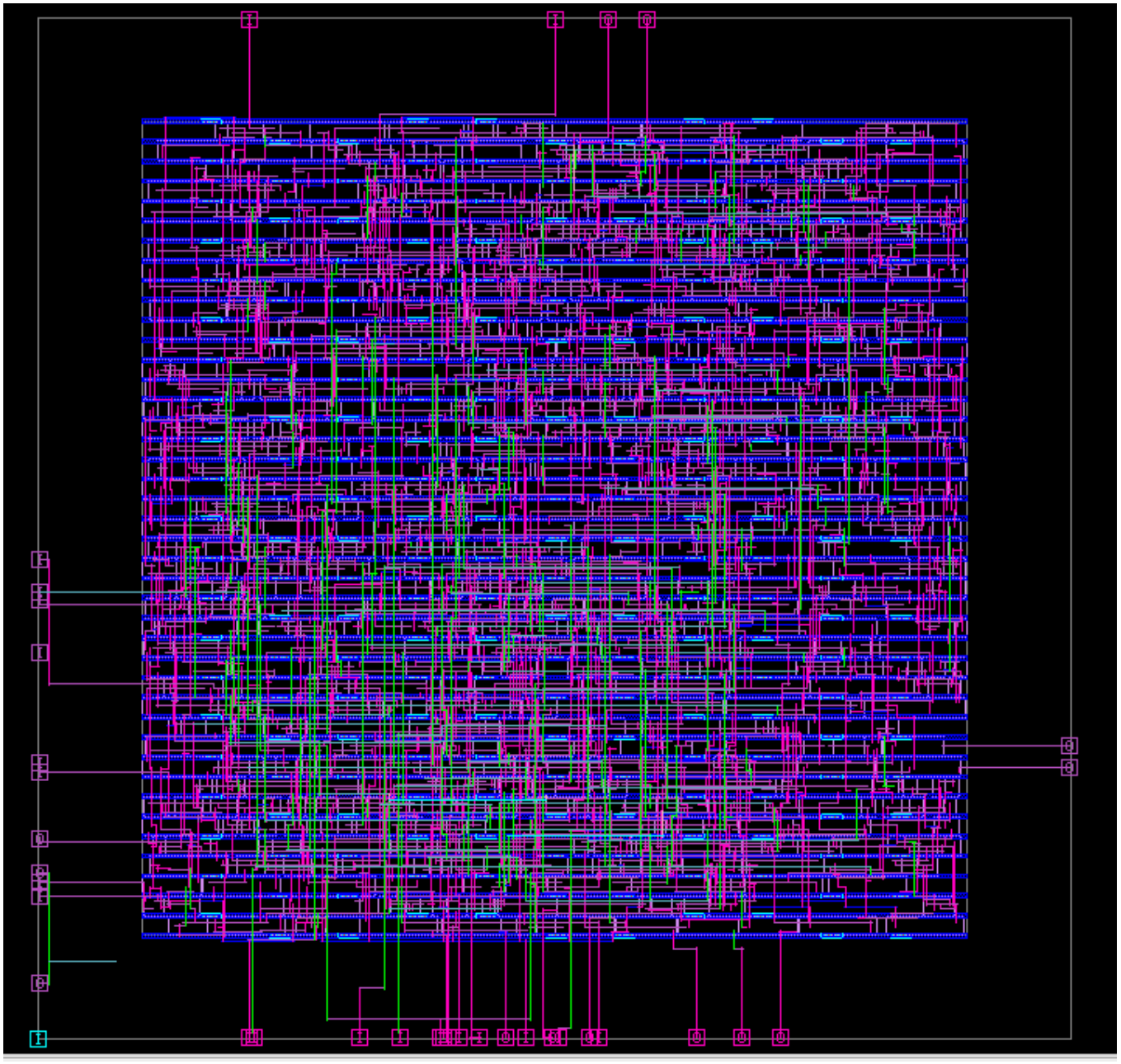
Worst-case setup path after CTS :

Open | hold_CTS.rpt ~/logic_project/PnR/report | Save

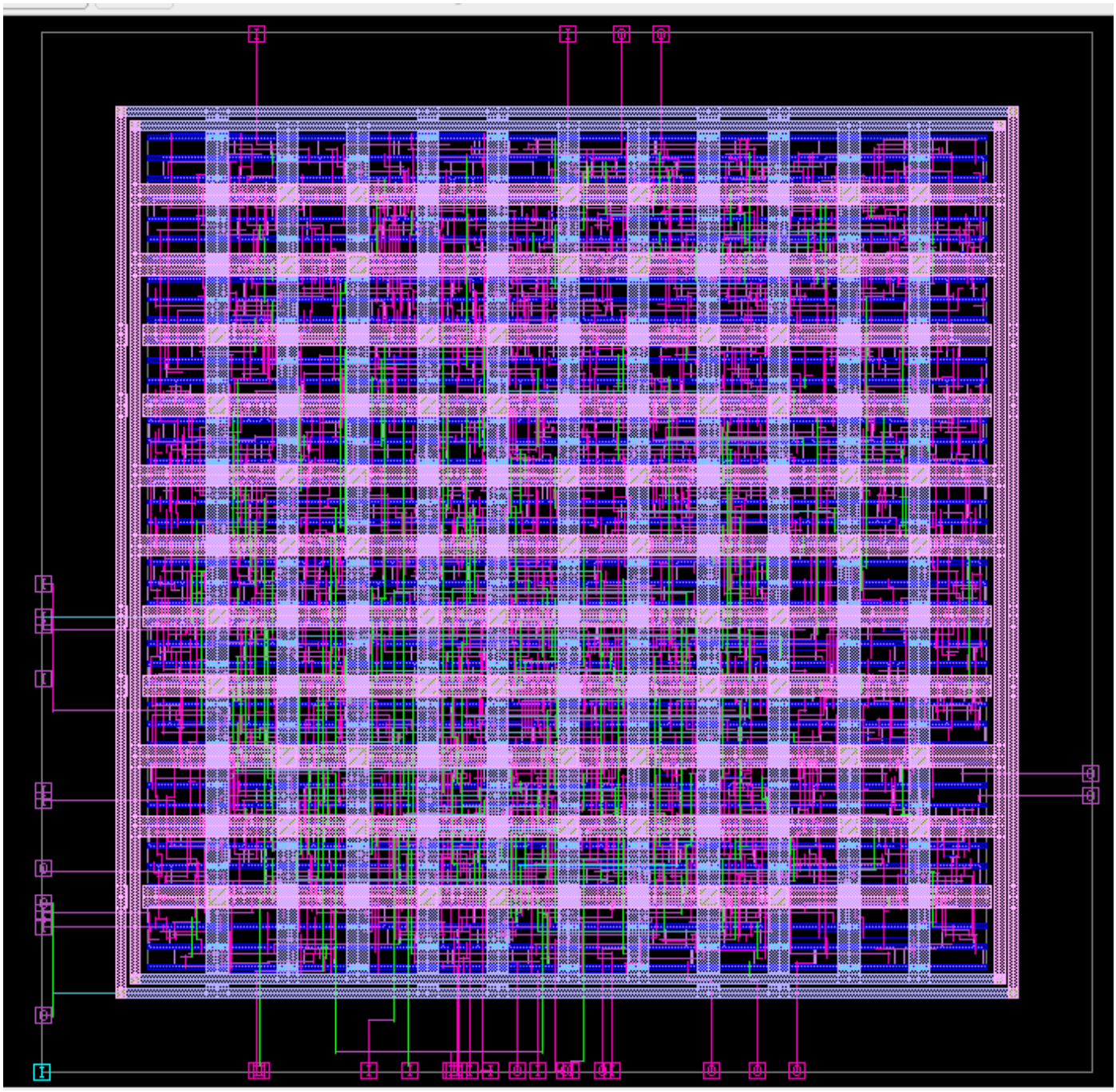
```
  Startpoint: txr_reg_4_ (rising edge-triggered flip-flop clocked by clk)
  Endpoint: txr_reg_4_ (rising edge-triggered flip-flop clocked by clk)
  Mode: default
  Corner: default
  Scenario: default
  Path Group: clk
  Path Type: min

  Point                                    Fanout     Cap      Trans      Incr      Path
-------------------------------------------------------------------------------------------
  clock clk (rise edge)                                                   0.00      0.00
  source latency                                                          0.00      0.00
  wb_clk_i (in)                                                  0.63     0.25      0.25 r
  wb_clk_i (net)                             153    419.27
  txr_reg_4_/CLK (DFFARX1)                                       0.63     0.01      0.25 r

  txr_reg_4_/CLK (DFFARX1)                                       0.63     0.00      0.25 r
  txr_reg_4_/Q (DFFARX1)                                         0.05     0.24      0.50 f
  txr[4] (net)                                 3      9.04
  U77/IN1 (AO22X1)                                               0.05     0.00      0.50 f
  U77/Q (AO22X1)                                                 0.03     0.08      0.58 f
  n122 (net)                                   1      2.41
  txr_reg_4_/D (DFFARX1)                                         0.03     0.00      0.58 f
  data arrival time                                                                 0.58

  clock clk (rise edge)                                                   0.00      0.00
  source latency                                                          0.00      0.00
  wb_clk_i (in)                                                  0.68     0.27      0.27 r
  wb_clk_i (net)                             153    459.80
  txr_reg_4_/CLK (DFFARX1)                                       0.68     0.01      0.28 r

  clock reconvergence pessimism                                          -0.02      0.25
  clock uncertainty                                                       0.30      0.55
  library hold time                                                       0.02      0.58
  data required time                                                                0.58

-------------------------------------------------------------------------------------------
  data required time                                                                0.58
  data arrival time                                                                -0.58

-------------------------------------------------------------------------------------------
  slack (MET)                                                                       0.00
```

- Hold violation are resolved in CTS

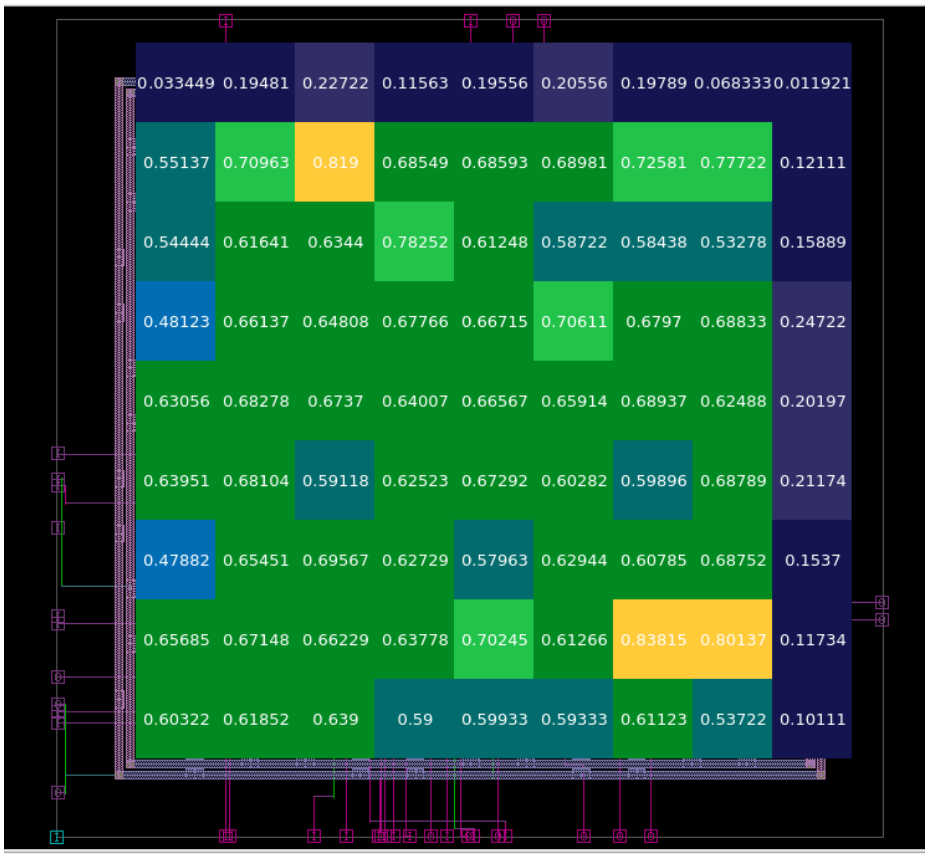
Routing & Routing Optimization :

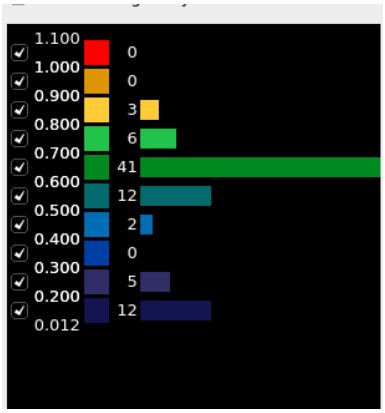


Final chip :

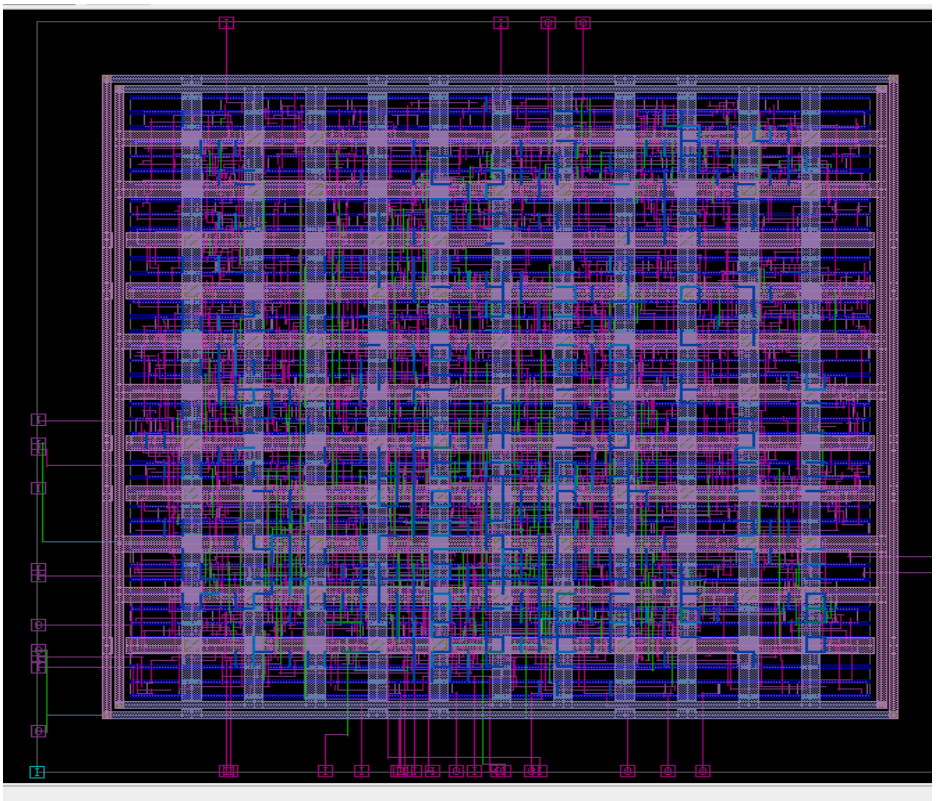


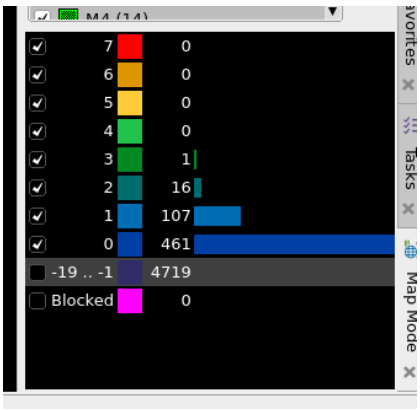
Cell density report :





Congestion report :





After this step, we did some checks to check design reliability and went to prime time to confirm that the design met timing finally, we created the GDS file

Final worst-case setup path after :

```
  Startpoint: wb_rst_i (input port clocked by clk)
  Endpoint: byte_controller/bit_controller/cnt_reg_0_ (rising edge-triggered flip-flop clocked
by clk)
  Mode: default
  Corner: default
  Scenario: default
  Path Group: clk
  Path Type: max

  Point                                                 Incr       Path
  ---------------------------------------------------------------------------
  clock clk (rise edge)                                 0.00       0.00
  clock network delay (ideal)                           0.00       0.00
  input external delay                                  2.00       2.00

  wb_rst_i (in)                                         0.00       2.00 r
  HFSINV_242_3/ZN (INVX0)                               0.25       2.25 f
  byte_controller/bit_controller/U43/QN (NAND4X0)
                                                        0.33       2.58 r
  byte_controller/bit_controller/U49/QN (NOR2X0)        0.32       2.90 f
  byte_controller/bit_controller/U27/QN (NOR2X0)        0.29       3.19 r
  byte_controller/bit_controller/U34/Q (AO222X1)        0.16       3.35 r
  byte_controller/bit_controller/cnt_reg_0_/D (DFFARX1)
                                                        0.00       3.35 r
  data arrival time                                                3.35

  clock clk (rise edge)                                20.00      20.00
  clock network delay (ideal)                           0.00      20.00
  byte_controller/bit_controller/cnt_reg_0_/CLK (DFFARX1)
                                                        0.00      20.00 r
  clock uncertainty                                    -0.30      19.70
  library setup time                                   -0.07      19.63
  data required time                                              19.63
  ---------------------------------------------------------------------------
  data required time                                              19.63
  data arrival time                                               -3.35
  ---------------------------------------------------------------------------
  slack (MET)                                                     16.28
```

Final worst-case setup path after :

```
****************************************
Report : timing
         -path_type full
         -delay_type min
         -max_paths 50
         -report_by design
Design : i2c_master_top
Version: O-2018.06-SP1
Date   : Mon May 20 01:01:17 2024
****************************************

  Startpoint: txr_reg_6_ (rising edge-triggered flip-flop clocked by clk)
  Endpoint: txr_reg_6_ (rising edge-triggered flip-flop clocked by clk)
  Mode: default
  Corner: default
  Scenario: default
  Path Group: clk
  Path Type: min

  Point                                              Incr       Path
  -----------------------------------------------------------------------
  clock clk (rise edge)                              0.00       0.00
  clock network delay (ideal)                        0.00       0.00

  txr_reg_6_/CLK (DFFARX1)                           0.00       0.00 r
  txr_reg_6_/Q (DFFARX1)                             0.23       0.23 f
  U79/Q (AO22X1)                                     0.08       0.31 f
  txr_reg_6_/D (DFFARX1)                             0.00       0.31 f
  data arrival time                                             0.31

  clock clk (rise edge)                              0.00       0.00
  clock network delay (ideal)                        0.00       0.00
  txr_reg_6_/CLK (DFFARX1)                           0.00       0.00 r
  clock uncertainty                                  0.30       0.30
  library hold time                                  0.01       0.31
  data required time                                            0.31
  -----------------------------------------------------------------------
  data required time                                            0.31
  data arrival time                                            -0.31
  -----------------------------------------------------------------------
  slack (MET)                                                   0.00
```

Finally, Our Design meets timing !!

We know that period is too much for this design and if we have a spec. on frequency, we must decrease it but we don’t have a spec. now