MP2
Coherence Protocols

1. **Change**: Cache Size
   Cache Sizes: 256KB, 512KB, 1MB, 2MB
   Fixed:
   Block Size: 64
   Cache Associativity: 8
   Number of Processors: 4
   Trace File: canneal.04t.longTrace

   MSI Protocol:
   Cache size: 256kb

Sr.No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5775	5805	5771	5813
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.67%	4.77%	4.57%	4.66%
6	Writebacks	254	235	278	234
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6745	6740	6774	6761
9	Interventions	68	47	81	63
10	Invalidations	2014	2034	2008	2020
11	Flushes	113	92	120	88
12	BusRdX	716	700	725	714

Cache size: 512kb

Sr.No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5757	5792	5756	5796
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.76%	4.55%	4.65%
6	Writebacks	190	170	205	171
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6663	6662	6686	6681
9	Interventions	71	47	82	63
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	92	121	88
12	BusRdX	716	700	725	714

Cache size: 1Mb

Sr.No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5752	5781	5752	5796
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.65%
6	Writebacks	170	155	186	171
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6638	6636	6663	6661
9	Interventions	71	48	82	2020
10	Invalidations	2014	2034	2008	88
11	Flushes	116	93	121	714
12	BusRdX	716	700	725	714

Cache size: 2Mb

Sr.No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5750	5779	5751	5789
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks	166	143	176	152
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6632	6622	6652	6655
9	Interventions	71	48	82	64
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX	716	700	725	714

MESI Protocol
Cache size: 256kb

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5775	5805	5771	5813
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.67%	4.77%	4.57%	4.66%
6	Writebacks	254	235	278	234
7	Cache-to-Cache Transfers	4405	4441	4406	4411
8	Memory Transaction	1663	1640	1685	1675
9	Interventions	1468	1432	1469	1479
10	Invalidations	2014	2034	2008	2020
11	Flushes	113	92	120	88
12	BusRdX	39	41	42	39

Cache Size: 512kb

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5757	5792	5756	5796
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.76%	4.55%	4.65%
6	Writebacks	190	170	205	171
7	Cache-to-Cache Transfers	4392	4431	4396	4400
8	Memory Transaction	1594	1572	1607	1606
9	Interventions	1466	1429	1465	1474
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	92	121	88
12	BusRdX	39	41	42	39

Cache Size: 1Mb

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5752	5781	5752	5790
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks	170	155	186	157
7	Cache-to-Cache Transfers	4389	4422	4393	4395
8	Memory Transaction	1572	1555	1587	1591
9	Interventions	1464	1428	1464	1474
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX	39	41	42	39

Cache Size: 2Mb

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5750	5779	5751	5789
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks	166	143	176	152
7	Cache-to-Cache Transfers	4387	4420	4392	4394
8	Memory Transaction	1586	1543	1577	1586
9	Interventions	1464	1428	1464	1474
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX	39	41	42	39

Dragon Protocol
Cache Size: 256kb

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5635	5646	5644	5652
3	Writes	11942	11710	12383	12108
4	Write Misses	3	2	2	0
5	Total Miss Rate	4.52%	4.61%	4.43%	4.50%
6	Writebacks	226	243	232	234
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5864	5891	5878	5886
9	Interventions	1405	1396	1398	1430
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	9
12	BusRdX	0	0	0	0

Cache Size:512kb

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5601	5610	5610	5617
3	Writes	11942	11710	12383	12108
4	Write Misses	3	2	2	0
5	Total Miss Rate	4.50%	4.58%	4.41%	4.47%
6	Writebacks	128	127	135	141
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5732	5739	5878	5758
9	Interventions	1400	1388	1389	1418
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX	0	0	0	0

Cache Size: 1Mb

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5595	5604	5604	5611
3	Writes	11942	11710	12383	12108
4	Write Misses	3	2	2	0
5	Total Miss Rate	4.49%	4.57%	4.40%	4.47%
6	Writebacks	107	110	105	123
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5705	5716	5711	5734
9	Interventions	1398	1387	1387	1417
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX	0	0	0	0

Cache Size: 2Mb

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5591	5603	5601	5608
3	Writes	11942	11710	12383	12108
4	Write Misses	3	2	2	0
5	Total Miss Rate	4.49%	4.57%	4.40%	4.47%
6	Writebacks	102	105	98	121
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5696	5710	5701	5729
9	Interventions	1396	1387	1387	1416
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX	0	0	0	0

2. **Change**: Cache Associativity
   Cache Associativity: 4,8,16
   Fixed:
   Block Size: 64
   Cache Size: 1Mb
   Number of Processors: 4
   Trace File: canneal.04t.longTrace

   MSI Protocol
   Associativity: 4

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5768	5797	5762	5803
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.66%	4.76%	4.56%	4.65%
6	Writebacks	239	211	239	224
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6723	6708	6726	6741
9	Interventions	69	47	81	63
10	Invalidations	2014	2034	2008	2020
11	Flushes	114	92	120	88
12	BusRdX	716	700	725	714

Associativity: 8

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5752	5781	5752	5790
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks	170	155	186	157
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6638	6636	6663	6661
9	Interventions	71	48	82	64
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX	716	700	725	714

Associativity: 16

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5741	5772	5741	5780
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.64%	4.74%	4.54%	4.64%
6	Writebacks	120	101	130	98
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6577	6573	6596	6592
9	Interventions	71	48	83	64
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	122	89
12	BusRdX	716	700	725	714

MESI Protocol

Associativity: 4

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5768	5797	5762	5803
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.66%	4.76%	4.56%	4.65%
6	Writebacks	239	211	239	224
7	Cache-to-Cache Transfers	4402	4434	4401	4401
8	Memory Transaction	1644	1615	1642	1665
9	Interventions	1465	1431	1465	1480
10	Invalidations	2014	2034	2008	2020
11	Flushes	114	92	120	88
12	BusRdX	39	41	42	39

Associativity: 8

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5752	5781	5752	5790
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks	170	155	186	157
7	Cache-to-Cache Transfers	4389	4422	4393	4395
8	Memory Transaction	1572	1555	1587	1591
9	Interventions	1464	1428	1464	1474
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX	39	41	42	39

Associativity: 16

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5741	5772	5741	5780
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.64%	4.74%	4.54%	4.64%
6	Writebacks	120	101	130	98
7	Cache-to-Cache Transfers	4379	4415	4386	4386
8	Memory Transaction	1521	1499	1527	1531
9	Interventions	1463	1426	1461	1473
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	122	89
12	BusRdX	39	41	42	39

Dragon Protocol
Associativity:4

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5609	5619	5619	5626
3	Writes	11942	11710	12383	12108
4	Write Misses	3	2	2	0
5	Total Miss Rate	4.50%	4.59%	4.41%	4.48%
6	Writebacks	148	149	142	158
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5760	5770	5763	5784
9	Interventions	1400	1392	1388	1424
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX	0	0	0	0

Associativity:8

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5595	5604	5604	5611
3	Writes	11942	11710	12383	12108
4	Write Misses	3	2	2	0
5	Total Miss Rate	4.49%	4.57%	4.40%	4.47%
6	Writebacks	107	110	105	123
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5705	5716	5711	5734
9	Interventions	1398	1387	1387	1417
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX	0	0	0	0

Associativity: 16

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5576	5586	5586	5593
3	Writes	11942	11710	12383	12108
4	Write Misses	3	2	2	0
5	Total Miss Rate	4.48%	4.56%	4.39%	4.46%
6	Writebacks	47	43	62	57
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5626	5631	5650	5650
9	Interventions	1395	1382	1383	1411
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX	0	0	0	0

3. **Change**: Block Size: 64
   Block Size: 64, 128, 256
   Fixed:
   Cache Size: 1Mb
   Cache Associativity: 8
   Number of Processors: 4
   Trace File: canneal.04t.longTrace

   MSI Protocol
   Block size: 64

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5752	5781	5752	5790
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks	170	155	186	157
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6638	6636	6663	6661
9	Interventions	71	48	82	64
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX	716	700	725	714

Block Size: 128

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5340	5386	5341	5384
3	Writes	11942	11710	12383	12108
4	Write Misses	39	40	42	39
5	Total Miss Rate	4.32%	4.43%	4.23%	4.32%
6	Writebacks	275	250	283	269
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6344	6347	6369	6386
9	Interventions	119	84	127	110
10	Invalidations	2066	2089	2053	2068
11	Flushes	164	129	166	135
12	BusRdX	729	711	745	733

Block Size: 256

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5023	5070	5004	5084
3	Writes	11942	11710	12383	12108
4	Write Misses	39	40	42	39
5	Total Miss Rate	4.06%	4.17%	3.96%	4.08%
6	Writebacks	363	342	383	332
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	6137	6147	6167	6159
9	Interventions	166	133	192	145
10	Invalidations	2132	2157	2107	2148
11	Flushes	211	178	231	170
12	BusRdX	751	735	780	743

MESI Protocol
Block Size: 64

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5752	5781	5752	5790
3	Writes	11942	11710	12383	12108
4	Write Misses	39	41	42	39
5	Total Miss Rate	4.65%	4.75%	4.55%	4.64%
6	Writebacks	170	155	186	157
7	Cache-to-Cache Transfers	4389	4422	4393	4395
8	Memory Transaction	1572	1555	1587	1591
9	Interventions	1464	1428	1464	1474
10	Invalidations	2014	2034	2008	2020
11	Flushes	116	93	121	89
12	BusRdX	39	41	42	39

Block Size: 128

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5340	5386	5341	5384
3	Writes	11942	11710	12383	12108
4	Write Misses	39	40	42	39
5	Total Miss Rate	4.32%	4.43%	4.23%	4.32%
6	Writebacks	275	250	283	269
7	Cache-to-Cache Transfers	4124	4155	4115	4125
8	Memory Transaction	1530	1521	1551	1567
9	Interventions	1367	1337	1377	1385
10	Invalidations	2066	2089	2053	2068
11	Flushes	164	129	166	135
12	BusRdX	39	40	42	39

Block Size: 256

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5023	5070	5004	5084
3	Writes	11942	11710	12383	12108
4	Write Misses	39	40	42	39
5	Total Miss Rate	4.06%	4.17%	3.96%	4.08%
6	Writebacks	363	342	383	332
7	Cache-to-Cache Transfers	3938	3943	3903	3939
8	Memory Transaction	1487	1509	1526	1516
9	Interventions	1283	1284	1321	1309
10	Invalidations	2132	2157	2107	2148
11	Flushes	211	178	231	170
12	BusRdX	39	40	42	39

Dragon Protocol
Block Size: 64

Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5595	5604	5604	5611
3	Writes	11942	11710	12383	12108
4	Write Misses	3	2	2	0
5	Total Miss Rate	4.49%	4.57%	4.40%	4.47%
6	Writebacks	107	110	105	123
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5705	5716	5711	5734
9	Interventions	1398	1387	1387	1417
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	6
12	BusRdX	0	0	0	0

Block Size: 128

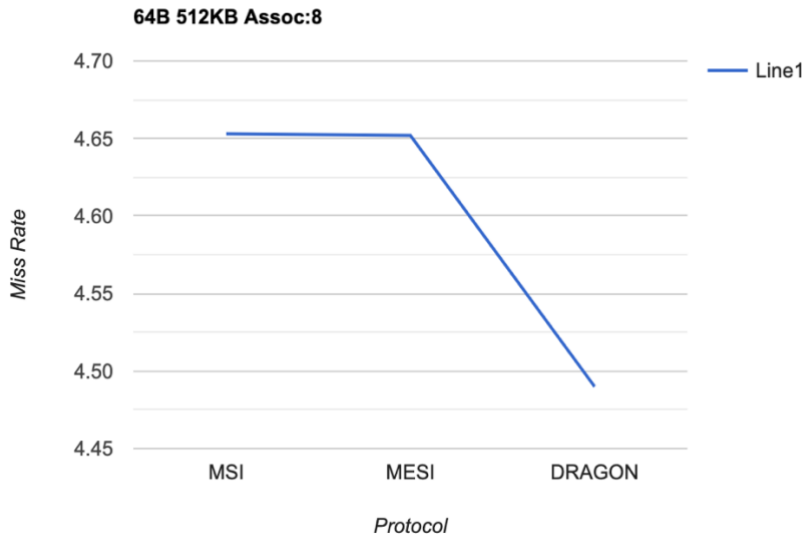
Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	5069	5080	5080	5086
3	Writes	11942	11710	12383	12108
4	Write Misses	3	1	2	0
5	Total Miss Rate	4.07%	4.15%	3.99%	4.05%
6	Writebacks	145	149	145	160
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	5217	5230	5227	5246
9	Interventions	1256	1266	1257	1287
10	Invalidations	0	0	0	0
11	Flushes	3	9	6	9
12	BusRdX	0	0	0	0

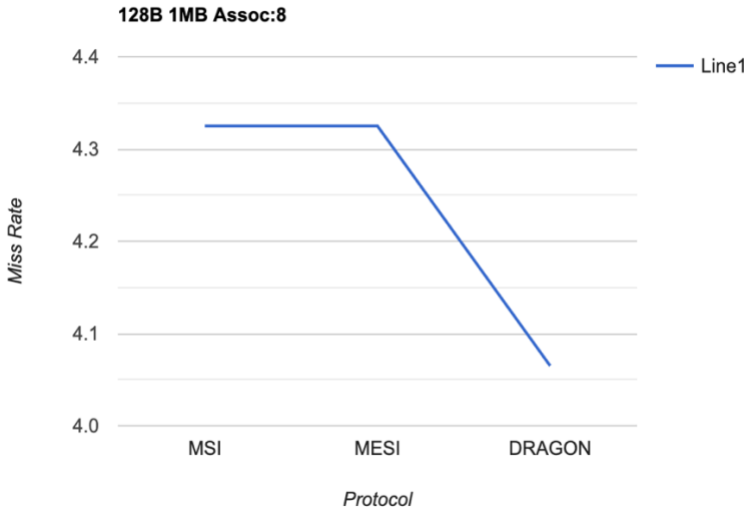
Block Size: 256

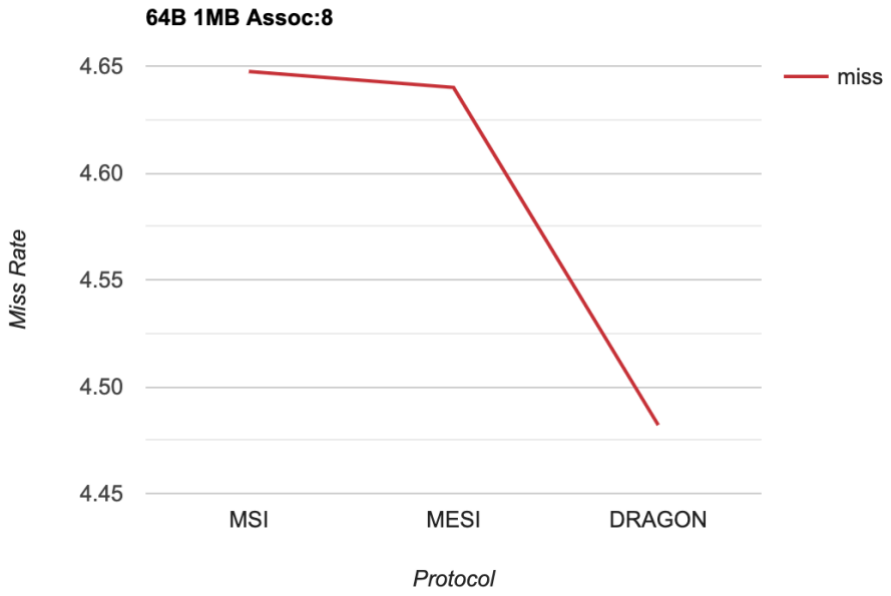
Sr. No.	Metric	C0	C1	C2	C3
1	Reads	112661	110830	114938	113428
2	Read Misses	4628	4633	4630	4640
3	Writes	11942	11710	12383	12108
4	Write Misses	3	1	2	0
5	Total Miss Rate	3.72%	3.78%	3.64%	3.70%
6	Writebacks	198	200	185	196
7	Cache-to-Cache Transfers	0	0	0	0
8	Memory Transaction	4829	4834	4817	4836
9	Interventions	1125	1175	1143	1176
10	Invalidations	0	0	0	0
11	Flushes	3	11	9	9
12	BusRdX	0	0	0	0

Observations & Analysis:

Graphical Analysis:



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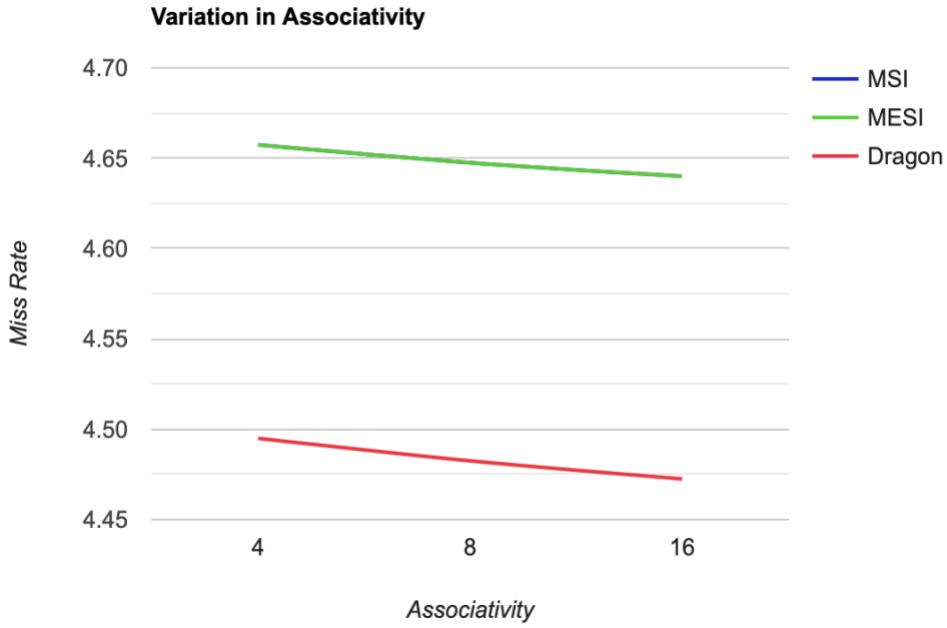
4.60
4.55
4.50
4.45
Miss Rate
MSI
MESI
DRAGON
Protocol
miss


Variation in Associativity
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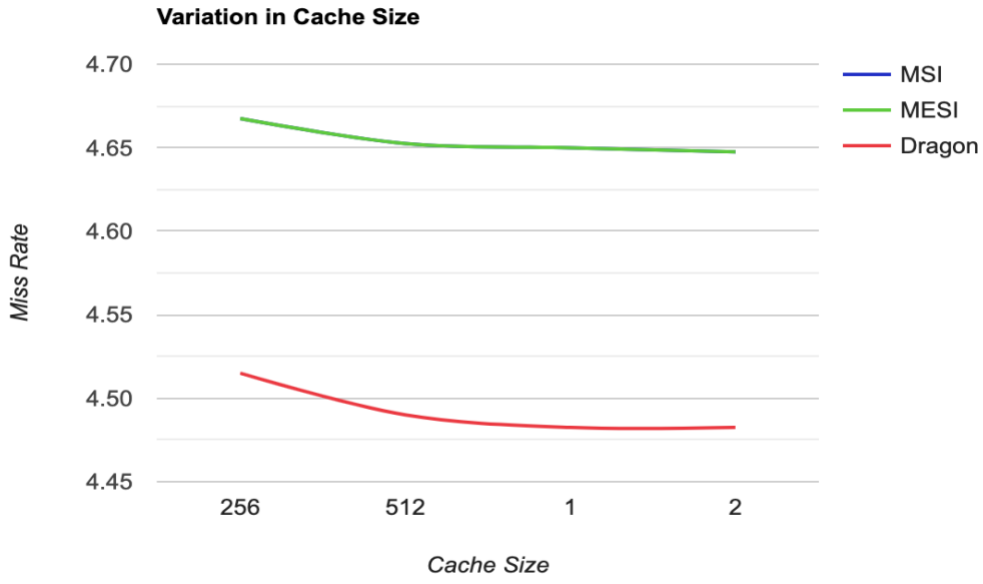
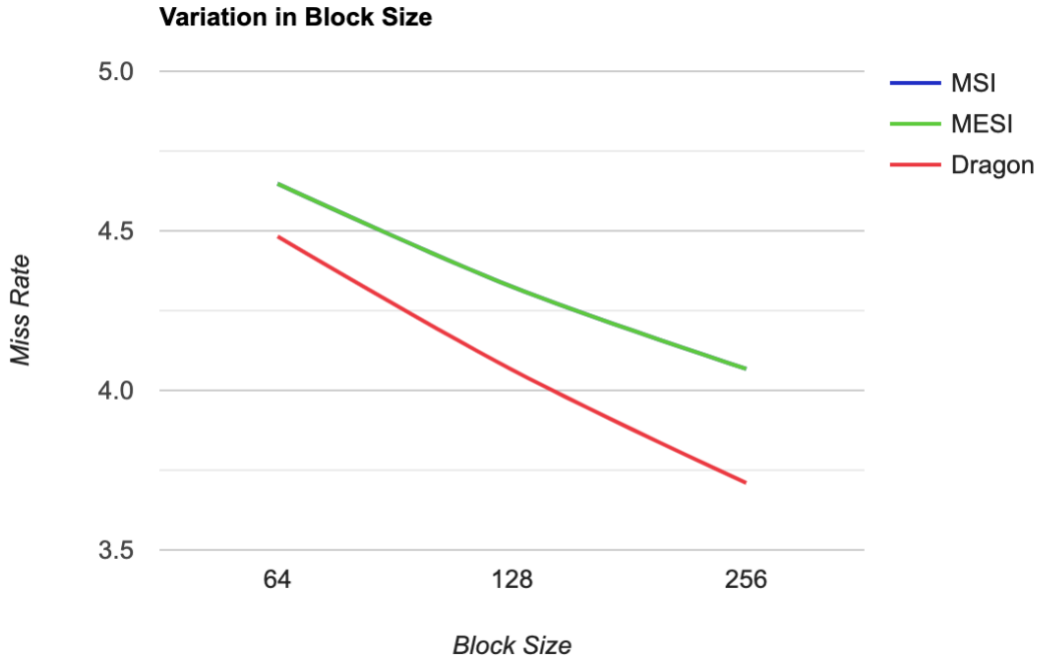
4.65
4.60
4.55
4.50
4.45
Miss Rate
4
8
16
Associativity
MSI
MESI
Dragon


Variation in Cache Size
4.70
4.65
4.60
4.55
4.50
4.45
Miss Rate
256
512
1
2
Cache Size
MSI
MESI
Dragon


Variation in Block Size
5.0
4.5
4.0
3.5
Miss Rate
64
128
256
Block Size
MSI
MESI
Dragon

Memory Transactions:
Access time for a cache configuration is proportional to the number of memory accesses.
In MSI, for every bus transaction request there is a memory access, hence, the number of memory transactions is much greater in MSI compared to MESI and Dragon.
MESI has the least number of memory transactions among the three protocols because cache-to- cache transfers are possible unlike the Dragon protocol. Here, memory is accessed for every 'PrRd' instruction even though the block is present in other caches. Number of memory transactions is indirectly proportional to cache size, associativity and block size. This is observed because the miss rate goes down.

Interventions:
It is observed that the number of interventions in MESI are much greater than MSI, whereas the number of interventions in Dragon are similar to that of MESI.
Since there is no exclusive state in MSI protocol, all clean blocks are placed in shared state.
In Dragon protocol, shifts from either M or E to Sm or Sc are considered as interventions. Therefore, we observe larger number of interventions in Dragon protocol comparatively.

Invalidations:
From the data, we observe that the number of invalidations in MSI and MESI are equal. Since Dragon protocol is a write-update protocol, there are no invalidations.
In MSI and MESI, whenever we make transition from Modified state to either Shared or Invalid state, we flush the block. In the case of Dragon protocol, a 'BusUpdate' is also present along with Flush. Due to updates, Flushes are issued only for the transition from Modified to Sm state. Thus, very few Flushes are observed in Dragon protocol.

BusRdX:
In case a processor needs to read a block which none of the other processors have and then write to it, here two bus transactions will take place in the case of MSI. First will be a BusRd request to read the block followed by a BusRdX request before writing to the block. The BusRdX request in this scenario is useless as none of the other caches have the same block, but there is no way for one cache to know about this. Thus, MESI protocol overcomes this limitation by adding an Exclusive state, which results in saving a bus request. This makes a huge difference when a sequential application is running. As only one processor will be working on it, all the accesses will be exclusive. The MSI would have performed very badly here. Even in the case of a highly parallel application where there is minimal sharing of data, MESI would be far faster
There is no BusUpgr transaction in the MSI protocol. Hence BusRdX are greater in MSI. BusRdX is issued even when we just want to invalidate the block in other caches. This adds to the latency in MSI protocol.
Since Dragon is write-update protocol, there is no 'BusRdX' signal in Dragon. The protocol directly updates the copies of the block present in other caches rather than invalidating it whenever there is a write to the block.

Miss Rate:
From observations, we can see that miss rate for Dragon protocol is lesser than that of MSI and MESI protocols. This is due to the fact that Dragon is a write-update protocol, whereas the other two protocols are write-invalidate protocols. In Dragon, the caches have an updated value of the block and therefore suffer lesser number of misses.
As cache size is increased, the number of capacity misses decrease for same block size and associativity. This shows up in an overall decrease in the miss rate. Miss rate also shows a decreasing trend with increasing cache associativity.
Conflict misses in the cache decrease with an increase in associativity. This results in an overall decrease in the miss rate for multiprocessor systems as well. With an increase in block size, the number of compulsory misses is reduced since a greater number of data bytes are brought into the cache when a single cache block is fetched.

From the results, we can see that MSI performs worse comparatively because it does not have an Exclusive state. This means that on a write, it needs to send out unnecessary write-invalidate messages on the bus. (All memory writebacks observed are due to cache evictions.)
The Dragon write-update protocol instead of invalidation sends an update to the other caches, so that they do no need to get a cache miss on each and every read. Hence, low number of bus transactions required by Dragon.