▼ Example

Write an instruction sequence to configure the SCI0 to use the following parameters:

- 9600 baud rate (E-clock is 24-MHz).
- 1 start bit, 8 data bits, and 1 stop bit format.
- No interrupt.
- Disable parity.

As usual, let's follow the procedure which was just explained prior.

1. Set the baud rate to 9600.

$$\text{baud rate} = \frac{24 \times 10^6}{16 \times 9600} = 156.25$$

$$156 \rightarrow \$9C$$

Assembly Copy

```
MOVB #$00,SCI0BDH MOVB #$9C,SCI0BDL
```

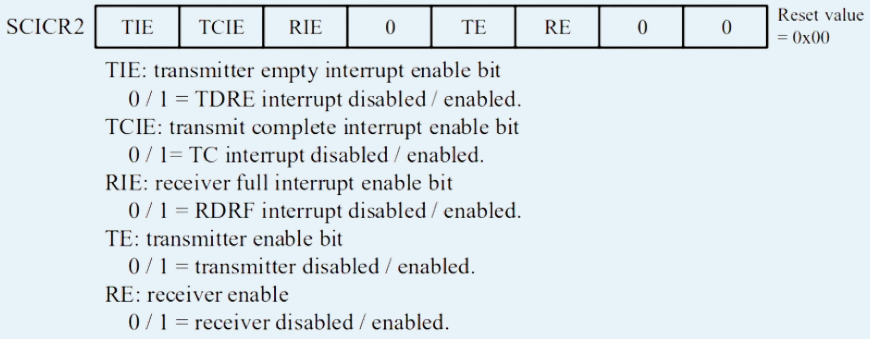
2. Select 8 data bits, no parity in the SCI control register 1.

SCISR1	TDRE	TC	RDRF	0	0	0	0	PF	Reset value = 0xC0

TDRE: transmit data register empty flag
0 / 1 = transmit data register is not empty / empty
TC: transmit complete flag
0 / 1 = transmission in progress / completed
RDRF: receiver data register full flag
0 / 1 = SCIxDR empty / full
PF: Parity error flag
0 / 1 = parity correct / incorrect

```
MOVB #$00,SCI0CR1
```

3. Enable transmitter and interrupt requests disabled.




```
MOVB #$08,SCI0CR2
```

2. Set a transmit procedure for each character.
   - Poll the transmit data register empty (`TDRE`) flag. If it is `1` , we can write on the SCI data registers (`SCIxDRH` / `SCIxDRL`).
   - We write the ninth bit on the MSB of `SCIxDRH` if the SCI is in 9-bit format.
   - A new transfer cannot happen until the `TDRE` flag has been cleared.
3. Repeat the previous step for each subsequent transmission.

To provide more information this topic, refer to the bullet points listed below.

- The `TDRE` flag becomes `1` when the SCI data register transfers a byte to the transmit shift register. It means that the SCI data register is ready to accept new data.
- If the transmitter empty interrupt enable (`TIE`) bit is also `1` , the `TDRE` flag generates a transmit interrupt request.
  - The transmitter empty interrupt bit refers to bit 7 of the SCI control register 2 (`SCIxCR2`).
- This `TDRE` bit is cleared by reading the `SCIxSR1` register and writing a byte into the `SCIxDRL` register.
- All status flags related to reception are cleared by reading the SCI status register following by reading the `SCIxDRL` register.

The SCI status registers (`SCIxR1` / `SCIxR2`) provides inputs to the interrupt logic circuits for generation of the SCI system interrupt.