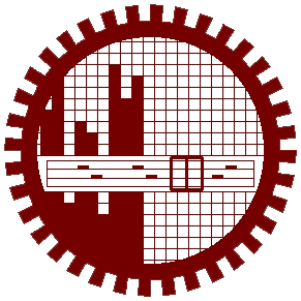
Bangladesh University of Engineering and Technology



Department of Electrical and Electronic Engineering

Course no: EEE 304
Course Title: Digital Electronics Laboratory
Project Title: Four player based Quiz System.

Course Instructors:
Mr. Hamidur Rahman
Rifat Shahriar

Level: 3 Term: 2
Section: A1
Group: 01

Group Members:
1706001- Mrinmoy Kundu
1706004- Aroni Ghosh
1706007- Md. Rafiqul Islam Rafi
1706032- Ayan Biswas Pranta

Introduction

We have implemented a four-player based quiz system using basic combinational and sequential logic elements. The rules of the games are -

- When the next quiz question has been asked, and the ‘Take Next Question’ buzzer is pressed, the first player who is pressed his/her buzzer will get the chance to answer.
- If the selected player is right, the judge will press the ‘Point Increase’ buzzer to add one point to his/her current score. If the answer was wrong, ‘Point Decrease’ buzzer will subtract one point.
- The highest scoring player will be declared as a winner.

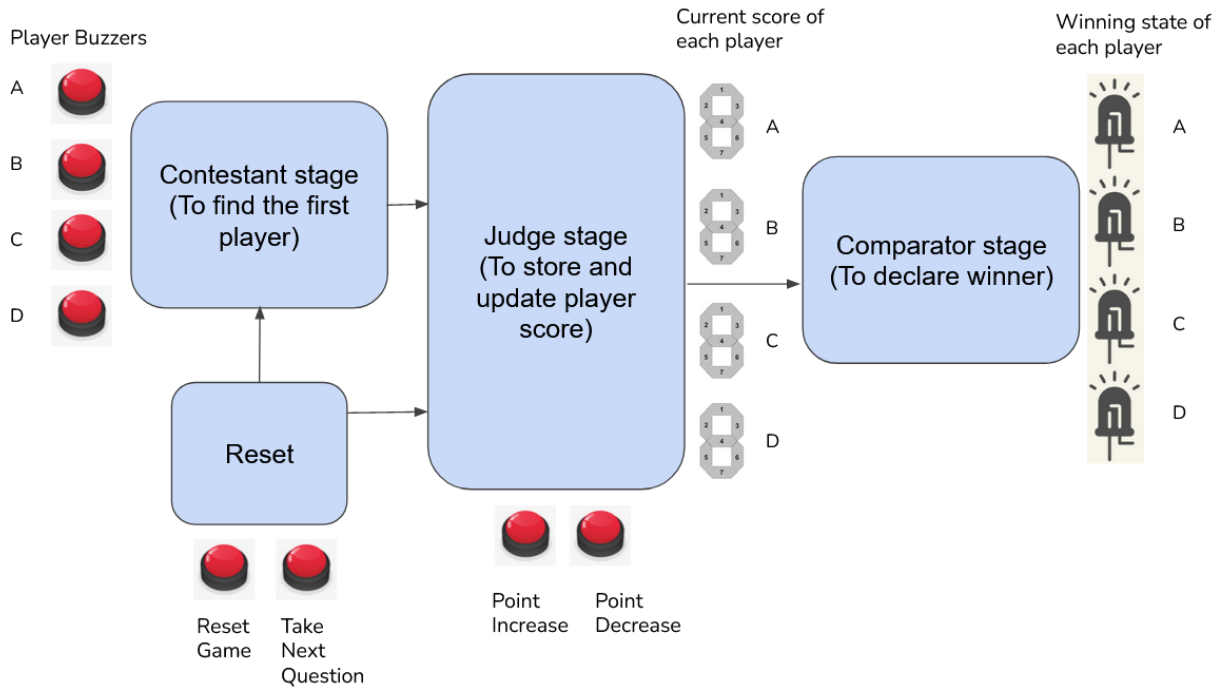


Figure : Working block diagram of the proposed 4-player quiz system

Other features of our designed system has -

- Number of players is limited to 4.
- Highest achievable score for each player is 9.
- There is no negative score, thus, if the player’s current score is 0, the wrong answer will not subtract any point.
- Inputs from players and judges are taken using buzzers.
- Winner/winners (in case of equal points) are declared using led light.

We have used Proteus software to simulate our project.

Workflow

Our proposed system consists of three parts/subcircuits. They are decided in detail in the following section.

Contestant stage

The goal of this subcircuit is to register the participant who toggles his switch earlier than anyone else.This logic implementation needs a memory capability, and cannot be achieved using only combinational circuits.

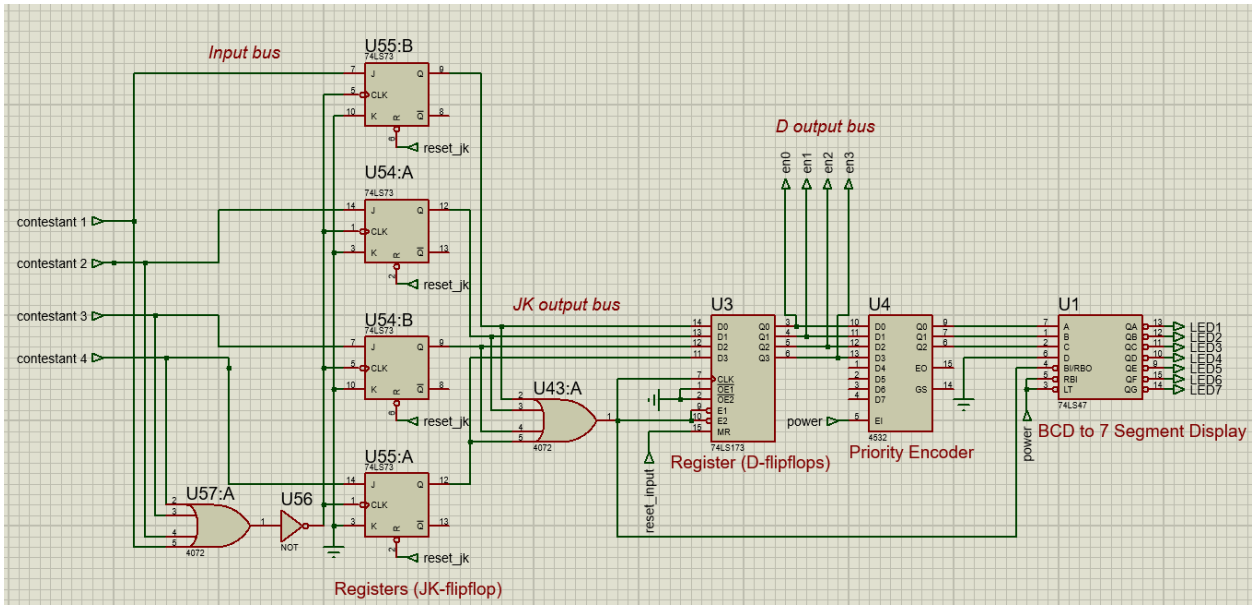


Figure : Circuit diagram of the contestant stage containing ‘Input bus’, ‘JK output bus’, ‘D output bus’

Let's say, the ‘Take Next Question’ switch has been toggled already, and this game is ready to go. Now, as the participants start to press the buzzers, the following steps will be executed -

- Whenever a contestant toggles a switch on the ‘Input Bus’, the corresponding information is registered as Q0, Q1, Q2, Q3 on the ‘JK output bus’ with active high information.
  This information is saved even if the contestant's inputs are off.
- Next, we need to show only the first participant. The clock of the positive edge triggered D flip flop is set as Clk = (Q0 | Q1 | Q2 | Q3), thus when only one Qi changes its state from 0 to 1 with the rest of the Qs’ being in state 0, the D flip flop will register the first high input signal Qi, and ignore the subsequent ones.
- Next, the 4-bit one hot vector of the 1st player’s information fed into a regular priority encoder, which encodes contestant number into 3 bit binary. We used 3 bits since we wanted to level the participants with ID no 1 (001), 2(010), 3(011) and 4(100).
- Finally, the encoded ID no is converted into BCD to show thm on the 7-segment display.

We used IC 74LS73 as the J-K flip flop, IC 74LS173 as the 4-bit D flip flop register and IC 74LS47 and IC 4532 as the BCD to 7-segment decoder and 8-bit priority encoder.

Judge Stage

It is known that both synchronous and asynchronous counters are capable of counting “Up” or counting “Down”, but there is another more “Universal” type of counter that can count in both directions either up or down depending on the state of their input control pin and these are known as **Bidirectional Counters**. In sequential circuit fields, these types of counters have significant impact.

Bidirectional counters, also known as up/down counters.Generally most bidirectional counter chips can be made to change their count direction either up or down at any point within their counting sequence. This is achieved by using an additional input pin which determines the direction of the count, either Up or Down and the timing diagram gives an example of the counters operation as this Up/Down input changes state.

Nowadays, both up and down counters are incorporated into a single IC that is fully programmable to count in both an “up” and a “down” direction from any preset value producing a complete **Bidirectional Counter** chip. Common chips available are the 74HC190 4-bit BCD decade Up/Down counter, the 74F569 is a fully synchronous up/down binary counter and the CMOS 4029 4-bit Synchronous up/down counter.In our project,we have used 74LS193 up/down counter chip.

The 74LS193 is an up/down DIP-16 Binary Counter. Separate count up and count down clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs. Separate terminal count up and terminal count down outputs are provided which are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load (PL) and the Master Reset (MR) inputs asynchronously override the clocks.

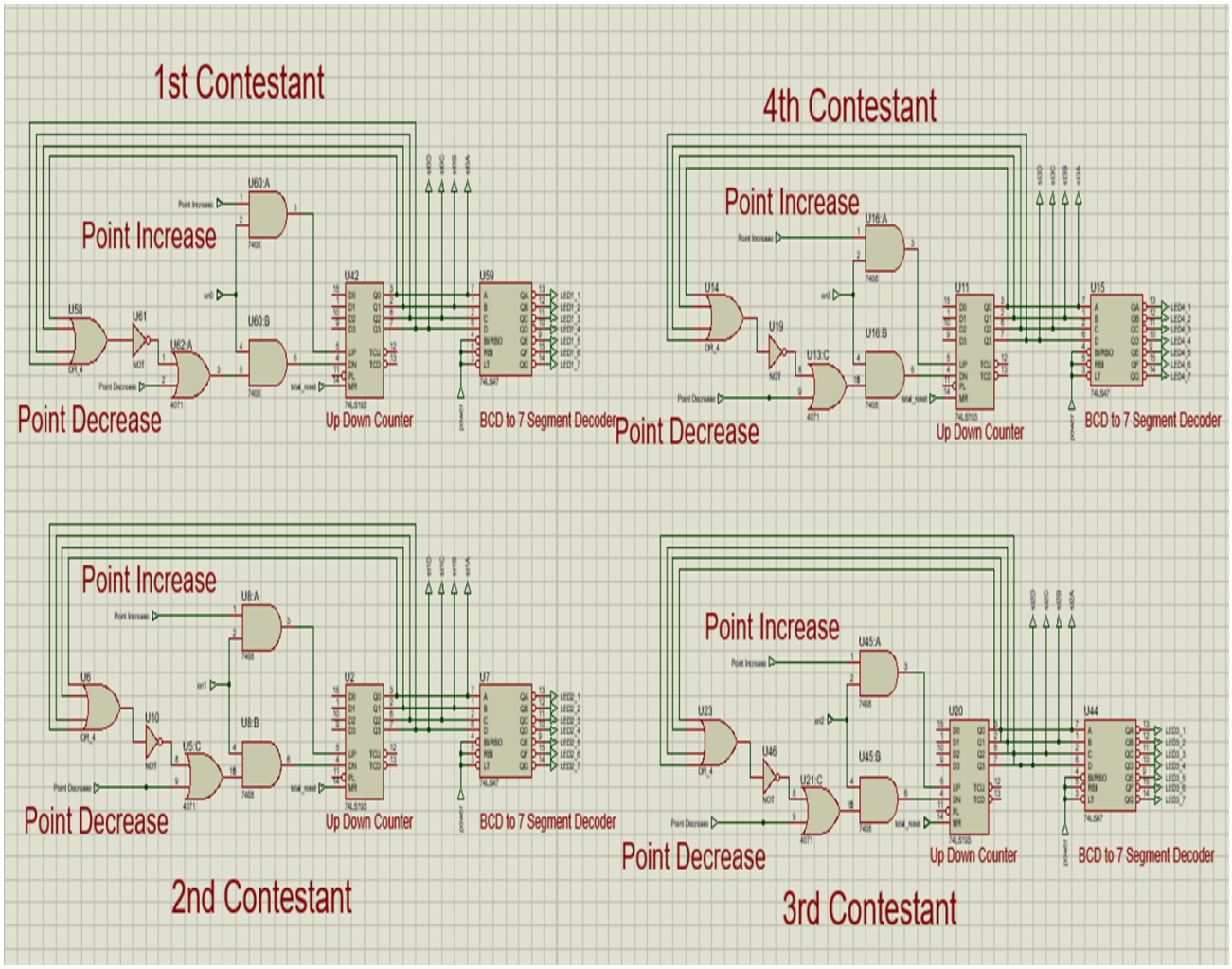


Figure: Since we have considered four participants in our quiz competition, hence the number of scoring interfaces is four. But all of them are the same in structure (i.e.used gates/ICs are identical). For point increasing & decreasing, only two logic toggles have been used for the whole system so that judges needn't worry about which participant gives the correct/wrong answer ,rather their only job is to verify answers and adding/subtracting scores. Points are shown in the "BCD to 7 segment Decoder".

Now, let's analyze the circuit portion of the first contestant.

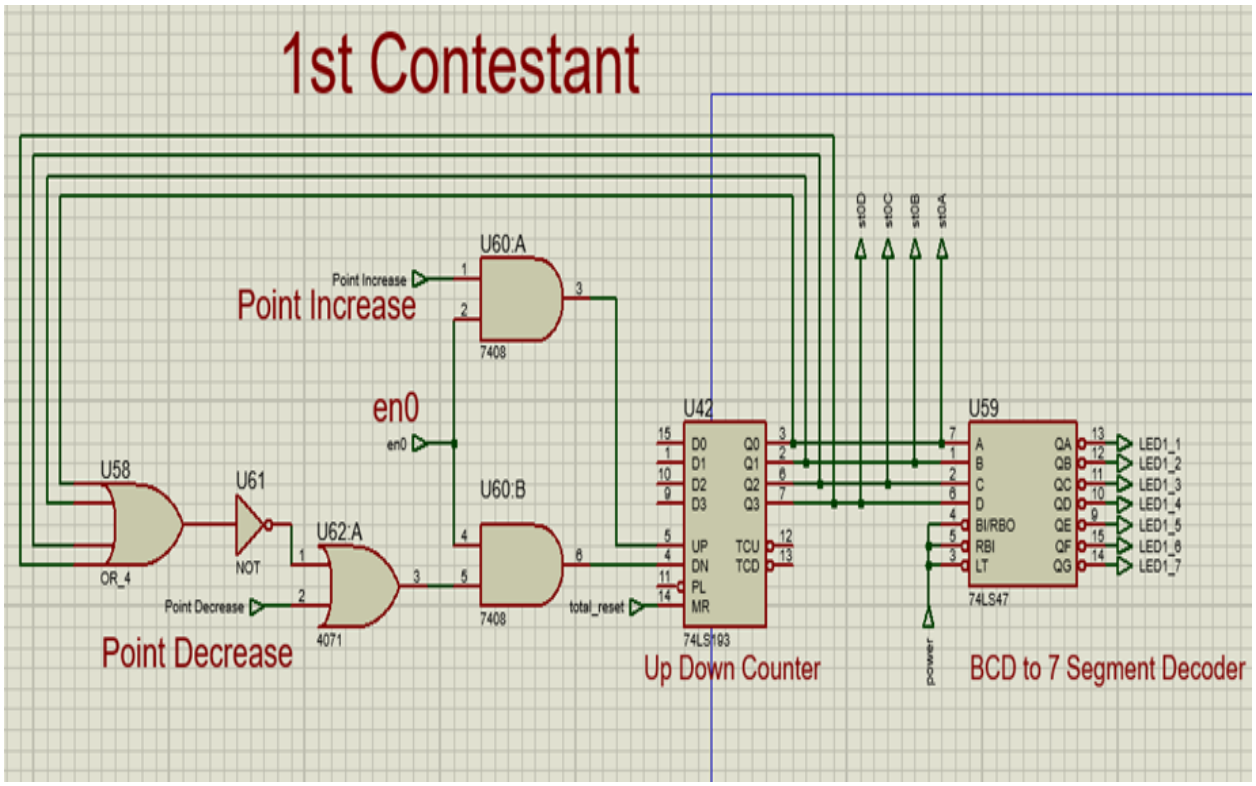


Figure: When contestant-1 presses the buzzer first, 'en0' becomes 1. Now, if "point increase" is toggled, then the current score will be increased by one and the value at UP terminal becomes, UP = ("en0" & "Point increase"). On the other hand, if "point decrease" is toggled, then the current score will be decreased by one if the current (score!=0), otherwise points will remain zero. So the value at DOWN terminal becomes, DN = ("en0" & ("Point decrease" | !"Current score"))

Comparator Stage

Cumulative scores of four participants are compared in this stage and the winner is declared to be the highest scorer among four. Output scores from the judge panel stage are inputs in this stage. We have developed an efficient design with 3 comparators only. We have used 4 bit magnitude comparators IC 7485 each providing 3 outputs whether A=B, A<B or A>B.

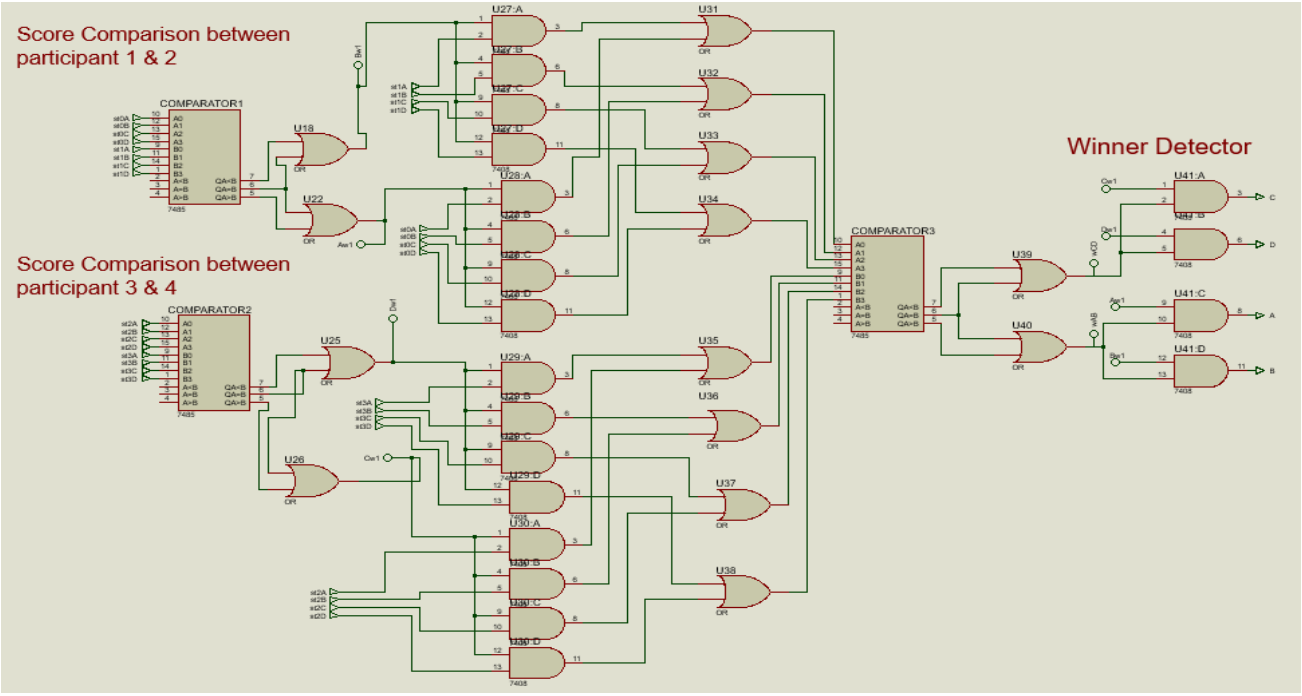


Figure: Comparator Stage consisting of 3 comparators with Comparator 1 comparing scores between participants 1 and 2, comparator 2 comparing scores between participants 3 and 4, and comparator 3 comparing highest score from comparator 1 and 2. Final outputs in the winner detector portion- A, B, C and D can hold values of either 0 or 1, deciding the winner of the game. First input in comparator 3: $(Aw1 \ \& \ A)$ | $(Bw1 \ \& \ B)$ while 2nd input is $(Cw1 \ \& \ C)$ | $(\ Dw1 \ \& \ D)$

Inputs		*Outputs*		
A	B	$A > B$	$A = B$	$A < B$
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Figure: Truth Table for a 1 bit Comparator

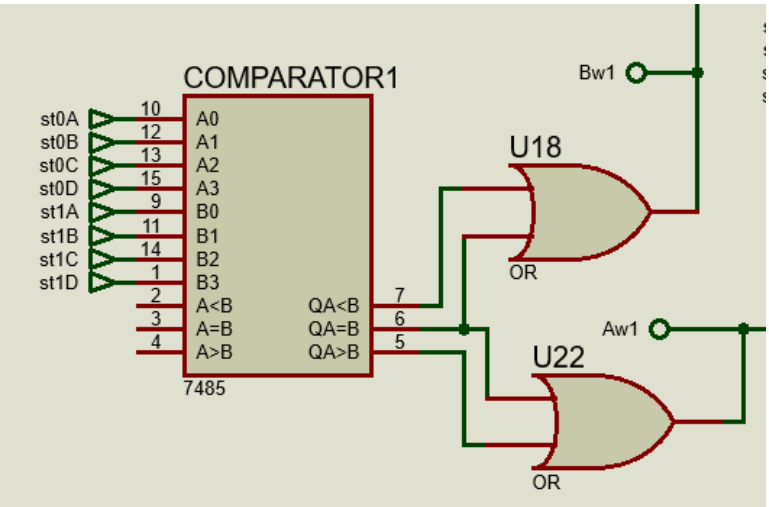


Figure: Comparator 1 output Aw1= QA>B or QA=B and Bw1= QA<B or QA=B. Likewise, comparator 2 provides output Cw1 and Dw1. These 4 parameters detect the ultimate winner.

Winner Detection

Case 1:

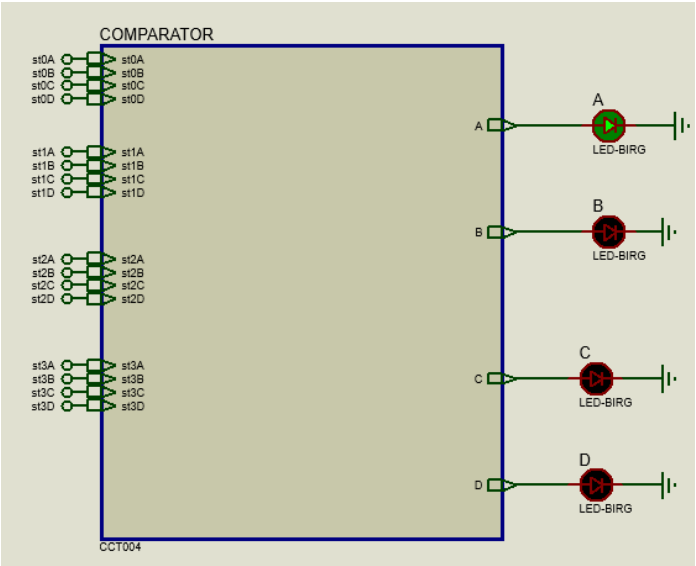


Figure: Comparator stage output A or LED A is ON, winner is participant 1

Case 2:

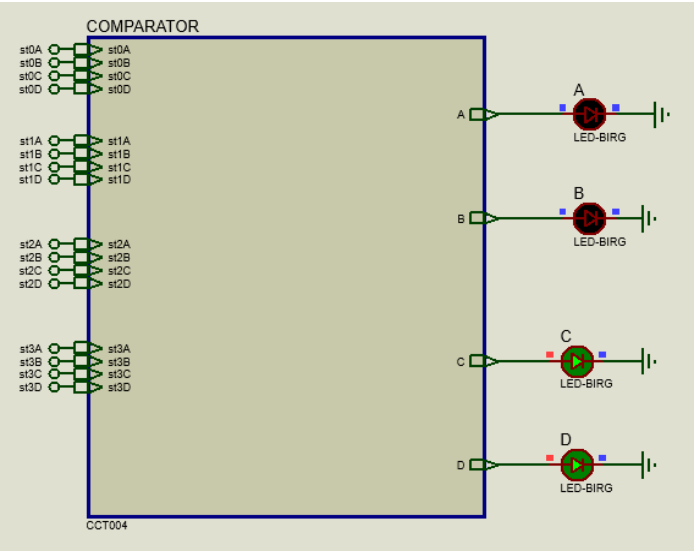


Figure: LED C & D are on, match is tie between participants 3 and 4.

Case study

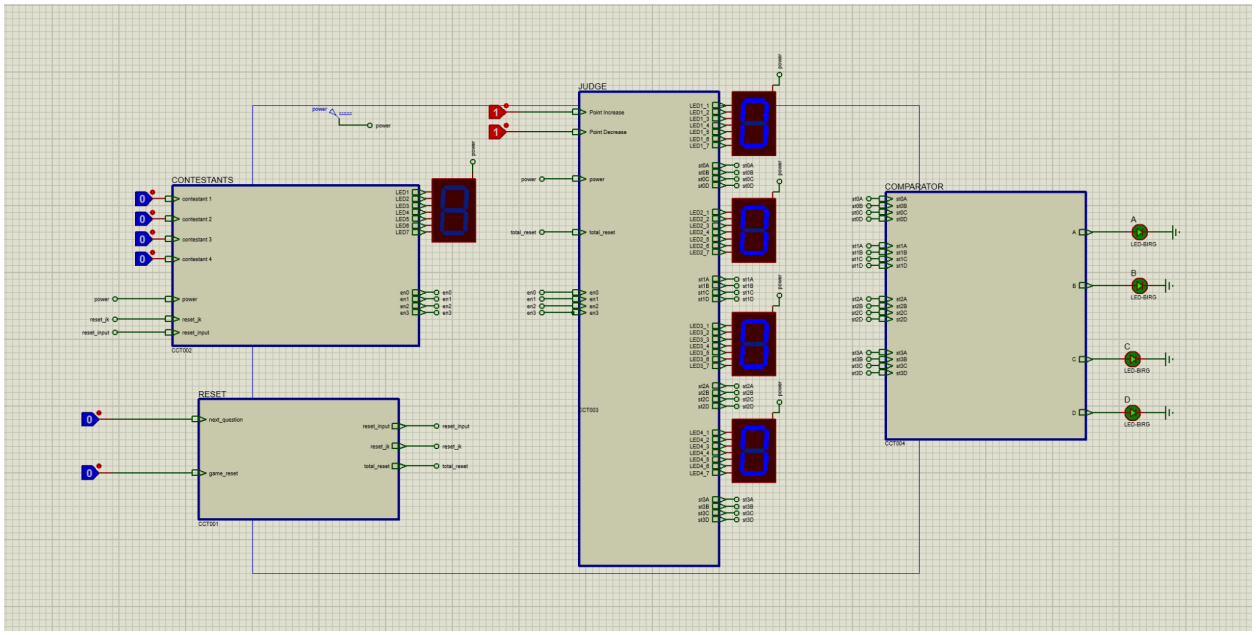


Figure: Initially all contestants have cumulative score 0 and all output LEDs are green, declaring everyone in 1st position.

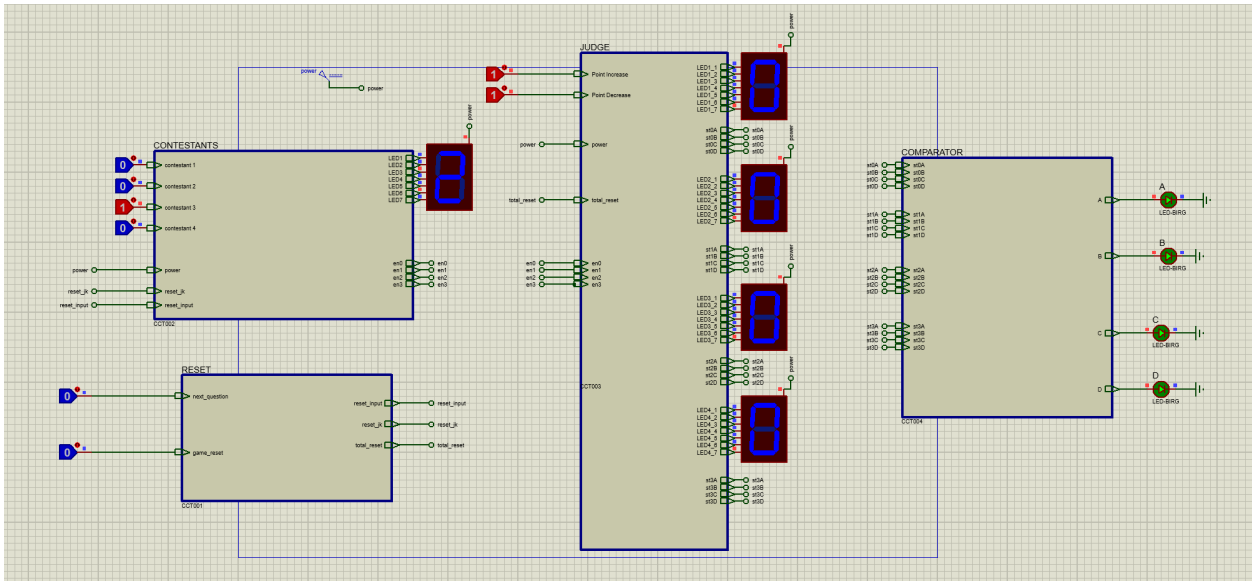


Figure: Contestant 2 presses the buzzer in the fastest manner, and the display is showing only contestant 2 is allowed to answer. Contestant 3 is pressing the buzzer too but in vain, as contestant 2 was faster than him/her.

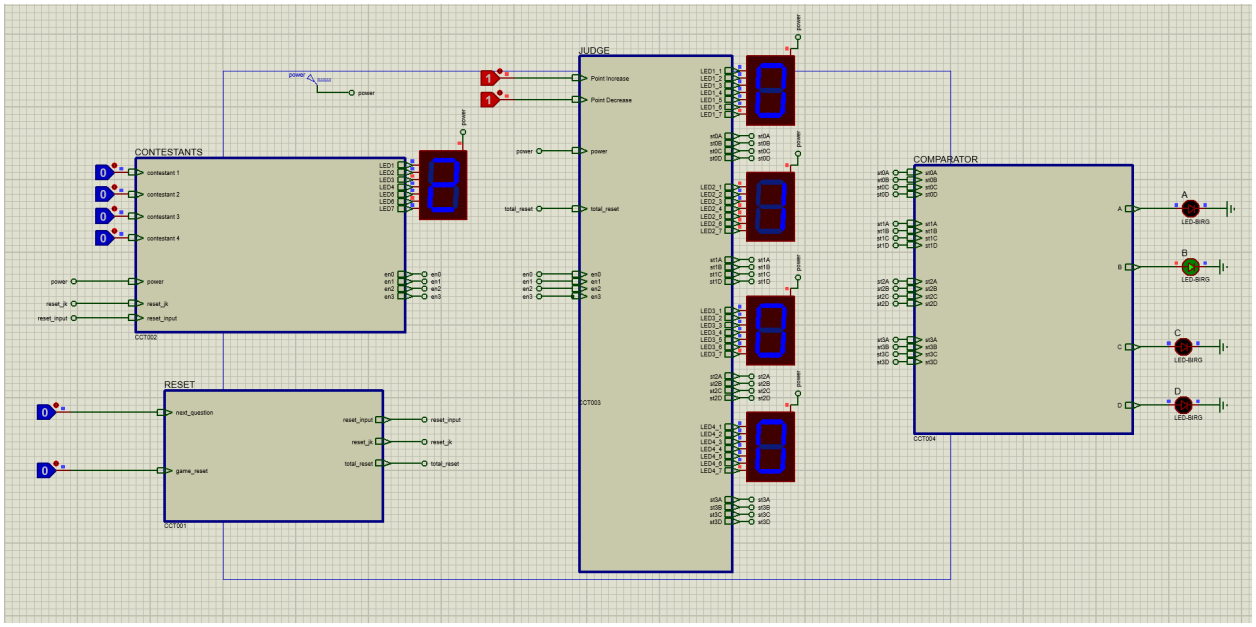


Figure: Contestant 2 answers correctly and the judge increases his/her mark by 1. Now the LEDs are showing contestant 2 is at first position currently. After marking is done, the host goes to next question by the “next question” button.

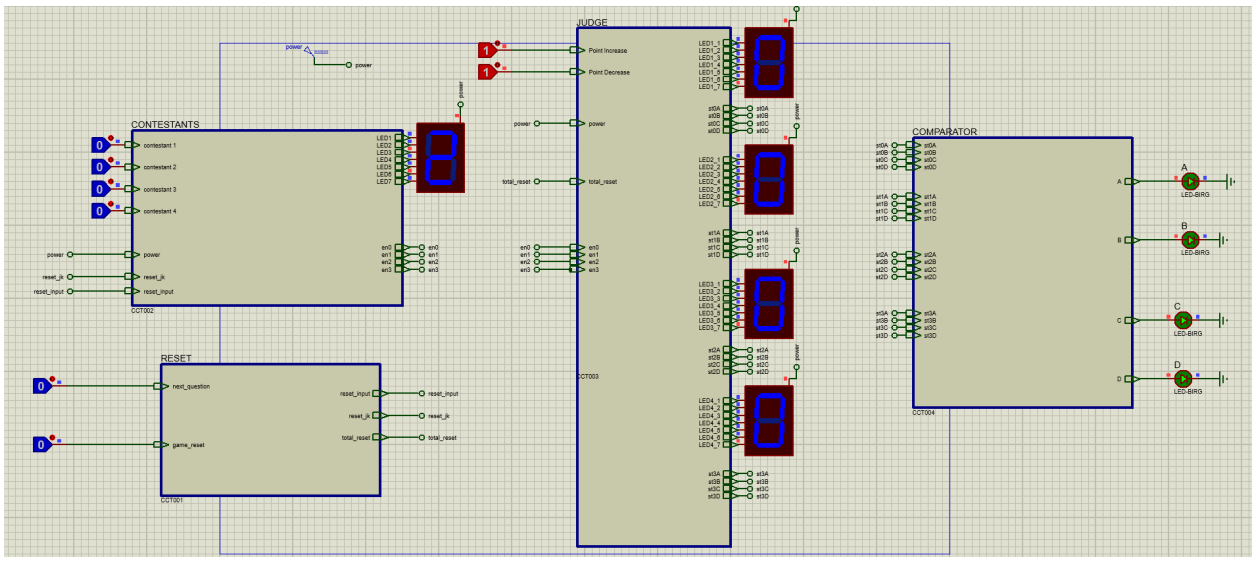


Figure: Contestant 2 presses the buzzer again before everyone, but this time he/she answers wrong. So, the judge decreases his mark and now the total score of him/her is 0.

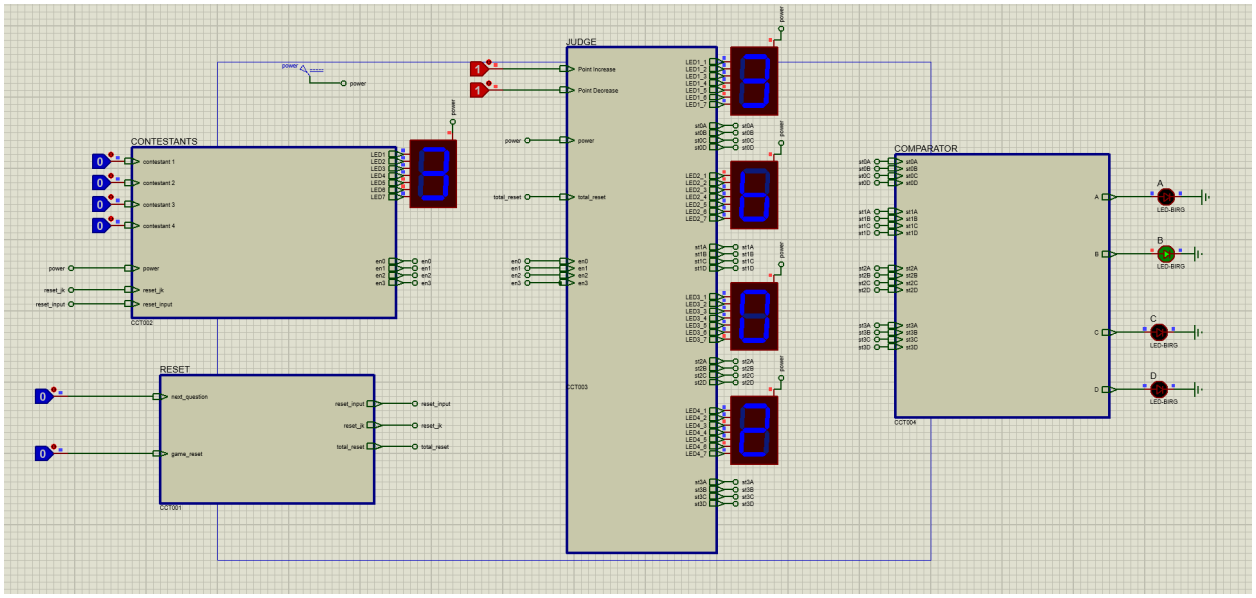


Figure: Here, contestant 3 presses the buzzer before everyone but gets the answer wrong. The judge tries to decrease his point by pressing the “point decrease” button but his total score is not decreased as his previous total score was 0 and total score can’t be negative.We can also see contestant 2 is being shown first as he has the most cumulative score. The cumulative scores can be reset by the “game reset” button.

Components & Cost Analysis

Parts Name	Total Units	Corresponding IC units	Price(Tk)
OR Gate	36	IC 7432 (4 gate per IC)	25X9= 225
AND	28	IC 7408 (4 gate per IC)	20X7=140
NOT	6	IC 7404(6 gate per IC)	25X1= 25
BCD to 7 segment decoder	5	IC 74LS47	50X5= 250
JK Flip-Flop	4	IC 74LS73 (2 per IC)	68X2 = 136

Up-Down Binary Counter	4	IC 74LS193	60X4 = 240
4-bit D type register	1	IC 74LS173	48X1= 48
8 bit priority encoder	1	IC 4532	48X1= 48
7 segment LED display common cathode	5	-	10X5= 50
		Total	1102

Future Prospects

From our futuristic point of view, we hope to add features like increasing question numbers by updating double-digit based score display. We can generalize our system so that more than four players can play and for that purpose, improve comparator design for winner detection. We can modify the system in a way such that it accepts answers from a participant only within a certain time limit. Also, we can upgrade it to a multiple-round based game where a single participant is eliminated in each round.

Conclusion

The target of this Proteus based project was to establish a system for quiz competition and make it handy for contestants, judges and host. With proper opportunities, this project could have been implemented in hardware using basic circuits and IC. But the simulation has provided insights about the operation and features of manipulating the system and widen our instinct to implement any idea we need to. With our future prospects being applied, we hope to continue it to industrial level with details taken care of.