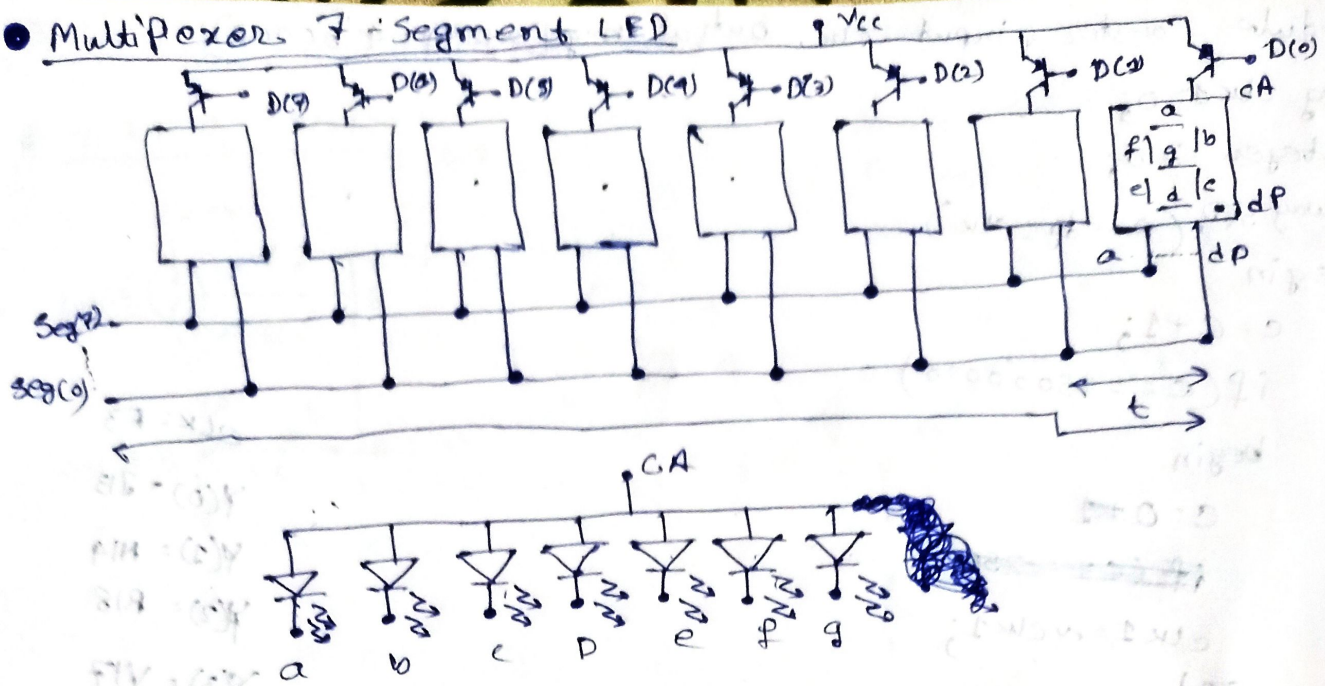
Multiplexer 7-Segment LED



module seg7 (input clk, output reg [7:0] D = 8'hFE, output reg [7:0] seg);

```
reg clk1=0;
integer c=0;
reg [2:0]n=0;
always @(posedge clk)
begin
   c=c+1;
   if (c==100000)
    begin
       c=0;
       clk1=~clk1;
    end
end
always @(posedge clk1)
begin
    n=n+1'b1;
    D={D[6:0],D[7]};
end
```

```
always@(n)
begin
 case(n)
 0: seg=8'h03;
 1: seg=8'h9F;
 2: seg=8'h25;
 3: seg=8'h0D;
 4: seg=8'h99;
 5: seg=8'h49;
 6: seg=8'h41;
 7: seg=8'h1F;
 default: seg=8'hFF;
 endcase
 end
 endmodule
```

CLK = E3

D(0) = J17	seg(0) = H15
D(1) = J18	seg(1) = L18
D(2) = T9	seg(2) = T11
D(3) = J14	seg(3) = P15
D(4) = P14	seg(4) = K13
D(5) = T14	seg(5) = K16
D(6) = K2	seg(6) = R10
D(7) = U13	seg(7) = T10