SCHEMATIC , TEST BENCH AND LAYOUT OF A INVERTER USING CADENCE VIRTUOSO

by

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As someone just starting out with Cadence Virtuoso, this was my first hands-on experience with the tool. My goal was to get familiar with the interface, understand how to build a basic circuit, and run a simple simulation. I chose to design a CMOS inverter because it's a fundamental building block in digital electronics and a great starting point for learning the workflow

Although layout design is more advanced, I briefly explored the layout editor. I created a layout view, placed the NMOS and PMOS devices, and tried routing the connections. I didn't go too deep yet, but I learned about DRC (Design Rule Check) and LVS (Layout vs. Schematic), which are used to verify the physical design.

Reflections

This first project helped me understand:

- How to navigate Cadence Virtuoso
- The process of building a schematic
- How to set up and run basic simulations
- The connection between schematic and layout design

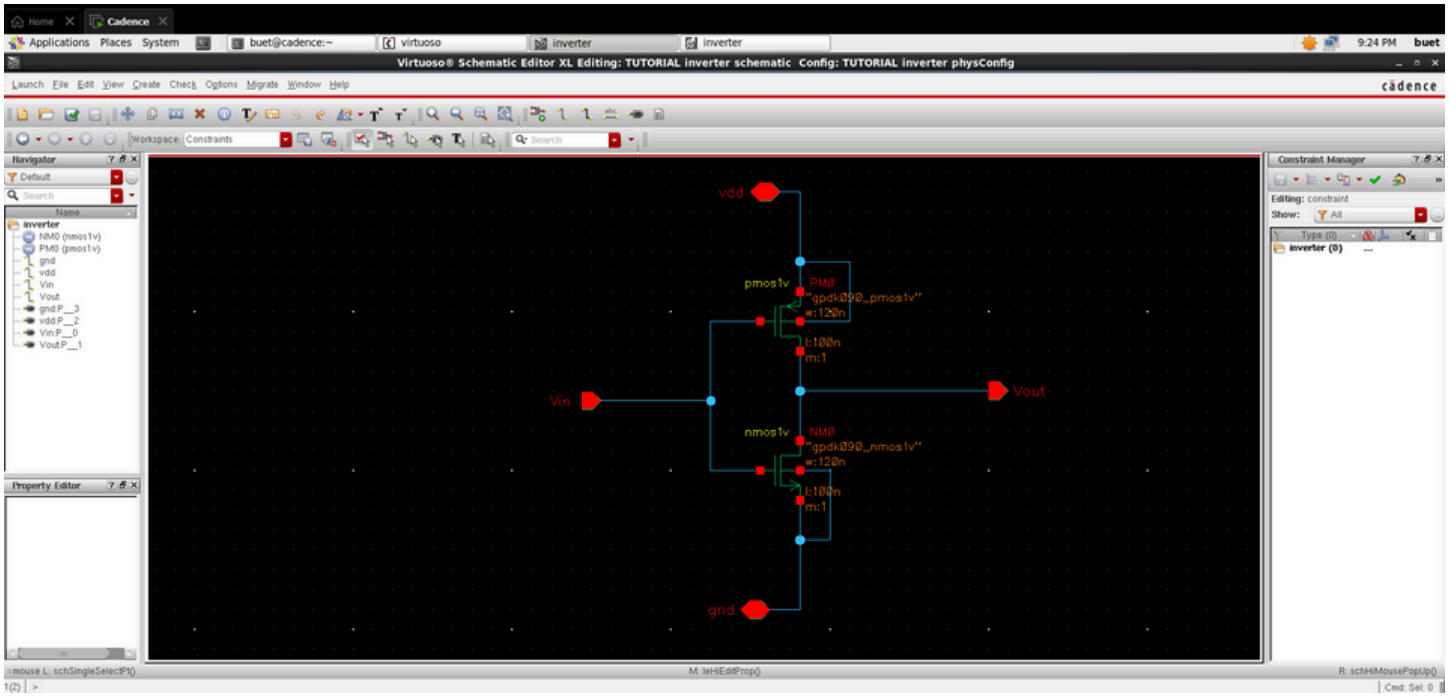
As a beginner, I found the experience challenging but rewarding. It gave me the confidence to start exploring more complex designs, like metasurface absorbers and graphene-based circuits, which I'm really interested in.

In Cadence Virtuoso, the terms schematic, test bench, and layout refer to distinct stages in the IC design and simulation workflow. Here's a breakdown of each:

Schematic

The schematic is the graphical representation of your circuit using symbols for components like transistors, resistors, capacitors, etc.

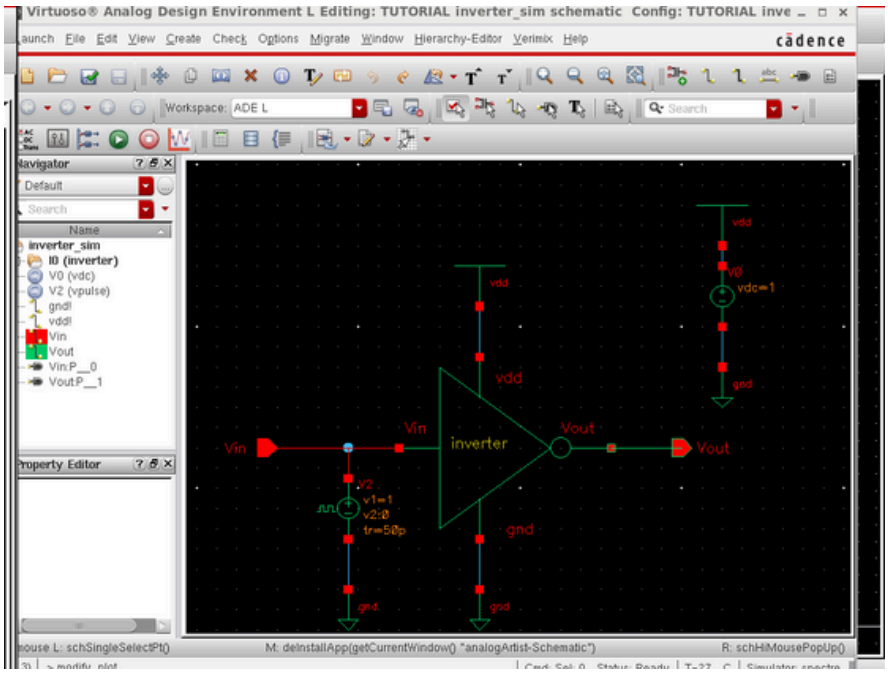
- Purpose: Captures the logical connectivity of the circuit.
- Tools: Created using the Schematic Editor in Virtuoso.
- Features:
  - You can instantiate components from libraries (e.g., analogLib).
  - Wire them together to define the circuit topology.
  - Assign parameters like transistor dimensions or voltage levels.
- Next Step: Once the schematic is complete, you can create a symbol view for reuse in other designs or test benches.



🧪 Test Bench

A test bench is a separate schematic used to simulate and verify the behavior of your design under specific conditions.

- Purpose: Provides stimulus and environment for simulation.
- Components:
  - Your design under test (DUT), instantiated as a symbol.
  - Voltage sources, pulse generators, loads, and measurement probes.
- Simulation Setup:
  - Use ADE (Analog Design Environment) or Maestro/ADE XL to configure simulations (e.g., DC, transient, AC).
  - Define variables, select outputs, and run simulations.



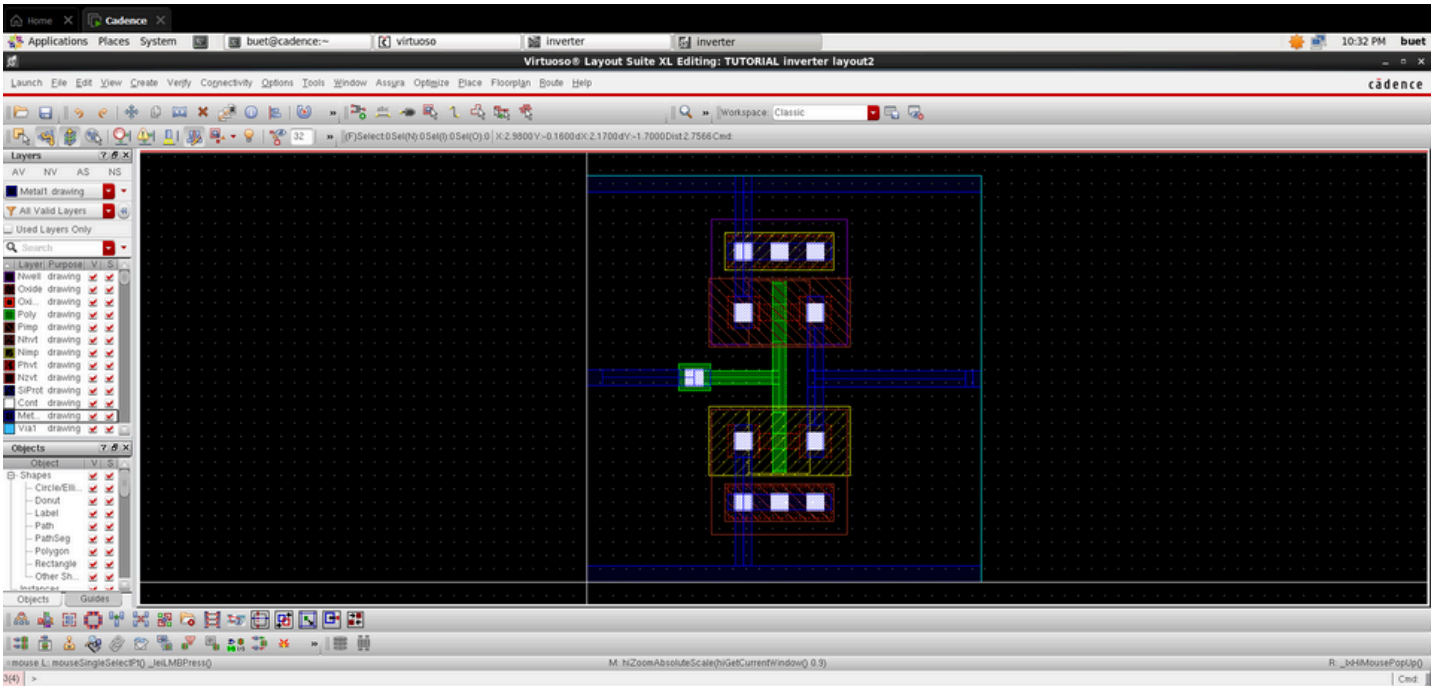
🧱 Layout

The layout is the physical implementation of your schematic, defining how the circuit will be fabricated on silicon.

- Purpose: Maps the circuit to actual geometries and layers used in manufacturing.
- Tools: Created using the Layout Editor in Virtuoso.
- Features:
  - Place and route transistors, wires, vias, and other elements.
  - Ensure design rules are met (DRC).

- Perform LVS (Layout vs. Schematic) checks to verify consistency.

- Post-Layout Simulation: You can extract parasitics and simulate the layout using the same test bench setup with an extracted view.



Objective

To design, simulate, and understand the behavior of a CMOS inverter using the gpdk90nm process technology in Cadence Virtuoso. The inverter is a fundamental digital logic gate that outputs the opposite logic level of its input.

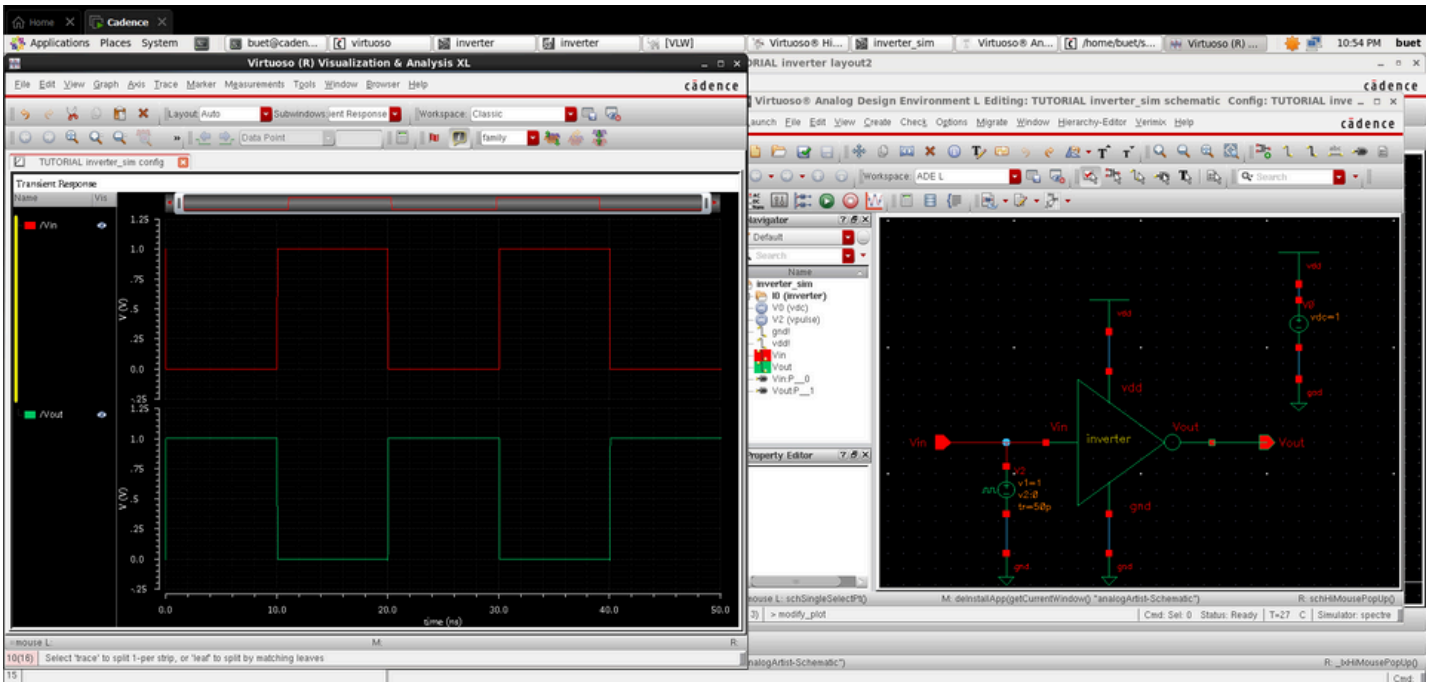
- Process Design Kit (PDK): gpdk090 (90nm generic process)
- Tool: Cadence Virtuoso
- Libraries: analogLib for basic components, gpdk090 for technology-specific devices

To design and implement the layout of a CMOS inverter using the gpdk90nm process technology in Cadence Virtuoso. The goal is to translate the schematic-level circuit into its physical representation, ensuring proper device placement, routing, and adherence to design rules. This step is essential for preparing the circuit for fabrication and for performing post-layout verification such as DRC (Design Rule Check) and LVS (Layout vs. Schematic) to confirm functional and structural correctness.

📊 Observations

After running the transient simulation of the CMOS inverter in Cadence Virtuoso, the output graph clearly illustrates the inverter's fundamental behavior. As the input voltage waveform transitions between low and high states, the output responds by switching in the opposite direction. When the input is at a low voltage level (close to 0V), the PMOS transistor conducts, pulling the output high toward the supply voltage (typically 1.2V in gpdk90nm technology). Conversely, when the input rises to a high level, the NMOS transistor turns on, pulling the output down to ground.

The waveform viewer displays this dynamic as a clean, sharp transition between logic levels. The output waveform is essentially an inverted replica of the input pulse, with minimal delay and distortion, assuming ideal conditions. The edges of the output signal are steep, reflecting the fast switching speed of the 90nm transistors. There may be a slight propagation delay between the input and output transitions, which is typical in real circuits and can be analyzed further for timing optimization.



✅ Conclusion

Designing a CMOS inverter in Cadence using gpdk90nm technology provides a solid introduction to digital circuit design. It demonstrates the basic principles of complementary MOS logic and prepares the foundation for more complex digital and mixed-signal systems.