EE529 **EMBEDDED SYSTEMS**

Laboratory Assignment #1

1. Consider a *2x2* switch. It has two input data ports, *x(0)* and *x(1)*, and a *2* bit control signal *ctrl*. The input data are routed to output ports *y(0)* and *y(1)* according to the ctrl signal. The function table is specified as follows:

Input	***Output***		*Function*
ctrl	***y(1)***	***y(0)***	
00	*x1*	*x0*	pass
01	*x0*	*x1*	cross
10	*x0*	*x0*	broadcast x0
11	*x1*	*x1*	broadcast x1

2. Consider an arithmetic circuit that can perform four operations: *a+b*, *a-b*, *a+1* and *a-1*, where *a* and *b* are *16* bit unsigned numbers and the desired operation is specified by a *2* bit control signal ctrl.
   (a) Design the circuit using two adders, one incrementor and one decrementor. Derive the VHDL code.
   (b) Design the circuit using only one adder. Derive the VHDL code.
   In both the cases, start with the data-flow model of a half adder circuit. Then use the half adder as components in your hierarchical structural design.

3. In an analog amplifier, the output voltage becomes saturated (i.e. reaching the most positive voltage, *+Vcc* or the most negative voltage, *-Vcc*), when the output exceeds the maximal range. In some digital signal processing applications, we wish to design an *8* bit signed saturation adder that mimics the behavior of an analog amplifier; i.e. if the addition result overflows, the result becomes the most positive or the most negative numbers. Draw the top level diagram and derive the VHDL code accordingly.