EE529 **EMBEDDED SYSTEMS**

Laboratory Assignment #4

1. Model a half adder circuit using VHDL. Use the data flow style of model. Now realize the half adder using FPGA. Provide the inputs through slide switches and observe the output in LEDs. Study the RTL schematic and technology schematic and analyze how the logic function of the half adder has been realized using the configurable logic blocks of the FPGA.

2. Use the half adder in problem 1 to realize a full adder.

3. Use the full adder in problem 2 to realize a 4 bit ripple carry adder and carry look-ahead adder. Study the technology schematic of the two adders. What can you infer from this?

4. Realize a system on FPGA board such that once you raise a slide switch, you will be able to see the corresponding number on the LED 7 segment displays

5. Repeat problem no. 1 using push button switches.

6. Modify the design in problem 3 to realize a 4 bit adder subtractor.