EE593 : Low Power VLSI Design
CMOS Inverter Design

CMOS Inverter Design

A CMOS inverter can be designed with one PMOS in the pull up network and one NMOS in the pull down network. The minimum size of the inverter is 1 (2:1 is the ratio of PMOS to NMOS width, width of PMOS is twice of the NMOS). The goal of this experiment is to design a CMOS inverter and then estimating the power and energy consumption through spice simulations.

1. Design a CMOS inverter with the following specification

   (a) switching threshold = $\frac{1}{2}V_{DD}$

   (b) Propagation delay, $\tau_{p-lh} = \tau_{p-hl}$

   Report the values of the inverter sizes. Explain the procedure to estimate the switching threshold and propagation delay. Report the errors as a percentage in the report. **[5 Marks]**

2. Estimate the propagation delay and power consumed for a CMOS inverter varying the input rise time as 10 ps, 50 ps, 100 ps, 500 ps, and 1000 ps. (assume the same time period for the input for all cases) Assume $C_L = 1.5fF$. **[5 Marks]**

3. Estimate the propagation delay and power consumed for a CMOS inverter varying the load capacitance $C_L = 0.5fF$ to $15fF$. (at least five variations). **[5 Marks]**

4. With the same sizes, check the operation of the inverter when $V_{dd} = V_{tn} + |V_{tp}|$ and report the power and delay. **[5 Marks]**

Submission: [10 Marks]

- Prepare a two-page report (in LaTeX two-column) and submit a PDF in Moodle. One submission per group.
- Give all your calculated values in a single table.
- One simulation plot to show the output with varying rise/fall time of input, and one simulation plot with varying load capacitance.
- Give justification and reasons for the behavior of your plots.
- *Extra marks will be given to those who present results effectively through comparison plots and analysis.*

Marks - 30