Analysis of Delay and Power in a CMOS Inverter

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I. Effect of Inverter Sizing on Switching Threshold

Methodology

The switching threshold V_M of a CMOS inverter is defined as the input voltage at which $V_{in} = V_{out}$. A DC voltage transfer characteristic (VTC) analysis is carried out by sweeping the input voltage from 0 to V_{DD}. The switching threshold is identified at the intersection of the VTC curve with the line $V_{out} = V_{in}$.

The transistor sizes are adjusted to achieve a switching threshold close to $\frac{V_{DD}}{2} = 0.9\,\text{V}$. The percentage error is calculated as

$$\%\ \text{Error} = \frac{\left|V_M - \frac{V_{DD}}{2}\right|}{\frac{V_{DD}}{2}} \times 100 \tag{1}$$

Table I lists the measured switching thresholds for different inverter sizing factors (β) along with their percentage error with respect to the ideal value(900mV).

TABLE I: Percentage Error in Switching Threshold for Different Inverter Sizes

Inverter Size (β)	V_m (mV)	Error (%)
2	813.93	-9.56
3	857.69	-4.70
4	891.30	-0.97
5	919.21	+2.13

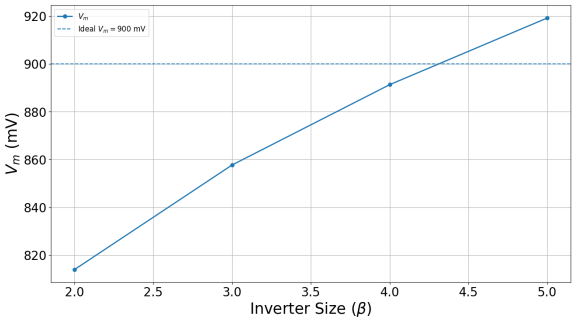

Fig. 1: Switching Threshold Voltage for Different Sizing Factors (β)

It is observed that increasing the inverter size reduces the percentage error, bringing the switching threshold closer to the ideal value. For larger sizing factors, the switching threshold slightly exceeds the ideal value.

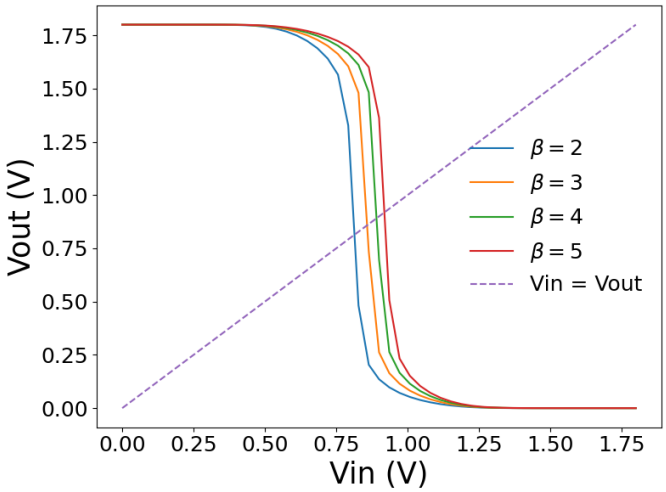

Fig. 2: Voltage Transfer Characteristics (VTC) of CMOS inverter for different sizing factors (β)

II. Effect of Inverter Sizing on Propagation Delay

A. *Methodology*

Propagation delay is estimated using transient analysis by applying a periodic input pulse. The low-to-high ($\tau_{p\text{-}lh}$) and high-to-low ($\tau_{p\text{-}hl}$) delays are measured between the input and output voltage crossings at 50% of V_{DD}.

The average propagation delay is given by

$$\tau_p = \frac{\tau_{p\text{-}lh} + \tau_{p\text{-}hl}}{2} \tag{2}$$

The percentage error for each transition is then evaluated separately. The error corresponding to the high-to-low transition is calculated as

$$\%\ \text{Error}_{hl} = \frac{|\tau_p - \tau_{p\text{-}hl}|}{\tau_p} \times 100 \tag{3}$$

Similarly, the percentage error for the low-to-high transition is given by

$$\%\ \text{Error}_{lh} = \frac{|\tau_p - \tau_{p\text{-}lh}|}{\tau_p} \times 100 \tag{4}$$

Table II lists the measured low-to-high (t_{PLH}) and high-to-low (t_{PHL}) propagation delays for different inverter sizing factors (β), along with the average propagation delay (t_p) and the corresponding percentage error with respect to t_p.

It is observed that for lower inverter sizes, a noticeable mismatch exists between t_{PHL} and t_{PLH}, resulting in a higher

TABLE II: Propagation Delay and Percentage Error for Different Inverter Sizes

β	t_{PHL} (ps)	t_{PLH} (ps)	t_p (ps)	Error (%) (t_{PHL}, t_{PLH})
2	30.98	42.81	36.90	(-16.03, +16.03)
3	35.52	37.34	36.43	(-2.49, +2.49)
4	39.41	34.31	36.86	(+6.92, -6.92)
5	43.18	32.26	37.72	(+14.48, -14.48)

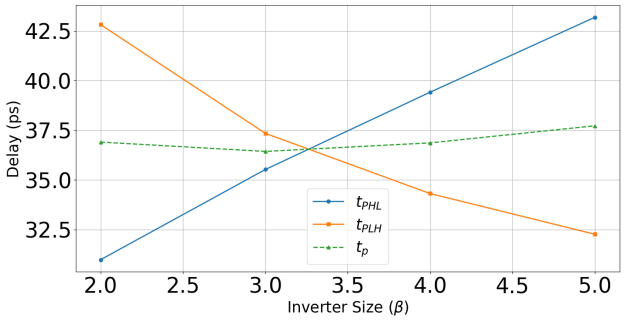

Fig. 3: Delay for Different Sizing Factors (β)

percentage error with respect to the average propagation delay. As the inverter size increases, the relative dominance of either the pull-up or pull-down network causes one delay component to exceed the average while the other falls below it. An optimal balance between t_{PHL} and t_{PLH} is observed for $\beta = 3$, where the percentage error is minimized.

III. Effect of Input Rise Time on Propagation Delay

The propagation delay of a CMOS inverter is characterized by the high-to-low (t_{PHL}) and low-to-high (t_{PLH}) transition delays. The average propagation delay is defined as

$$t_p = \frac{t_{PHL} + t_{PLH}}{2} \tag{5}$$

Table III summarizes the measured delays for different input rise times.

TABLE III: Propagation Delay and Percentage Error with Respect to Average Delay for Different Input Rise Times (T_r)

T_r(ps)	t_{PHL}(ps)	t_{PLH}(ps)	t_p(ps)	Error(%) (t_{PHL}, t_{PLH})
10	12.73	42.61	27.67	(-54.00, +54.00)
50	20.89	42.61	31.75	(-34.20, +34.20)
100	26.78	42.61	34.70	(-22.83, +22.83)
500	40.80	42.61	41.71	(-2.18, +2.18)
1000	35.73	42.61	39.17	(-8.79, +8.79)

It is observed that t_{PHL} increases with increasing input rise time due to slower NMOS discharge, while t_{PLH} remains nearly constant, indicating a stronger PMOS pull-up network. Consequently, the overall propagation delay increases with input transition time.

IV. Effect of Input Rise Time on Power Consumption

The total power consumption of a CMOS inverter consists of static power, mainly arising from leakage and short-circuit currents, and dynamic power due to the charging and discharging of load capacitance ($C_L = 1.5$ fF).

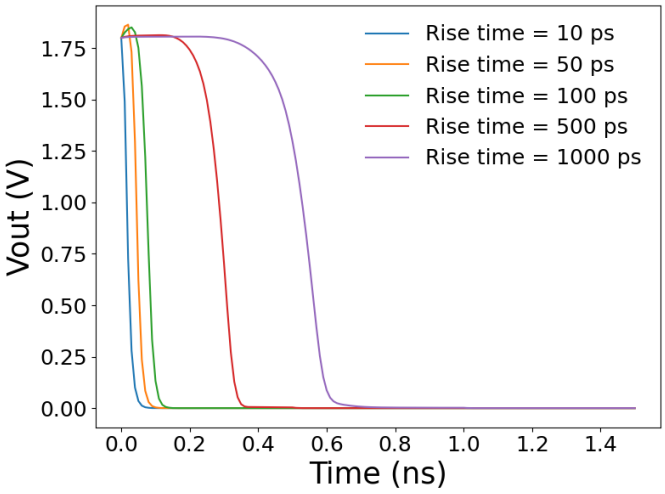

Fig. 4: Output high-to-low transition for different input rise times

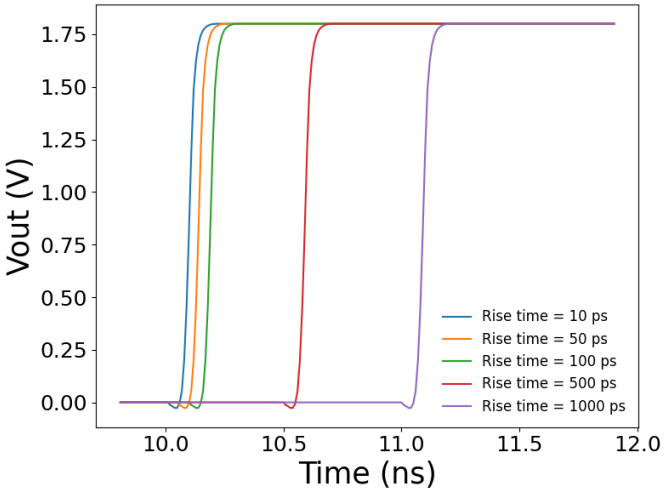

Fig. 5: Output low- -high transition for different input rise times

TABLE IV: Power Consumed for Different Input Rise Times

Input Rise Time	Power Consumed (μW)
1 ns	1.4890
500 ps	1.1316
100 ps	0.9220
50 ps	0.9231
10 ps	0.9512

The plot shows the variation of power consumption with respect to input rise time. As the input rise time decreases from 1 ns to 100 ps, the power consumption reduces significantly due to lower short-circuit current. For very fast rise times (below 100 ps), the power shows a slight increase, indicating the dominance of parasitic and dynamic switching effects. Overall, the plot highlights the impact of input signal transition speed on circuit power dissipation.

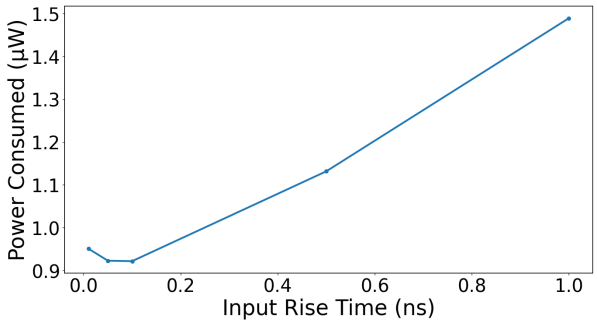

Fig. 6: Comparison plot for output low-to-high transition with different input rise times

V. Effect of Load Capacitance on Propagation Delay

The propagation delay of a CMOS inverter strongly depends on the load capacitance connected at the output node. An increase in load capacitance results in a longer charging and discharging time, thereby increasing both the low-to-high (t_{PLH}) and high-to-low (t_{PHL}) propagation delays. Table V summarizes the measured delays for different load capacitance values.

TABLE V: Propagation Delay Variation with Load Capacitance

Load Capacitance (fF)	t_{PLH} (ps)	t_{PHL} (ps)
0.5	34.97	20.60
3.4	54.15	40.73
6.3	69.65	52.98
9.2	85.15	64.00
12.1	100.57	74.94
15.0	116.10	85.86

It is observed that both t_{PLH} and t_{PHL} increase almost linearly with load capacitance, confirming the dominant role of capacitive charging and discharging in determining CMOS inverter delay.

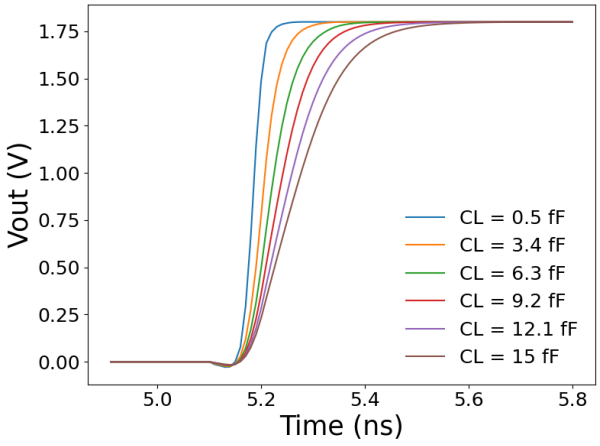

Fig. 7: Output voltage waveform for low-to-high transition with varying load capacitance

VI. Effect of Load Capacitance on Power Consumption

TABLE VI: Power Consumption for Different Load Capacitances

Load Capacitance (fF)	Power Consumed (μW)
0.5	0.6476
3.4	1.4660
6.3	2.1940
9.2	2.8180
12.1	3.5460
15.0	4.2730

Fig. 7 illustrates the output voltage waveform for the low-to-high transition (t_{PLH}) under different load capacitance conditions. As the load capacitance increases, the output charging time increases significantly, resulting in slower voltage transitions and higher propagation delay.

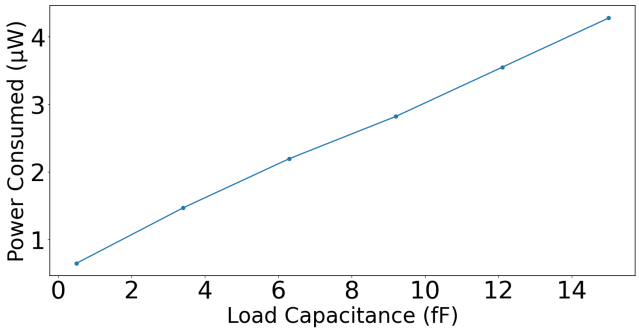

Fig. 8: Effect of load capacitance on power consumption

VII. Voltage Transfer Characteristics at $V_{DD} = V_{thp} + V_{thn}$

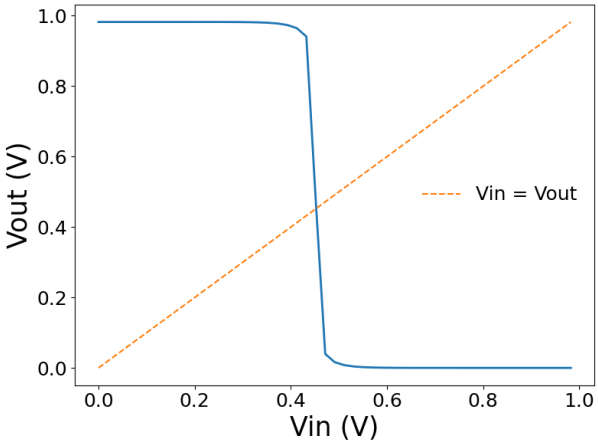

Fig. 9: Voltage transfer characteristics of CMOS inverter at $V_{DD} = 982.319$ mV

The voltage transfer characteristics (VTC) of a CMOS inverter were evaluated under a reduced supply voltage condition, where the supply voltage is set equal to the sum of the NMOS and PMOS threshold voltages, $V_{DD} = V_{thp} + V_{thn} = 982.319$ mV. The inverter was simulated with a load capacitance of 1.5 fF and an input rise time of $T_r = 100$ ps.

Fig. 9 illustrates the resulting VTC along with the reference line $V_{in} = V_{out}$. Even at this reduced supply voltage, the inverter exhibits a clear switching region, confirming correct logic inversion.

The average power consumption under this operating condition was measured to be 245 nW. These values indicate ultra-low-power operation, characteristic of near-threshold CMOS circuits, where leakage and switching energies are both substantially reduced compared to nominal supply voltage operation. The measured values for delays are $t_{PLH} = 0.099936$ ns, $t_{PHL} = 0.06483$ ns and the average propagation delay is $t_p = 0.082$ ns.