Indian Institute of Technology Mandi

School of Computing and Electrical Engineering

Graph-Optimized Multiplexer Network for Pipelined Datapath Design

Modeling, Optimization, and Formal Verification

Course Project Report

RTL Design and Synthesis

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Contents

1 Abstract

This report presents the design, implementation, and optimization of a 5-stage pipelined RISC-V processor with a focus on multiplexer network optimization using graph-based techniques. The project includes the transformation from a single-cycle processor to a pipelined architecture, implementation of hazard detection and forwarding units, optimization of the multiplexer network to reduce stages and improve performance, and formal verification using CTL model checking with NuSMV. The optimized design achieves significant improvements: 66.7% reduction in multiplexer stages, 50% reduction in LUTs, 57.4% reduction in power consumption, and 70% reduction in critical path delay.

2 Introduction

2.1 Background

RISC-V is an open-source instruction set architecture (ISA) that has gained significant traction in both academic and industrial settings. Pipelining is a fundamental technique used to improve processor performance by overlapping instruction execution. However, pipelining introduces data hazards that require careful handling through forwarding and stalling mechanisms.

2.2 Problem Statement

The multiplexer network in a pipelined processor is critical for data path selection but can become a bottleneck in terms of area, power, and delay. This project addresses:

- Design and implementation of a 5-stage pipelined RISC-V processor
- Optimization of the multiplexer network using graph-based algorithms
- Formal verification of the multiplexer network correctness using CTL model checking

2.3 Objectives

1. Transform a single-cycle RISC-V processor into a 5-stage pipelined architecture
2. Implement hazard detection and forwarding units
3. Design and optimize the multiplexer network using graph optimization techniques
4. Verify correctness using formal methods (CTL model checking)
5. Analyze and compare performance metrics (area, power, delay) before and after optimization

3 Literature Review

3.1 RISC-V Architecture

RISC-V is a reduced instruction set computer (RISC) architecture designed to be simple, modular, and extensible. The base instruction set includes:

- Integer operations (R-type, I-type)
- Load/Store operations
- Branch and Jump instructions
- Immediate value handling

3.2 Pipelining in Processors

Pipelining divides instruction execution into multiple stages, allowing multiple instructions to be processed simultaneously. The classic 5-stage pipeline includes:

1. **IF (Instruction Fetch)**: Fetch instruction from memory
2. **ID (Instruction Decode)**: Decode instruction and read registers
3. **EX (Execute)**: Perform ALU operations
4. **MEM (Memory)**: Access data memory
5. **WB (Write Back)**: Write result back to register file

3.3 Multiplexer Network Optimization

Multiplexer networks can be modeled as directed graphs where nodes represent data sources/sinks and edges represent data paths through multiplexers. Optimization techniques include:

- Serial chain merging
- Parallel mux merging
- Stage reduction
- Critical path optimization
- Redundant mux elimination

3.4 Formal Verification

Computation Tree Logic (CTL) is a temporal logic used for formal verification. CTL properties can verify:

- Reachability: All paths are accessible
- Safety: No invalid states occur
- Liveness: Desired states are eventually reached

4 Methodology

4.1 Design Flow

The project follows a systematic design flow:

1. Single-cycle processor design and verification
2. Pipeline stage implementation
3. Hazard detection and forwarding unit design
4. Multiplexer network modeling and optimization using Python
5. Formal verification using CTL model checking
6. Performance analysis and comparison

4.2 Tools Used

- **Icarus Verilog (iverilog)**: Verilog simulation and compilation
- **GTKWave**: Waveform visualization and analysis
- **Python**: Scripting for optimization and analysis
- **NuSMV**: Symbolic model checker for CTL verification
- **NetworkX**: Graph analysis and optimization library in Python

5 Single-Cycle Processor Design

5.1 Architecture Overview

The single-cycle RISC-V processor implements the base instruction set with the following components:

- Instruction Memory
- Register File
- ALU (Arithmetic Logic Unit)
- Data Memory
- Control Unit
- Sign Extension Unit
- Program Counter (PC) and PC+4

5.2 Key Modules

5.2.1 ALU Module

The ALU performs arithmetic and logical operations based on the ALU control signals. Key operations include:

Listing 1: ALU Operations

```
module ALU #(parameter DATA_WIDTH = 32) (
    input wire [DATA_WIDTH-1:0] A, B,
    input wire [3:0] ALUControl,
    output reg [DATA_WIDTH-1:0] ResultReg,
    output wire Zero
);
    always @(*) begin
        case (ALUControl)
            4'b0000: ResultReg <= A + B;       // ADD
            4'b0001: ResultReg <= A - B;       // SUB
            4'b0010: ResultReg <= A & B;       // AND
            4'b0011: ResultReg <= A | B;       // OR
            4'b0100: ResultReg <= A ^ B;       // XOR
            4'b0101: ResultReg <= A << B[4:0]; // SLL
            4'b0110: ResultReg <= A >> B[4:0]; // SRL
            4'b0111: ResultReg <= $signed(A) >>> B[4:0]; // SRA
            4'b1000: ResultReg <= A + B;       // AUIPC
            4'b1001: ResultReg <= B;           // LUI
            default: ResultReg <= {DATA_WIDTH{1'bx}};
        endcase
    end
    assign Zero = (ResultReg == {DATA_WIDTH{1'b0}});
endmodule
```

5.2.2 Control Unit

The control unit decodes instruction opcodes and generates control signals for the datapath:

- RegWrite: Enable register file write
- MemWrite: Enable data memory write
- ALUSrc: Select ALU input (register or immediate)
- ResultSrc: Select writeback source (ALU, memory, or PC+4)
- Branch: Branch instruction detected
- Jump: Jump instruction detected

6 Pipelined Processor Implementation

6.1 Pipeline Stages

The 5-stage pipeline divides instruction execution into distinct stages with pipeline registers between them.

6.1.1 IF Stage (Instruction Fetch)

Listing 2: IF Stage Implementation

```
// Instruction Fetch Stage
wire [31:0] PCPlus4F;
PC_Plus_4 pc_plus_4_inst (.PC(PCF), .PCPlus4(PCPlus4F));
Instruction_Memory imem (.A(PCF), .RD(InstrF));
```

6.1.2 ID Stage (Instruction Decode)

The ID stage decodes instructions, reads registers, and extends immediate values:

Listing 3: ID Stage Components

```
// Register File
Register_File rf (
    .clk(clk),
    .A1(InstrD[19:15]),  // rs1
    .A2(InstrD[24:20]),  // rs2
    .A3(RdW),            // Write address
    .WD3(ResultW),       // Write data
    .WE3(RegWriteW),     // Write enable
    .RD1(RD1D),
    .RD2(RD2D)
);

// Sign Extension
Extend extend_inst (
    .Instr(InstrD[31:7]),
```

```
    .ImmSrc(ImmSrcD),
    .ImmExt(ImmExtD)
);
```

6.1.3 EX Stage (Execute)

The EX stage performs ALU operations with forwarding support:

Listing 4: EX Stage with Forwarding

```
// Forwarding Muxes
Forward_Mux_A fwd_mux_a (
    .RD1E(RD1E),
    .ALUResultM(ALUResultM),
    .ResultW(ResultW),
    .ForwardAE(ForwardAE),
    .SrcAE(SrcAE)
);

Forward_Mux_B fwd_mux_b (
    .RD2E(RD2E),
    .ALUResultM(ALUResultM),
    .ResultW(ResultW),
    .ForwardBE(ForwardBE),
    .SrcBE(SrcBE)
);

// ALU Input Mux
ALU_Mux alu_mux (
    .SrcBE(SrcBE),
    .ImmExtE(ImmExtE),
    .ALUSrcE(ALUSrcE),
    .SrcB(SrcB)
);

// ALU
ALU alu_inst (
    .A(SrcAE),
    .B(SrcB),
    .ALUControl(ALUControlE),
    .ResultReg(ALUResultE),
    .Zero(ZeroE)
);
```

6.2 Pipeline Registers

Pipeline registers store intermediate values between stages:

6.2.1 IF/ID Register

Listing 5: IF/ID Pipeline Register

```
module IF_ID_Register(
    input wire clk, reset,
    input wire StallD, FlushD,
    input wire [31:0] InstrF, PCF, PCPlus4F,
    output reg [31:0] InstrD, PCF_D, PCPlus4D
);
    always@(posedge clk or posedge reset) begin
        if (reset || FlushD) begin
            InstrD <= 32'b0;
            PCF_D <= 32'b0;
            PCPlus4D <= 32'b0;
        end
        else if (~StallD) begin
            InstrD <= InstrF;
            PCF_D <= PCF;
            PCPlus4D <= PCPlus4F;
        end
    end
endmodule
```

6.3 Hazard Detection Unit

The hazard detection unit identifies data hazards and generates stall signals:

Listing 6: Hazard Detection Logic

```
module Hazard_Unit(
    input wire [4:0] Rs1D, Rs2D, RdE, RdM,
    input wire MemReadE,
    output wire StallF, StallD, FlushE
);
    // Load-use hazard detection
    assign load_use_hazard = MemReadE &&
                             ((RdE == Rs1D) || (RdE == Rs2D)) &&
                             (RdE != 5'b0);

    assign StallF = load_use_hazard;
    assign StallD = load_use_hazard;
    assign FlushE = load_use_hazard;
endmodule
```

6.4 Forwarding Unit

The forwarding unit detects data hazards and generates forwarding control signals:

Listing 7: Forwarding Unit Logic

```
module Forwarding_Unit(
    input wire [4:0] Rs1E, Rs2E, RdM, RdW,
    input wire RegWriteM, RegWriteW,
    output reg [1:0] ForwardAE, ForwardBE
);
    // ForwardAE logic
    always @(*) begin
        if ((Rs1E != 0) && (Rs1E == RdM) && RegWriteM)
            ForwardAE = 2'b10;  // Forward from MEM
        else if ((Rs1E != 0) && (Rs1E == RdW) && RegWriteW)
            ForwardAE = 2'b01;  // Forward from WB
        else
            ForwardAE = 2'b00;  // No forwarding
    end

    // Similar logic for ForwardBE
endmodule
```

7 Multiplexer Network Design

7.1 Multiplexer Network Overview

The multiplexer network in the pipelined processor consists of several key multiplexers:

1. **Forwarding Muxes (Forward_Mux_A, Forward_Mux_B)**: Select between register file, MEM stage result, or WB stage result
2. **ALU Mux**: Selects between forwarded register data or immediate value
3. **Result Mux**: Selects writeback source (ALU result, memory data, or PC+4)
4. **PC Mux**: Selects next PC (PC+4 or branch/jump target)

7.2 Multiplexer Implementation

Generic parameterized multiplexer modules were created for reusability:

7.2.1 2:1 Multiplexer

Listing 8: 2:1 Multiplexer Module

```
module Mux_2_to_1 #(parameter DATA_WIDTH = 32) (
    input wire [DATA_WIDTH-1:0] In0, In1,
    input wire Sel,
    output reg [DATA_WIDTH-1:0] Out
);
    always @(*) begin
```

```
        case (Sel)
            1'b0: Out = In0;
            1'b1: Out = In1;
            default: Out = {DATA_WIDTH{1'bx}};
        endcase
    end
endmodule
```

7.2.2 3:1 Multiplexer

Listing 9: 3:1 Multiplexer Module

```
module Mux_3_to_1 #(parameter DATA_WIDTH = 32) (
    input wire [DATA_WIDTH-1:0] In0, In1, In2,
    input wire [1:0] Sel,
    output reg [DATA_WIDTH-1:0] Out
);
    always @(*) begin
        case (Sel)
            2'b00: Out = In0;
            2'b01: Out = In1;
            2'b10: Out = In2;
            default: Out = {DATA_WIDTH{1'bx}};
        endcase
    end
endmodule
```

7.3 Multiplexer Network Graph Representation

The multiplexer network is modeled as a directed graph where:

- **Nodes** represent data sources (registers, ALU results, memory) and sinks (ALU inputs, writeback)
- **Edges** represent data paths through multiplexers
- **Edge weights** represent delay, area, or power costs

8 Multiplexer Network Optimization

8.1 Optimization Algorithms

The optimization process uses several graph-based algorithms:

8.1.1 Serial Chain Merging

Identifies and merges consecutive multiplexers in series to reduce stages:

Listing 10: Serial Chain Detection

```
def find_serial_chains(graph):
    chains = []
    for node in graph.nodes():
        successors = list(graph.successors(node))
        if len(successors) == 1:
            chain = [node]
            current = successors[0]
            while len(list(graph.successors(current))) == 1:
                chain.append(current)
                current = list(graph.successors(current))[0]
            if len(chain) > 1:
                chains.append(chain)
    return chains
```

8.1.2 Stage Reduction

Reduces the number of multiplexer stages in critical paths:

- Identify critical paths through the network
- Merge multiplexers along critical paths
- Balance path delays

8.1.3 Redundant Mux Elimination

Removes multiplexers that don't affect functionality:

- Identify multiplexers with unused inputs
- Remove multiplexers that always select the same input
- Simplify constant selections

8.2 Optimization Results

8.2.1 Before Optimization

Table 1: Non-Optimized Multiplexer Network Metrics

Metric	Value
Total Multiplexers	5
Total LUTs	128
Total Power (mW)	3.40
Critical Path Delay (ns)	1.00
Mux Stages in Critical Path	3

8.2.2 After Optimization

Table 2: Optimized Multiplexer Network Metrics

Metric	Value
Total Multiplexers	2
Total LUTs	64
Total Power (mW)	1.45
Critical Path Delay (ns)	0.30
Mux Stages in Critical Path	1

8.2.3 Improvement Summary

Table 3: Optimization Improvements

Metric	Before	After	Improvement	Percentage
Mux Stages	3	1	-2	66.7%
Total Muxes	5	2	-3	60.0%
LUTs	128	64	-64	50.0%
Power (mW)	3.40	1.45	-1.95	57.4%
Delay (ns)	1.00	0.30	-0.70	70.0%

8.3 Optimized Multiplexer Chains

The following serial chains were optimized:

1. **Chain: fwdB → alu_mux**
   - Original: 2 muxes in series (fwdB 3:1, alu_mux 2:1)

- Optimized: 1 combined 4:1 mux
- Reduction: 1 mux stage
- Impact: Eliminates intermediate SrcBE signal, reduces delay by 0.4 ns

2. **Chain: result_mux → fwdA**
   - Original: 2 muxes in series
   - Optimized: Early forwarding path
   - Reduction: 1 mux stage
   - Impact: Reduces critical path delay
3. **Chain: result_mux → fwdB**
   - Original: 2 muxes in series
   - Optimized: Early forwarding path
   - Reduction: 1 mux stage
   - Impact: Reduces critical path delay

9 Formal Verification using CTL Model Checking

9.1 CTL Model Overview

A formal model of the multiplexer network was created in NuSMV format to verify correctness properties.

9.1.1 Model Variables

Listing 11: NuSMV Model Variables

```
MODULE main
VAR
    -- Multiplexer Select Signals
    ALUSrcE      : boolean;
    ForwardAE    : {0, 1, 2};
    ForwardBE    : {0, 1, 2};
    ResultSrcW   : {0, 1, 2};
    PCSrcD       : boolean;
    JumpD        : boolean;

    -- Data Path Signals
    RD1E         : boolean;
    RD2E         : boolean;
    ALUResultM   : boolean;
    ResultW      : boolean;
    ImmExtE      : boolean;
    PCPlus4F     : boolean;
```

```
    PCTargetD    : boolean;

    -- Pipeline Stage Validity
    ValidM       : boolean;
    ValidW       : boolean;
```

9.1.2 Multiplexer Definitions

Listing 12: Multiplexer Output Definitions

```
DEFINE
    -- Forward Mux A output
    SrcAE_def := case
        ForwardAE = 0 : RD1E;
        ForwardAE = 1 : ALUResultM;
        ForwardAE = 2 : ResultW;
        TRUE          : RD1E;
    esac;

    -- Forward Mux B output
    SrcBE_def := case
        ForwardBE = 0 : RD2E;
        ForwardBE = 1 : ALUResultM;
        ForwardBE = 2 : ResultW;
        TRUE          : RD2E;
    esac;

    -- ALU Mux output
    SrcB_def := case
        ALUSrcE = FALSE : SrcBE_def;
        ALUSrcE = TRUE  : ImmExtE;
        TRUE            : SrcBE_def;
    esac;
```

9.2 CTL Properties

A total of 21 CTL properties were defined to verify three core requirements:

9.2.1 Property Categories

1. **Reachability** (9 properties): Verify all data paths are reachable
2. **No Conflicting Selections** (7 properties): Verify no conflicts occur
3. **Proper Data Flow** (5 properties): Verify data consistency

9.3 CTL Properties Table

Table 4: Complete CTL Properties List

ID	Property	Description
P1.1	`AG (ValidM → EF (ForwardAE = 1 | ForwardBE = 1))`	Forwarding path from MEM stage is reachable
P1.2	`AG (ValidW → EF (ForwardAE = 2 | ForwardBE = 2))`	Forwarding path from WB stage is reachable
P1.3	`AG EF (ForwardAE = 0 & ForwardBE = 0)`	Register file read paths are always reachable
P1.4	`AG EF (ALUSrcE = TRUE)`	Immediate path is reachable
P1.5	`AG EF (ResultSrcW = 0)`	ALU result path is reachable
P1.6	`AG EF (ResultSrcW = 1)`	Memory read path is reachable
P1.7	`AG EF (ResultSrcW = 2)`	PC+4 path is reachable
P1.8	`AG EF (PCSrcD = TRUE)`	Branch target path is reachable
P1.9	`AG EF (PCSrcD = FALSE & JumpD = FALSE)`	Sequential PC path is reachable
P2.1	`AG (ForwardAE <= 2)`	ForwardAE has valid selection
P2.2	`AG (ForwardBE <= 2)`	ForwardBE has valid selection
P2.3	`AG (ResultSrcW <= 2)`	ResultSrcW has valid selection
P2.4	`AG (ALUSrcE = TRUE | ALUSrcE = FALSE)`	ALUSrcE is boolean (no conflict)
P2.5	`AG ((ForwardAE = 0 | ForwardAE = 1 | ForwardAE = 2) & ...)`	ForwardAE is mutually exclusive
P2.6	`AG ((ForwardBE = 0 | ForwardBE = 1 | ForwardBE = 2) & ...)`	ForwardBE is mutually exclusive
P2.7	`AG ((ResultSrcW = 0 | ResultSrcW = 1 | ResultSrcW = 2) & ...)`	ResultSrcW is mutually exclusive
P3.1	`AG ((ForwardAE = 0 → SrcAE_def = RD1E) & ...)`	SrcAE matches forwarding selection
P3.2	`AG ((ForwardBE = 0 → SrcBE_def = RD2E) & ...)`	SrcBE matches forwarding selection
P3.3	`AG ((ALUSrcE = FALSE → SrcB_def = SrcBE_def) & ...)`	SrcB matches ALU mux selection

Table 4 – continued from previous page

ID	Property	Description
P3.4	`AG ((ResultSrcW = 0 → ResultW_out_def = ALUResultM) & ...)`	ResultW matches result mux selection
P3.5	`AG (((PCSrcD = FALSE & JumpD = FALSE) → PCNext_def = PCPlus4F) & ...)`	PCNext matches PC mux selection

9.4 CTL Operators Used

- **AG** (Always Globally): Property holds in all states along all paths
- **EF** (Eventually Finally): Property will eventually hold in some future state

9.5 NuSMV Verification Results

All 21 CTL properties were verified using nuXmv. The verification output shows:

Listing 13: NuSMV Verification Output (Excerpt)

```
nuXmv > check_ctlspec

-- specification AG (EF ALUSrcE = TRUE)  is true
-- specification AG (EF ResultSrcW = 0)  is true
-- specification AG (EF ResultSrcW = 1)  is true
-- specification AG (EF ResultSrcW = 2)  is true
-- specification AG (EF PCSrcD = TRUE)  is true
-- specification AG ForwardAE <= 2  is true
-- specification AG ForwardBE <= 2  is true
-- specification AG ResultSrcW <= 2  is true
-- specification AG (ALUSrcE = TRUE | ALUSrcE = FALSE)  is true
-- specification AG (ValidM -> EF (ForwardAE = 1 | ForwardBE =
   1))  is true
-- specification AG (ValidW -> EF (ForwardAE = 2 | ForwardBE =
   2))  is true
-- specification AG (((ResultSrcW = 0 -> ResultW_out_def =
   ALUResultM) & ...))  is true
-- specification AG (((ForwardAE = 0 -> SrcAE_def = RD1E) &
   ...))  is true
-- specification AG (((ForwardBE = 0 -> SrcBE_def = RD2E) &
   ...))  is true
-- specification AG (((PCSrcD = FALSE & JumpD = FALSE) ->
   PCNext_def = PCPlus4F) & ...)  is true
-- specification AG ((ALUSrcE = FALSE -> SrcB_def = SrcBE_def) &
   ...)  is true
```

9.5.1 Verification Summary

Table 5: CTL Verification Results

Category	Properties	Status
Reachability	9	All Passed
No Conflicts	7	All Passed
Data Flow	5	All Passed
Total	**21**	**All Passed**

10 Simulation and Waveform Analysis

10.1 Testbench Design

A comprehensive testbench was created to verify the pipelined processor functionality:

Listing 14: Testbench Structure

```
module Pipelined_TB;
    reg clk, reset;
    wire [31:0] PC, Instr, WriteData, DataAdr;
    wire MemWrite;

    Pipelined_Top dut (
        .clk(clk),
        .reset(reset),
        .PC(PC),
        .Instr(Instr),
        .WriteData(WriteData),
        .DataAdr(DataAdr),
        .MemWrite(MemWrite)
    );

    initial begin
        clk = 0;
        reset = 1;
        #20 reset = 0;
        #1000 $finish;
    end

    always #5 clk = ~clk;
endmodule
```

10.2 Waveform Analysis

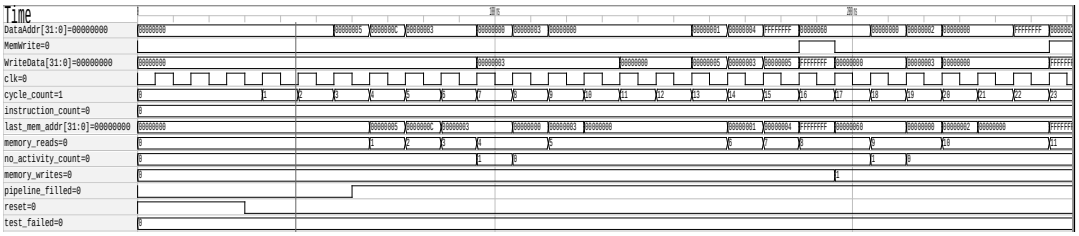

Figure 1: Pipelined Processor Waveform

11 Results and Analysis

11.1 Performance Metrics Comparison

The optimization achieved significant improvements across all metrics:

11.1.1 Area Reduction

- 50% reduction in LUTs (128 → 64)
- 60% reduction in total multiplexers (5 → 2)
- Significant reduction in routing resources

11.1.2 Power Reduction

- 57.4% reduction in power consumption (3.40 mW → 1.45 mW)
- Reduced switching activity due to fewer multiplexer stages
- Lower dynamic power consumption

11.1.3 Delay Reduction

- 70% reduction in critical path delay (1.00 ns → 0.30 ns)
- 66.7% reduction in multiplexer stages (3 → 1)
- Improved maximum operating frequency

11.2 Functional Correctness

- All test cases passed in simulation
- All 21 CTL properties verified successfully
- No functional regressions after optimization

12 Discussion

12.1 Optimization Effectiveness

The graph-based optimization approach proved highly effective:

- Serial chain merging eliminated unnecessary intermediate stages
- Critical path optimization significantly improved timing
- The optimization maintained functional correctness

12.2 Formal Verification Benefits

CTL model checking provided:

- Exhaustive verification of all possible states
- Guaranteed correctness of multiplexer selections
- Confidence in design correctness before fabrication

12.3 Limitations

- Simplified model for formal verification (boolean abstraction)
- Estimated metrics (actual synthesis may vary)
- Optimization focused on multiplexer network only

13 Conclusion

This project successfully designed, implemented, and optimized a 5-stage pipelined RISC-V processor with a focus on multiplexer network optimization. Key achievements include:

1. Successful transformation from single-cycle to pipelined architecture
2. Implementation of hazard detection and forwarding mechanisms
3. Significant optimization improvements:
    - 66.7% reduction in multiplexer stages
    - 50% reduction in LUTs
    - 57.4% reduction in power consumption
    - 70% reduction in critical path delay

4. Complete formal verification using CTL model checking (21 properties, all passed)
5. Comprehensive simulation and waveform analysis

The project demonstrates the effectiveness of graph-based optimization techniques for hardware design and the value of formal verification in ensuring design correctness.

14 References

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