



Delta-Sigma ($\Delta\Sigma$) ADC Design

For Space-Grade Devices

TEAM - 82

The Challenge: ISRO's Vision

Design and develop a high-resolution Delta–Sigma ADC architecture suitable for ASIC implementation. The objective is to achieve 16–19 bits ENOB across 0.5–2 ksps (or wider) Nyquist sampling rates through:

- 1 Exploration of Delta-Sigma modulator architectures (discrete/continuous-time, hybrid).
- 2 Evaluation of digital/decimation filters such as SINC, FIR, and IIR, and selection of optimal order.
- 3 Trade-off analysis between sampling rate, modulator order, filter design, quantization, and ENOB.
- 4 Study of flicker noise impact and assessment of noise-reduction schemes for >16-bit performance.
- 5 MATLAB/Simulink modeling, followed by RTL implementation of the selected digital/decimation filter in Verilog/VHDL.
- 6 Execution of ASIC design flow: synthesis, place-and-route, and post-layout simulation.

—

Why Delta-Sigma ADCs? The Technical Edge

Advantages over other ADC's

- Excellent for low-bandwidth, high-precision sensing, where accuracy matters more than speed
- Oversampling reduces in-band quantization noise, improving SNR without complex analog circuitry
- Noise shaping pushes most quantization noise out of the signal band ($\propto f^{2N}$), enabling very high effective resolution
- Relaxed analog component requirements — integrators and comparators do not need tight matching
- High resolution achievable with a simple 1-bit quantizer, eliminating DAC linearity and matching issues

Fundamental Relationships

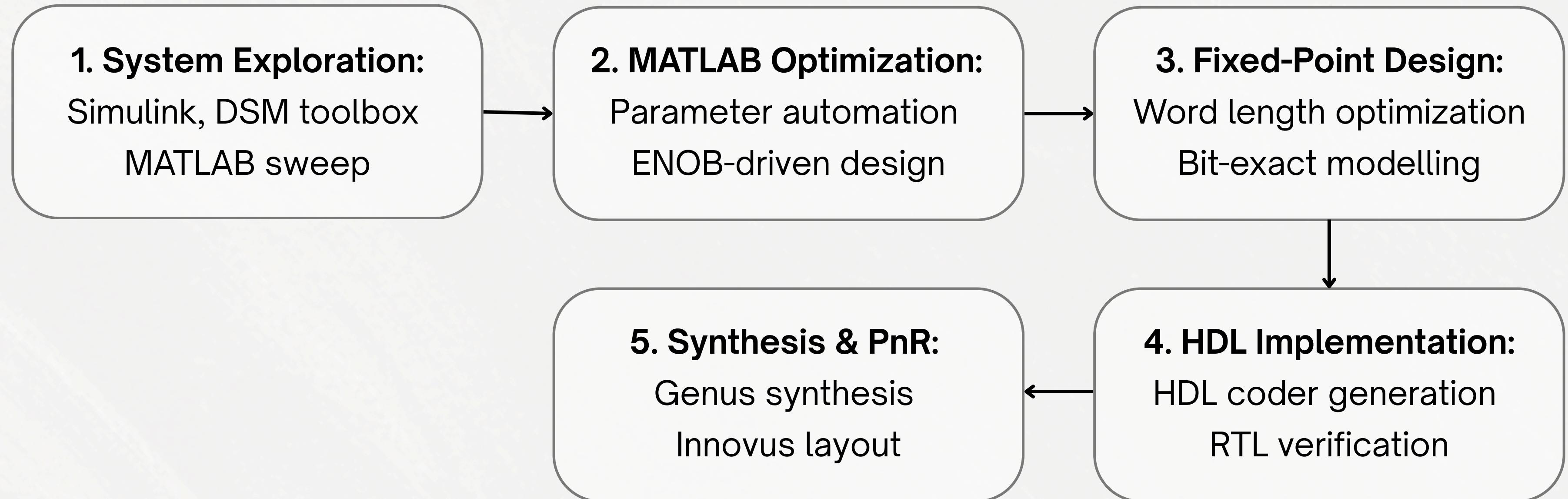
$$ENOB \approx \frac{SNDR - 1.76}{6.02} \text{ dB}$$

For 16 bits: Need $SNDR \geq 98 \text{ dB}$

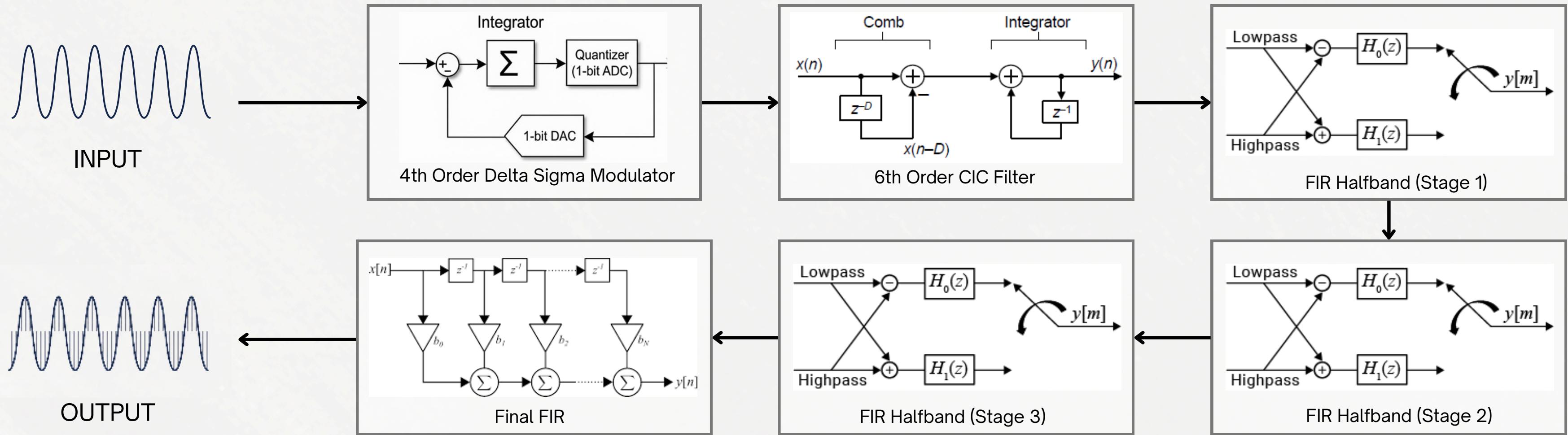
Design Trade Offs

Order $\uparrow \Rightarrow ENOB \uparrow, \text{Stability} \downarrow$

Our Design Methodology



Complete Architecture



MODULATOR: CONVERTS ANALOG SIGNAL TO HIGH-FREQUENCY 1-BIT STREAM (8.192 MHZ)

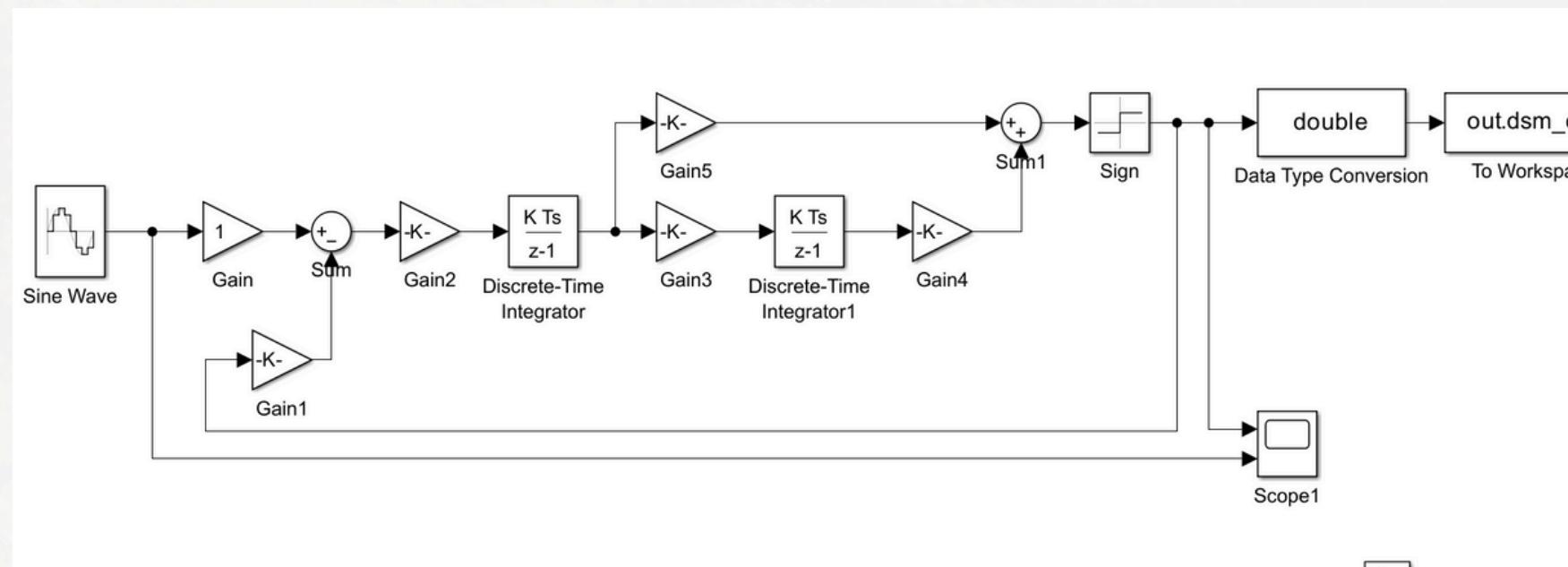
CIC FILTER: FIRST-STAGE DECIMATION REMOVES OUT OF BAND NOISE ($\rightarrow 32$ KHZ)

HALFBANDS: MULTI-STAGE EFFICIENT LOWPASS FILTERING ($\rightarrow 4$ KHZ)

FINAL FIR: SHARP ANTI-ALIASING FILTER FOR CLEAN OUTPUT ($\rightarrow 2$ KHZ)

RESULT: 20-BIT DIGITAL OUTPUT WITH 16+ BITS EFFECTIVE RESOLUTION

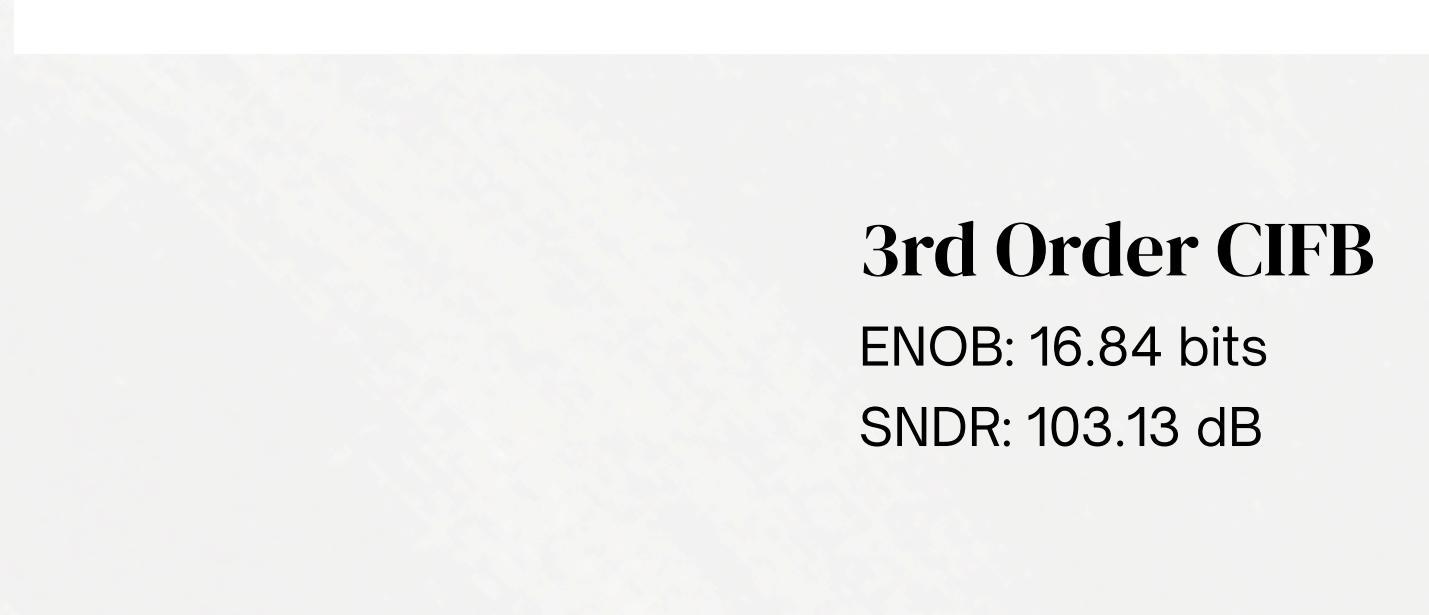
Evaluated Modulator Architectures (no noise)



2nd Order CIFF

ENOB: 16.43 bits

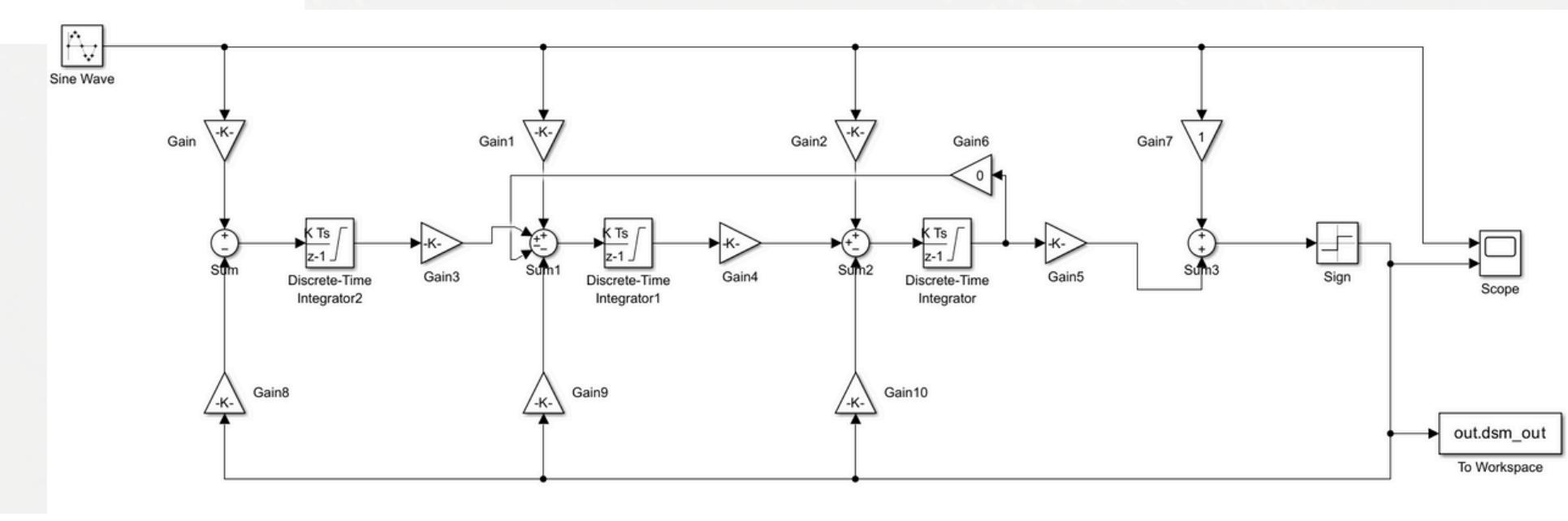
SNDR: 100.66 dB



3rd Order CIFB

ENOB: 16.84 bits

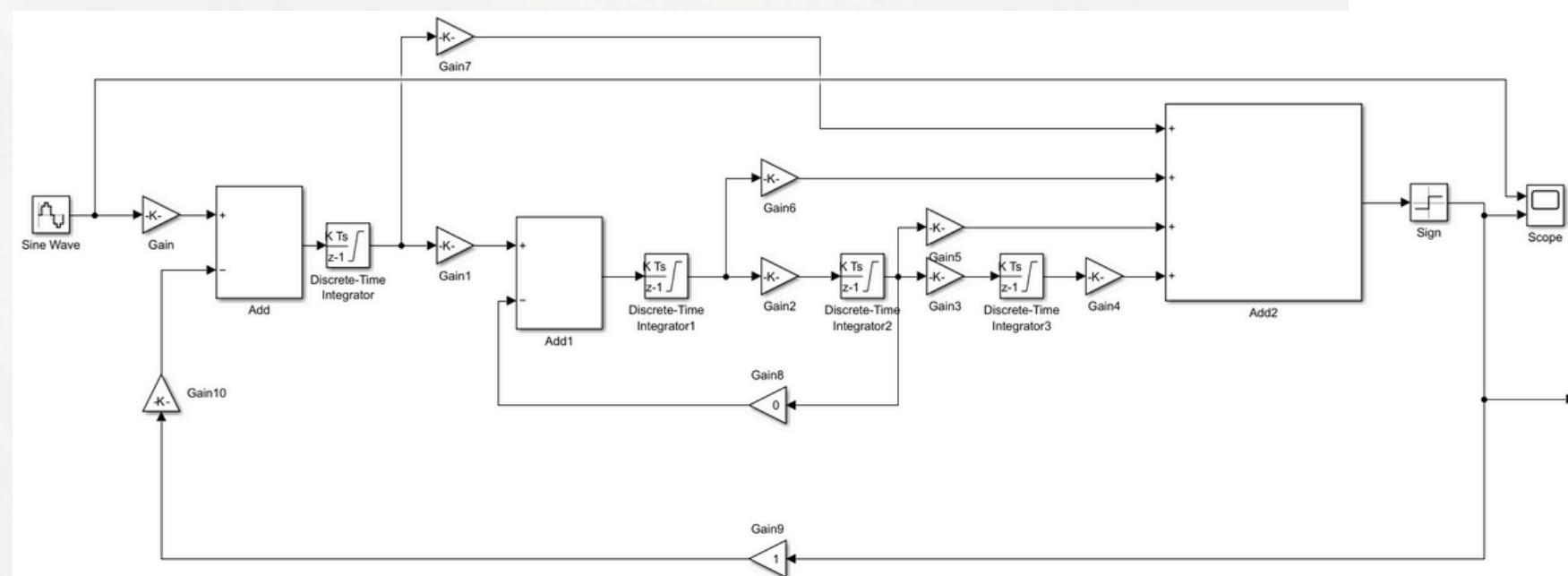
SNDR: 103.13 dB



4th Order CIFF

ENOB: 17.92 bits

SNDR: 109.63 dB



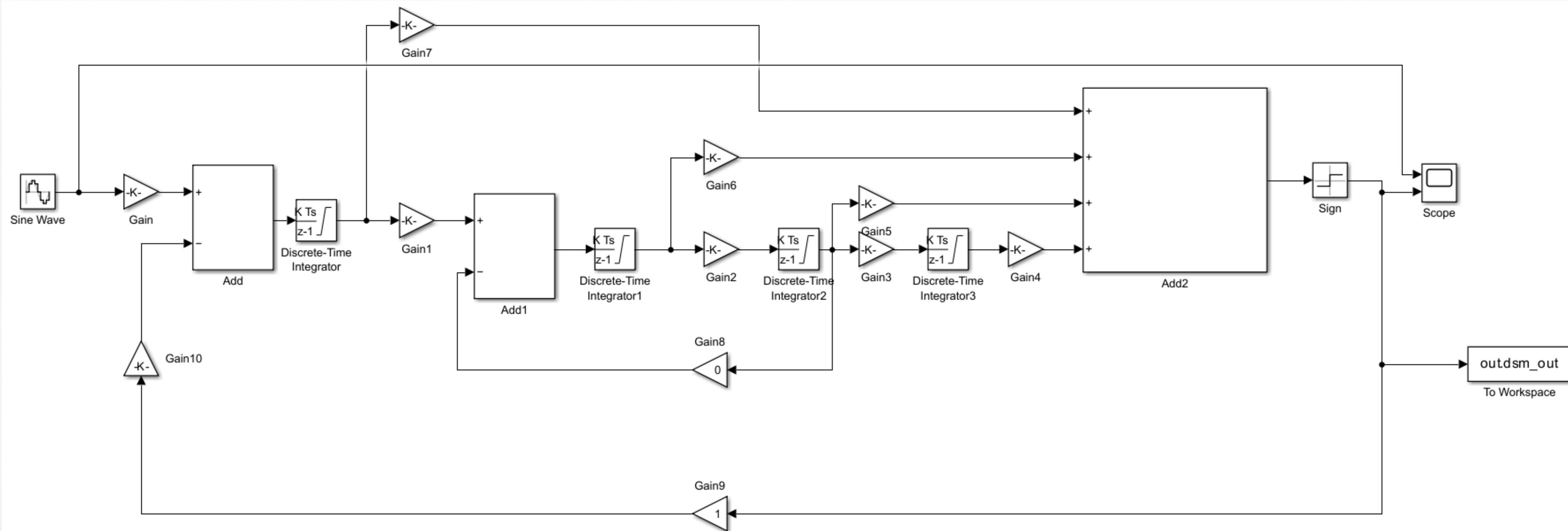
— Why 4th Order DT CIFF Structure

1. Delivers the Highest ENOB, consistently exceeding the 16-bit requirement at 2 ksps
2. Stable at High OSR (4096) with properly optimized NTF coefficients and loop filter design
3. Stronger Noise Shaping ($\propto f^8$), significantly suppresses in-band quantisation noise compared to lower-order loops
4. Noise Resistant Architecture: Robust to Flicker Noise, maintains >16-bit ENOB even with injected 1/f noise

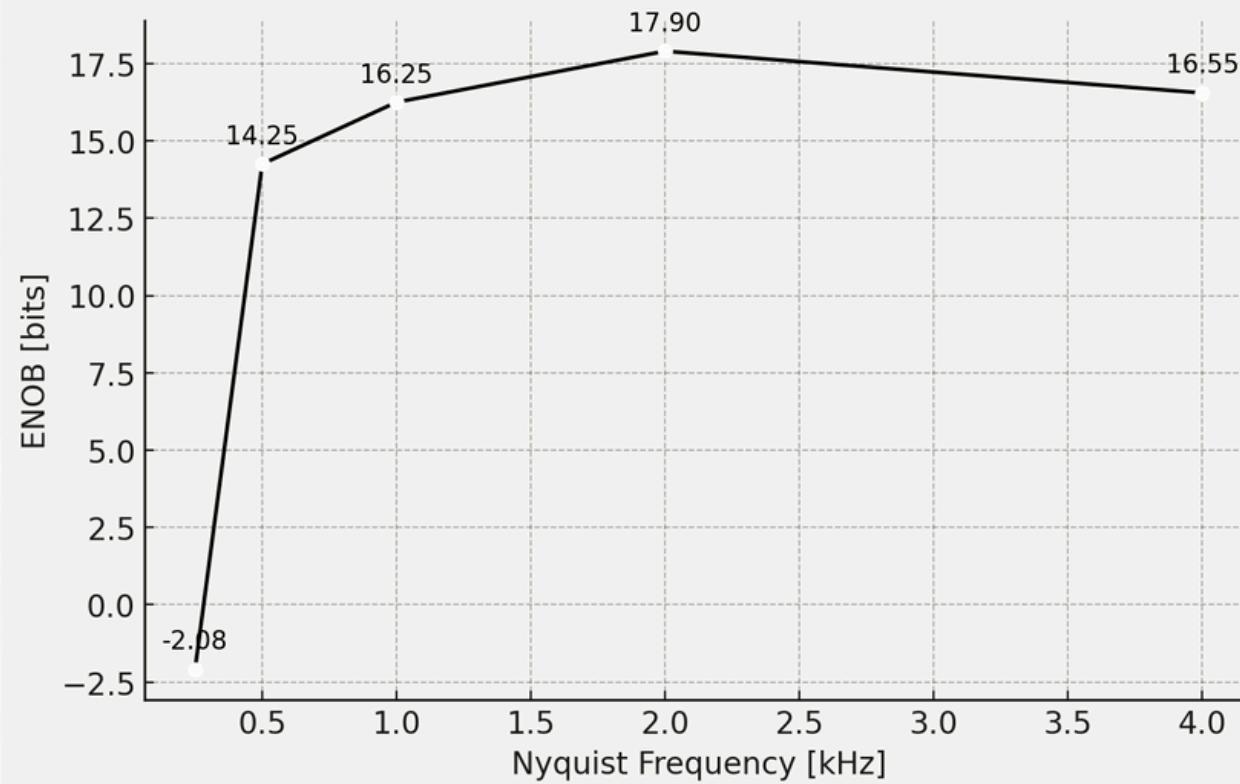
**MODULATOR PERFORMANCE
AT 2KSPS, OSR = 4096**

Order	Type	SNDR	ENOB
2nd	DT	100.66	16.43
3rd	DT	103.13	16.84
4th	DT	109.63	17.92

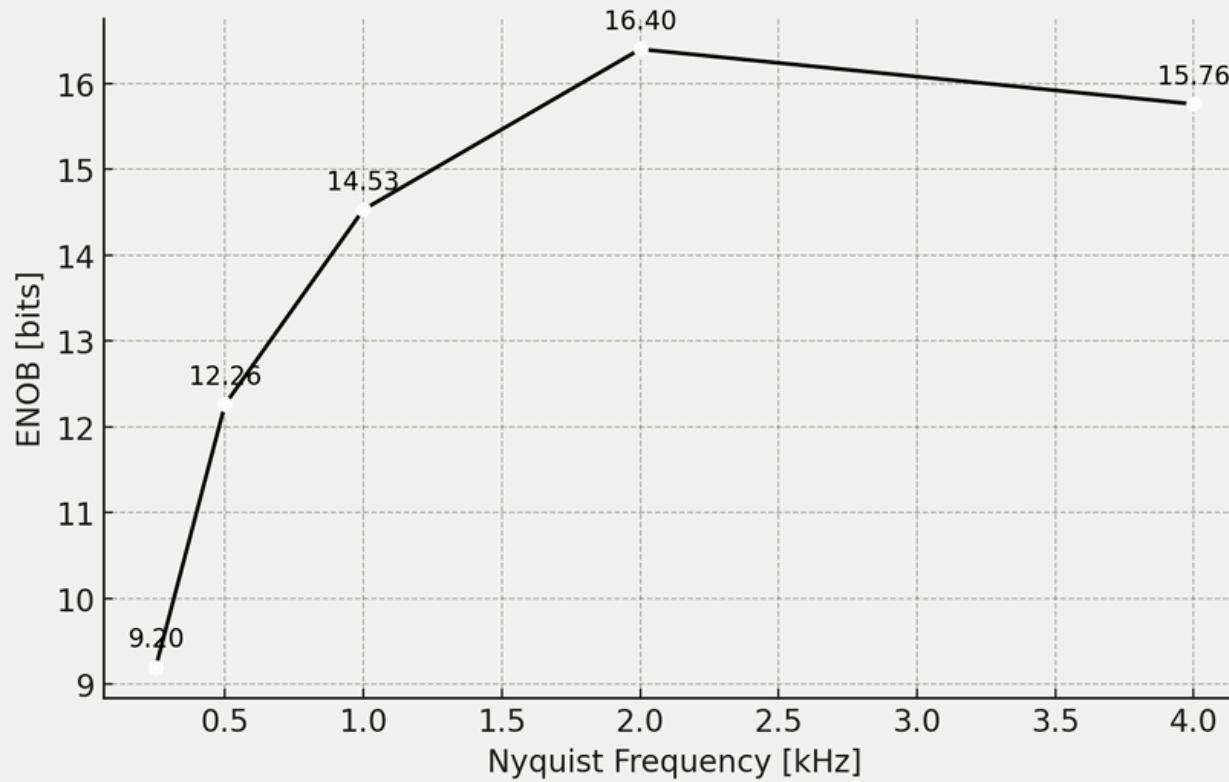
4th Order DT CIFF Structure



Trade-off simulation studies between Nyquist sampling rate and ENOBs



4th Order Trade-off analysis



2nd Order Trade-off analysis

TRADE OFF 2ND

NYQUIST FREQ.	ENO B
0.25 KSPS	9.20
0.50 KSPS	12.26
1.00 KSPS	14.53
2.00 KSPS	16.43
4.00 KSPS	15.76

TRADE OFF 4TH

NYQUIST FREQ.	ENO B
0.25 KSPS	-2.08
0.50 KSPS	14.25
1.00 KSPS	16.25
2.00 KSPS	17.92
4.00 KSPS	16.55

The Flicker Noise Challenge in DSM

The Problem :

- At low frequencies, $1/f$ (flicker noise) dominates.
- Destroys ENOB in precision applications.
- Spectral Power Density: $S_f \propto 1/f$
- Oversampling does not significantly suppress $1/f$ noise

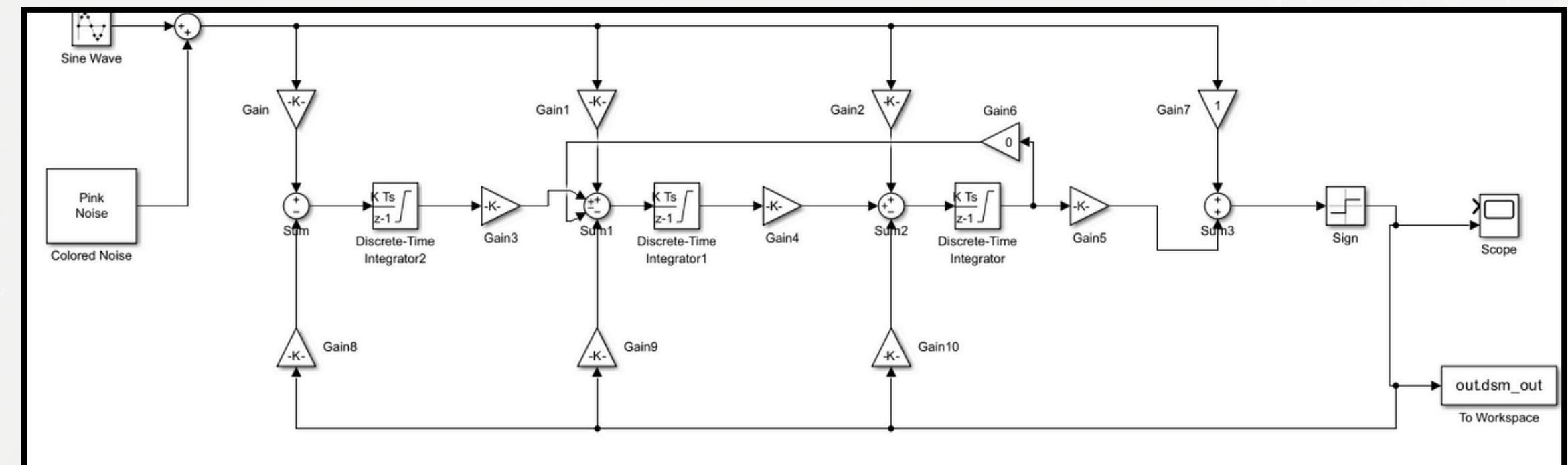
Impact on ENOB

Without mitigation, 3rd-order modulator

- 1.Ideal ENOB: 16.84 bits
- 2.With flicker: 4.09 bits
- 3.Catastrophic degradation!

Why It Matters:

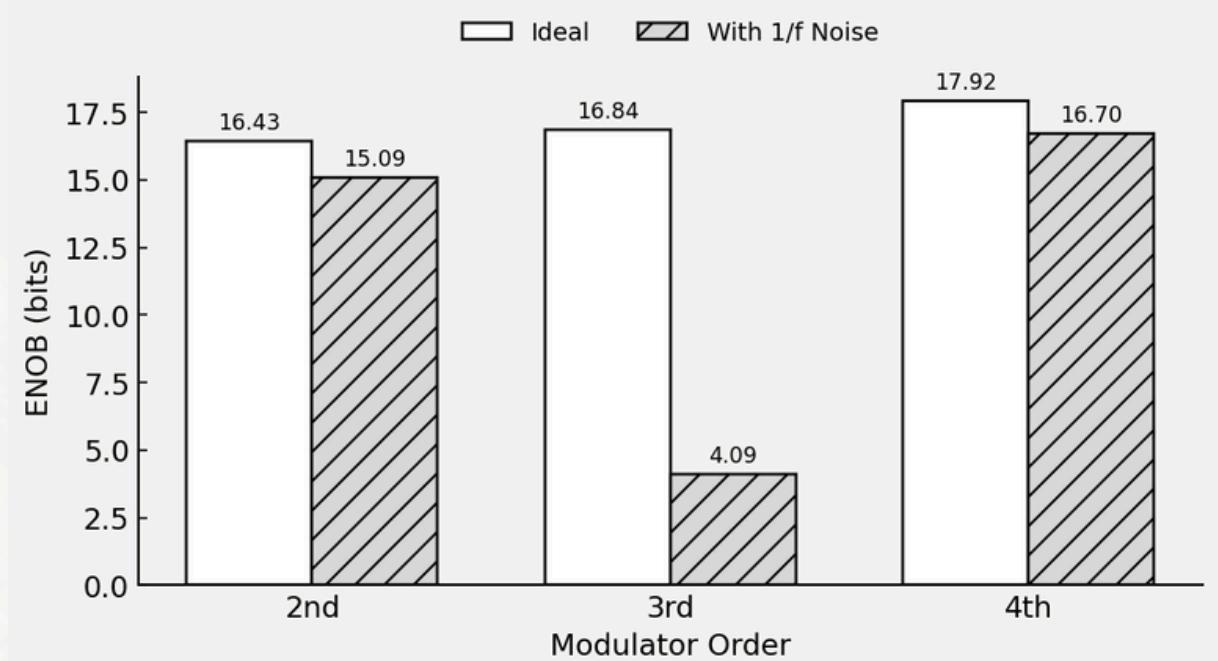
- Target: 0.5–2 kS/s (very low frequency)
- Flicker noise corner: typically 100 Hz – 10KHz



3th-order modulator with injected flicker noise

Noise Mitigation and Results

Order	WITHOUT NOISE		WITH NOISE	
	SNDR	ENOB	SNDR	ENOB
2nd	100.66	16.43	92.60	15.09
3rd	103.13	16.84	26.38	4.09
4th	109.63	17.92	102.29	16.70



4TH-ORDER MAINTAINS >16 ENOBS
WITH NOISE

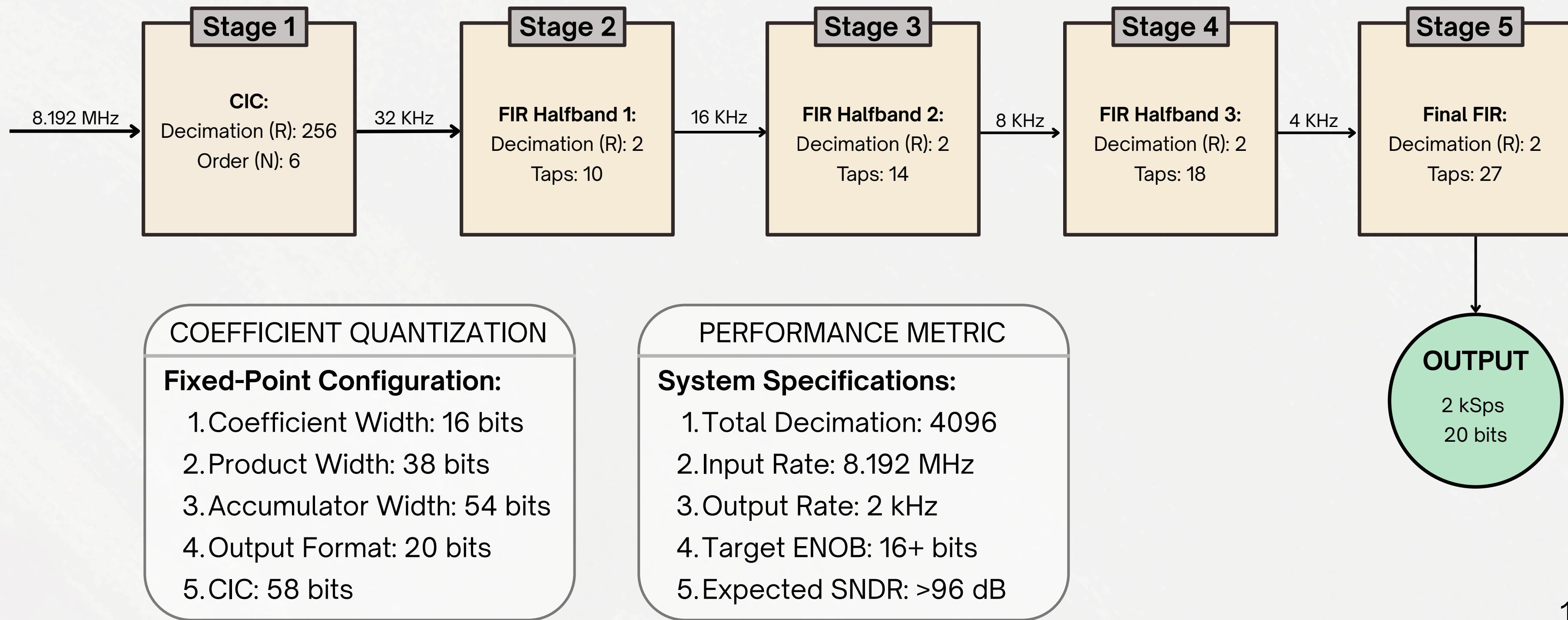
Reason for Noise Resistance of the 4th-Order Architecture

- Loop dynamics suppress and redistribute internal error sources, improving noise immunity.
- Flicker noise from the integrators—especially the first stage—is reduced by high loop gain and shaped by the NTF so that most of its energy moves out of the signal band.
- A large OSR lowers in-band noise density and provides ample spectrum for displaced noise.
- Consequently, even with significant 1/f noise, most disturbances are pushed out-of-band and removed by the decimation filter, preserving high ENOB.

Effect of Nested Chopping Circuitry

On adding nested chopper circuits in feedback loop with the 1st integrator, we saw an increase on **0.32 ENOBs**, which is not sufficient enough to justify the hardware overhead and increased complexity. Further, the low noise architecture fulfills the required ENOBs of > 16

Decimation Filter: The Digital Workhorse



Filter specifications and performance

PERFORMANCE COMPARISON

PARAMETER	VALUE
Input Rate	8.192 MHz
Output Rate	2 kHz
Input Format	1-bit stream
Output Format	20 bit
Passband	0-0.7 kHz
Passband Ripple	< 0.1 dB
Stopband Edge	> 0.8 kHz
Stopband Atten.	> 96 dB
Group Delay	Linear

ENOB PRESERVED > 16 BITS

HARDWARE RESOURCES

STAGE	TAPS	MULTIPLIERS
CIC (SINC ⁶)	-	0
Halfband 1	10	5
Halfband 2	14	7
Halfband 3	18	9
Final FIR	27	27
Total	69	48

OPTIMIZATION TECHNIQUE

- Halfband symmetry → 50% multiplier savings
- Zero-tap elimination

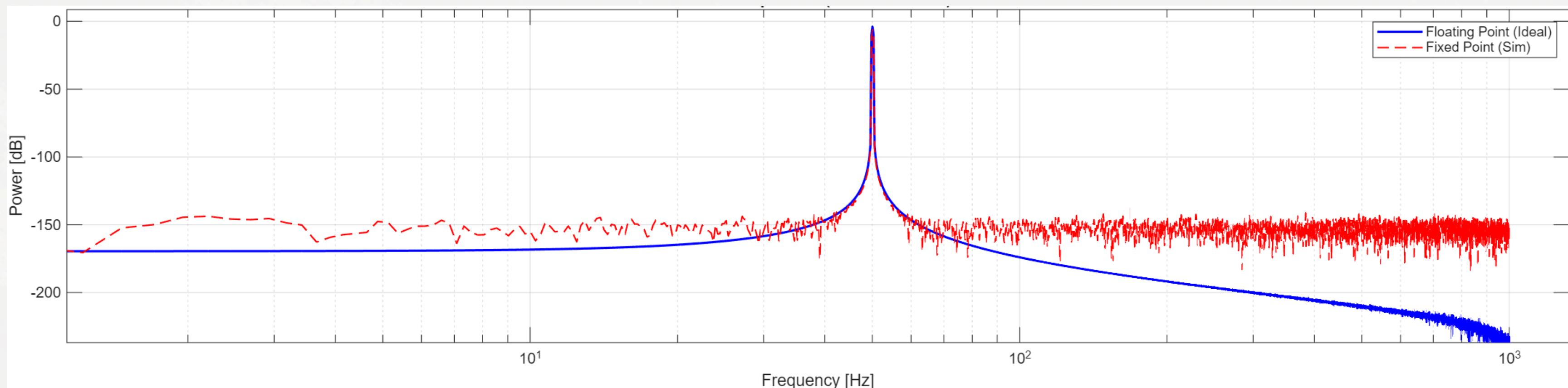
Floating point vs Fixed point Implementation

COMPARISON RESULT

Metric	Fixed Pt.	Floating Pt.
SNDR (dB)	109.55	117.47
ENOB (bits)	17.92	19.22

Implementation Loss: 1.3 bits

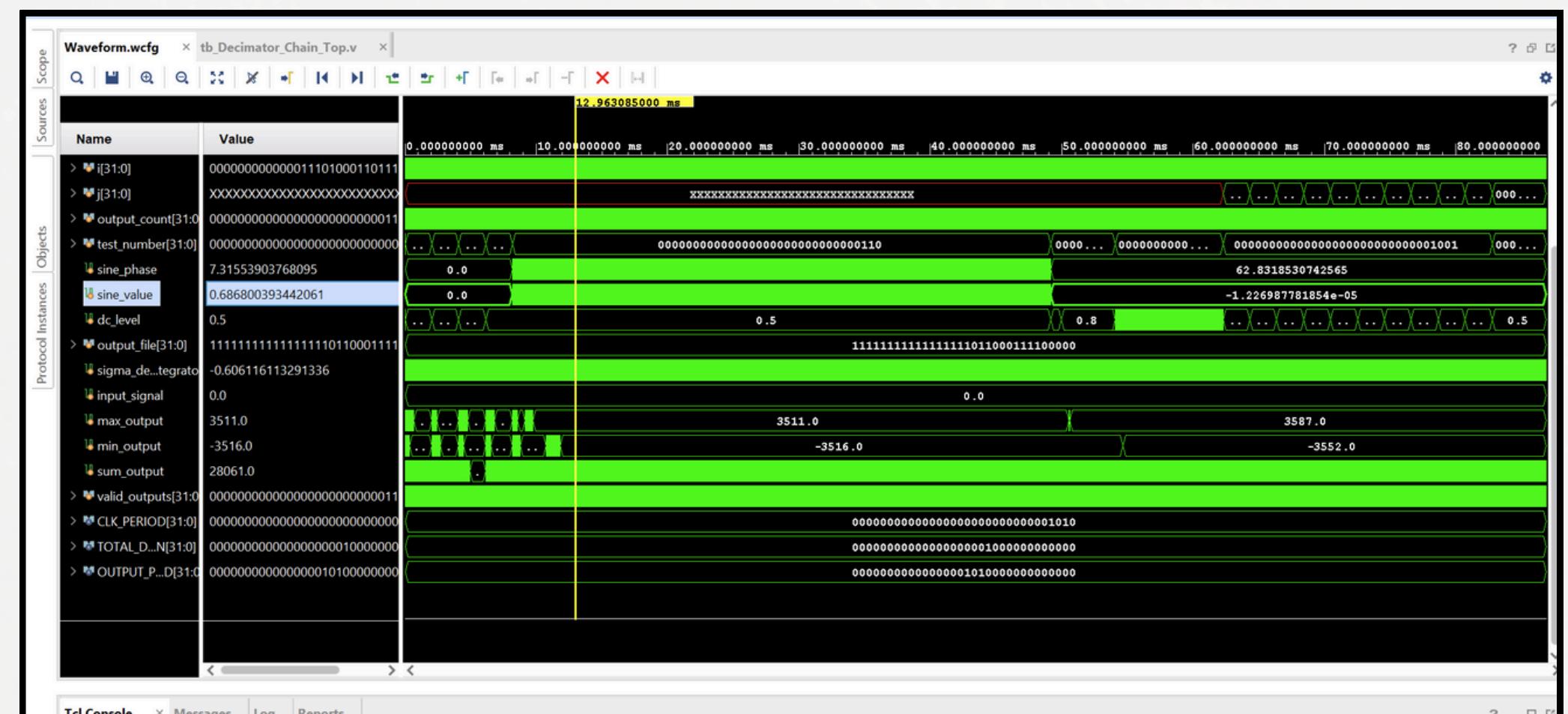
An ideal floating-point MATLAB model was benchmarked against our fixed-point HDL implementation to verify numerical accuracy and design equivalence.



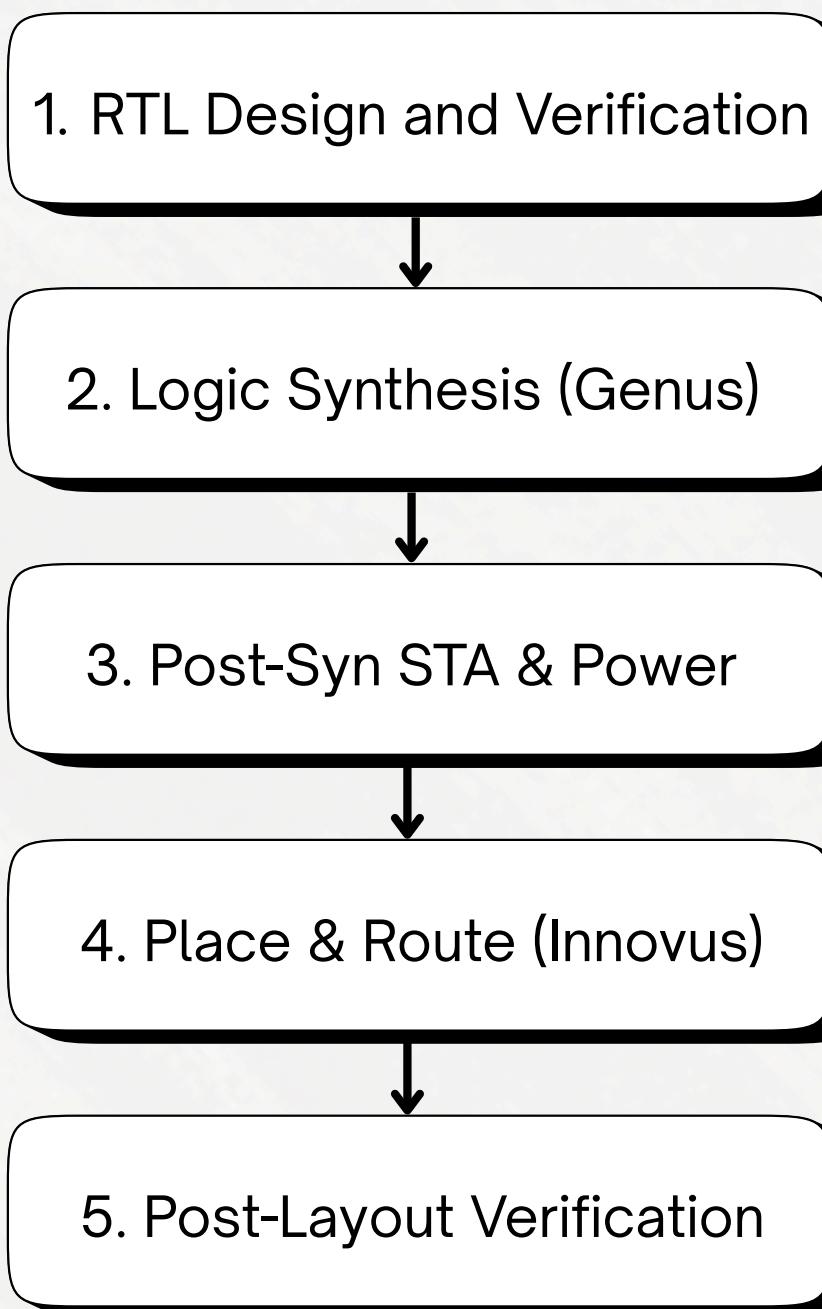
HDL Implementation of Multistage Decimator

Key Implementation Features:

- 1 Fully synchronous – single clock domain
- 2 No inferred latches or gated clocks
- 3 Synthesis-friendly – no combinational loops
- 4 CSD multipliers – 30% area reduction
- 5 Polyphase decimation ensures that we balance efficient decimation while minimizing logic



ASIC Flow and Results



POST SYNTHESIS METRIC	
Silicon Area:	0.167 mm ²
Logic Block Count:	10947 Blocks
Total Power:	2.57 mW
Average density:	0.993
Timing Closure:	Met
Setup Violations:	0
Hold Violations:	0
Critical Path Delay:	10.17ns
Positive Slack:	111.7833ns

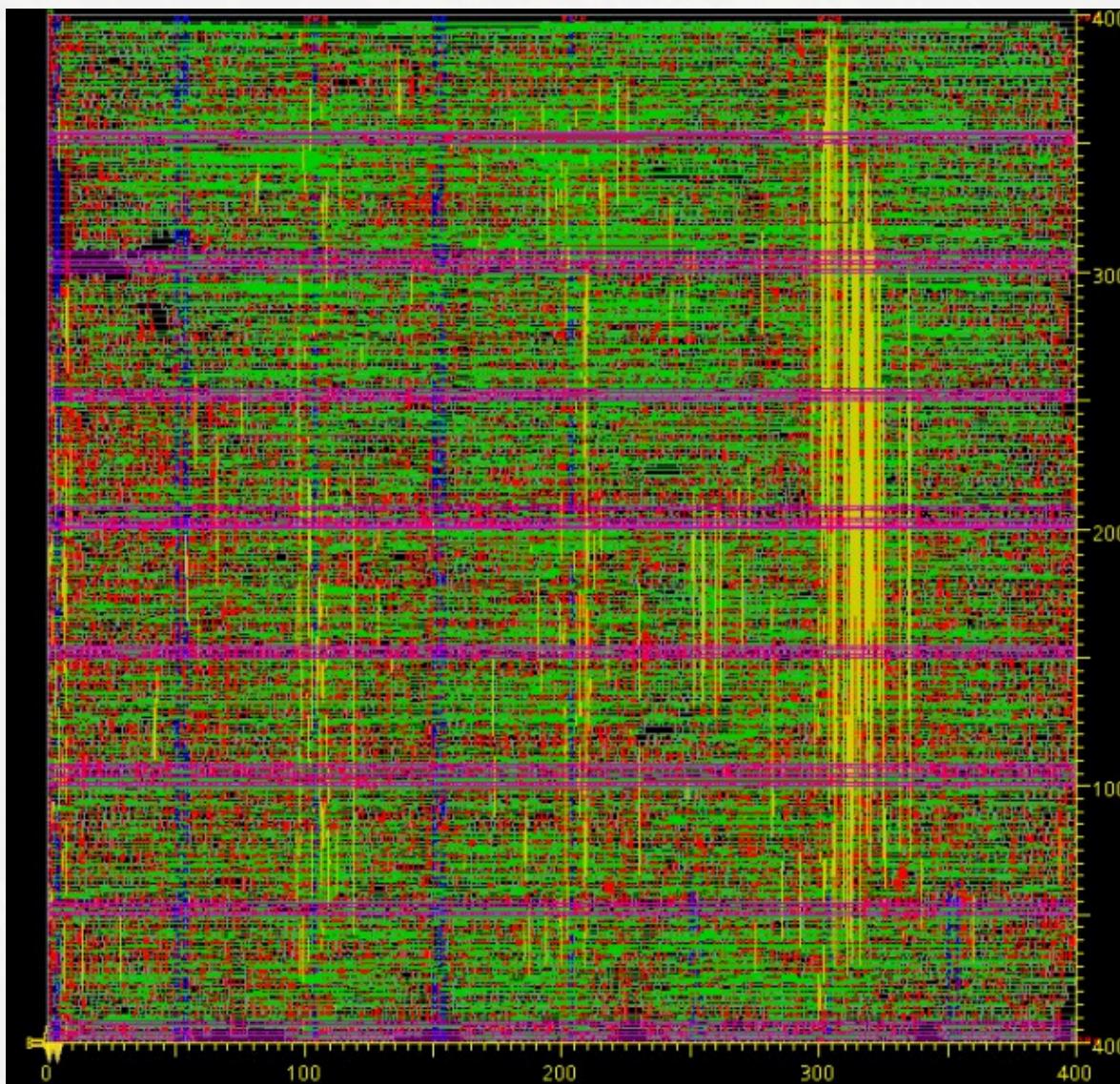
TECHNOLOGY:
UMC 90 NM CMOS

STANDARD CELLS:
LOW-POWER LIBRARY

TARGET CLOCK:
8.192 MHZ

TOOLS:
CADENCE GENUS + INNOVUS

Layout: Physical Implementation



Layout Highlights

Die Area - 0.169 mm^2

Dense placement - high utilization

Clean Routing - no DRC violations

Filler cells - properly inserted

Final Results

Modulator Architecture

Architecture = 4th order CIFF
Quantizer level = 1-bit
OSR = 4096

Noise Analysis

ENOB (Without noise) = 17.92 bits
ENOB (With (1/f) noise) = 16.70 bits
SNDR (without noise) = 109.63 dB
SNDR (with noise) = 102.29 dB

Filter

CIC → HB → HB → HB → FIR
Stopband attenuation > 96 dB
Passband ripple < 0.1 dB

Synthesis

UMC 90 nm CMOS technology
Max frequency > 80 MHz
No critical path issues

Implementation

Low-power decimation pipeline
Optimized CIC + HB chain

The Challenges

1

Filter-ENOB Trade-off

Problem: Aggressive filters fair synthesis
Solution: 5-stage cascade
Result: 16+ bits

2

MATLAB-RTL Match

Problem: Rounding mismatch
Solution: Bit-exact fixed-point
Result: <0.01% error

3

Synthesis

Problem: Critical paths
Solution: Hierarchical design
Result: First-pass closure

4

Flicker Noise

Problem: ENOB destruction
Solution: 4th-order arch.
Result: 16.70 bits, no extra HW

References

- 1** Nadeem Tariq Beigh, Prince Nagar, Aamir Bin Hamid, Faizan Tariq Beigh, and Faroze Ahmad, “2nd Order Sigma Delta Modulator Design using Delta Sigma Toolbox,” Asian Journal of Electrical Sciences, Vol. 7, No. 2, 2018, pp. 41–45.
- 2** “Design of a Fourth-Order Continuous-Time Delta-Sigma A/D Modulator with Clock Jitter Correction,” M.S. Thesis, University of Minnesota, October 2009.
- 3** R. Schreier and G. C. Temes, Understanding Delta-Sigma Data Converters, Wiley-IEEE Press, 2004.
- 4** <https://in.mathworks.com/help/dsp/ref/cicdecimation.html>
- 5** <https://in.mathworks.com/help/signal/ug/fir-filter-design.html>

Thank You

Appendix

Why Discrete Time

Advantage of DT

1. Precise loop coefficients (capacitor ratios) which gives high stability across PVT
2. Lower sensitivity to jitter

Disadvantage of CT

1. Loop response heavily depends on RC exact values, which drift under temperature and radiation
2. Very sensitive to excess loop delay, op-amp GBW limits, and DAC edge timing
3. Clock jitter directly corrupts the loop, causing SNR loss

Disadvantage of Hybrid

1. Harder to guarantee loop stability across PVT as CT drift while DT does not.
2. Needs perfect timing alignment between the CT front-end and DT sampling, failing which the output gets distorted.

Noise Reduction Techniques

Nested Chopper

1. Provides strongest 1/f noise and offset suppression across multiple stages
2. Very stable, as chopping happens at several points in the loop

Chopper

1. Effectively removes 1/f noise by shifting it out of the signal band
2. Can introduce chopping ripple / tones that must be filtered out

Auto Zeroing

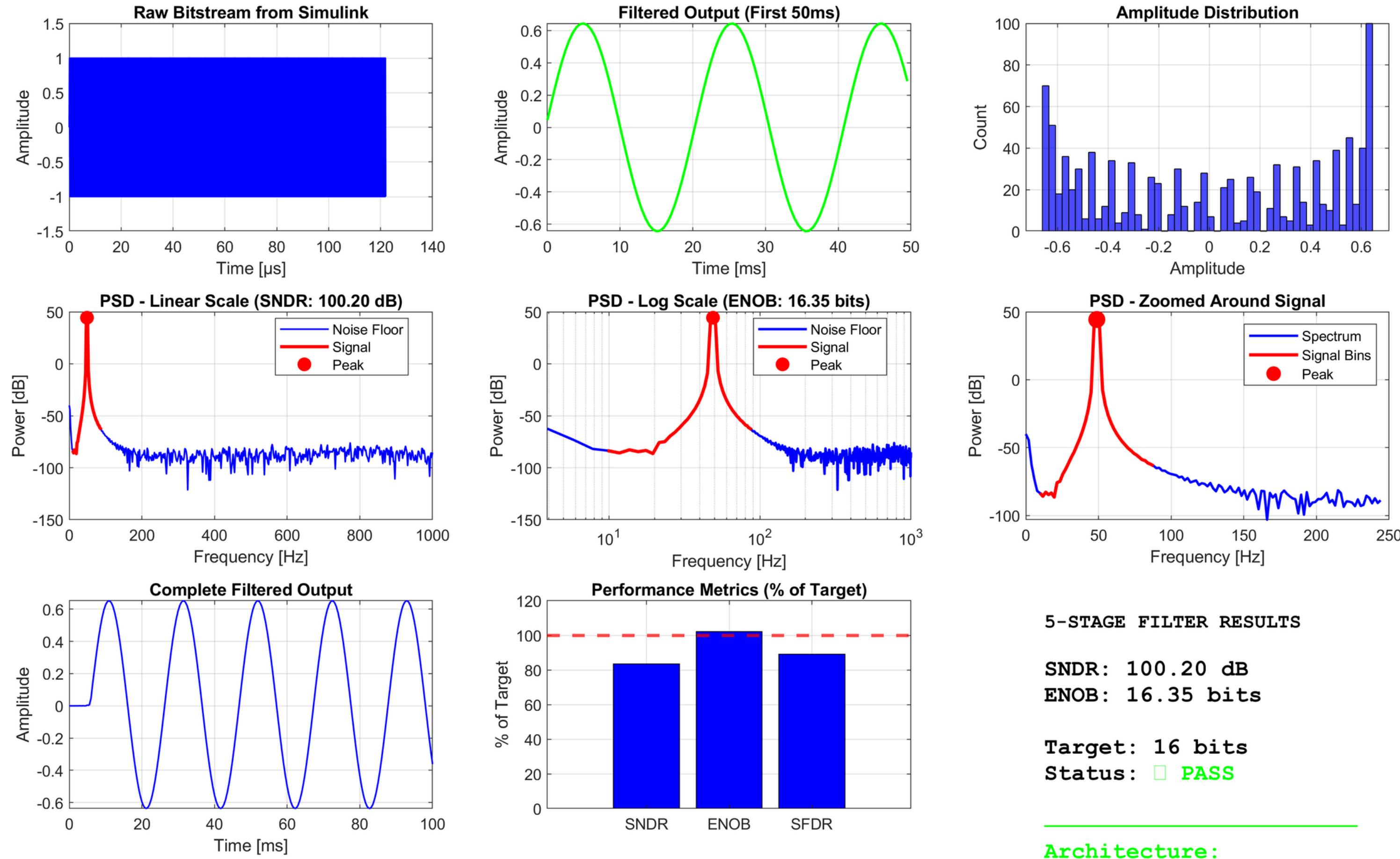
1. Adds some sampling noise and reduces bandwidth

We choose nested chopping because it provides the most effective suppression of 1/f noise and offset among all the noise-reduction techniques. This makes nested chopping the most reliable option for high-resolution, low-bandwidth Delta-Sigma ADCs.

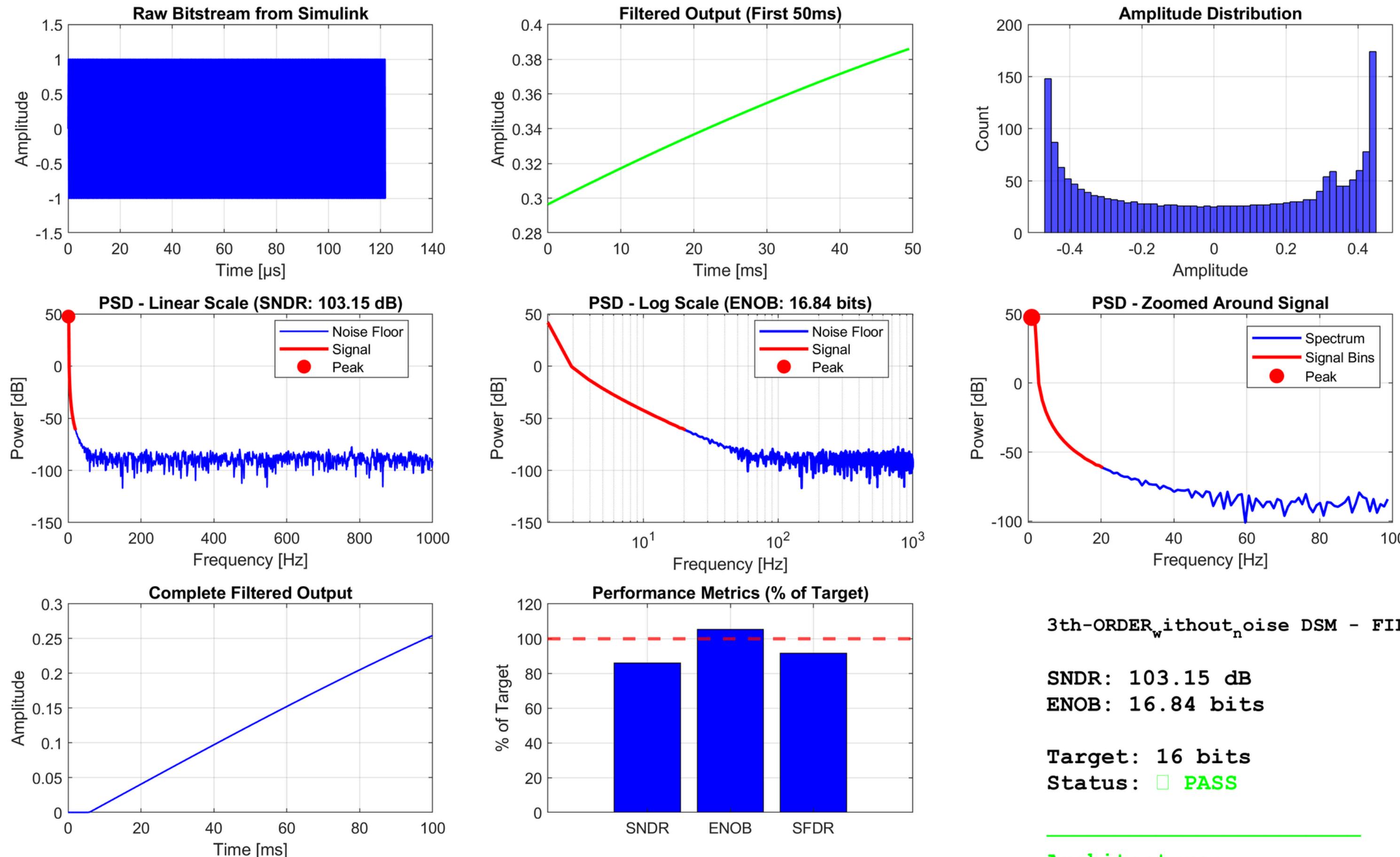
Future developments

- 1 Currently, the design uses a parallel architecture with ~130 multipliers that often sit idle due to the low data rate in later stages. By implementing a Time-Multiplexed (Serial) Architecture, we can replace these banks with just 1-3 shared multipliers that reuse hardware during idle cycles. This "Folding" technique utilizes the faster system clock to process taps sequentially, potentially reducing arithmetic logic area by ~90% and total footprint by ~50-60% with no loss in precision.
- 2 The current architecture has not yet been evaluated under radiation effects. As future work, we plan to perform radiation testing and develop a radiation-hardened version of the circuit to ensure reliability in space environments. Techniques such as Enclosed Layout Transistors (ELTs) and guard rings will be added to suppress leakage and improve robustness, along with evaluating SOI-based processes for better isolation.

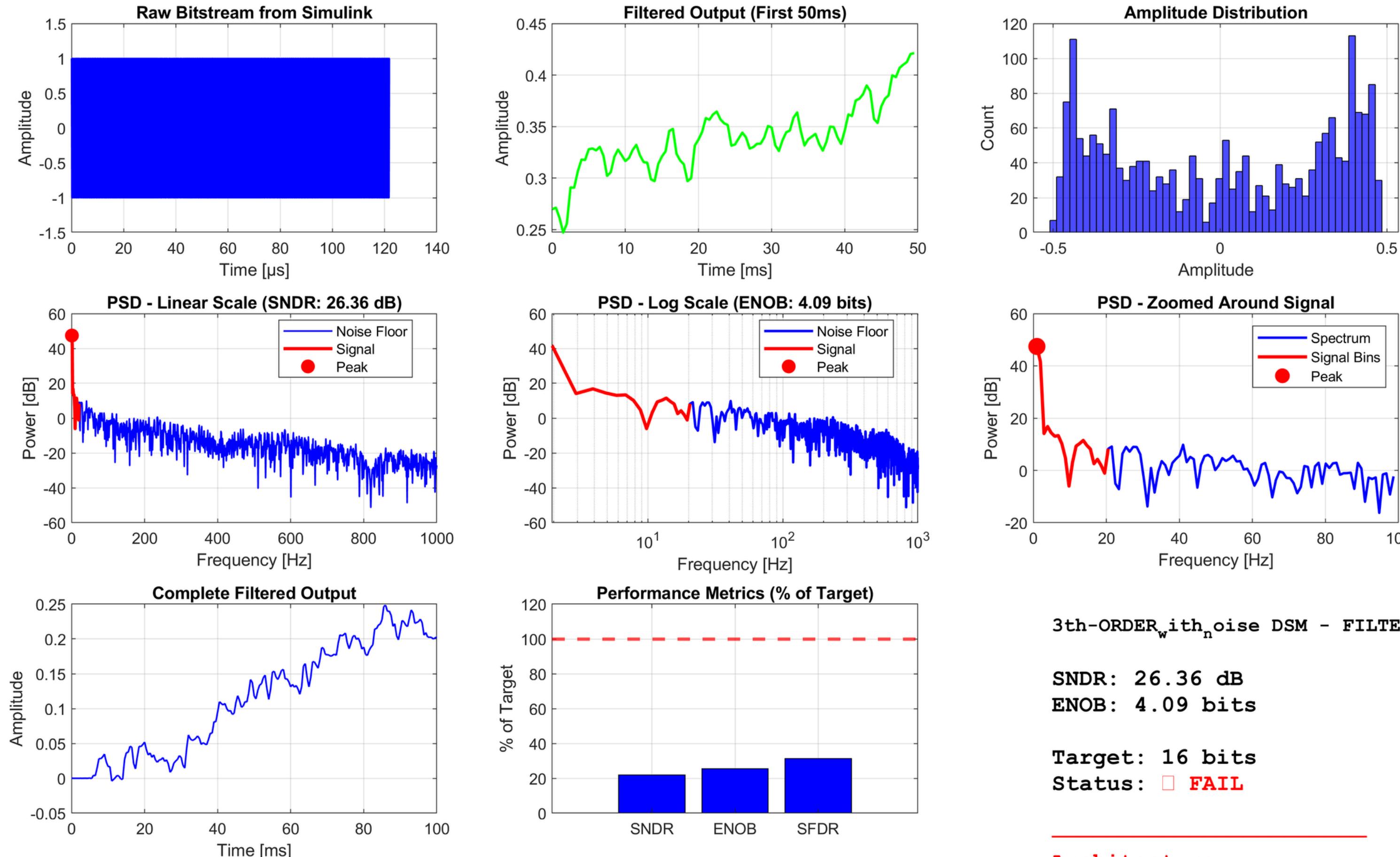
2nd Order DT CIFF Output



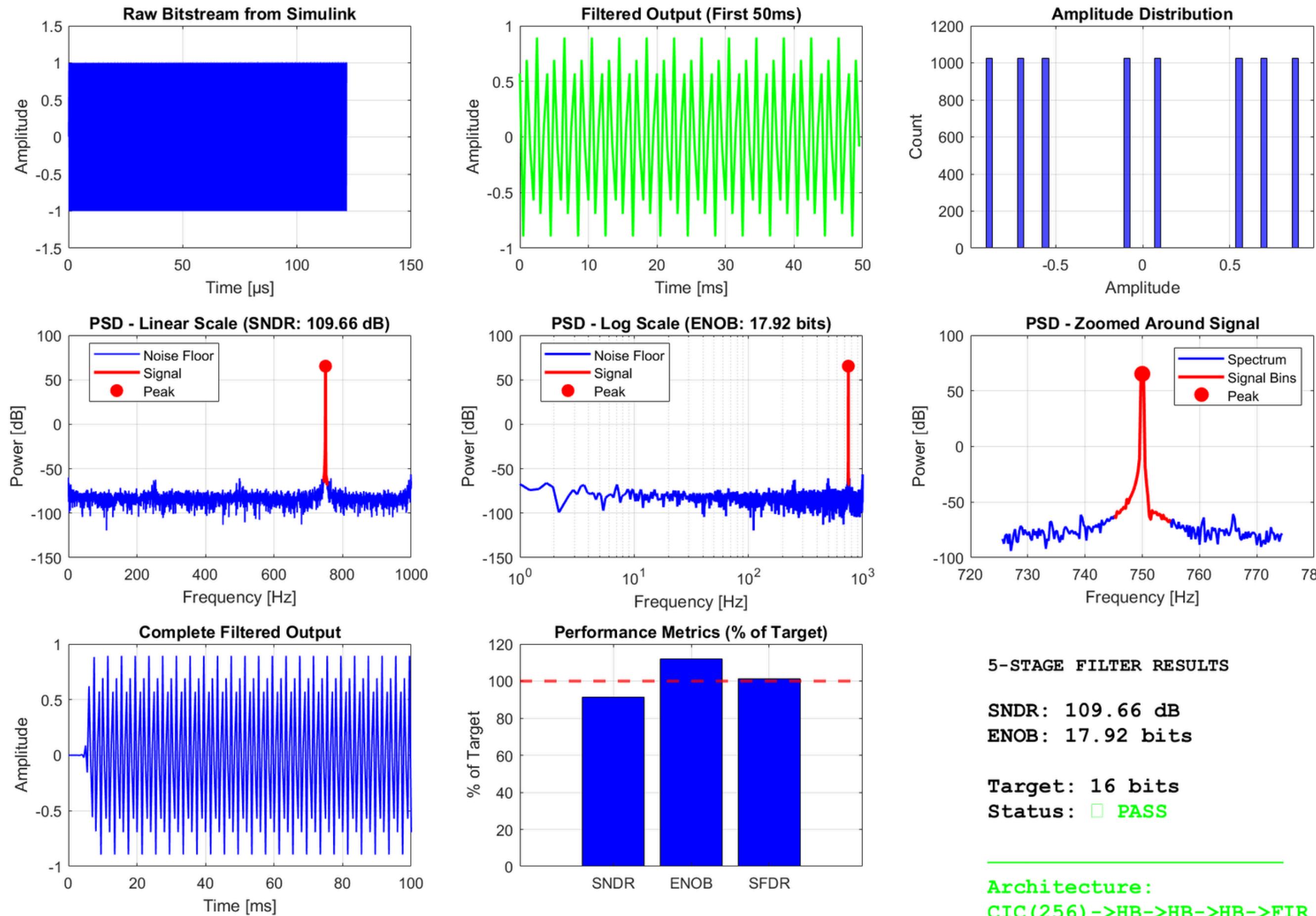
3rd Order DT CIFB Output



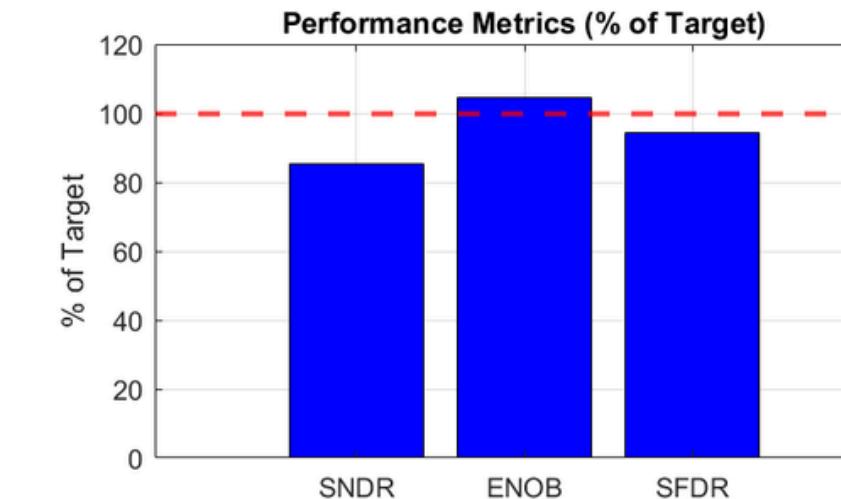
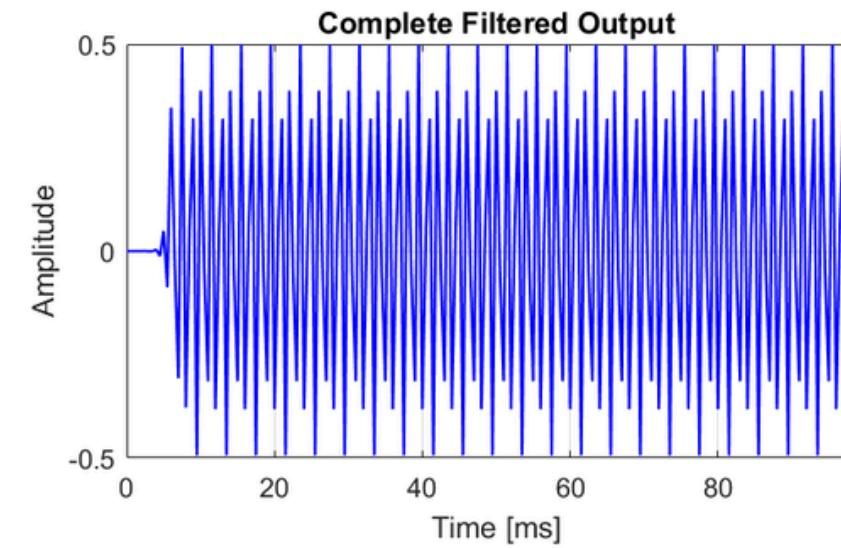
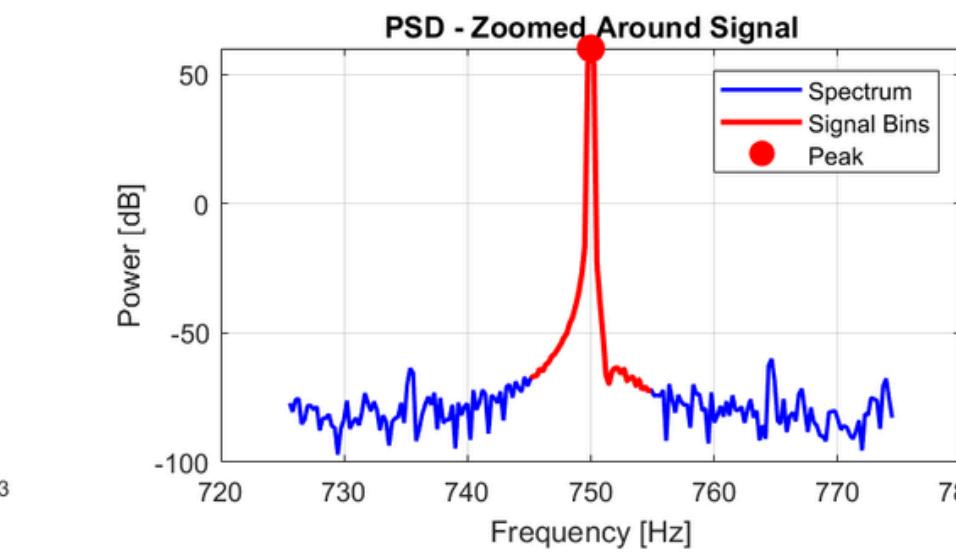
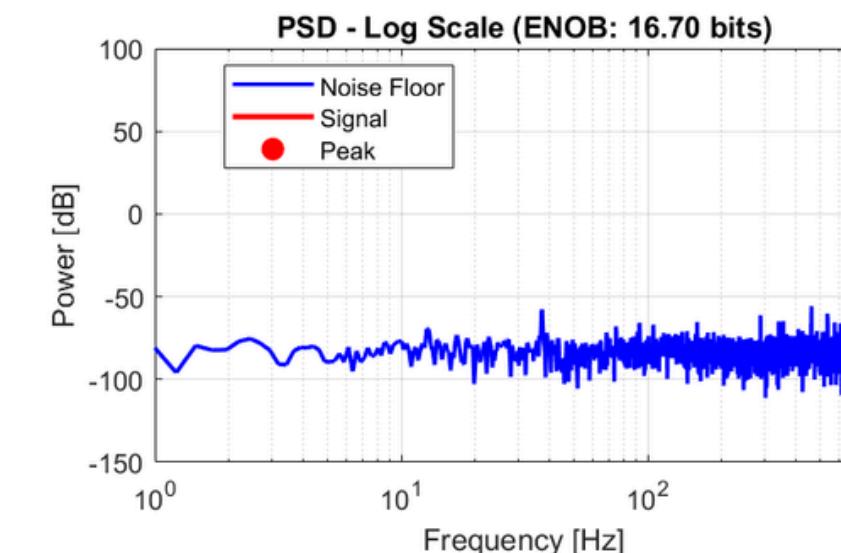
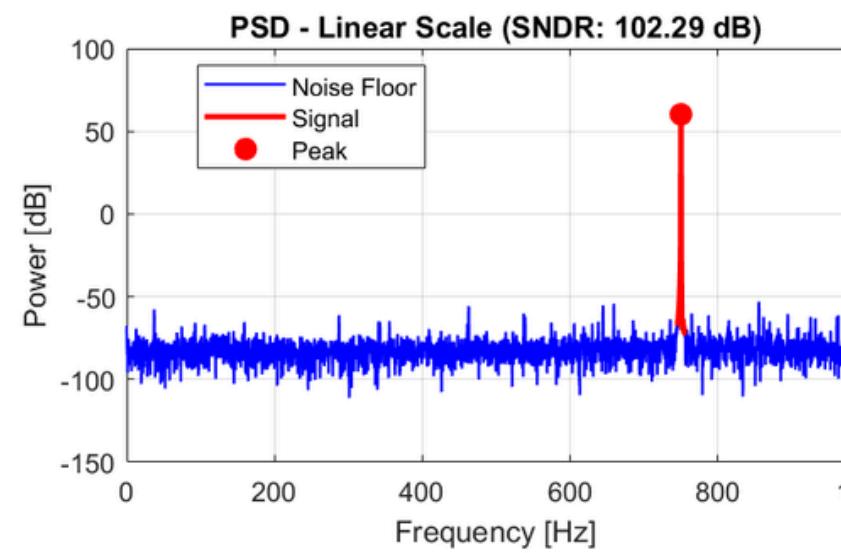
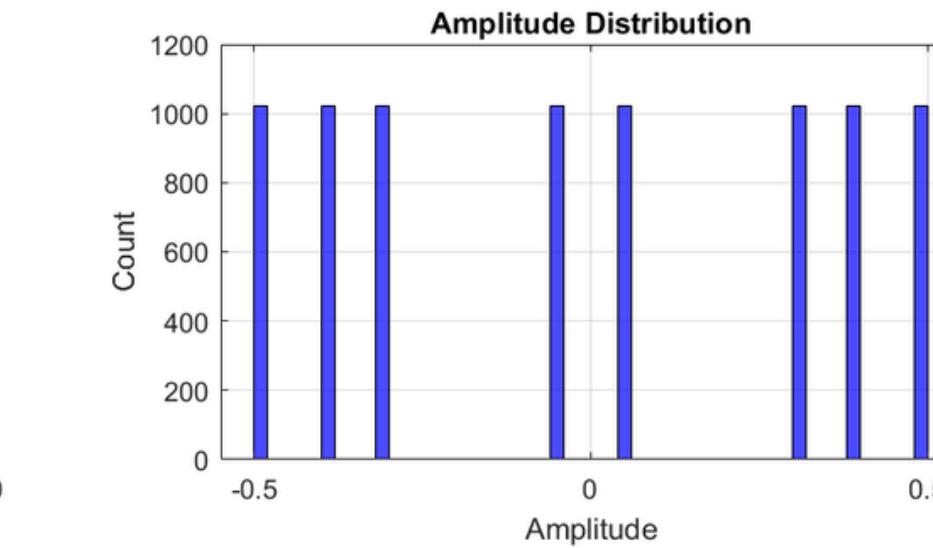
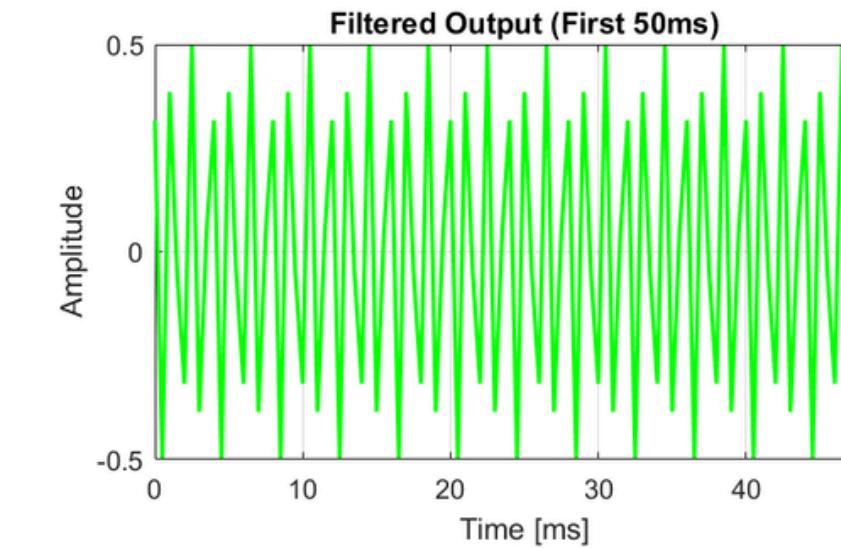
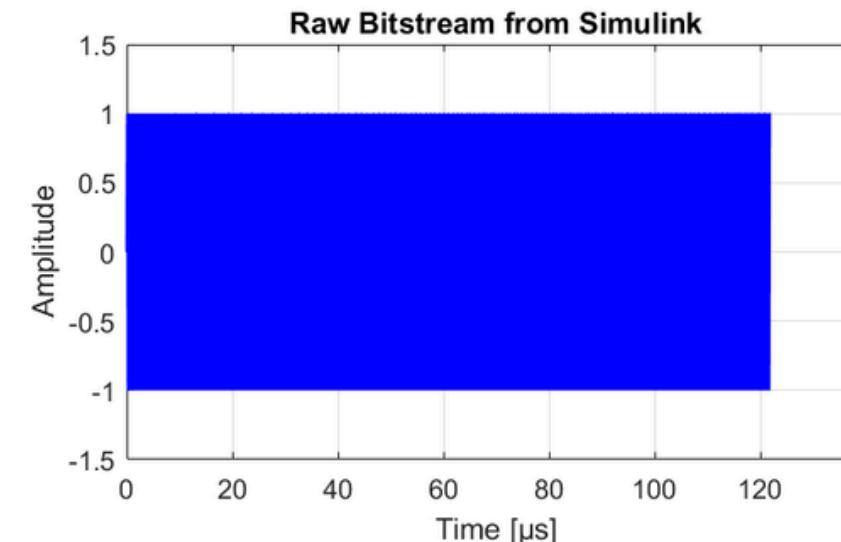
3rd Order DT CIFB Output (With Noise)



4th Order DT CIFF Output



4th Order DT CIFF with noise Output



5-STAGE FILTER RESULTS

SNDR: 102.29 dB
ENOB: 16.70 bits

Target: 16 bits
Status: PASS

Architecture:
CIC(256) → HB → HB → HB → FIR
Final FIR: 33 taps

Signal: 750.00 Hz

END