ASIC Flow Files – Decimator Block

Inter–IIT ISRO–VLSI Project

Team 82

1. Overview

This directory contains the ASIC–flow artefacts for the **digital decimator** used in the Delta–Sigma ADC project. It collects, in one place, the files that show the path from RTL to synthesized gate–level netlist and final layout snapshot.

The aim is that someone familiar with a standard–cell ASIC flow can reproduce or audit the implementation without needing any extra project context.

2. Directory map

2.1 `1. Synthesis scripts + reports/`

Everything related to logic synthesis of the decimator.

- **Synthesis Script**/
  - `synth_decimator.tcl` – top–level TCL script that drives the synthesis tool. In a typical flow it:
    - reads in the RTL (Verilog) design for the decimator,
    - sets up technology libraries and timing / I/O constraints,
    - runs compile / optimization, and
    - writes out reports and the gate–level netlist.
- **Reports**/
  - `area.rpt` – cell and area utilization summary.
  - `power.rpt` – power estimation report (dynamic and leakage, depending on tool settings).
  - `timing.rpt` – static timing analysis, including worst slack and critical paths.
  - `qor.rpt` – overall "quality of results" summary from the synthesis tool.
  - `check_design.rpt` – structural and consistency checks on the synthesized design.

These report files correspond to the synthesis run that produced the netlists in `2. Netlist files/`.

2.2 `2. Netlist files/`

Gate–level Verilog netlists produced by synthesis for the decimator.

- `Netlist.v` – main synthesized gate–level netlist for the decimator block (default version to use for gate–level simulation or hand–off to PnR).

- `Netlist_2.v` – alternate netlist (e.g. from a different constraint set or a slightly different run). Included for completeness and comparison.

Unless otherwise mentioned in the report, `Netlist.v` should be treated as the final sign–off netlist.

2.3 `3. Layout/`

Physical layout artefacts.

- `layout.png` – exported screenshot of the final placed–and–routed layout of the decimator. This is used for documentation and for the end–term report to demonstrate that the block has been successfully taken through PnR.

No GDS or DEF is included here to keep the submission light; those can be regenerated from the sign–off database if needed.

Desktop–related `desktop.ini` files in each folder are automatically generated by the operating system and are not part of the ASIC flow.

3. How to use these files

- **Re–running synthesis**
  Open your synthesis tool (e.g. Design Compiler / Genus) and source `synth_decimator.tcl`, updating technology–library paths and environment variables for your CAD setup.
- **Gate–level simulation**
  Use `Netlist.v` with the same testbench that was used for RTL simulation. Make sure to include the relevant standard–cell library models in the simulator command line or project.
- **Reporting and documentation**
  Pull numerical values from `area.rpt`, `power.rpt`, `timing.rpt` and `qor.rpt` into tables/plots in the written report, and insert `layout.png` as the layout illustration for the decimator block.

4. Notes

- File names have been kept descriptive and minimal so that it is clear which stage of the flow each file belongs to.
- Paths, library names and exact tool commands inside `synth_decimator.tcl` may need minor edits when the design is moved to a different machine or CAD installation.