Introduction to Computing Systems
Homework 4

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1

A: BRnzp -171 B: JSR -171 Both A and B result in the PC being changed to (PC+1)-171. However, B saves the linkage information in R7 and A does not affect R7.

The instruction A stands for BR(Branches), while B is a JSR. After A, PC would be loaded with $(PC^{+} + SEXT(101010101))$. And after B, PC would be loaded with $(PC^{+} + SEXT(11101010101))$.

The main differences is that the instruction with opcodes 0000 needs bit[11:9] to check n,z,p; while the one with opcodes 0100 needs bit[11] to check whether it is a JSR or JSRR. So the offset in BR can only get 9 bits, while in JSR, it can get to 11 bits, which means a larger range is available.

2

a

0001 011 010 1 00000 (ADD R3, R2, #0) Using only NOT.

```
1001 011 010 111111          ; NOT R3, R2
1001 011 011 111111          ; NOT R3, R3
```

b

```
1001 001 011 111111          ; NOT R1, R3
0001 001 001 1 00001         ; ADD R1, R1, #1
0001 001 010 000 001         ; ADD R1, R2, R1
```

c

```
0101 001 001 000 001         ;AND R1, R1, R1
```

d

No. The condition codes in LC3 is based on the last value loaded into a general purpose register. And this value cannot be both negative and zero at the same time.

e

```
0101  001  001  1  00000          ;AND R1, R1, #0
```

3

```
0001  101  000  1  11000
```

4

Including PC, MEMORY(and MDR, MAR), IR, CONTROL UNIT, REG FILE, MAR-MUX.

5

a

Turn R0 into $R0 \times 2^4$. Or Turn R0 into $R0 << 4$.

b

PC	R0	R1	R2	R3	R4	R5	R6	R7	N	Z	P
x3006(since there's a breakpoint)	x0050	x0000	x0000	x0000	x0000	x0000	x0000	x0000	0	1	0

c

instruction	clock cycles
AND	1+5+1+1+1=9
ADD	1+5+1+1+1=9
LD	1+5+1+1+1+5+1=15
BRp	1+5+1+1+1=9

And the program uses 1 AND, (1+4*2=9) ADDs, 1 LD, 4 BRps.
So the total number would be $\underline{1 \times 9 + 9 \times 9 + 1 \times 15 + 4 \times 9 = 141}$

6

The numbers of ones in x3100 would be stored into R0.

7

```
0110  001  000  000000          ;LD R1, R0, #0
0000  100  000000010            ;BRn
```