Introduction to Computing Systems
Homework 2

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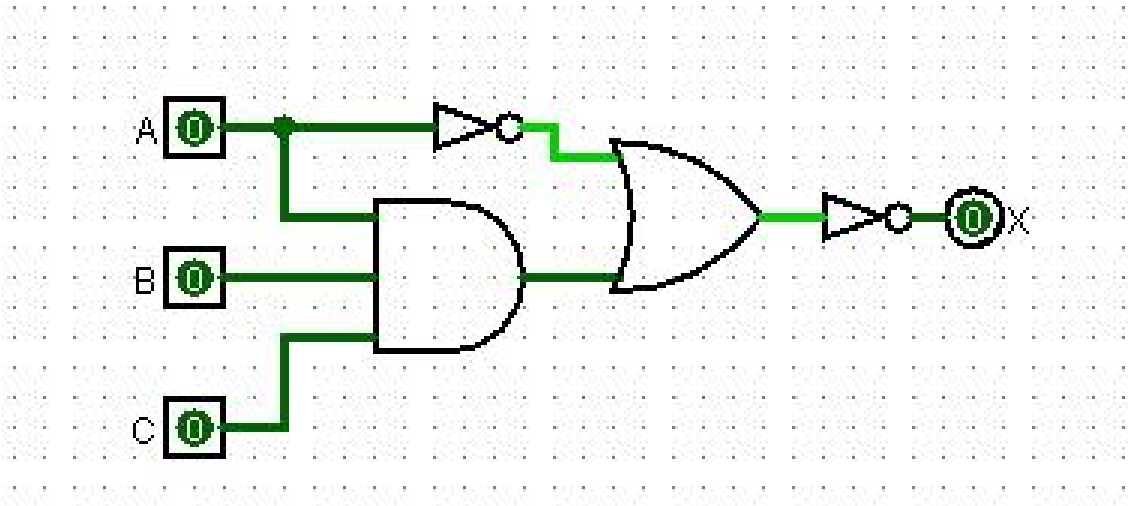
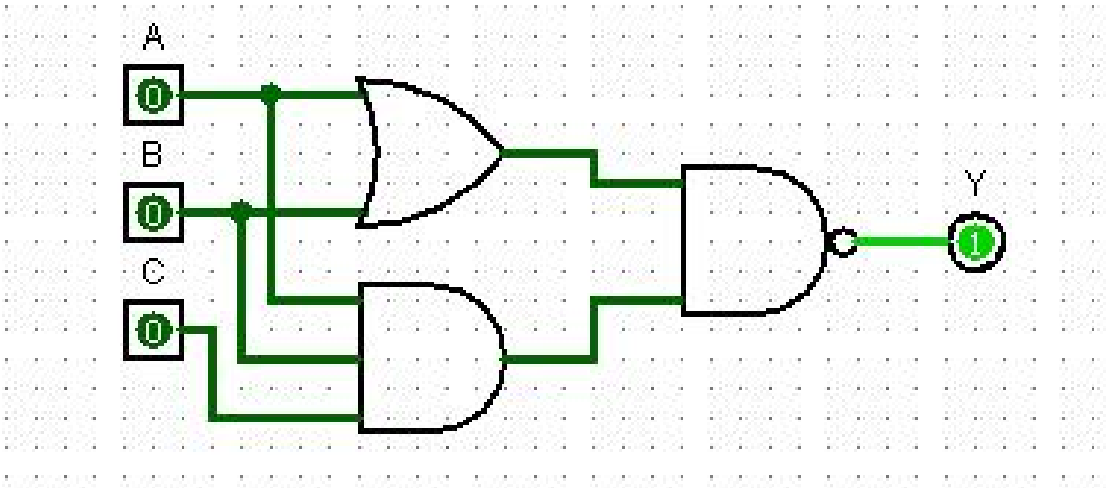
1

a



b

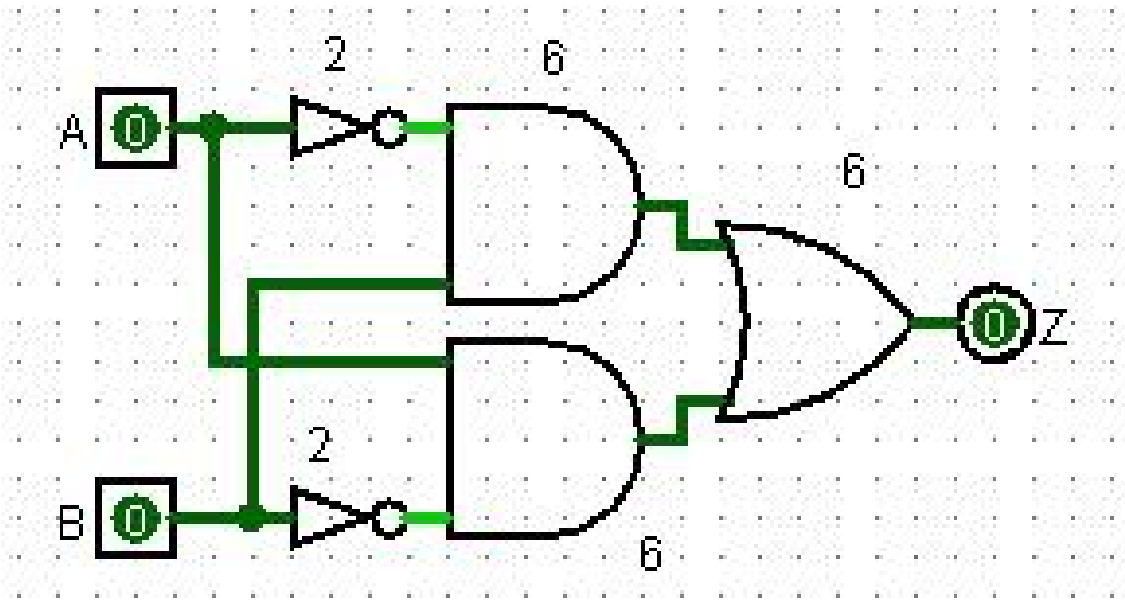


2

a

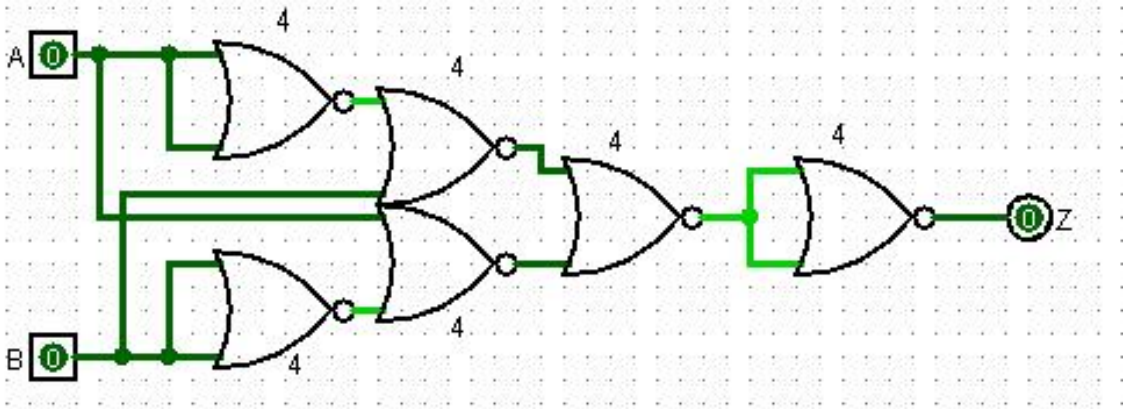
Way 1

As shown below, it needs 22 transistors in all.



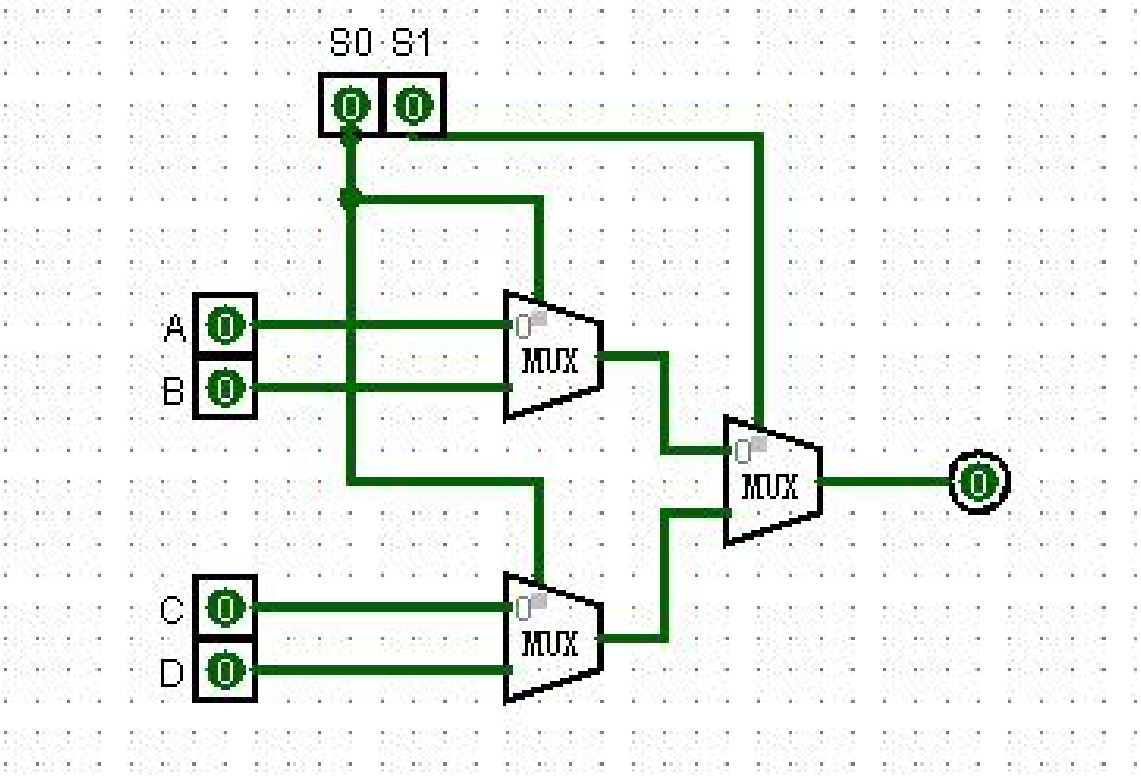
Way 2

As shown below, it needs 24 transistors in all.



b

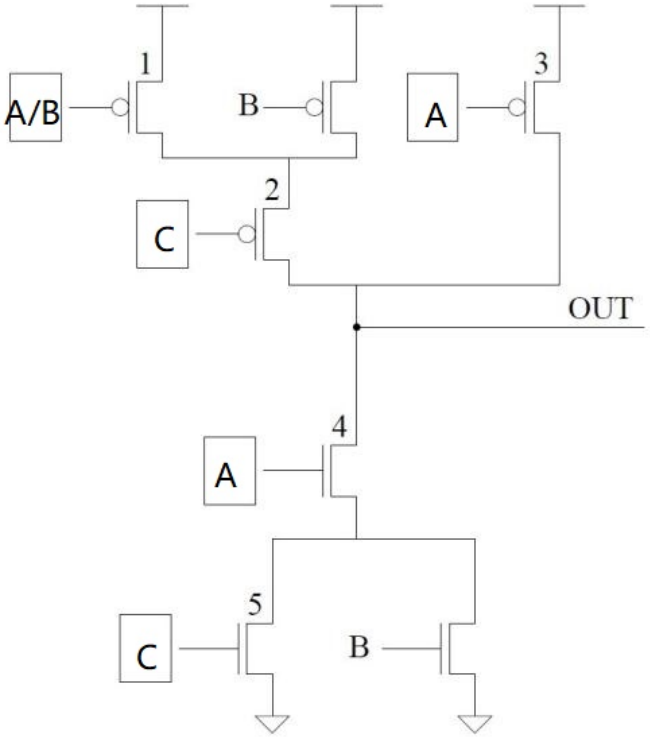
Below is the circuit.



Below is the truth table.

S1	S0	OUT
0	0	A
0	1	B
1	0	C
1	1	D

3



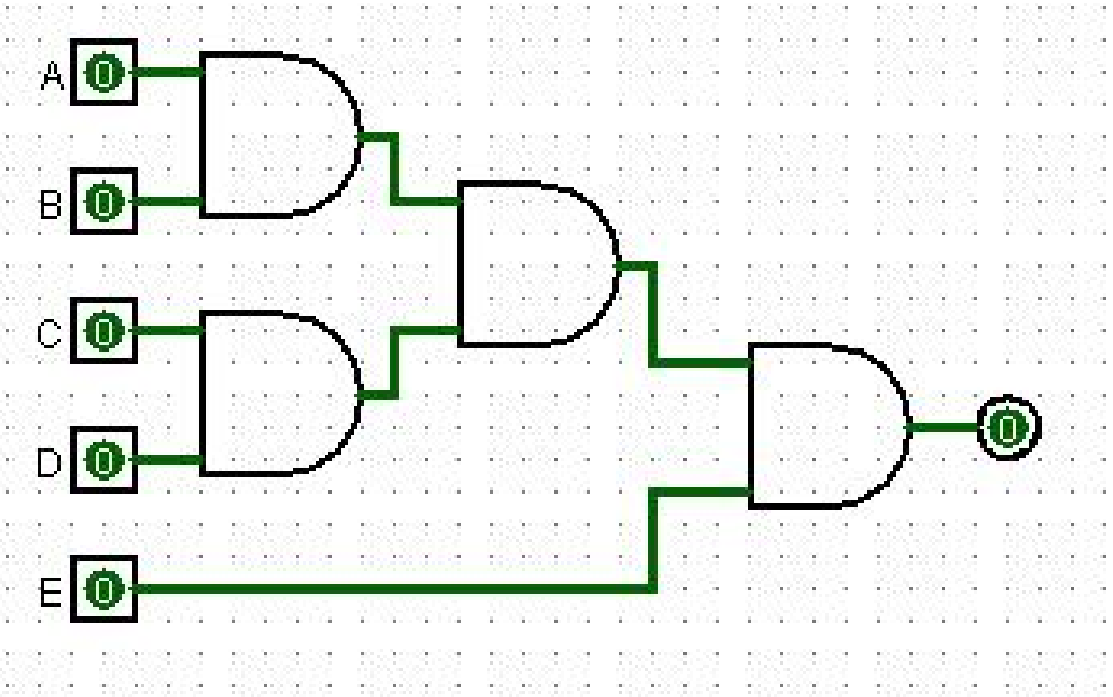
A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

4 3.19

When the input A goes from 0 to 1, output D in Figure 3.36 turns from the value of C to the value of D, while output D in Figure 3.37 will maintain its value. Besides, Figure 3.36 shows a combinational logic circuit while Figure 3.37 shows a sequential logic circuit.

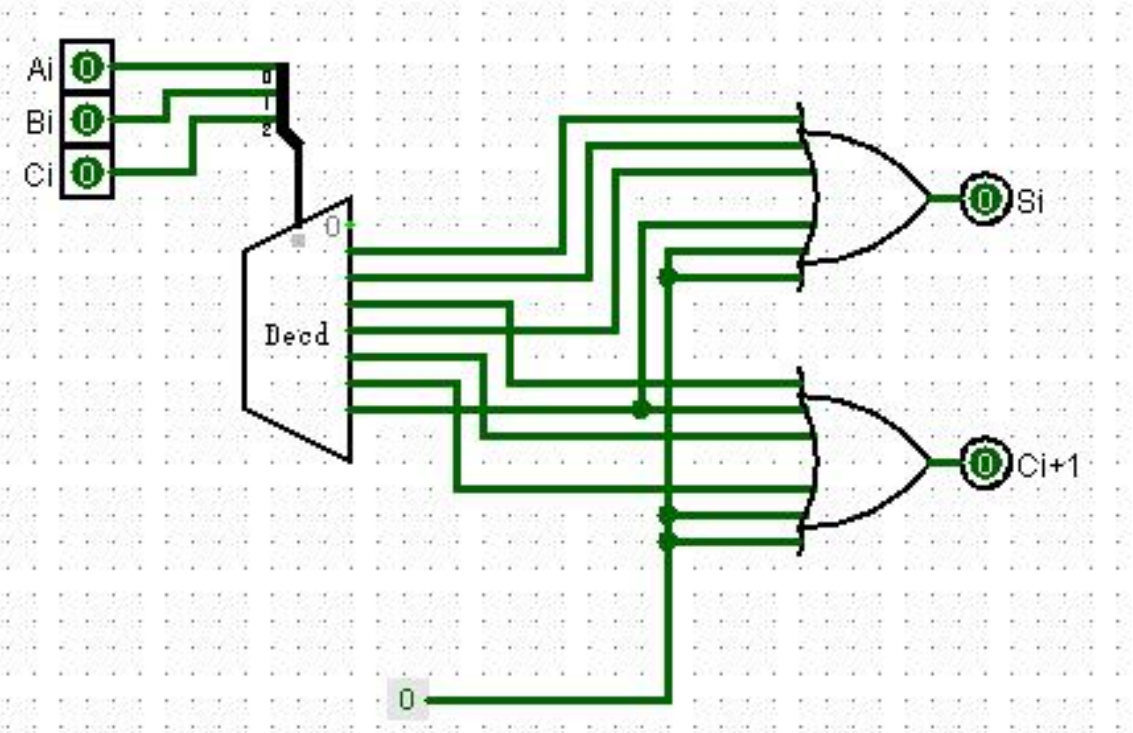
5 Adapted from 3.25

a. 3
b. 16　　每个全加器 3 个延迟，总共 3*4=12 个
c. As shown below,



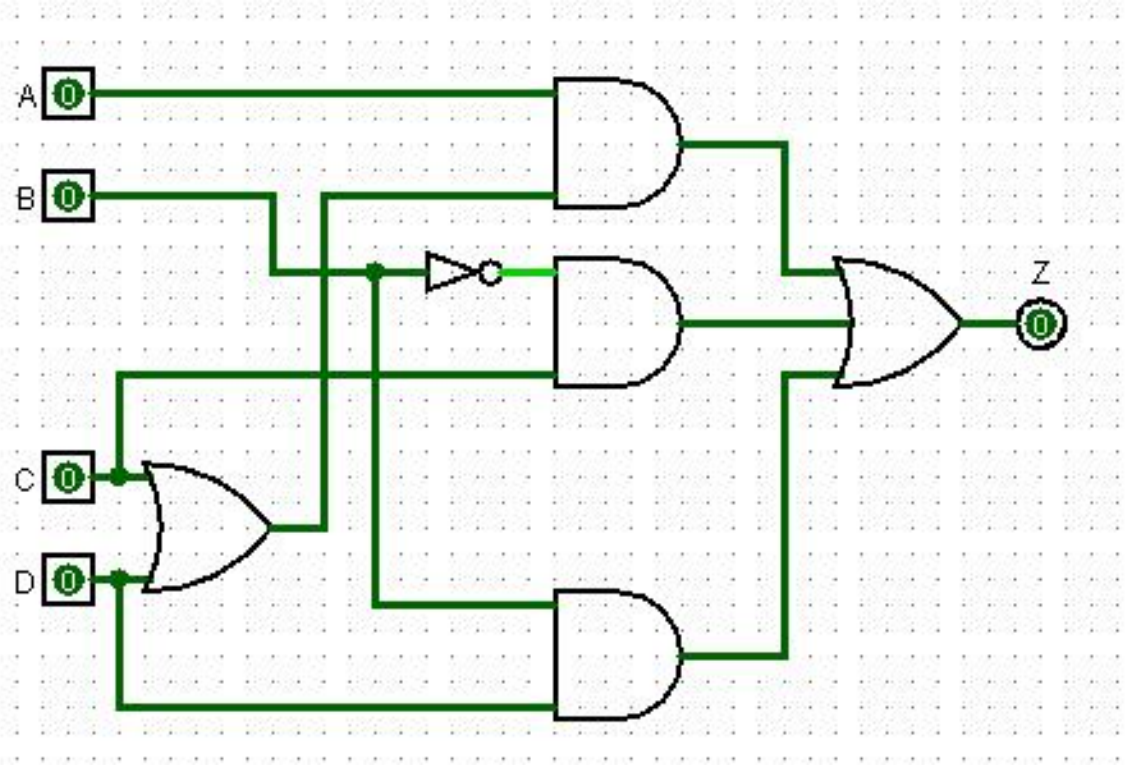
6 3.26

As shown below,



7

As shown below,



8 Adapted from 3.30

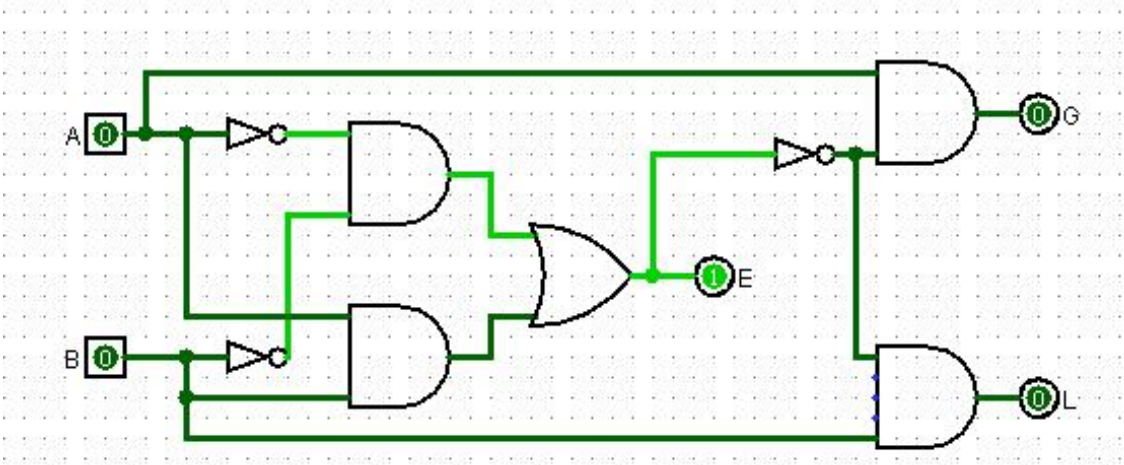
a.

As shown below,

A	B	G	E	L
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

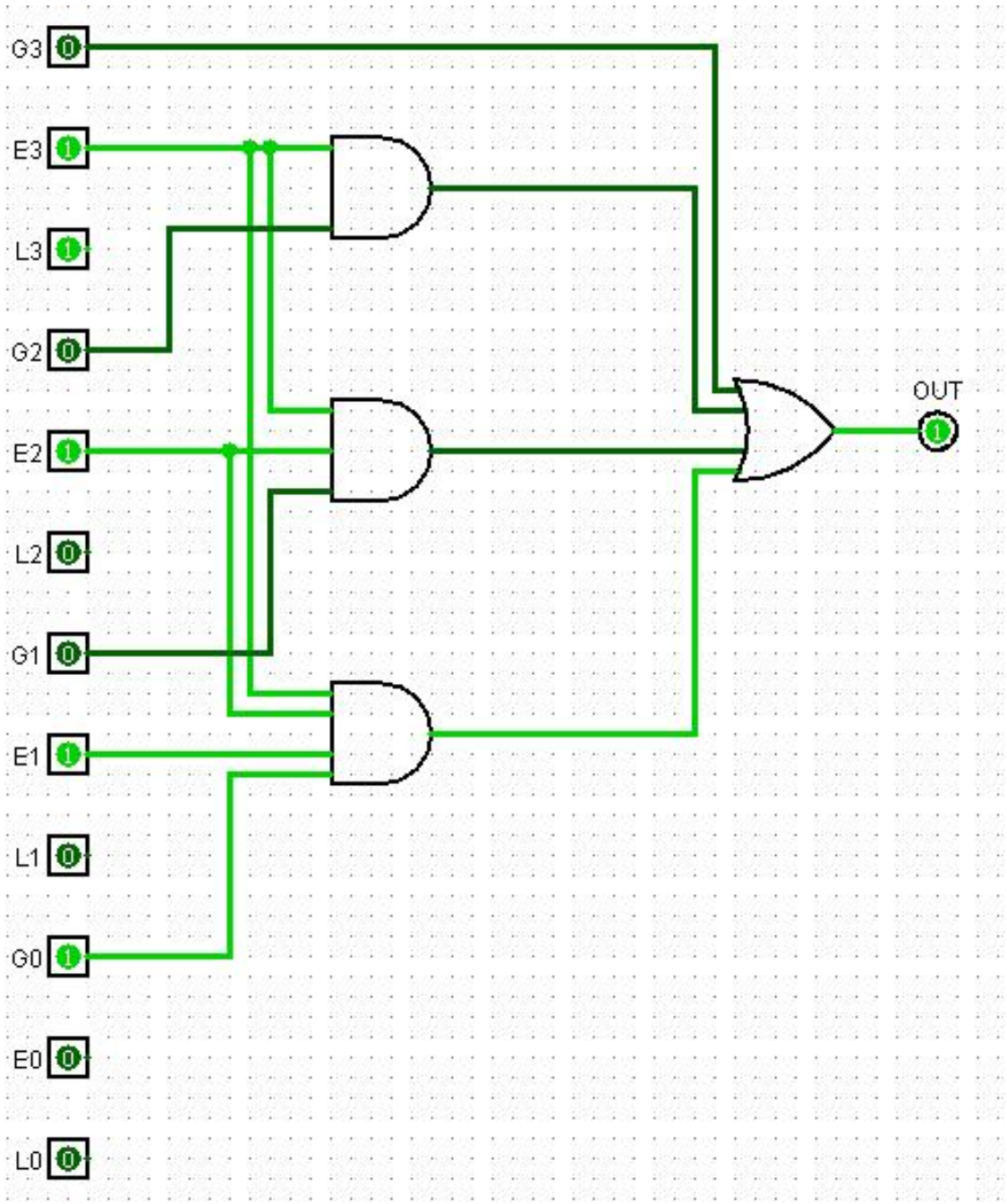
b.

As shown below,



c.

As shown below,



9

正确的顺序应该是这样的:000000, 100000, 111000, 111110, 011111, 000111, 000001, 100000...
周期是 6，所以 50 个周期以后，是 111000

After the first cycle, the state becomes 100000, due to the input of the first D Letch is 1. After the second cycle, it turns into 110000. And then 111000, 111100, 111110, 111111, 011111, 001111, 000111, 000011, 000001, 000000. Here are 12 states in total.

As we can see, after 50 cycles, the state will be changed to 110000. And it takes 12 cycles for a specific state to show up again.

10

a.

应该是 (100*100)*4*100*4*101*2*901 = 2912032000000

The number of the whole states is $100 + 100 + 4 + 100 + 4 + 50 + 50 + 2 + 60 * 15 = 1310$. So the minimum number of bits that we need to use to store the state required is $\lceil log_2 1310 \rceil = \underline{11}$.

b.

(1). 应该是 7*2bits
$\lceil log_2(100 + 100) \rceil = \underline{8}$
(2). $\lceil log_2 4 \rceil = \underline{2}$
(3). $\lceil log_2 100 \rceil = \underline{7}$
(4). $\lceil log_2 4 \rceil = \underline{2}$
(5). $\lceil log_2(50 + 50) \rceil = \underline{7}$
(6). $\lceil log_2 2 \rceil = \underline{1}$
(7). $\lceil log_2(15 * 60) \rceil = \underline{10}$

c.

First, since these variables are not quite relevant, so they can just be seperated to build several simpler circuits instead of a complex circuit. Second, the gates number that a circuit used to decode a 11 bits data will be larger than that for serveral data with 8,2,7,2,7,1,10 bits.

11

a.

The truth table is shown below.

floor[1]	floor[0]	$Q^n[1]$	$Q^n[0]$	$Q^{n+1}[1]$	$Q^{n+1}[0]$
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	1	1

b.