LINEAR INTEGRATED CIRCUITS. IV SEM

ISA - 1

KEY ANSWERS

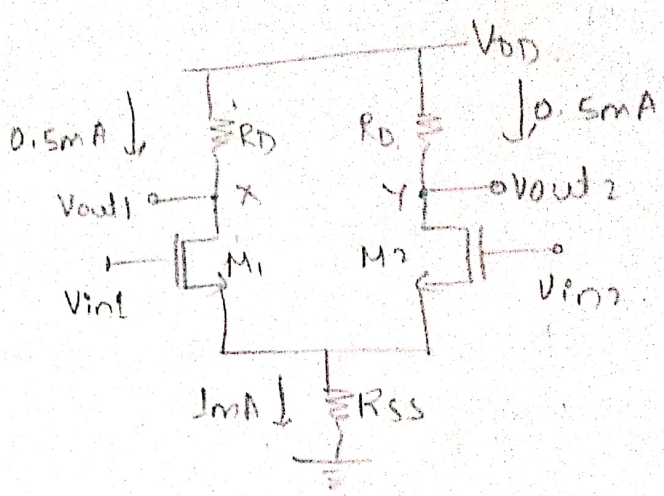
1) a) $\left(\frac{W}{L}\right)_{1,2} = \frac{25}{0.5}$, $V_{RSS} = 0.6V$

$\mu_n C_{ox} = 50\mu A/V^2$

$V_{th} = 0.5V$

$\lambda = \gamma = 0$

$V_{DD} = 3V$.



i) $V_{in} = V_{cm(min)}$

$= V_{GS1} + V_{RSS}$ —— (i)

$I_{D1} = \mu_n C_{ox}\left(\frac{W}{L}\right)_1 \frac{(V_{GS1} - V_t)^2}{2}$

$\frac{1mA}{2} = 50\times10^{-6} \times \frac{25}{0.5} \times \frac{(V_{GS1} - 0.5)^2}{2}$

$0.5\times10^{-3} = 50\times10^{-6} \times 50 \times \frac{(V_{GS1} - 0.5)^2}{2}$

$4\times10^{-4} \times 10^{-3} \times 10^{+6} = (V_{GS1} - 0.5)^2$

$0.4 = (V_{GS1} - 0.5)^2$

$V_{GS1} - 0.5 = 0.632V$.

$\boxed{V_{GS1} = 1.132V.}$

$V_{cm(min)} = 1.132 + 0.6$ (From eq. (1))

$\boxed{V_{cm(min)} = 1.732V.}$

ii) $R_D = ?$ diff. gain $= 5$

$\rightarrow A_d = g_m R_{DS} \Rightarrow g_m = \frac{2I_D}{V_{ov}}$.

$\rightarrow g_m = \frac{2\times0.5\times10^{-3}}{1.132 - 0.5} = 1.58\times10^{-3}$. $\Rightarrow R_d = \frac{5}{1.58\times10^{-3}}$

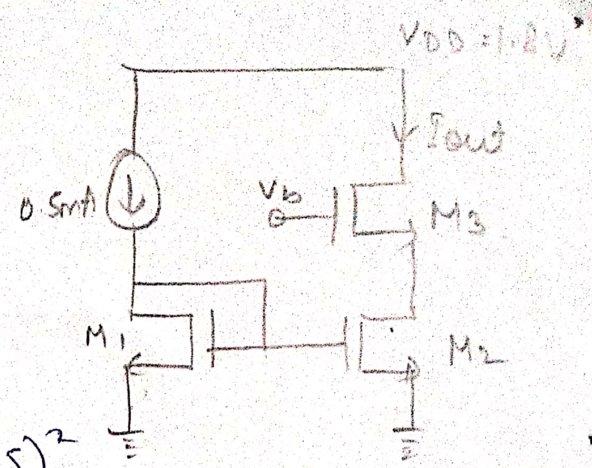
$\rightarrow \boxed{R_D = 3.164 K\Omega}$

1) b). $\left(\frac{W}{L}\right)_{1,3} = \frac{5\mu}{0.18\mu}$.

$\mu_n C_{ox} = 100\ \mu A/V^2$

$V_t = 0.5V$.

$I = 0.5mA$



$I = \mu_n C_{ox}\left(\frac{W}{L}\right)\frac{(V_{GS}-V_t)^2}{2}$

$0.5\times10^{-3} = 100\times10^{-6}\times\frac{5}{0.18}\times\frac{1}{2}(V_{GS}-0.5)^2$

$0.36 = (V_{GS}-0.5)^2 \Rightarrow V_{GS}-V_t = 0.6. = V_{DS(min)2}$

$\boxed{V_{GS} = 1.1V.}$

$V_b = 2V_{GS}$. $\quad (V_{gs3}+V_{gs2}) = (2V_{gs})$.

$V_b = 2\times1.1$

$\boxed{V_b = 2.2V}$

or $V_b = V_{GS(M3)} + V_{DS(min)2}$

$V_b = 1.1 + 0.6$

$\boxed{V_b = 1.7V.}$

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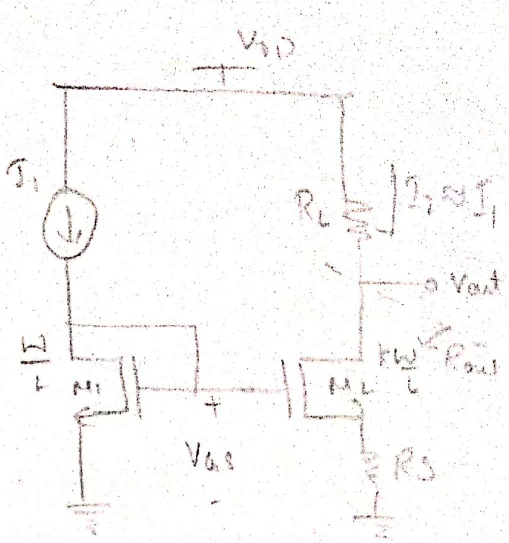
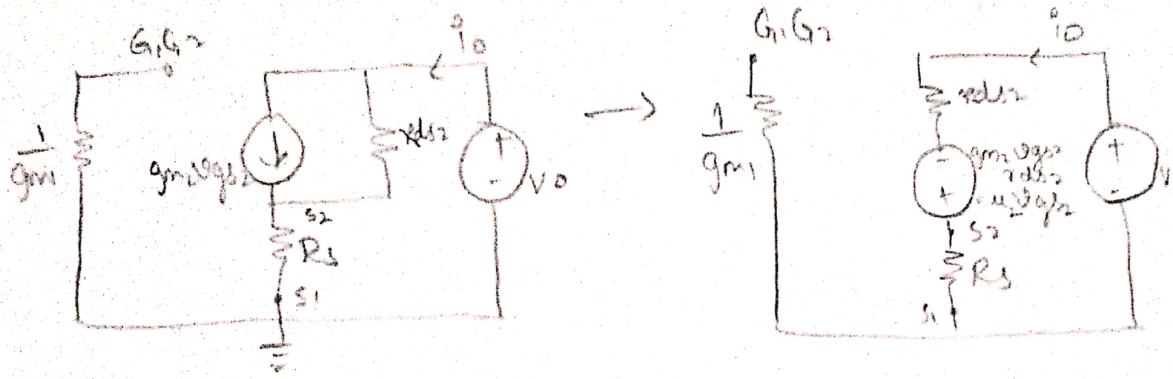
1) c) Widlar current mirror.

→ To improve performance parameter or the output resistance, we have to flatten the curve by increasing size of M_2 (increasing length) but the topological approach is to attach R_s at the source terminal.

- For better current mirror high o/p resistor is must.





→ $V_{g1} = V_{g2} = V_{S1} = 0$

→ $V_{S2} = i_o R_s$.

→ $V_{gs2} = 0 - i_o R_s = -i_o R_s$.

→ KVL to the loop ⇒ $V_o - i_o r_{ds2} + \mu_2 V_{gs2} - i_o R_s = 0$.

$= V_o - i_o r_{ds2} - \mu_2 i_o R_s - i_o R_s = 0$

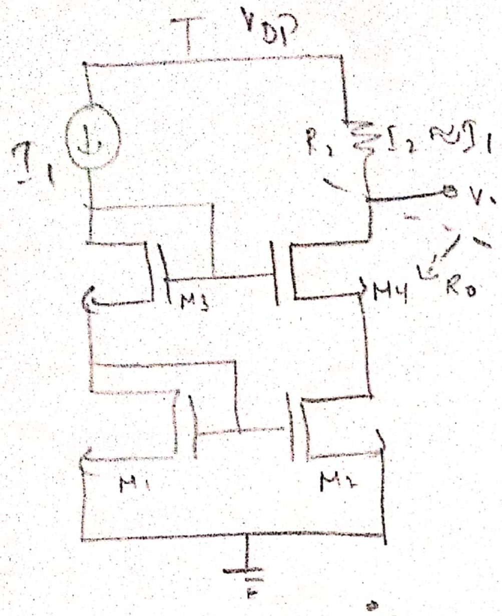
$\therefore V_o = i_o (r_{ds2} + R_s + \mu R_s)$

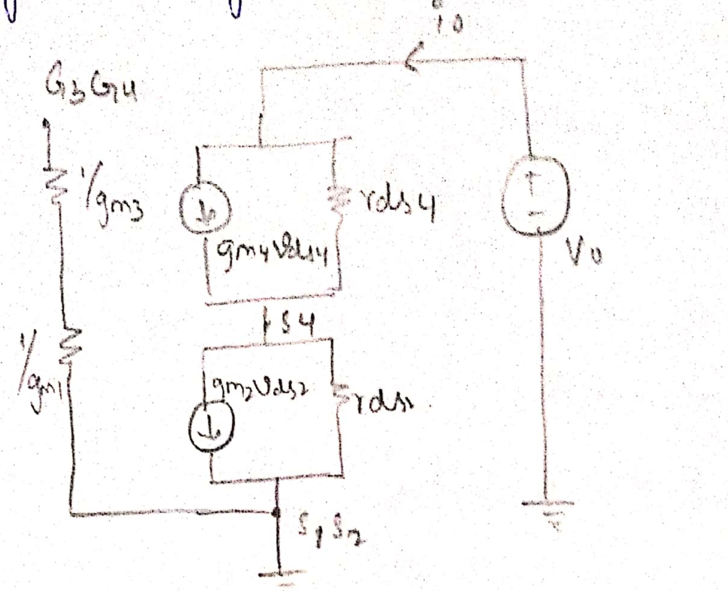
considering all $r_{ds} = r_{ds}$.

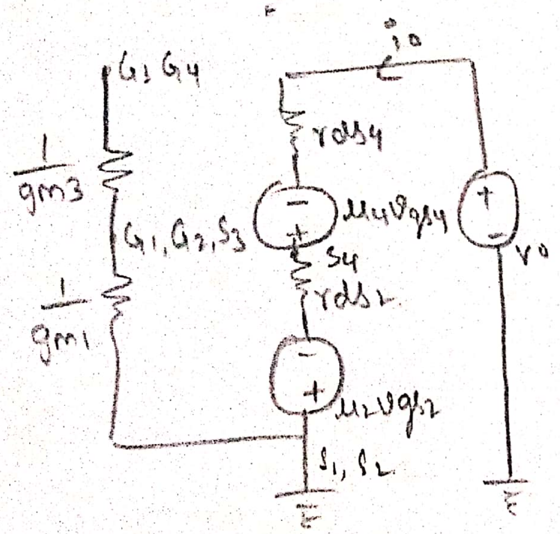
$\therefore R_o = \frac{V_o}{i_o} = r_{ds} + R_s + \mu R_s = \boxed{r_{ds} + (\mu + 1) R_s}$

- If R_L inc, $I_2 R_L$ inc. terminal voltage of M_2 dec. i.e. V_{DS} decreases, current reduces so voltage drop across R_s also decreases. So V_{gs} tends to increase
- Effectively R_o is increased. (by $(1+\mu) R_s$).

To increase the output resistance
Cascode current mirror.
Source resistance replaced by current mirror.







$V_{S1} = V_{S2} = 0.$

$V_{g1} = V_{g2} = V_{g3} = V_{S3} = V_{g4} = 0.$

$V_{S4} = i_o r_{ds2} + \mu_2 V_{gs2}$

$V_{S4} = i_o r_{ds2}$

$V_{gs4} = -i_o r_{ds2}.$

$V_o - i_o r_{ds4} + \mu_4 V_{gs4} - i_o r_{ds2} + \mu_2 V_{gs2} = 0$

$V_o - i_o r_{ds4} - \mu_4 i_o r_{ds2} - i_o r_{ds2} = 0$

$\frac{V_o}{i_o} = R_o = r_{ds4} + \mu_4 r_{ds4} + r_{ds2}$

$= r_{ds2} = r_{ds4} = r_{ds}$ (Because all gm are same)

$\frac{V_o}{i_o} = R_o = 2r_{ds} + \mu_4 r_{ds}.$

Therefore output resistance is

$$\boxed{R_o = (2+\mu)\, r_{ds}.}$$

If $r_{ds} = 100k\Omega$

$g_m = 1mA/V.$

$\mu = g_m r_{ds}.$

$\mu = 100.$

$R_o = (2+100)\, r_{ds}.$

$= (102)(100)k$

$= 10200k.$

$$\boxed{R_o = 10.2M\Omega}$$

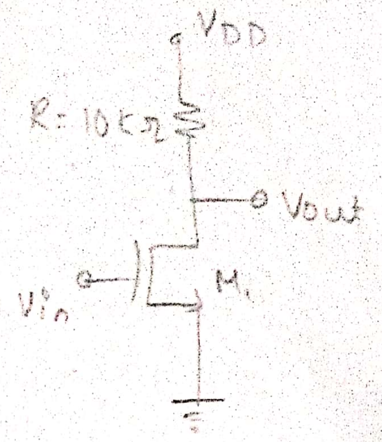
Hence the output resistance is increased by 100 times.

2a) $\frac{W}{L} = 2$.

$V_{DD} = 2V$

$\mu_n C_{ox} = 100\mu A/V^2$

$V_{th} = 0.5V$.



Considering MOSFET is in sat. region.

$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)^2$.

$\frac{2 - V_{out}}{10\times10^3} = \frac{1}{2}\times100\times10^{-6}\times2\times(V_{in}-0.5)^2$.

$2 - V_{out} = (V_{in}-0.5)^2$

$V_{in} = V_{GS}$.

$V_{out} = V_{DS}$.

$2 - V_{DS} = (V_{GS}-0.5)^2$.

Transistor switches from sat. to linear region when

$V_{DS} < V_{GS} - V_t$.

$= V_{DS} = 2 - (V_{GS}-0.5)^2$

$= 2 - (V_{GS}-0.5)^2 < V_{GS} - 0.5$. Let $(V_{GS}-0.5) = x$

$= 2 - x^2 < x$.

$= x^2 + x - 2 > 0$.

$= (x+2)(x-1) > 0$

$= (x+2) > 0$ & $(x-1) > 0$ or $(x+2) < 0$ & $(x-1) < 0$.

$=$ considering $x > 1$.

$x - 1 > 0$ & $x + 2 > 0$

$x > 1$ & $x > -2$.

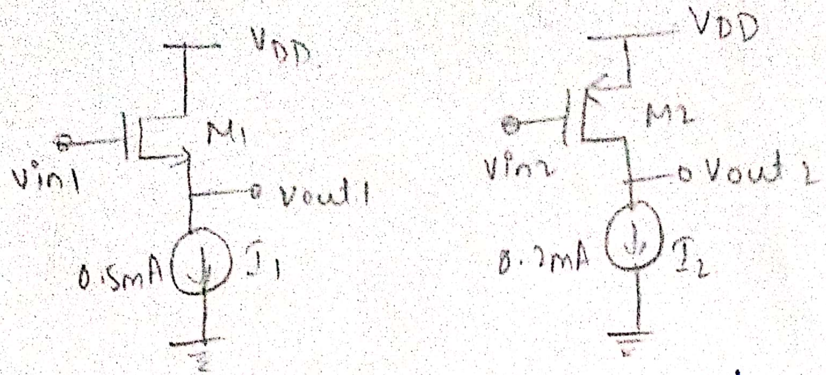
$\Rightarrow V_{GS} - 0.5 > 1 \Rightarrow V_{GS} > 1.5. \Rightarrow \boxed{V_{in} > 1.5V.}$ (Transition occurs)

$\Rightarrow I_{DS} = \frac{1}{2}\times100\times10^{-6}\times2(1.5-0.5)^2 \Rightarrow \boxed{I_{DS} = 100\mu A}$

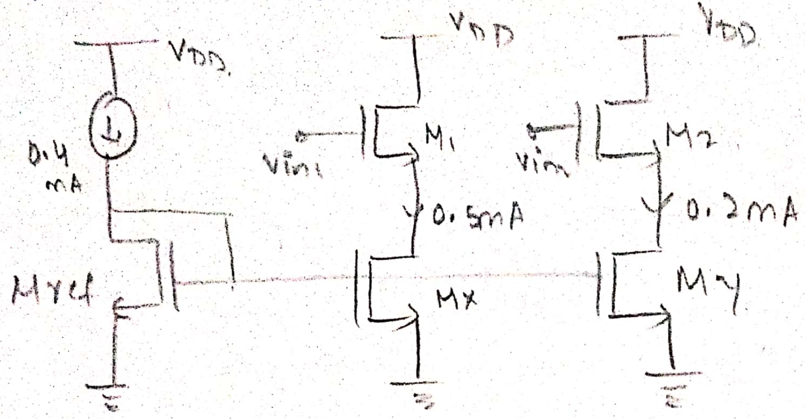
$\Rightarrow V_{GS} = 1.5 - 0.5 = 1V. \Rightarrow V_{GS} > 1.5V \rightarrow$ Saturation

$V_{GS} < 1.5V \rightarrow$ Triode.

Q b)



⟹ Application of multiple current source.



⟹ WKT $\frac{I_{out}}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1}$.

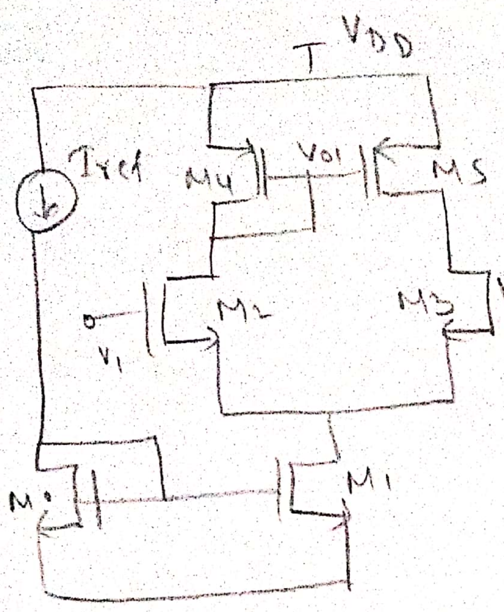
⟹ $\frac{I_2}{I_{ref}} = \frac{(W/L)_x}{(W/L)_{ref}}$.

$$= \boxed{\left(\frac{W}{L}\right)_x = \left(\frac{5}{4}\right)\left(\frac{W}{L}\right)_{ref}}$$

⟹ $\frac{I_3}{I_{ref}} = \frac{(W/L)_y}{(W/L)_{ref}}$.

$$= \boxed{\left(\frac{W}{L}\right)_y = \left(\frac{1}{2}\right)\left(\frac{W}{L}\right)_{ref}}$$

2) c). 5-pack differential amplifier.



AC eq. ckt

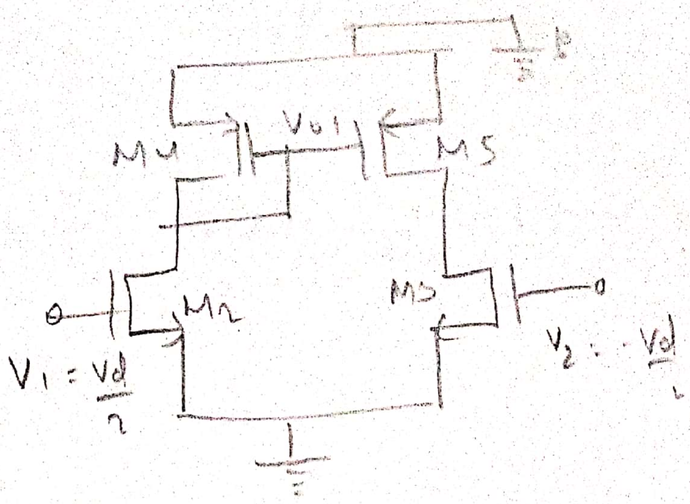


Fig-1 - M1 replacing tail resistance.
- Tail Rs inc. CMRR.
- IT shared b/w M4 & M5.

Fig-2 $V_o = V_o' + V_o''$ — (1)

$V_o' \rightarrow V_1$; path $M_2 \rightarrow M_4 \rightarrow M_5$. $(V_1 \rightarrow V_{o1}, V_o')$

$V_o'' \rightarrow V_2$; path $M_3 \rightarrow M_5$.

- Network is not symmetric.

Case (1) $V_i = \frac{V_d}{2} = V_1 = V_o'$

$V_{o1} = -g_{mn}(r_{dsn} \| 1/g_{mp})\, V_d/2$ — (2)

$V_o' = -g_{mp}\,(r_{dsp} \| r_{dsn})\, V_{o1}$ — (3)

Put (2) in (3)

$V_o' = g_{mn} g_{mp} (r_{dsn} \| 1/g_{mp})(r_{dsp} \| r_{dsn})\, V_d/2$ — (4)

Since $1/g_{mp} <<< r_{dsn}$; $\|^{el}$ comb gives $1/g_{mp}$.

All rds & gm are same.

$V_o' = \frac{g_m r_{ds} V_d}{4}$ — (5)

Case ② $V_i = -\frac{V_d}{2}$; V_o''

$V_o'' = -g_{mp}(r_{dsn} \parallel r_{dsp})(-V_d/2)$

$V_o'' = \frac{g_m r_{ds} V_d}{4}$ — ⑥

Put ⑤ & ⑥ in ①

$$\boxed{V_o = \frac{g_m r_{ds} V_d}{2}} \quad \text{— ⑦}$$

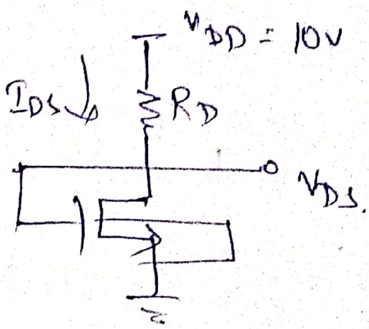
$$\boxed{A_d = \frac{V_o}{V_d} = \frac{g_m r_{ds}}{2}}$$

3) a) $V_{DD} = 10V$

$\mu_n C_{ox} = 10^{-4} A/V^2$

$V_t = 1V$.

$I_{DS} = 0.5mA$.



$I_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\frac{(V_{GS}-V_t)^2}{2}$

$0.5 \times 10^{-3} = 10^{-4} \times 1 \times \frac{(V_{GS}-1)^2}{2}$.

$V_{DS} = V_{GS}$

$V_{GS} = 4.16V$

$\boxed{V_{DS} = 4.16V}$

$V_{DD} - I_D R_D = V_{DS}$

$R_D = \frac{V_{DD} - V_{DS}}{I_D} = \frac{10 - 4.16}{0.5m}$.

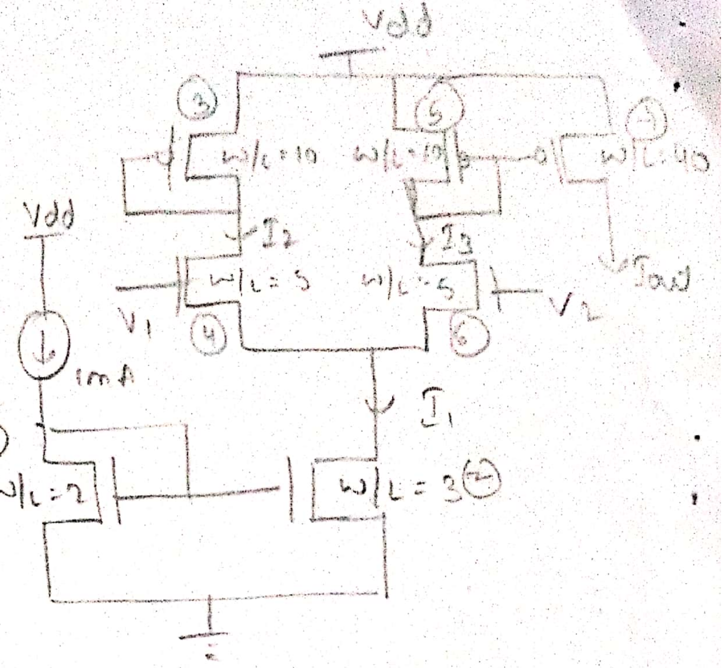
$\boxed{R_D = 11.68 k\Omega}$

3b) From 1st stage

$$\frac{I_1}{1mA} = \frac{(W/L)_2}{(W/L)_1}$$

$$I_1 = \frac{3}{2}(1mA)$$

$$\boxed{I_1 = 1.5mA}$$



Since $V_1 = 0$, transistor 3 is off.
Hence no current will flow from transistor 3 and 4

$I_1 = I_3 = 1mA$

Now transistors 5 & 7 are matched.

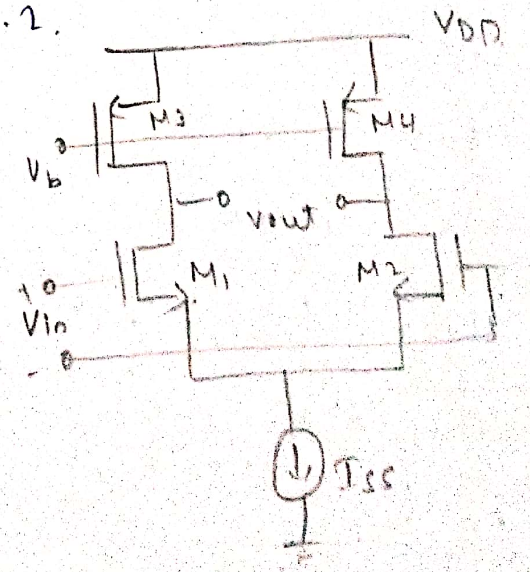
$$I_3\left(\frac{W}{L}\right)_7 = I_{out}\left(\frac{W}{L}\right)_5.$$

$$(1.5)(40) = I_{out}(10).$$

$$I_{out} = \left(\frac{40}{10}\right)(1.5)$$

$$\boxed{I_{out} = 6mA.}$$

c) $(W/L)_{1-4} = 100$, $I_{SS} = 1mA$, $\lambda_n = 0.1$, $\lambda_p = 0.2$.



$I_{SS} = 1mA$

$$r_{dsn} = \frac{1}{\lambda_n \cdot \frac{I_{SS}}{2}} = \frac{1}{0.1 \times \frac{1}{2}mA}$$

$$\boxed{r_{dsn} = 20k\Omega}$$

$$r_{dsp} = \frac{1}{\lambda_p \cdot \frac{I_{SS}}{2}} = \frac{1}{0.2 \times \frac{1}{2}mA}$$

$$\boxed{r_{dsp} = 10k\Omega}$$

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$$A_{d1} = \frac{g_{m1}}{2\left(\frac{1}{r_{dsn}} + \frac{1}{r_{dsp}}\right)}$$

$$g_{mn1} = \sqrt{2 \mu_n C_{ox} (W/L) I_D}$$

$$= \sqrt{2 \times 134 \times 10^{-6} \times 100 \times 0.5 \times 10^{-3}}$$

$$= \sqrt{13.4 \times 10^{-6}}$$

$$g_{mn1} = 3.66 \times 10^{-3} \mho$$

$$\boxed{g_{m1} = 3.66 m\mho.}$$

$$A_{d1} = \frac{3.666 m\mho}{\left(\frac{1}{20} + \frac{1}{10}\right)}$$

$$A_{d1} = 12.2.$$

$\therefore$ Gain $A_d = A_{d2} - A_{d1} = 2A_d = 12.2 \times 2$

$$\boxed{A_d = 24.4.}$$

→ $V_{out1,min} = V_{DG1} + V_{incm}$

$$= V_{DS1} - V_{GS1} + V_{incm}.$$

For Vout to be minimum, V_{DS1} should be minimum

$V_{DS1min} = V_{GS1} - V_t.$

$V_{out.min} = V_{incm} - V_t$

$$= 1.5 - 0.7$$

$$\boxed{V_{out\,min} = 0.8V}$$

$V_{out1\,max} = V_{DD} - V_{SD3}.$

For Vout to be max, V_{SD3} should be minimum

$V_{SD3\,min} = V_{SG3} - |V_{tp}|.$

$V_{out1max} = V_{DD} - V_{SG3} + |V_{tp}|$

$$= 3 - V_{SG} + 0.8.$$

from current equation

$$V_{SG3} - |V_{tp}| = \sqrt{\frac{2 I_D}{\mu_p C_{ox}(W/L)}} = \sqrt{\frac{2 \times 0.5 \times 10^{-3}}{38 \times 10^{-6} \times 100}}.$$

$V_{SG3} = 0.512 + 0.8$

$\boxed{V_{SG3} = 1.312\,V}$

$\boxed{V_{out1}\,max = 2.48\,V.}$

output voltage swing $= 2(2.48 - 0.8)$

$= \boxed{3.36\,V}$

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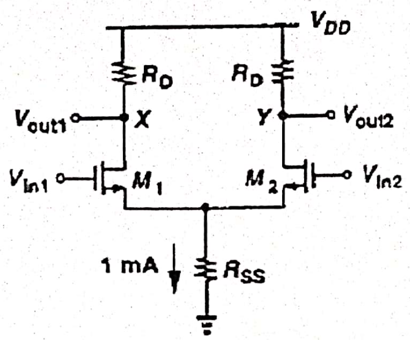
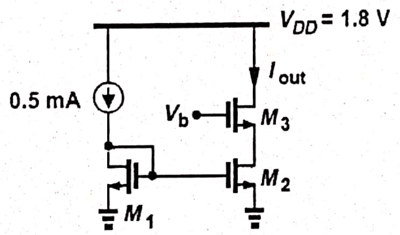
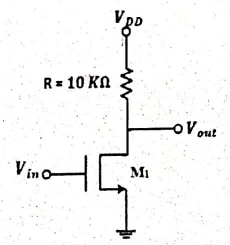
Course Title: Linear Integrated Circuits Duration: 75min Max. Marks: 40	CourseCode:19EECC203 Date:27-05-2023 Time:8.15am to 9.30pm

Q. No	Note: Answer any two full questions	Marks
1a	For the differential amplifier configuration given in Fig. Q1a, with (W/L)1,2=25/0.5, μ_nC_{ox}=50μA/V^2, V_{TH}=0.5V, λ=γ=0 and V_{DD} =3V. i)What is the required input CM for which R_{SS} sustains 0.6V? ii)Calculate R_D for a differential gain of 10  Fig.Q1a	06
b	Fig. Q1b depicts a cascode current source whose value is defined by the mirror arrangement, M_1-M_2. Assume W/L = 5μm/0.18 μm for M_1-M_3. Compute the value of V_b that I_{out} is precisely equal to 0.5 mA.  Fig.Q1b	06
c	With a neat circuit diagram of Widlar current mirror, explain and modify the circuit to increase the output resistance and derive the expression.	08
2a	For the MOSFET M_1 shown in Fig.Q2a, assume W/L=2, V_{DD}=2V, μ_nC_{ox} =100μA/V^2 and V_{TH}=0.5V. Compute the value of Vin (volts) for which the transistor M_1 switches from saturation region to linear region.  Fig.Q2a	06
b.	An integrated circuit employs the source follower and the common-source stage shown in Fig.Q2b. Design a current mirror that produces I_1 and I_2 from a 0.4mA reference.	06

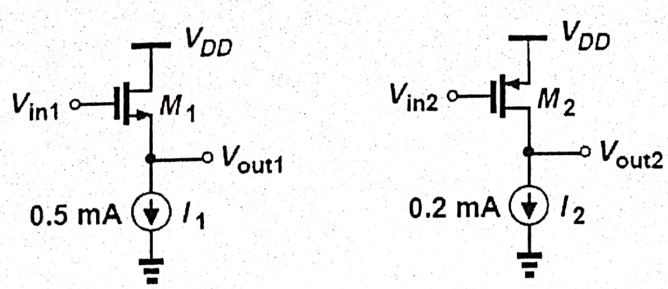


Fig.Q2b

c Draw the circuit of 5 pack differential amplifier, explain and derive the equation for voltage gain. **08**

3a Given NMOS circuit as shown in Fig. Q3a, the specifications of the circuit are: V_{DD} =10V, $\mu_n C_{ox}$ = 10^{-4} A/V^2, V_T=1V and I_{DS}=0.5mA. Evaluate V_{DS} and R_D. Neglect body effect. **06**

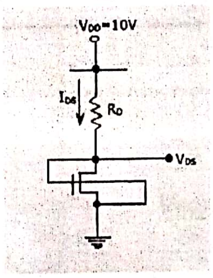


Fig.Q3a

b In the circuit shown in Fig.Q3b, V_1=0V and V_2=Vdd. The relevant parameters are mentioned in the Fig. Q3b. Ignoring the effect of channel length modulation and body effect, Compute the I_{out} **06**

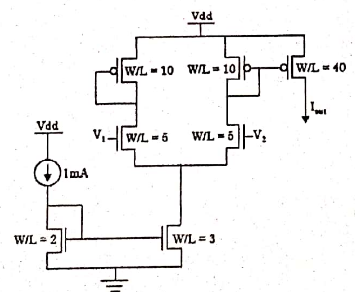


Fig.Q3b

c For the circuit shown in Fig. Q3c, (W/L) 1-4 =50/0.5, ISS=1mA, λn=0.1and λp=0.2, what is the small signal differential gain? For Vin,CM=1.5V, What is maximum allowable output voltage swing? **08**

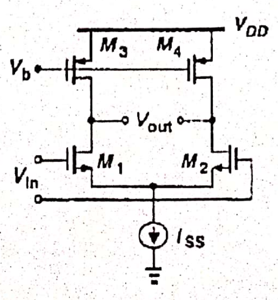


Fig.Q3c