

Instruction Format

Instructions OP-CODE

0	0	0	0	0	SWAP
0	0	0	0	1	ADD
0	0	0	1	0	IADD
0	0	0	1	1	SUB
0	0	1	0	0	AND
0	0	1	0	1	OR
0	0	1	1	0	SHL
0	0	1	1	1	SHR
0	1	0	0	0	NOP
0	1	0	0	1	NOT
0	1	0	1	0	INC
0	1	0	1	1	DEC
0	1	1	0	0	OUT
0	1	1	0	1	IN
1	0	0	0	0	JZ
1	0	0	0	1	JMP
1	0	0	1	0	CALL
1	0	1	0	0	RET
1	0	1	0	1	RTI
1	0	1	1	0	RESET
1	0	1	1	1	INTERRUPT
1	1	0	0	0	PUSH
1	1	0	0	1	POP

Instruction Format

1	1	1	0	0	LDM
1	1	1	0	1	LDD
1	1	1	1	0	STD

Registers codes

0	0	0	R0
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	R4
1	0	1	R5
1	1	0	R6
1	1	1	R7

Instruction Format

2OP

0	0	0	0	X	X	X	Rsrc1	Rsrc2	Rdst			
15	14	13	12	11	10	9	8	6	5	3	2	0

2OP SWAP

0	0	0	0	0	0	0	Not Used	Rsrc1	Rdst			
15	14	13	12	11	10	9	8	6	5	3	2	0

2OP SHL/SHR

0	0	0	0	1	1	X	Not Used	
15	14	13	12	11	10	9	8	0

2OP SHL/SHR immediate val

IMMEDIATE	
15	0

1OP

0	0	0	1	X	X	X	Not Used			Rdst		
15	14	13	12	11	10	9	8	3			2	0

1OP NOP

0	0	0	1	0	0	0	Not Used	
15	14	13	12	11	10	9	8	0

BR JZ/JMP/CALL

0	0	1	0	0	X	X	Not Used			Rdst
15	14	13	12	11	10	9	8	3 2 0		

BR Ret/RTI/Reset/Interrupt

0	0	1	0	1	X	X	Not Used	
15	14	13	12	11	10	9	8	0

MEMO op LDM/STD/LDD

0	0	1	1	1	X	X	Not Used	
15	14	13	12	11	10	9	8	

16 bit of EA	
15	0

X	X	X	X	Not Used
15	14	13	11	0

MEMO op PUSH/POP

No up PUSH/POP											
0	0	1	1	0	0	X	Not Used			Rdst	
15	14	13	12	11	10	9	8	3 2			0