Control Signals interpretation:

DecEnable (DE): 0 disables IF/ID buffer.

FetchEnable (FE): 0 disables PC register (preserve its value for stalling).

ALUsrc: selects R2 (1) or immediate value (0) to enter ALU as 2nd operand.

Swap?: 1 indicates the processed instructions is swap (raise in 2nd state only)

SP?: 1 indicates the processed instruction uses SP register.

MR: 1 indicates memory read operation.

MW: 1 indicates memory write operation.

RW: 1 indicates register write operation.

MemtoReg: 1 indicates the value to be written in register evolves from the memory rather than ALU (in case RW = 0, its value is don't care)

Control Signals per instruction in every state:

State 1:

Instruction	DecEnable (DE)	FetchEnable (FE)	ALU src	SP?	MR	MW	RW	MemToReg
NOP	1	1	X	0	0	0	0	X
Not, Inc, Dec	1	1	X	0	0	0	1	0
Add, SUB, And, OR	1	1	1	0	0	0	1	0
Swap	0	0	1	0	0	0	0	X
IAdd, SHL, SHR, LDM	0	1	X	0	0	0	0	X
LDM	0	1	X	0	0	0	0	X
LDD, SDD	0	1	X	0	0	0	0	X
Push	1	1	X	1	0	1	0	X
Pop	1	1	X	1	1	0	1	1
Ret, RTI	0	0	X	1	1	0	0	X
Interrupt	0	0	X	1	0	1	0	X
Reset	0	0	X	0	1	0	0	X
IN	1	1	X	0	0	0	1	X
OUT	1	1	X	0	0	0	0	X

State 2

IAdd/SHL	1	1	0	0	0	0	1	0
LDM	1	1	0	0	1	0	1	1

Swap	1	1	1	0	0	0	1	0
LDD, SDD	0	1	0	0	0	0	0	X
Ret	0	0	X	0	0	0	0	X
RTI	0	0	X	1	1	0	0	X
Interrupt	0	0	X	0	1	0	0	X

State 3

LDD	1	1	0	0	1	0	1	1
SDD	1	1	0	0	0	1	0	0
Ret, RTI	0	1	X	0	0	0	0	0
Interrupt	0	1	X	1	0	1	0	0

** Reset has zero signals in states 2 and 3

Other signals:-

- For LDD, SDD, a signals: EAH is the enable of the 4-bit registers which carry the effective address high 4 bits.

  In state2: EAH =1
  Otherwise, EAH =0 (until Mem)

- FromEA?: a signal that raise only in state 3 (when input is an EA instruction opcode), a mux selector that passes the address of the memory from EA registers, instead of the ALU output. (used in memory stage) (until Mem)
- Call, Int, push: All indicate that SP is modified after memory stage, Int raises when interrupt occurs (state1). (until Ex)
- Swap?: signifies the swap instruction to switch the RegDest address, prompts ALU to Nop R2 instead of R1, raises in state 2 only and zero otherwise.
- Ret: prompts PC mux to select the output of the memory in Ret and RTI. (Mem)
- RTI: raises in 2nd state in RTI instructions to restore flags and increment SP.
- intS2 (Mem), intS3 (Ex): raises in interrupt state 2,3 to prompt pc's mux or decrement SP and preserve flags.
- In, out: raise to enable out port or selects input port to be written back.

Stage	Decode	Execute		Memory		Write back	
control signal	DE, FE, Swap? ALUsrc	ALUsrc	SP?	MR	MW	RW	MemtoReg
Total until	22	18		7		2	