Commodity Hardware today

There are two parts of chipset in personal computers and smaller computers. Those are north bride and south bridge. North bridge is connected to front side bus and it has memory controller and performance types of RAM such as DRAM (Dynamic RAM) and SDRAM (Synchronous DRAM), Rambus. South bridge control communication wit I/O devices. (use SATA, USB etc). These bridges able to be communicate with each other. This structure has a few of ponderable sequel and few disadvantages which there is struggling between CPU and DMA(Direct memory access) to access to bus and older system, can't implement parallel access because system used one bus. At the one time, if multiple threads try to access to memory , there will be a long waiting time. By using eternal controllers, can improve the memory bandwidth. Other way is, combine multiple memory controllers to a CPU, then connect to the memory. This technology is known as NUMA (Non- Uniform Memory Architecture). I here a CPU want to access to a other memory, that CPU has to communicate through a interconnection which between two CPUs. NUMA factor tells about the additional time which used for access remote memory.

RAM Type

Basically, there are two types of RAM such as SRAM (Static RAM) and DRAM (Dynamic RAM). Because of the price and the speed, both SRAM and DRAM are used in computer. In SRAM, there are six transistors in a cell. need constant power to charge. There is no refresh cycle for cell. In DRAM, one capacitor and one transistor are contained in one cell of DRAM. But current discharge the capacitor. This is known as the leakage. So, DRAM cells have to always refresh. In the mean time can not read data from the cell without a sense amplifier. DRAM takes time more than SRAM to respond because capacitors take some time to discharge and charge. Sometimes we use DRAM for main memory except some hardware such as network routers. Because of the high speed and limited size usually SRAM are used for cache memory.

DRAM Access

Virtual address which is include in program is translated by processor to a physical address. After that memory controller responds to select relevant RAM chip to above address. 1 and 0

used for encoding the address and demultiplexer is used to decode it. Demultiplexer's size expand with number of cells. Because of that increment of the number of cells is not good. To prevent that DRAM cell, follow a concept which row and columns. Because of that demultiplexer can reduce size.

DRAM Access Technical Details

There are two types of DRAM , asynchronous DRAM and synchronous DRAM. Synchronous DRAM has a time source(frequency) and from that decide speed of the FSB.

Recharging

In consonance with JEDEC(Joint Electron Device Engineering Council) specification, for every 64ms every DRAM cell has to refresh.

Memory types

If memory cells and data transfer rate are same, then called SDR(Single Data Rate). If throughput is grown of the DRAM chip, frequency and energy consumption also increase by together. DDR1(also known as DDR SDRAM) can increase the throughput without improve the relevant frequency. DDR1 different from SSD, cause amount of data is carried per cycle in twice(rising edge and falling edge). This scenario known as double pumped bus. Buffer is used to prevent the increment of frequency

In every DDR RAM, it is very difficult to create parallel data buses cause increment of the frequency of the bus. AMD used Opteron line and Intel used CSI technology to solve this problem. Intel introduced FB-DRAM(Fully Buffered DRAM) which similar to DDR2. FB-DRAM use serial bus which need high energy because have high frequency to drive. It is better than parallel bus. FB-DRAM is better than DDR2 and DDR3.

High performance cards(Mass storage controllers and network card) need DMA. Other buses such as USB need FSB(not use DMA). Graph cards is effect to system performance