DSD OEL

FPGA-Based Temperature Measurement

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Contents

Introduction

The objective of this project is to design and implement an FPGA-based temperature sensing system using the Nexys A7 development board. The system interfaces with an ADT7420 digital temperature sensor via the I²C communication protocol, reads temperature data, and displays it simultaneously on LEDs and 7-segment displays. FPGAs provide a flexible and high-performance platform for real-time sensor interfacing, making them ideal for applications that require rapid data acquisition and visual output.

This project demonstrates the integration of modular hardware design, clock generation, I²C protocol handling, and display control. Through simulation and verification, the functionality of the I²C master and temperature display modules is validated, ensuring accurate sensor readings and reliable hardware operation. The design emphasizes modularity, reusability, and efficient FPGA resource utilization, providing a foundation for more complex embedded system implementations.

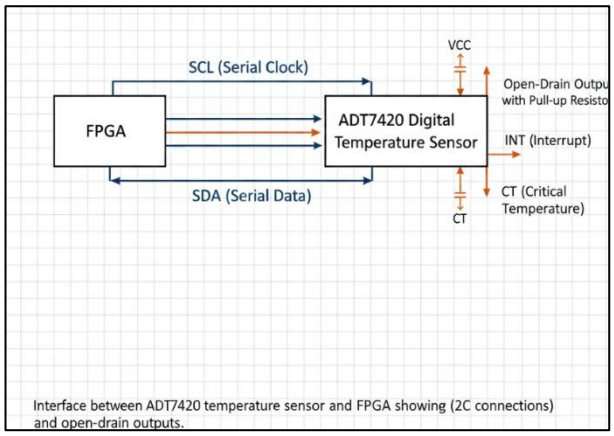
Hardware Details on the Nexys A7

The temperature sensor system was implemented on the Nexys A7 FPGA board, interfacing with the ADT7420 digital temperature sensor via I²C. Temperature readings are displayed on both the onboard LEDs and 7-segment displays for immediate visual feedback.

ADT7420 Temperature Sensor

The Nexys A7 board comes equipped with an Analog Devices ADT7420 temperature sensor via highly accurate digital temperature sensor with these specifications:

- **Resolution:** Up to 16-bit precision
- **Accuracy:** Better than 0.25°C typical
- **Interface:** I²C (Inter-Integrated Circuit)
- **Slave Address:** 0x4B
- **Operating Range:** -40°C to +150



Interface between ADT7420 temperature sensor and FPGA showing (2C connections) and open-drain outputs.

Understanding of I2C Protocol

I²C Protocol

I²C uses just two lines:

- SCL (Serial Clock): Clock signal generated by the master
- SDA (Serial Data): Bidirectional data line

Key characteristics:

- Multi-master, multi-slave architecture
- Half-duplex communication (not simultaneous send/receive)
- Open-drain outputs requiring pull-up resistors
- Typical speeds: 100 kHz (Standard) or 400 kHz (Fast mode)

I²C Transaction Flow

A typical I²C read transaction looks like this:

1. START condition (SDA falls while SCL is high)
2. Send slave address (7 bits) + Write bit (0)
3. Send register address to read from
4. RESTART condition
5. Send slave address + Read bit (1)
6. Receive data byte(s)
7. STOP condition (SDA rises while SCL is high).

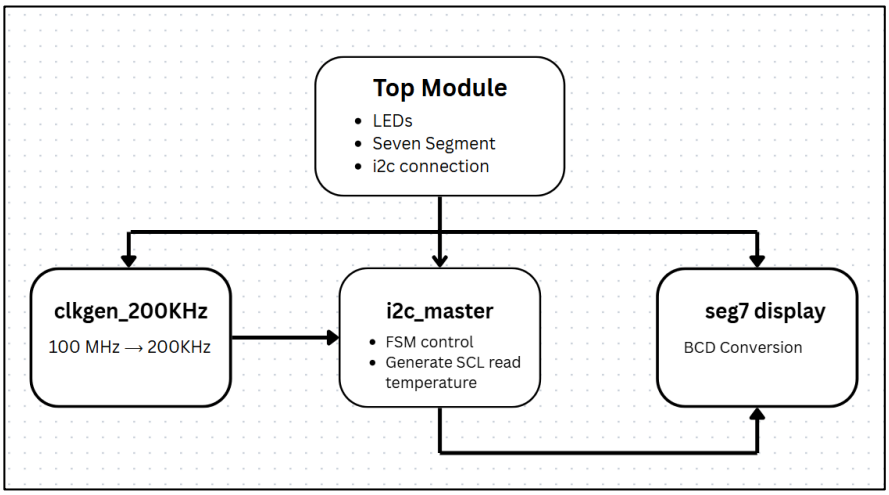
Design Methodology

The design of the FPGA-based temperature sensor system for the Nexys A7 board is organized in a modular and hierarchical manner to ensure clarity, reusability, and efficient hardware implementation. The overall methodology involves the following stages:

1. ### Top-Level Design Integration:
   The top module serves as the primary integration layer, connecting all submodules. It interfaces with the 100 MHz system clock (CLK100MHZ), a reset input, the ADT7420 temperature sensor via I²C (TMP_SDA and TMP_SCL), LEDs, and 7-segment displays. The design ensures that the temperature data read from the sensor is output both as binary values on the LEDs and as human-readable digits on the 7-segment displays.
2. ### Clock Generation:
   A dedicated clkgen_200kHz module generates a 200 kHz clock from the 100 MHz system clock. This 200 kHz clock drives the I²C master and serves as the timing reference for the serial communication with the temperature sensor. The module uses a simple counter to divide the input clock to the desired frequency.
3. ### I²C Master Implementation:
   The i2c_master module, obtained from a GitHub repository and slightly modified for reset and timing corrections, handles all I²C communication with the ADT7420 sensor. The module generates a 10 kHz SCL clock from the 200 kHz input and implements a finite state machine

(FSM) to send the sensor address, read temperature data, and handle acknowledgments. The FSM ensures sequential transmission of address bits, read/write control, reception of MSB and LSB temperature data, and proper acknowledgment handling. The temperature data is buffered in an 8-bit register for output.

4. 7-Segment Display Control:
   The seg7 module converts the 8-bit temperature data into BCD format and drives four 7-segment displays to show the temperature in Celsius. Digit selection and display refreshing are handled using counters to ensure a flicker-free display at a visible refresh rate.
5. Simulation Methodology:
   Since the project focuses on verifying I²C communication, a testbench for the i2c_master module was created. The testbench applies a clock signal, a reset pulse, and monitors the SDA and SCL lines. By simulating the FSM of the I²C master, the waveform shows toggling of TMP_SCL and the sequential reception of temperature data bits, verifying correct protocol operation. Simulation was conducted using a short-accelerated clock to observe multiple SCL cycles in a reasonable virtual time frame.
6. Data Output and Monitoring:
   The received temperature is simultaneously displayed on the LEDs and the 7-segment displays. This dual output provides immediate visual confirmation of correct sensor readings during both simulation and hardware implementation.



Design Flow

The system uses the ADT7420 digital temperature sensor, which communicates with the FPGA using the I²C protocol. I²C (Inter-Integrated Circuit) is a serial communication protocol that uses two lines:

- SDA (Serial Data Line) – carries the data.
- SCL (Serial Clock Line) – synchronizes data transfer.

The FPGA acts as the I²C master, initiating communication with the sensor. The process begins when the master sends the 7-bit sensor address along with a read command. The sensor acknowledges the request and sends back the temperature data, usually in 16-bit format (MSB and LSB). This data is received by the FPGA and stored in a buffer register for further processing.

Once the FPGA has the temperature value, the data is sent to two outputs simultaneously:

1. **LEDs:** The 8-bit temperature value is displayed in binary on the onboard LEDs, providing a direct visual representation of the raw sensor reading.
2. **7-Segment Displays:** The same 8-bit value is converted into Binary-Coded Decimal (BCD) format, then sent to the 7-segment display controller. The display controller multiplexes the digits and drives the appropriate segment lines to show the human-readable temperature value, including the degrees symbol and Celsius unit.

Implementation

Verilog Modules Descriptions

Top Module

The top module (top) serves as the primary integration point for the FPGA-based temperature sensor system, connecting all submodules and managing the overall data flow.

Inputs:

- **CLK100MHZ** – 100 MHz system clock for initialization and synchronization
- **reset** – resets the system
- **TMP_SDA and TMP_SCL** – I²C lines interfacing with the ADT7420 temperature sensor

Outputs:

- **Onboard LEDs** – display the raw 8-bit temperature value in binary
- **7-segment display signals (SEG, AN, NAN**) – provide a human-readable decimal representation of the temperature

The top module coordinates all submodules, ensuring proper timing, correct communication with the sensor, and consistent visual output across LEDs and displays.

Clock generator module

The clock generator module (clkgen_200kHz) divides the 100 MHz system clock down to 200 kHz to provide the timing reference for the I²C master.

Input: CLK100MHZ (high-frequency system clock)

Output: clk_200kHz (slower clock used for I²C timing)

This reduced-frequency clock ensures that I²C communication is correctly timed and that the SCL signals from the FPGA are accurate and reliable.

The I²C master module (i2c_master) manages all communication between the FPGA and the ADT7420 temperature sensor.

Inputs: clk_200kHz and reset

Outputs:

- **SDA** – data line for communication
- **SCL** – clock line for I²C
- **SDA_dir** – indicates data direction
- Buffered 8-bit temperature data

Internally, the module uses a finite state machine to send the sensor address, read temperature data, and handle acknowledgments. It acts as the interface that converts the sensor's serial data into usable temperature information for the FPGA.

7-segment display module

Finally, the 7-segment display module (seg7) converts the 8-bit temperature data from the I²C master into Binary-Coded Decimal (BCD) format and drives the 7-segment displays for human-readable output.

Input: 8-bit temperature value

Outputs:

- **SEG** – signals controlling each segment
- **AN** – digit select signals for multiplexing
- **NAN** – used to turn off unused digits

The module refreshes the displays in sequence to show the correct digits without flickering, providing a clear and readable visualization of the measured temperature.

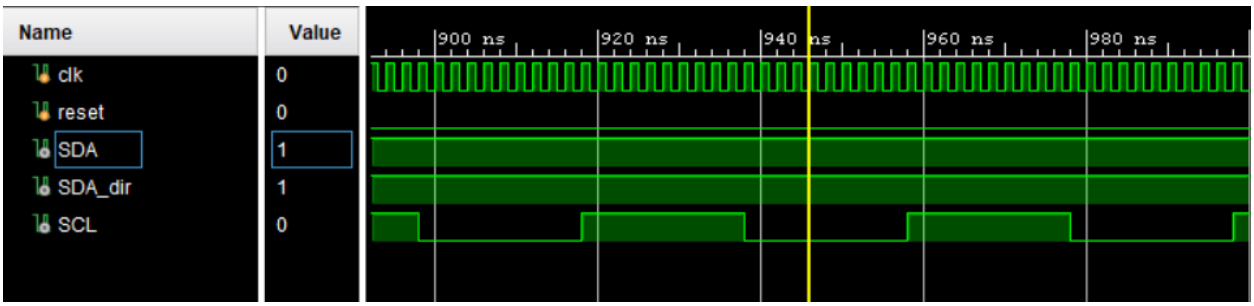
Simulations and Waveforms

Simulation was performed on both the **I²C master module** and the **top module** to verify correct functionality before hardware deployment.

For the `i2c_master` module, the testbench (`i2c_master_TB.v`) applies a 200 kHz clock and a reset signal, then monitors the SDA and SCL lines. The module's finite state machine is observed in the waveform to ensure proper sequencing of I²C operations, including sending the sensor address, reading temperature data, and handling acknowledgments. The simulation produces a VCD waveform that shows correct toggling of the clock (SCL) and data (SDA) lines over multiple cycles.

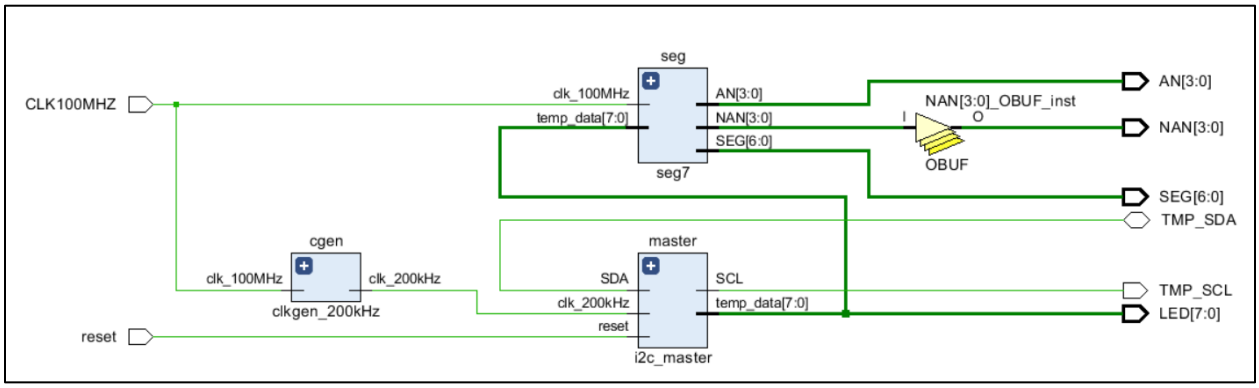
Code:

Simulation Waveform



RTL and Resource Utilization

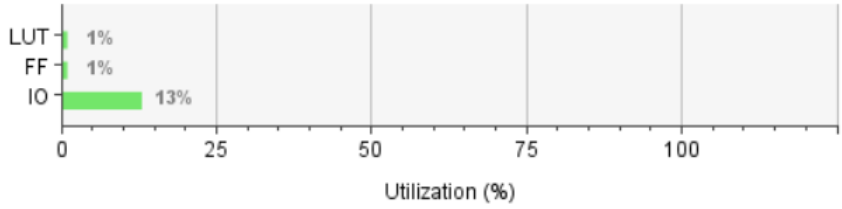
RTL



Resource Utilization

Summary

Resource	Utilization	Available	Utilization %
LUT	142	63400	0.22
FF	74	126800	0.06
IO	27	210	12.86



Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	142	0	63400	0.22
LUT as Logic	142	0	63400	0.22
LUT as Memory	0	0	19000	0.00
Slice Registers	74	0	126800	0.06
Register as Flip	67	0	126800	0.05
Register as Latc	7	0	126800	<0.01
F7 Muxes	7	0	31700	0.02
F8 Muxes	0	0	15840	0.00

IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bounded IOB	27	27	210	12.86

Clocking

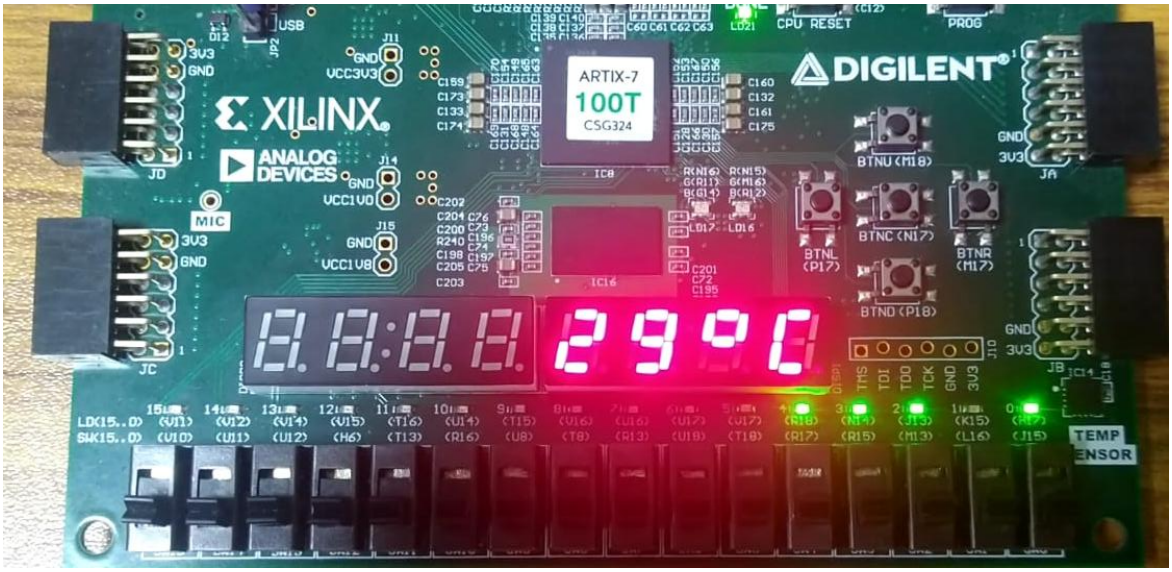
Site Type	Used	Fixed	Available	Util%
BUFGCTRL	2	0	32	6.25

No memory was required and thus not utilized by the design. Logic usage is very low since the design is very simple, and minimal logic is required for temperature sensor functionality.

Result Analysis

The FPGA-based temperature sensor system was successfully implemented and tested. During testing, the system accurately measured normal room temperature, reporting 28 °C under typical conditions. When exposed to slightly higher temperatures, the sensor output reflected the increase, giving a reading of 31 °C, demonstrating the design's sensitivity and correctness in capturing temperature variations.

The results indicate that the system is functioning as intended, with correct interfacing between the FPGA and the ADT7420 temperature sensor, and reliable data receiving via the I²C communication protocol.



References

- https://medium.com/@roshik789/mastering-i%C2%B2c-on-fpga-reading-temperature-data-from-the-adt7420-in-verilog-45b01927d0e9
- https://github.com/FPGADude/Digital-Design/blob/main/FPGA%20Projects/NexysA7_Temp_Sensor_I2C/i2c_master_TB.v
- https://github.com/FPGADude/Digital-Design/blob/main/FPGA%20Projects/NexysA7_Temp_Sensor_I2C/i2c_master_TB.v