Your name Leroy Ng 93

CS 350 Quiz 2: Wed Nov 10

Lectures 9 – 16 and Labs 5 – 8

Instructions

- The quiz is closed book, one 8.5"×11" page of notes (both sides). No sharing notes and no support equipment (calculators, phones, etc). The usual penalty for copying or sharing answers on a quiz or exam is a final grade of E for the course. If you have any questions, please ask during the quiz, not after. You have 60 minutes.
- Unless otherwise specified, questions involving machine instructions are for the LC-3.
- Note: The spacing in the instructions might not correspond to the ones on the LC-3 summary sheet.

True/False [2 pts each]

1. Sequential logic circuits use clocks to separate memory reads and computations from memory writes. True

2. A master-slave flip-flop alternates between reading and writing the value of a bit but disallows doing both at the same time. True

3. One major use for finite state machines is implementing regular expression pattern matching. True

4. In a von Neumann computer, "program counter" is something of a misnomer because the program counter doesn't actually contain a count. True

5. To read a value from memory, we copy its address to the MAR, read the MDR, and signal "Read" (in that order). False

Multiple Choice [choose exactly one alternative; 3 pts each]

6. Say we have a computer (not necessary the LC-3) with word addressability, k-bit words, and m-bit addresses. What relationship is necessary between k and m?

   (a) $k \leq m$
   (b) $k < m$
   (c) $k \geq m$
   (d) k and m can be totally unrelated.

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7. Where does decoding of an instruction occur?
   (a) In the program counter.
   (b) In the instruction register.
   (c) In the memory data register.
   (d) In the memory address register.

8. Which of the below is part of the instruction cycle for all LC-3 instructions?
   (a) Decode Instruction
   (b) Calculate Effective Addresses
   (c) Retrieve Operand Values
   (d) Store Results

9. Branch/jump instructions cause a branch/jump by
   (a) Modifying the PC during the Fetch Instruction phase of the instruction cycle.
   (b) Modifying the PC during the Execute Instruction phase of the instruction cycle.
   (c) Modifying the PC during the Store Result phase of the instruction cycle.
   (d) (a) and (b)

10. For all instructions, when is incrementing the PC done during the instruction cycle?
   (a) During Fetch Instruction, before reading the instruction from memory.
   (b) During Fetch Instruction, after reading the instruction from memory.
   (c) As part of Decode Instruction.
   (d) After Store Results but before the next Fetch Instruction.
   (e) Just before calculating a PC offset.

11. Which of the following can be used to set `R1` to zero?
   (a) `ADD 001 001 100000`
   (b) `AND 001 111 100000`
   (c) `ADD 001 000 000 000`
   (d) (a) and (b)
   (e) (b) and (c)

12. If `R1` contains the integer 283, what does `NOT 001 001 111111` do?
   (a) It sets `R1` ← `0`
   (b) It sets `R1` ← `-283`
   (c) It sets `R1` ← `-284`
   (d) It sets `R1` ← `32767 - 283`
   (e) None of the above.

13. Which of the following can be used to copy R1 to R7?
    (a) ADD 111 001 100000
    (b) ADD 111 001 000000
    (c) AND 111 001 111111
    (d) LDR 111 001 000000
    (e) (a) and (b)
    (f) (b) and (c)
    (g) (a) and (c)

14. What does LD 000 111111111 do?
    (a) It sets R0 ← -1
    (b) It sets R0 ← x21FF
    (c) It sets R0 ← PC - 1
    (d) We can't determine this without knowing more about the contents of memory.

15. If R0 = x0030 = 48, then what does TRAP x21 do?
    (a) It prints the character "0"
    (b) It prints the 2 characters "48"
    (c) It prints the 5 characters "x0030"
    (d) It reads a character from the keyboard and overwrites R0 with it.

16. Suppose R6 = x4000, M[x4000] = x5000, and M[x5000] = 12. What does the instruction LDR 101 110000000 do, assuming the instruction is at x3050?
    (a) It sets R5 ← x4000
    (b) It sets R5 ← x5000
    (c) It sets R5 ← x6000
    (d) It sets R5 ← 12
    (e) None of the above.

17. Suppose R2 = x4000, M[x3100] = x5000, M[x4000] = 14, and M[x5000] = 48. What does the instruction LDI 101 010101111, assuming the instruction is at x3050?
    (a) It sets R5 ← x3100
    (b) It sets R5 ← x4000
    (c) It sets R5 ← x5000
    (d) It sets R5 ← 14
    (e) It sets R5 ← 48
    (f) None of the above.

18. Suppose R2 = x4000, M[x3100] = x5000, M[x4000] = 14, and M[x5000] = 48. What does the instruction LEA 101 010101111, assuming the instruction is at x3050?

x3051
x00AF
x3100

(a) It sets R5 ← x3100
(b) It sets R5 ← x4000
(c) It sets R5 ← x500
(d) It sets R5 ← 14
(e) It sets R5 ← 48
(f) None of the above.

19. What immediate values can be used in the ADD instruction?

(a) -256 ≤ value ≤ 255
(b) -512 ≤ value ≤ 511
(c) -16 ≤ value ≤ 15
(d) None of the above.

20. What PC offsets can be used in the load instruction (LD)?

(a) -256 ≤ offset ≤ 255
(b) -512 ≤ offset ≤ 511
(c) -16 ≤ offset ≤ 15
(d) None of the above.

21. Which of the following instructions set the condition code?

(a) ADD
(b) LD
(c) ST
(d) BR
(e) (a) and (b)
(f) (b) and (c)
(g) (a), (b), and (c)
(h) (a), (b), (c), and (d)

22. When does BR 010 ... cause a branch?

(a) When the condition code indicates < 0.
(b) When the condition code indicates = 0.
(c) When the condition code indicates ≤ 0.
(d) When R2 is zero.
(e) When R2 is not zero.
(f) None of the above.

23. When does `BR 000 ...` cause a branch?
    (a) When the condition code indicates = 0.
    (b) When the condition code indicates ≠ 0.
    (c) It never causes a branch.
    (d) When R0 is zero.
    (e) When R0 is not zero.
    (f) None of the above.

24. Suppose `R7 = M[x4020] = x40F0`. What does `BR 111 000100000` do, assuming the instruction is at `x3FFF`?
    (a) We go to x4020.
    (b) We go to x40F0.
    (c) We go to x4110.
    (d) It depends on the condition code, which wasn't given.

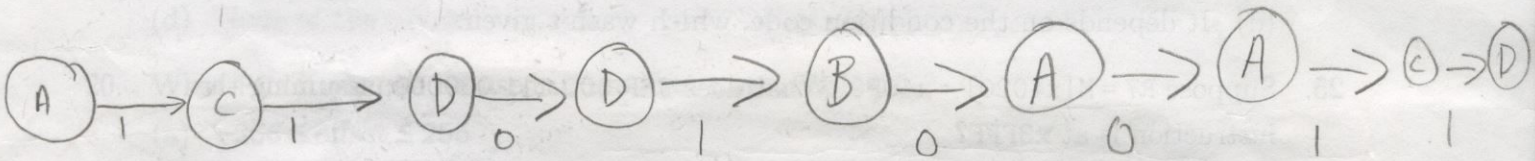
25. Suppose `R7 = M[x4020] = x40F0`. What does `JMP 000 111 000000`, assuming the instruction is at `x3FFF`?
    (a) We go to x4020.
    (b) We go to x40F0.
    (c) We go to x4110.
    (d) It depends on the value of R0, which wasn't given.

Short Answer [pts as marked]

For Questions 26 and 27, use the finite state machine with the state transition table as shown. Assume state A is the start state and state D is the only accepting state.

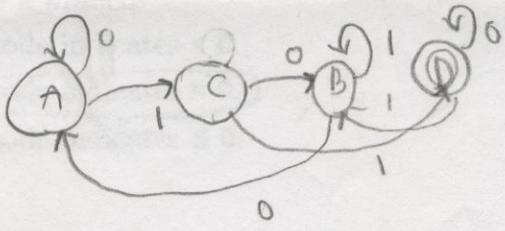
State	Input	New State
A	0	A
A	1	C
B	0	A
B	1	B
C	0	B
C	1	D
D	0	D
D	1	B

26. [8 pts] Trace the execution of this machine on the input `11010011` by listing the sequence of states the machine is in. Also say whether the input string is accepted or not.



Sequence: A C D D B A A C D

String is in accepting state



Your name Ambika Murali 48

CS 350 Quiz 1, Mon Feb 14, 2011

(30 minutes, 50 points total)

Instructions

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Short Answer Questions [points as marked]

1. [3 pts] What is the bitstring that represents the most negative 6-bit 2's complement number? What is the decimal value of this number?

100000
011111
+ 1
100000

100000
-32 ?
$2^5 = 32$

2. [3 pts] What bitstring(s) represent zero in 6-bit 2's complement?

000000

3. [8 pts] Convert the decimal calculation 6 – 25 = 6 + (–25) = –19 = –(19) into 6-bit 2's complement. (Show the converted values of 6, 25, –25, 19, and –19.)

2|6
2|3 0
2|1 1

(6) (–25) (6)
000110 + (–011001) = 000110 + (100110+1)
(6) (–25) (–19)
= 000110 + 100111 = 101101

010011 = 101100+1 = 101101
(–19)

2|25
2|12 1
2|6 0
2|3 0
2|1 1

000110
+100111
101101

(19)
2|19
2|9 1
2|4 1
2|2 0
2|1 0

15 - 1111
16 - 10000
17 - 10001
18 - 10010 19 - 10011 20 - 10100 21 - 10101
22 - 10110 23 - 10111 24 - 11000 25 - 11001

4. [3 pts] What is the hexadecimal representation for the bitstring 1111101011 ?

0011 | 1110 | 1011
3 E B

3EB ✓

1010 - A
1011 - B
1100 - C
1101 - D
1110 - E

5. [3 pts] What 9-bit string does octal 752 represent?

752
111 101 010

111 101 010 ✓

6. [3 pts] What decimal number does 8-bit 2's complement hexadecimal AC represent?

AC
1010 1100

-84
watch - signs

10101100
01010011
+ 1
01010100 → $(1\times2^2)+(1\times2^4)+(1\times2^6)$
$= 4+16+64$
$= 84$ ✓

7. [3 pts] What decimal number does 7-bit 2's complement octal 126 represent?

126
001 010 110

-42

01010110
01010010
+ 1
01010101 $2^1+2^3+2^5$
$= 2+8+32$
$= 42$ ✓

8. [3 pts] Let A('0'), A('1'), ... be the ASCII representation numbers of the characters '0', '1', ... What is the relationship between A('0'), 6, and A('6') ?

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A('0') and A('6') have the hexadecimal representations of 30 +36 whereas 6 is the decimal representation of 54.

$A('6') = 36_{16} = 54_{10}$ $A('6') = A('0') + 6$

9. [6 pts] What is the binary representation of 9.625_{10}? What is its scientific notation representation?

9.625_{10}

$9 \rightarrow 1001$

$1001.\frac{1}{1/2}\frac{0}{1/4}\frac{1}{1/8}$ (Binary Rep)

$1/8 = 8 \overline{)1000}$ = 0.125

$\frac{1}{2} + \frac{1}{4} = 0.75$

1.001101×2^3 ← scientific

$\frac{1}{2} + \frac{1}{8} = \frac{3}{8} = 0.5$

$+ 0.125 = 0.625$

10. [6 pts] What is the IEEE 32-bit representation for $1.1010011_2 \times 2^5$? (Feel free to add extra spaces for readability.)

$5 + 127 = 132$

0 (sign-bit) 10000100 (Exponent) 10100110000000000000000 (fraction)

132 % 2 = 0
66 % 2 = 0
33 % 2 = 1
16 % 2 = 0
8 % 2 = 0
4 % 2 = 0
2 % 2 = 0
1 % 2 = 1

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11. [9 pts] Write a truth table for NOT (X OR (NOT Z AND Y)). Include columns for the subexpressions (X OR (NOT Z AND Y)) and (NOT Z AND Y). (You can include other subexpressions if you want.)

X	Y	Z	NOT	(X OR	(NOT Z AND Y))
0	0	0	1	0	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	1	1	0	0
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	0	1	1
1	1	1	0	1	0

↑ expression column

X	Y	Z	NOT(X OR(NOT Z AND Y))
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0